Intel's Silicon Technology Development Pipeline

case study - HiK Metal Gate CMP

Since first introducing the microprocessor in 1971, Intel has fueled the personal computer industry through its relentless pursuit of Moore's law – doubling the performance and value of its integrated circuit products every 18 months. For three decades, Intel relied primarily on the shrinking of circuit dimensions each technology cycle to obtain this performance boost. Smaller circuitry yielded greater circuit functionality, due to greater packing density of circuits, and as well as faster circuits since transistor speed increased at the smaller dimensions. This combination higher packing density and faster transistors were the basis achieving Moore's Law.

However, since the 90nm technology node, short channel effects and loss of strain has caused transistor speed to decrease with shrinking circuit dimensions. Shrinking dimensions still provides increased functionality, but greater changes must be made to increase transistor performance. As a result, maintaining the pace of Moore's Law requires significantly more complex and disruptive changes to silicon processing requiring the IC maker to take on significantly greater risk with each technology node. Intel's introduction of HiK-metal gate at the 45 nm node is an excellent example of how a disruptive technology change can lead to significant performance benefits when executed well.

This talk will begin with a discussion on how Intel manages this increased complexity and risk via it's technology development pipeline – containing four distinct phases of development. Changes are first conceived of and tested for feasibility in the Research phase, fully tested and selected in the Pathfinding phase, synchronized and integrated in the Development phase, and then brought to HVM in the In-situ Ramp phase. As the most significant change to silicon technology in recent history, the conversion to HiK-metal gate will be used to demonstrate how Intel successfully mitigates risk in the execution complex changes. The talk will also discuss how Intel has leveraged its advanced chemical mechanical polishing capability to 1) implement HiK metal gate significantly ahead of the rest of the industry using a novel replacement metal gate (gate last) technique as 2) advance this lead in the 32nm node.

The talk will lastly look at the prognosis for continuing the cadence of Moore's Law at the 22nm node and beyond. As shrinking continues, both the challenges faced by the semiconductor industry as well as the changes required to meet these challenges will intensify. The industry is researching a multitude of different methods by which these challenges may be met.