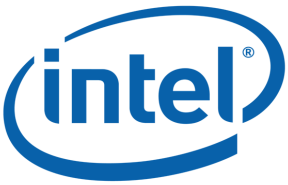


Intel® 81348 I/O Processor SRAM DMA

Application Note

May 2007

Reference Number: 317459-001US

Contents

Figures

No Figures Used At This Time

Tables

Revision History

Date	Revision	Description
May 2007	001	Initial release.

1.0 Introduction

This chapter describes the operation and control of the SRAM DMA (SDMA) Unit.

2.0 Overview

The SRAM DMA (SDMA) unit provides a means for memory to be transferred between local memory (SRAM) and host memory through the PCIe bus. The SDMA provides two separate channels (HostToLocal and LocalToHost) that operate independently from one another.

The HostToLocal channel performs DMA operations from Host Memory to Local Memory (SRAM). The LocalToHost channel performs DMA operations from Local Memory to Host Memory (SRAM).

3.0 Theory of Operation

To perform a DMA operation, the firmware writes to either the HostToLocal or LocalToHost registers, depending on the direction of transfer. One DMA is underway in each direction simultaneously.

Each SDMA channel provides a "single-shot" DMA capability, in other words, one DMA operation at a time. There is no ability to queue multiple DMA requests in a given channel.

Before programming any of the registers, firmware must ensure that the DMA channel is not active by ensuring that all previous DMA operations have completed (for example by reading the Interrupt Counter / Interrupt Acknowledge and comparing that against the last DMA operation requested). Firmware then writes the Host Addresses, Local Addresses, and the Byte Count. The firmware then sets the CHGO bit to start the DMA.

Upon completion of the DMA operation, the firmware receives an interrupt. Two interrupts are associated with the SDMA, a Normal and an Error interrupt.

In either case the firmware reads the Interrupt Counter of the channel(s) it has programmed. Note that because the HostToLocal and LocalToHost channels are independent then when both have been programmed the firmware needs to read each channel Interrupt Counter to determine which channel has completed its DMA.

After reading the Interrupt Counter, firmware writes that counter value back to the Interrupt Acknowledge field in the same register. This clears the interrupt, and another DMA on that channel is started.

Errors are indicated by flags within each channel Control/Status registers. Further information on the errors is obtained by examining the ATU or XSI System Controller error registers.

Example 1. Pseudo Code Programming Example: (RedBoot* command line prompts shown)

To perform a single shot DMA of 0x40 from local SRAM offset 0x0 to host address 0x20_0000:

INITIAL SETUP:

1. Assure the registers are enabled for access by setting bit 0 of the control/status register.
   mfill -b 0xFFD9823c -l 0x4 -p 0x1
2. Unmask SDMA error and status registers in INTCTL2 bits 12 and 13.

TO PERFORM A DMA:

1. Check to make sure that the channel is idle by reading the Int Counter/Ack register and assuring the upper and lower counts are equal.
   x -b 0xFFD98238 -l 0x4 -4
2. Set bit 30 in the byte swap register to disable byte swapping.
   mfill -b 0xFFD98200 -l 0x4 -p 0x40000000
3. Set the host destination address lower and upper.
   mfill -b 0xFFD98204 -l 0x4 -p 0x200000
   mfill -b 0xFFD98208 -l 0x4 -p 0x0
4. Set the source offset from the base of SRAM.
   mfill -b 0xFFD9820C -l 0x4 -p 0x0
5. Write the byte counts in both the upper and lower parts of the byte count register.
   mfill -b 0xFFD98218 -l 0x4 -p 0x00400040
6. Write the channel go bit (its OK to assure bit 0 is set at the same time).
   mfill -b 0xFFD9823c -l 0x4 -p 0x3
7. Read the Int Counter/Ack register.
   x -b 0xFFD98238 -l 0x4 -4
8. Assume step 7 resulted in a value of 0x0300002, now write the int counter back to the int Ack.
   mfill -b 0xFFD98238 -l 0x4 -p 0x3
9. Upon INT, check status.
   x -b 0xFFD9823c -l 0x4 -4

3.1 Interrupt Control for SDMA

Refer to the silicon C Spec for full register definitions, the following control the SDMA:

INTPND2:
- bit 13: SDMA Error Interrupt Pending
- bit 12: SDMA Normal Interrupt Pending

INTCTL2:
- bit 13: SDMA Error Interrupt Mask.
  - 0 = Masked
  - 1 = Not Masked
- bit 12: SDMA Normal Interrupt Mask.
  - 0 = Masked
  - 1 = Not Masked

INTSTR2
- bit 13: SDMA Error Interrupt Steering.
  - 0 = Interrupt Directed to internal IRQ
  - 1 = Interrupt Directed to internal FIQ
- bit 12: SDMA Normal Interrupt Steering.
  - 0 = Interrupt Directed to internal IRQ
  - 1 = Interrupt Directed to internal FIQ

INTSRC2
- bit 13: SDMA Error Interrupt
  - 0 = Not Interrupting or Not steered to internal IRQ exception or masked by INTCTL2
  - 1 = Interrupting and steered to internal IRQ exception and unmasked by INTCTL2
- bit 12: SDMA Normal Interrupt
  - 0 = Not Interrupting or Not steered to internal IRQ exception or masked by INTCTL2
  - 1 = Interrupting and steered to internal IRQ exception and unmasked by INTCTL2

FINTSRC2
- bit 13: SDMA Error Interrupt
  - 0 = Not Interrupting or Not steered to internal FIQ exception or masked by INTCTL2
  - 1 = Interrupting and steered to internal FIQ exception and unmasked by INTCTL2
- bit 12: SDMA Normal Interrupt
  - 0 = Not Interrupting or Not steered to internal FIQ exception or masked by INTCTL2
  - 1 = Interrupting and steered to internal FIQ exception and unmasked by INTCTL2

IPR
- 27:26: SDMA Error Interrupt Priority
- 25:24: SDMA Normal Interrupt Priority

4.0 Register Definitions

The SDMA controller contains separate LocalToHost (L2H) and HostToLocal (H2L) channels that are independent of each other. These are used simultaneously thus allowing full duplex transfer to occur.

The location of these registers are specified as a relative offset to a 512KB aligned global PMMR offset. The default for the 512KB aligned offset is 0 FFD8 0000H defined by the PMMRBAR register.

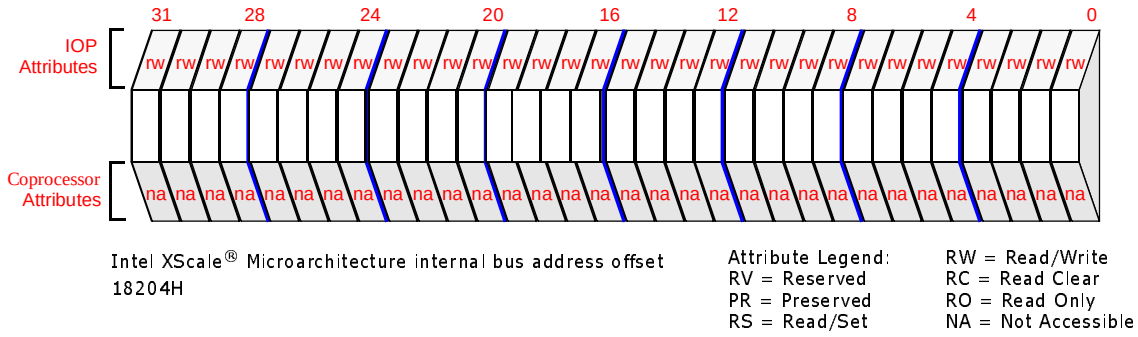
Table 1. SDMA Controller Unit Registers

Section, Register Name, Acronym, Page
Section 4.1, "LocalToHost Destination Lower Address Register - L2H_DLAR" on page 11
Section 4.2, "LocalToHost Destination Upper Address Register - L2H_DUAR" on page 11
Section 4.3, "LocalToHost Source Lower Address Register - L2H_SLAR" on page 12
Section 4.4, "LocalToHost Byte Count Register - L2H_BCR" on page 12
Section 4.5, "LocalToHost Interrupt Counter/Acknowledge Register L2H_ICAR" on page 13
Section 4.6, "LocalToHost Control/Status Register - L2H_CSR" on page 14
Section 4.7, "LocalToHost Byte Swap Control Register - L2H_BSCR" on page 15
Section 4.8, "HostToLocal Destination Lower Address Register - H2L_DLAR" on page 16
Section 4.9, "HostToLocal Source Upper Address Register - H2L_SUAR" on page 16
Section 4.10, "HostToLocal Source Lower Address Register - H2L_SLAR" on page 17
Section 4.11, "HostToLocal Byte Count Register - H2L_BCR" on page 17
Section 4.12, "HostToLocal Interrupt Counter/Acknowledge Register - H2L_ICAR" on page 18
Section 4.13, "HostToLocal Control/Status Register - H2L_CSR" on page 19
Section 4.14, "HostToLocal Byte Swap Control Register - H2L_BSCR" on page 20

4.1 LocalToHost Destination Lower Address Register - L2H_DLAR

The LocalToHost Destination Lower Address Registers (L2H_DLAR) represent the lower 32-bits of the destination (host) address.

Table 2. LocalToHost Destination Lower Address Register - L2H_DLAR

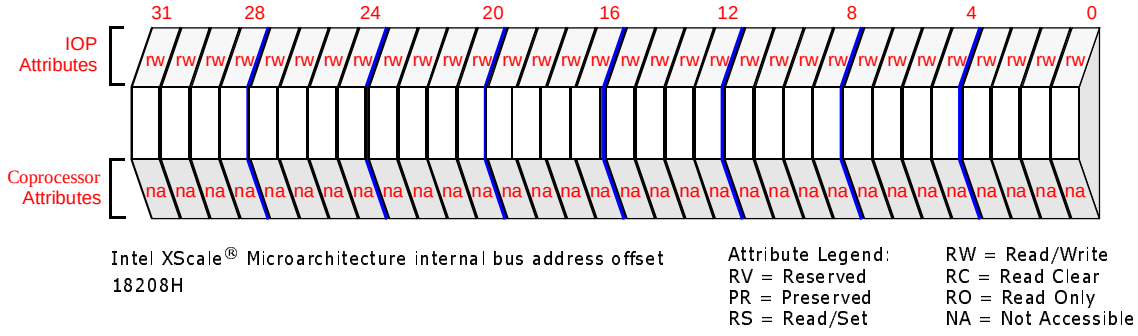


Bit	Default	Description
31:00	00000000H	Destination Lower Address Register (DLAR) - Read/Write This field specifies the low-order 32 bits of the destination (host) memory address. This field is CLEARED by a hardware or software reset.

4.2 LocalToHost Destination Upper Address Register - L2H_DUAR

The LocalToHost Destination Upper Address Register (L2H_DUAR) represents the upper 32-bits of the destination (host) address.

Table 3. LocalToHost Destination Upper Address Register - L2H_DUAR

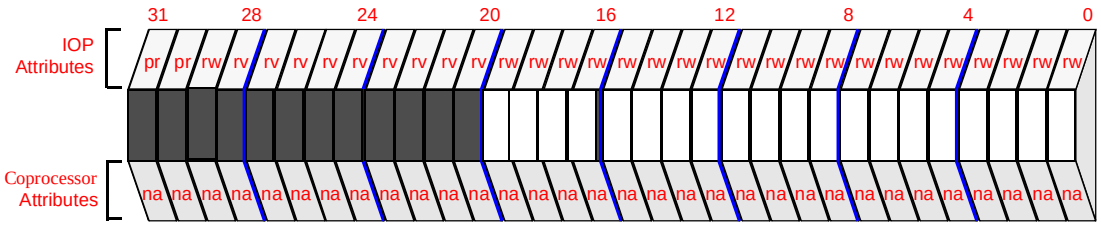


Bit	Default	Description
31:00	00000000H	Destination Upper Address Register (DUAR) - Read/Write This field specifies the upper-order 32 bits of the destination (host) memory address. This field is CLEARED by a hardware or software reset.

4.3 LocalToHost Source Lower Address Register - L2H_SLAR

The LocalToHost Source Lower Address Register (L2H_SLAR) represents the lower 32 bits of the source (local) address. The upper address bits are zero, as local memory is limited to 1 Mbyte.

Table 4. LocalToHost Source Lower Address Register - L2H_SLAR



Intel XScale® Microarchitecture internal bus address offset 1820CH

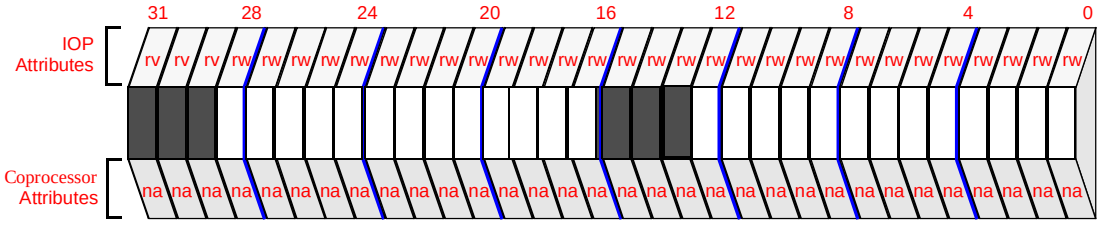
Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31:20	000H	Reserved. Must be written as zero.
19:00	00000H	Source Lower Address Register (SLAR) - Read/Write Specifies first source (local) memory starting byte address that SDMA Processor uses to read data. The field decodes a 1MB local memory address space that represents of the offset from the base of SRAM.

4.4 LocalToHost Byte Count Register - L2H_BCR

The LocalToHost Byte Count Register (L2H_BCR) represents the byte count associated with data to be moved. Note for internal architecture reasons the byte count must be entered in two locations within this register.

Table 5. LocalToHost Byte Count Register - L2H_BCR



Intel XScale® Microarchitecture internal bus address offset 18218H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

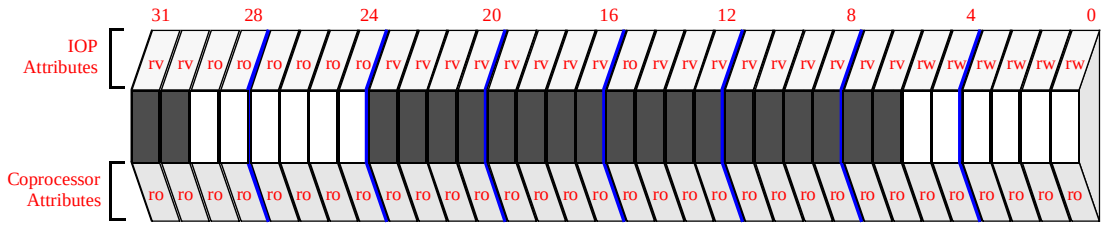
Bit	Default	Description
31:29	000_2	Reserved. Must be written as zero.
28:16	00000H	Byte Count Register (BCR) This field specifies the length in bytes that is for the data to be transferred. The maximum transfer count value is 4096 bytes (1000H). This field is CLEARED by a hardware or software reset.
15:13	000_2	Reserved. Must be written as zero.
12:00	000H	Byte Count Register (BCR) This field specifies the length in bytes that is for the data to be transferred. The maximum transfer count value is 4096 bytes (1000H). This field is CLEARED by a hardware or software reset. This must be written the same as bits 28:16, otherwise unpredictable results occur.

Note: It is required that the byte count be written to both the upper and lower parts of this register (bits 28:16 and bits 12:00). Failure to put the byte count in both locations renders unpredictable results.

4.5 LocalToHost Interrupt Counter/Acknowledge Register L2H_ICAR

Firmware uses the LocalToHost Interrupt Counter/Acknowledge Register (L2H_ICAR) to keep track of and acknowledge interrupts.

Table 6. LocalToHost Interrupt Counter/Acknowledge Register - L2H_ICAR



Internal bus address offset
18238H

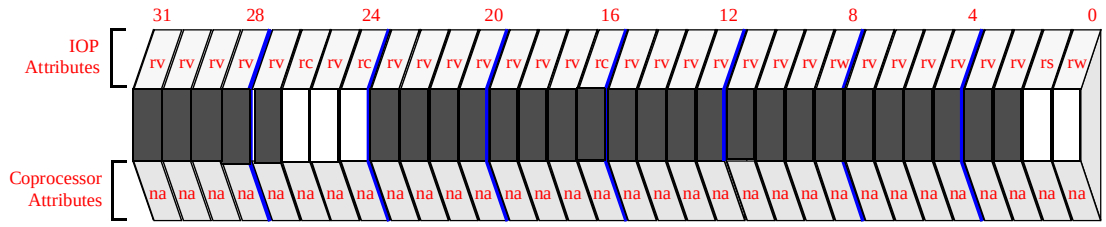
Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31:30	0H	Reserved
29:24	000000_2	Interrupt Counter - Read Only The Interrupt Counter is a counter of the number of interrupts on this DMA channel. It is monotonically increasing (by 1) and wraps around to zero after reaching its maximum value. When a DMA completes for this channel, the Interrupt Counter is incremented and an interrupt is asserted. Firmware reads the Interrupt Counter of each channel to determine which one raised the interrupt. Firmware then writes back the Interrupt Counter value to the Interrupt Acknowledge to clear the interrupt.
23:06	0000H	Reserved
05:00	00H	Interrupt Acknowledge - Read/Write The Interrupt Acknowledge is used to clear interrupts. Firmware reads the Interrupt Counter and then writes that value back to the Interrupt Acknowledge field.

4.6 LocalToHost Control/Status Register - L2H_CSR

The LocalToHost Control/Status Register (L2H_CSR) provides the control and status for the LocalToHost channel.

Table 7. LocalToHost Control/Status Register - L2H_CSR



Internal bus address offset
1823CH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

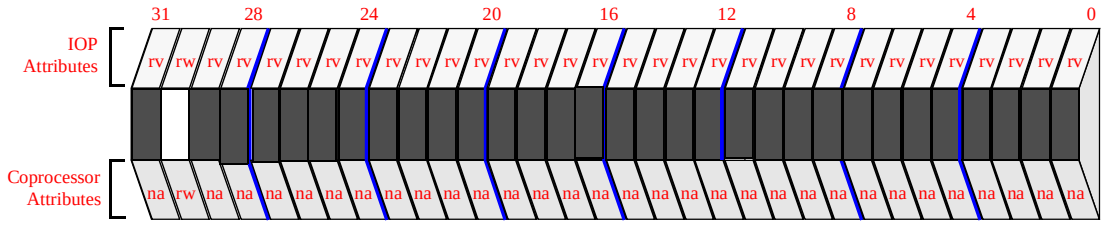
Bit	Default	Description
31:27	00000_2	**Reserved**
26:24	000_2	Error Flags - Read/Clear One or more of these bits is set to indicate an error has occurred with the DMA operation. The precise cause of the error is determined by reading the ATU or XSISC error registers.
23:02	0000H	Reserved
01	0_2	Channel Go (CHGO) - Read/Set Set this bit to begin the DMA operation. This bit must be cleared while the DMA registers are being set up. The CHGO bit is set by firmware to begin the DMA operation. When the DMA operation begins the hardware clears this bit. Note that clearing of this bit does not indicate the DMA operation is complete, rather that the hardware has started processing it.
00	0_2	Enable Register - Read/Write Must be set for proper operation. A value of zero (when the CHGO bit is set) has unpredictable results.

4.7 LocalToHost Byte Swap Control Register - L2H_BSCR

The LocalToHost Byte SWap Control Register (L2H_BSCR) provides the control to enable/disable byte swapping.

Note: The "Default" *enables* byte swapping.

Table 8. LocalToHost Byte Swap Control Register - L2H_BSCR



Internal bus address offset
18200H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

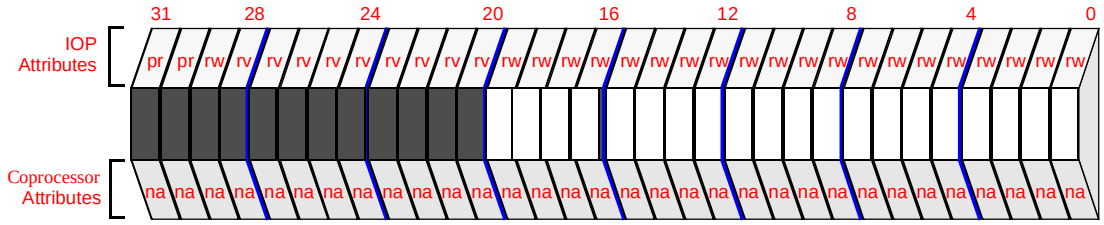
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31	00	**Reserved.**
30	00	Byte Swap Disable - Read/Write This bit must be set to prevent SDMA transfers from byte swapping.
29:0	00	**Reserved.**

4.8 HostToLocal Destination Lower Address Register - H2L_DLAR

The HostToLocal Destination Lower Address Register - H2L_DLAR represents the local memory address.

Table 9. HostToLocal Destination Lower Address Register - H2L_DLAR



Channel # Intel XScale® Microarchitecture internal bus address offset
1825CH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

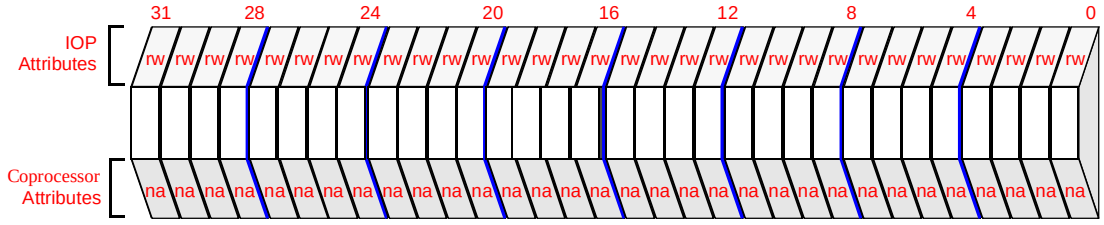
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31:20	000H	Reserved
19:00	00000H	Destination Lower Address Register (DLAR) - Read/Write This field specifies the destination (local) memory starting byte address that the SDMA Processor uses to write data. The field decodes a 1MB local memory address space that represents of the offset from the base of SRAM.

4.9 HostToLocal Source Upper Address Register - H2L_SUAR

The HostToLocal Source Upper Address Register (H2L_SUAR) represents the upper 32-bits of the source (host) address.

Table 10. HostToLocal Source Upper Address Register - H2L_SUAR



Intel XScale® Microarchitecture internal bus address offset
18258H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

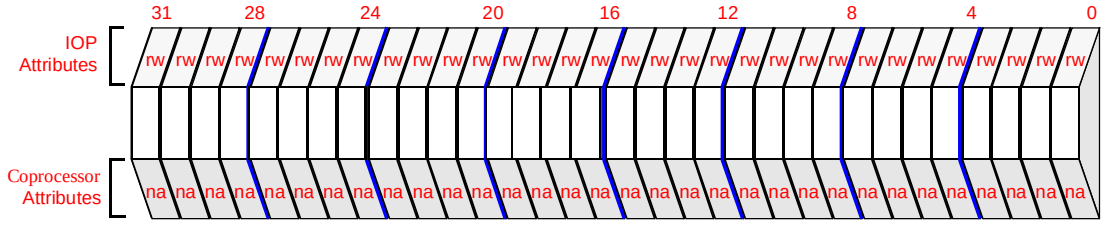
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31:00	00000000H	Source Upper Address Register (SUAR) - Read/Write This field specifies the upper-order 32 bits of the source (host) memory address. This field is CLEARED by a hardware or software reset.

4.10 HostToLocal Source Lower Address Register - H2L_SLAR

The HostToLocal Source Lower Address Register (H2L_SLAR) represent the lower 32-bits of the source (host) address.

Table 11. HostToLocal Source Lower Address Register - H2L_SLAR



Intel XScale® Microarchitecture internal bus address offset
18254H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

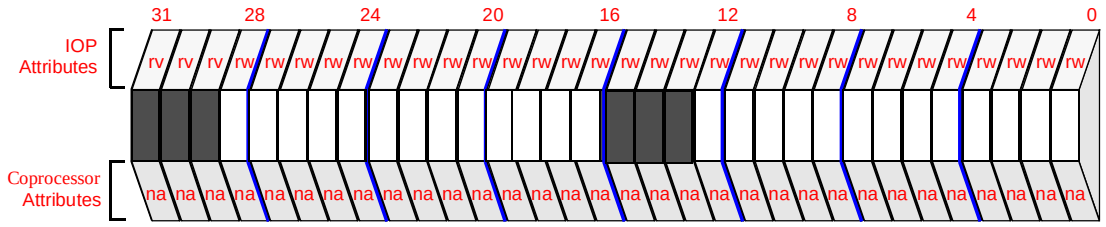
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31:00	00000000H	Source Lower Address Register (SLAR) - Read/Write This field specifies the low-order 32 bits of the source (host) memory address. This field is CLEARED by a hardware or software reset.

4.11 HostToLocal Byte Count Register - H2L_BCR

The HostToLocal Byte Count Registers (H2L_BCR) represent the byte count of the DMA.

Table 12. HostToLocal Byte Count Register - H2L_BCR



Intel XScale® Microarchitecture internal bus address offset
18268H

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

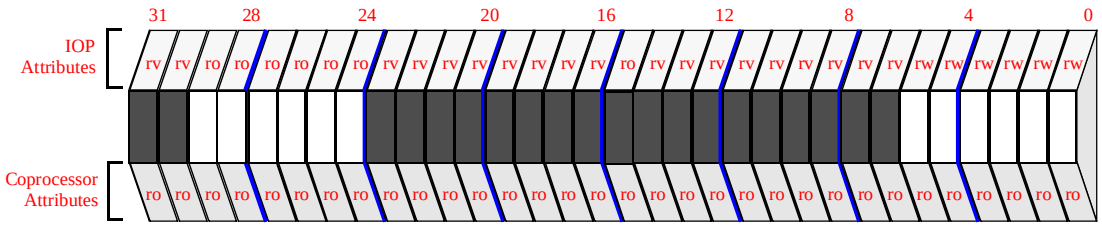
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31:29	000_2	Reserved
28:16	00000H	Byte Count Register (BCR) This field specifies the length in bytes that is for the data to be transferred. The maximum transfer count value is 4096 bytes (1000H). This field is CLEARED by a hardware or software reset.
15:13	000_2	Reserved. Must be written as zero.
12:00	000H	Byte Count Register (BCR) This field specifies the length in bytes that is for the data to be transferred. The maximum transfer count value is 4096 bytes (1000H). This field is CLEARED by a hardware or software reset. This must be written the same as bits 28:16, otherwise unpredictable results occur.

4.12 HostToLocal Interrupt Counter/Acknowledge Register - H2L_ICAR

Firmware uses the HostToLocal Interrupt Acknowledge Register (H2L_ICAR) to keep track of and acknowledge interrupts.

Table 13. HostToLocal Interrupt Counter/Acknowledge Register - H2L_ICAR



Internal bus address offset
18288H

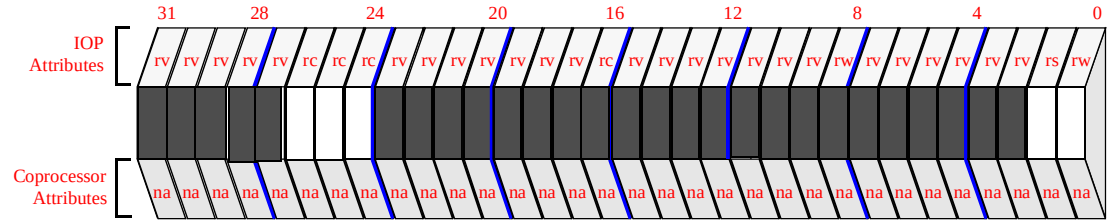
Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set
RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

Bit	Default	Description
31:30	0H	Reserved
29:24	000000_2	Interrupt Counter - Read Only The Interrupt Counter is a counter of the number of interrupts on this DMA channel. It is monotonically increasing (by 1) and wraps around to zero after reaching its maximum value. When a DMA completes for this channel, the Interrupt Counter is incremented and an interrupt is asserted. Firmware reads the Interrupt Counter of each channel to determine which one raised the interrupt. Firmware then writes back the Interrupt Counter value to the Interrupt Acknowledge to clear the interrupt.
23:06	0000H	Reserved
05:00	00H	Interrupt Acknowledge - Read/Write The Interrupt Acknowledge is used to clear interrupts. Firmware reads the Interrupt Counter and then writes that value back to the Interrupt Acknowledge field.

4.13 HostToLocal Control/Status Register - H2L_CSR

The HostToLocal Control/Status Register (H2L_CSR) provides the status and control of the HostToLocal channel.

Table 14. HostToLocal Control/Status Register - H2L_CSR



Internal bus address offset
1828CH

Attribute Legend:
RV = Reserved
PR = Preserved
RS = Read/Set

RW = Read/Write
RC = Read Clear
RO = Read Only
NA = Not Accessible

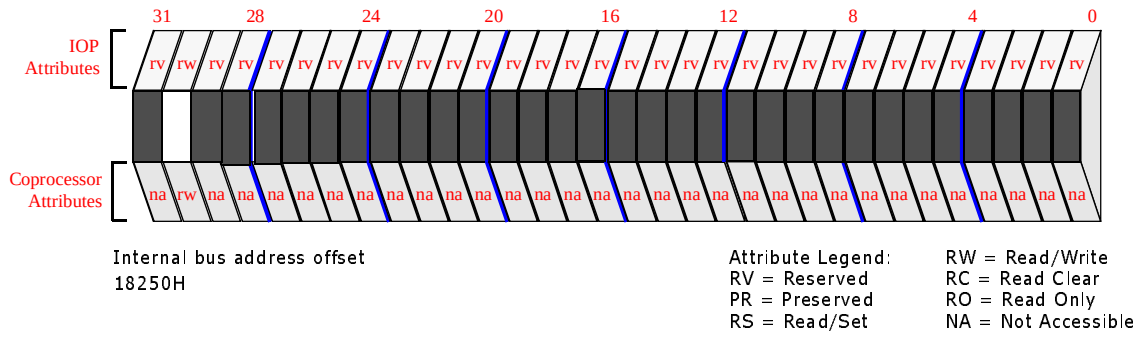
Bit	Default	Description
31:27	00000_2	Reserved
26:24	000_2	Error Flags - Read/Clear One or more of these bits is set to indicate an error has occurred with the DMA operation. The precise cause of the error is determined by reading the ATU or XSISC error registers.
23:02	0000H	Reserved
01	0_2	Channel Go (CHGO) - Read/Set Set this bit to begin the DMA operation. This bit must be cleared while the DMA registers are being set up. The CHGO bit is set by firmware to begin the DMA operation. When the DMA operation begins the hardware clears this bit. Note that clearing of this bit does not indicate the DMA operation is complete, rather that the hardware has started processing it.
00	0_2	Enable Register - Read/Write Must be set for proper operation. A value of zero (when the CHGO bit is set) has unpredictable results.

4.14 HostToLocal Byte Swap Control Register - H2L_BSCR

The LocalToHost Byte SWap Control Register (H2L_BSCR) provides the control to enable/disable byte swapping.

Note: The "Default" *enables* byte swapping.

Table 15. HostToLocal Byte Swap Control Register - H2L_BSCR



Bit	Default	Description
31	00	**Reserved.**
30	00	Byte Swap Disable - Read/Write This bit must be set to prevent SDMA transfers from byte swapping.
29:0	00	**Reserved.**