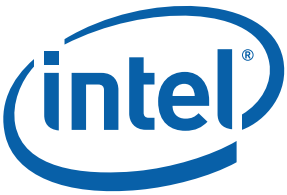

Intel® 413808 and 413812 SAS/SATA I/O Controllers

Design Review Checklist

May 2007

Order Number: 315046-003US

Contents

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Revision History

Date	Revision	Description
October 2006	002	Reformatted Variable attributes
September 2006	001	Launch Release.

1.0 Introduction

This document highlights design considerations the designer must review prior to manufacturing an adapter card or motherboard that implements the Intel® 413808 and 413812 SAS/SATA I/O Controllers (413808 and 413812).

The checklists address important connections to the 413808 and 413812 and any critical supporting circuitry. However, the checklists are only for reference; for complete design instructions, refer to the *Intel® 413808 and 413812 SAS/SATA I/O Controllers Design Guide*. These checklists are not necessarily complete and do not guarantee proper function of a design.

Note: This document is updated more frequently than the design guide and the latest terminations will supercede recommendations in the design guide.

2.0 List of References

Table 1. List of References

Document	Reference
Intel® 81348 I/O Processor Developer's Manual	315036
Intel® 413808 and 413812 SAS/SATA I/O Controllers Datasheet	315040
Intel® 413808 and 413812 SAS/SATA I/O Controllers Design Guide	315055
Intel® 413808 and 413812 SAS/SATA I/O Controllers Thermal Application Note	315052
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com/specifications/conventional/conventional_pci
PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a	http://www.pcisig.com/specifications/pcix_20
PCI Express Specification, Revision 1.0a	http://www.pcisig.com/specifications/pciexpress
PCI Express Base Specification 1.0a	http://www.pcisig.com/specifications/pciexpress
PCI Express Card Electromechanical Specification 1.0a	http://www.pcisig.com/specifications/pciexpress

3.0 Checklist Recommendations

The following tables provide the recommended pull-up and pull-down terminations for a 413808 and 413812 layout.

3.1 Important Design and Debug Requirements

The following details are required for all 413808 and 413812 designs. Note that these tables are not an inclusive list. We recommend that the design guide is referenced for additional details.

Note: Without implementing the debug requirements Intel is extremely limited in its ability to assist with debug issues involving the transport firmware and device driver.

Table 2. Design and Debug Checklist

Recommendations	Comments	Compliance	
		Yes	No
Debug Requirements			
• The serial console port connector to the UART0 port must be implemented to assist in debug of Intel transport firmware.	**UART0** is dedicated as the debug port for the transport FW. This port is also implemented on Intel development boards. Without the **UART0** port the debug of the transport firmware is extremely limited. ***Note:*** This port can be depopulated on production boards.		
• The JTAG port must be implemented on the board to assist in debug of third party device drivers.	A JTAG port provides the ability to connect a 3rd party debugger to the 413808 and 413812. Using a debugger is the only way to pinpoint potential device driver and transport firmware issues. ***Notes:*** 1. JTAG port is required even when the customer has no plans to utilize this connector in their debug process. Without the JTAG port, the debug of the device driver is extremely limited. 2. A low profile 10-pin JTAG port is now recommended to save on board space. Refer to the JTAG chapter of the design guide for implementation recommendations. This port may be depopulated on production boards.		
Design Notes			
• Supported and validated Flash components include Intel® StrataFlash® - J3, J3D and Intel® StrataFlash® Embedded Memory - P30. • A minimum size of 2 MB is required for the transport firmware.	• For information on migrating from the J3-to-P30 refer to the following document: http://developer.intel.com/design/flcomp/applnots/306667.htm ***Note:*** Other CFI Flash memory may work but these components have not been validated.		
• Design Guide SAS routing recommendations must be followed to prevent compliance issues.	It is important that the SAS lane lengths <= 5 inches, routed as 100 ohms +/- 15% differential signals with no more than two vias per signal.		
• Separate the 1.2 V Core power from the SAS/SATA and PCIE planes.	Separating the 1.2 V core supply minimizes noise coupling.		
• The SAS PLL filtering must be connected to ground. All the other PLL filters are not connected ground.	Refer to Section 3.4.1 of this document		
• 1.2 V must be up before the 1.8 V. The 1.2 V must be down after the 1.8 V.	Refer to the power delivery chapter of the design guide for additional details.		
• JTAG **TRST_N** must be asserted at power-on	A reset supervisor to pulse **TRST_N** low on power-on and pull high after power-on. Refer to the JTAG section of the design guide.		

3.2 Termination Values Checklist

Table 3 lists these 413808 and 413812 termination values.

Table 3. Termination Values Checklist (Sheet 1 of 8)

Signal	Recommendations	Comments	Compliance	
			Yes	No
S_TXP[7:0], S_TXN[7:0]	• Connect each of **S_TXP[7:0]**, **S_TXN[7:0]** lines with a 10 nF series capacitor with low ESR. • Unused ports can be left unconnected.	**Storage Transmit:** carries the differential output serial data and embedded clock for the SAS/SATA interface.		
S_RXP[7:0], S_RXN[7:0]	• Connect each of **S_RXP[7:0]**, **S_RXN[7:0]** lines with a10 nF series capacitor with low ESR. • Unused ports can be left unconnected.	**Storage Receive:** carries the differential input serial data and embedded clock for the SAS/SATA interface.		
S_CLKN0, **S_CLKP0**	• connect to differential 125 MHz ±100 ppm or a 150 MHz ±100 ppm oscillator. • use a 0.1 µF AC coupling series capacitor on **S_CLKN0** and **S_CLKP0**.	Differential storage clock		
RBIAS[1:0]	• 6.49 KΩ 1% to **GND**. Refer to Figure 7.			
RBIAS_SENSE[1:0]	• Connect to the same **GND** point of the **RBIAS[1:0]** resistors. Refer to Figure 7.			
S_ACT0/SCLOCK0, S_STAT0/SLOAD0	• **NC** when not used. • **SGPIO[0] is disabled:** Connect to LED with series resistor to indicate activity and status for storage engine[0].			
S_ACT1, S_STAT1	• **NC** when not used. • **SGPIO[0] is disabled:** These signals can be connected to an LED with series resistor to indicate activity and status for storage engine[1].			
S_ACT2/SDATAIN0, S_STAT2/SDATAOUT0	• **NC** when not used. • **SGPIO[0] is disabled:** These signals can be connected to an LED with series resistor to indicate activity or status for storage engine[2].			
S_ACT3, S_STAT3	• **NC** when not used. • **SGPIO[0] is disabled:** These signals can be connected to an LED with series resistor to indicate activity and status for storage engine[3].			
S_ACT4/SCLOCK1, S_STAT4/SLOAD1	• **NC** when not used. • **SGPIO[1] is disabled:** These signals can be connected to an LED with series resistor to indicate activity/status for storage engine[4].			

Table 3. Termination Values Checklist (Sheet 2 of 8)

Signal	Recommendations	Comments	Compliance	
			Yes	No
S_ACT5, **S_STAT5**	• **NC** when not used. • **SGPIO[1]** is disabled: These signals can be connected to an LED with series resistor to indicate activity /status for storage engine[5].			
S_ACT6/SDATAIN1, **S_STAT6/ SDATAOUT1**	• **NC** when not used. • **SGPIO[1] is disabled:** These signals can be connected to an LED with series resistor to indicate activity/status for storage engine[6].			
S_ACT7/, **S_STAT7**	• **NC** when not used. • **SGPIO[1]** is disabled: These signals can be connected to an LED with series resistor to indicate activity/status for storage engine[7].			
REFCLKP, **REFCLKN**	• For PCI Express interface: connect to a 100 MHz oscillator. • PCI-X end point: connect the **REFCLKP** to a resistor divider such that the **REFCLKP** node is connected to both a 17.4 K to **VCC3P3** and a 4.7 K connected to **GND**. **REFCLKN** must be connected to **GND**.	***Note:*** 100 MHz oscillator is required for the PCI Express differential clock.		
PETP[7:0], **PETN[7:0]**	• Series capacitors with value of 75 nF to 200 nF (low ESR) on each of the lines.			
PERP[7:0], **PERN[7:0]**	• No series capacitor needed. • **NC** when not used.			
PE_CALP, **PE_CALN**	• 1.4 KΩ 1% resistor is connected between the **PE_CALP** and **PE_CALN**.			
P_AD[63:32], **P_CBE[7:4]#**, **P_PAR64**	• When only PCI Express interface active, these signals are internally pulled-up and can be left as **NC**. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • When the **PCIX_32BIT#** is enabled (32-bit bus width), these signals are internally pulled-up and can be left as **NC**s.			
P_AD[31:0], **P_CBE[3:0]#**	• When only PCI Express interface active these signals are internally pulled-up and can be left as **NC**.			
P_REQ#	• **PCI Express: P_GNT[0]#** / **P_REQ#** has an internal pull-up and can be left as a NC. • **PCI Endpoint mode (external arbiter) PCIX_EP# = 0:** This is the output request signal for the ATU and needs to connect to the external arbiter's **P_REQ#** lines.			

Table 3. Termination Values Checklist (Sheet 3 of 8)

Signal	Recommendations	Comments	Compliance	
			Yes	No
P_GNT#	• **PCI Express: P_REQ[0]# / P_GNT#** has an internal pull-up and can be left as a **NC**. • **PCI Endpoint mode (external arbiter): P_GNT#** is input grant signal for the ATU. This pin should be pulled up to **VCC3P3** with an 8.2 KΩ resistor.			
P_REQ64#	• When only PCI Express interface is active, these signals are internally pulled-up and can be left as a **NC**. • When the **PCIX_PULLUP#** is enabled (pulled to 0), this signal is internally pulled-up. • PCI endpoint mode the width of the bus is indicated by the state of **REQ64#** at the rising edge of **RST#**.			
P_ACK64#, P_PAR, P_SERR#, P_PERR#, P_INT[D:A]#	• When only PCI Express interface is active these signals are internally pulled-up and can be left as a **NC**. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up.			
P_FRAME#, P_IRDY#, P_TRDY#, P_STOP#, P_DEVSEL#	• When only PCI Express interface is active these signals are internally pulled-up and can be left as a NC. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • PCI endpoint mode the state of these signals are used as for PCI-X initialization pattern at the rising edge of **RST#**.	Refer to the *PCI-X Specification 1.0b* for more information on the PCI-X Initialization pattern.		
P_M66EN	• **PCI Express: P_M66EN** has an internal pull-up and can be left as a **NC**. • **PCI Endpoint mode PCIX_EP# = 0:** Refer to Section 3.1 of the Design Guide.			
P_IDSEL	• **PCI Express: P_IDSEL** has an internal pull-up and can be left as a **NC**. • **PCI Endpoint mode PCIX_EP# = 0:** Connect to AD lines Section 3.1.2 of the Design Guide.			
P_CLKIN	• For PCI Express only this signal should be connected to **GND**. • **PCI Endpoint mode (PCIX_EP# = 0)**: connect to the system PCI clock.			
P_PCIXCAP	• GND this pin.			
P_BMI	• **When PCI Express only:** this signal can be left as a no connect. • **For PCI-X:** no connect when not used.			

Table 3. Termination Values Checklist (Sheet 4 of 8)

Signal	Recommendations	Comments	Compliance	
			Yes	No
P_CAL[0], **P_CAL[2]**	• When PCI-X interface is used: This pin is connected to a separate 22.1 Ω 1% resistor to **GND**. See Section 3.5 for more information. • When PCI-X interface is not used: These pins can be left as **NC**s.	**PCI Calibration:** is connected to an external calibration resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations.		
P_CAL[1]	• When PCI-X is used: This pin is connected to a separate 121 Ω 1% resistor to **GND**. See Section 3.5 for more information. • When PCI-X interface is not used: These pins can be left as **NC**s.			
PE_CALP **PE_CALN**	Connect **PE_CALP** ball through 1.4 K 1% resistor to the **PE_CALN** ball. Refer to Figure 5.	Note: this is required even when the PCI-Express interface is not used.		
A[24:0], **POE#**, **PB_RSTOUT#**	• Unused pins can be left unconnected. • Refer to Design guide for PBI bus connection recommendations.			
D[15:0], **PCE[1:0]#**, **PWE#**	• These are also used for reset straps refer to the Reset Strap Table 3.3. • Refer to Design guide for PBI bus connection recommendations.			
HS_ENUM#	Can be left unconnected when Hot-Swap not used.			
HS_LSTAT	When Compact PCI Hot-Swap is not supported, this signal must be tied to **GND**.	Hot-Swap **Latch Status:** An input indicating the state of the ejector switch. 0 = Indicates the ejector switch is closed. 1 = Indicates the ejector switch is open. 0 = Connect to **GND**. 1 = 8.2 KΩ pull-up to **VCC**.		
HS_LED_OUT	• Connect to Hot-Swap blue LED. • When CompactPCI* Hot-Swap is not supported this signal can be left unconnected.			

Table 3. Termination Values Checklist (Sheet 5 of 8)

Signal	Recommendations	Comments	Compliance	
			Yes	No
HS_FREQ[1:0] / CR_FREQ[1:0]	See comments	Hot-Swap **Frequency:** While in Hot-Swap mode, (these are only valid when **PCIX_EP#** = 0 and **HS_SM#** = 0). 00 = 133 MHz PCI-X. 01 = 100 MHz PCI-X. 10 = 66 MHz PCI-X. 11 = 33 or 66 MHz. PCI (frequency depends on **P_M66EN**). **Central Resource Frequency:** While in Central Resource mode (these are only valid when **PCIX_EP#** = 1). 00 = 133 MHz. 01 = 100 MHz. 10 = 66 MHz. 11 = 33 MHz. ***Note:*** 0 = connect to **GND**. 1 = internal pull-up.		
P_INT[D:A]# / XINT[3:0]#/ GPIO[11:8]	• **When using as interrupts and PCIX_EP# = 0:** Act as outputs no termination is required • **When using as interrupts and PCIX_EP# = 1:** 8.2 KΩ pull-up required on each line • **When using as GPIOs:** 8.2 KΩ pull-up required on each line	• **When INTERFACE_SEL_PCIX# = 0:** PCI Interrupt: These outputs are level sensitive. • **When INTERFACE_SEL_PCIX# = 1:** External Interrupt: requests are used by external devices to request interrupt service. These pins are level-detect inputs and are internally synchronized. These pins go to the **XINT[3:0]#** inputs of the Interrupt Controller.		
HPI#, NMI0#, NMI1#, XINT[7:4]#	8.2 KΩ pull-ups			
GPIO[7:0] / XINT[15:8]# / CHAPOUT	8.2 KΩ pull-ups	• General Purpose I/O (default mode). • **External Interrupt:** These pins are level-detects and are internally synchronized. • **CHAPOUT: GPIO[7]** When enabled it will override the normal **GPIO[7]** function.		
SCL0, SDA0, SCL1, SDA1, SCL2, SDA2	• When used external pull-up to **VCC** is required. Refer to the I^2C specification for information on calculating the pull-up. ***Note:*** I^2C port 0 can only used for SEP enclosure management. ***Note:*** I^2C port 1 and port 2 are not available on 413808 and 413812 and must have pull-ups. • 2K pull-up when unused.	The pull-up value is dependent on the bus loading. Refer to the I^2C specification http://www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf		

Table 3. Termination Values Checklist (Sheet 6 of 8)

Signal	Recommendations	Comments	Compliance	
			Yes	No
SMBCLK	**For PCI Express adapter cards:** • When the SMBus is used, there should be isolation device such as the LTC4301 between this signal and **PE_SMCK** on the PCI Express connector. **For PCI Express motherboard applications:** • When SMBus is used a pull-up is required (value is dependent on the loading). • When SMBus is unused, a 8.2 KΩ pull-up is required.	LTC4301 is a hot-swappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website http://www.linear.com/pc/productDetail.do?navId=H0,C1,C1007,C1070,P2460. Refer also to the http://www.smbus.org for the latest specification.		
SMBDAT	**For PCI Express adapter cards:** • When the SMBus is used, there should be isolation device such as the LTC4301 between this signal and **PE_SMDAT** on the PCI Express connector. **For PCI Express motherboard applications:** • When SMBus is used a pull-up is required (value is dependent on the loading). • When SMBus is unused, a 8.2 KΩ pull-up is required.	LTC4301 is a hot-swappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website http://www.linear.com/pc/productDetail.do?navId=H0,C1,C1007,C1070,P2460. Refer also to the http://www.smbus.org for the latest specification.		
U0_RXD, U1_RXD	• The serial console port connector to the **UART0** port must be implemented to assist in debug of Intel transport firmware. • When unused, connect to **GND**. • UART 1 is not available for 413808 and 413812.	***Note:*** **UART0** is dedicated as the debug port for the transport firmware as implemented on Intel development boards.		
U0_TXD, U0_RTS#, U1_TXD, U1_RTS#	• The serial console port connector to the **UART0** port must be implemented to assist in debug of Intel transport firmware. • Can be left unconnected when unused. • **UART1** is not available for 413808 and 413812.	***Note:*** **UART0** is dedicated as the debug port for the transport firmware as implemented on Intel development boards.		
U0_CTS#, U1_CTS#	• The serial console port connector to the **UART0** port must be implemented to assist in debug of Intel transport firmware. • When unused, 8.2 KΩ pull-up. • **UART1** is not available for 413808 and 413812.	***Note:*** **UART0** is dedicated as the debug port for the transport firmware as implemented on Intel development boards.		
TCK	• The JTAG port must be implemented on the board to assist in debug of third party device drivers. • 8.2K pull-up when used. Refer to the JTAG chapter. • **GND** when unused.	**Test Clock:** Provides clock input for IEEE 1149.1 Boundary Scan Testing (JTAG).		

Table 3. Termination Values Checklist (Sheet 7 of 8)

Signal	Recommendations	Comments	Compliance	
			Yes	No
TDI	• The JTAG port must be implemented on the board to assist in debug. • 8.2K pull-up when used. Refer to the JTAG chapter. • NC when unused has weak pull-up.	**Test Data Input:** The JTAG serial input pin.		
TDO	• The JTAG port must be implemented on the board to assist in debug. • When used refer to the JTAG chapter. • NC when unused.	**Test Data Output:** The serial output pin for the JTAG feature.		
TRST#	• The JTAG port must be implemented on the board to assist in debug. • When used refer to the JTAG chapter. • GND when unused.	**Test Reset:** This pin has a weak internal pull-up.		
TMS	• The JTAG port must be implemented on the board to assist in debug. • 8.2 K pull-up when used. Refer to the JTAG chapter. • NC when unused has weak pull-up.	**Test Mode Select:** This pin has a weak internal pull-up.		
WARM_RST#	• When PCI-X interface is used: 1 K pull-up. • When PCI-Express used: This pin is used when the sticky bit functionality is required. In this scenario, the **WARM_RST#** pin must be tied to the system reset **PCI_RST#** signal while the **P_RST#** pin can be tied to the system power good signal.	**Warm Reset** is the same as a cold reset, except sticky configuration bits are ***not*** reset. Notes: - When the PCI Express interface is used as an endpoint, the PCI Express in-band Hot Reset Mechanism can also be used to provide the sticky bit functionality. - On the customer reference board, **WARM_RST#** is tied to the **SRST_N** to provide a JTAG debugger reset. -Driving **WARM_RST#** using any other methods than suggested above may result in unpredictable behavior of the device.		
NC	**No Connect:** pins have no usable function and must not be connected to any signal, power or ground.			
THERMDA	• Connect to the anode of the thermal diode. • **NC** when unused.			

Table 3. Termination Values Checklist (Sheet 8 of 8)

Signal	Recommendations	Comments	Compliance	
			Yes	No
THERMDC	• Connect to the cathode of the thermal diode. • **NC** when unused.			
PUR1	• This pin must be pulled up to **VCC3P3** with an external 8.2 KΩ 5% resistor for proper operation.			
VCCVIO	• For PCI-Express interface: connect to ground. • For PCI-X interface: Connect to 3.3 V.			

3.3 Reset Straps Checklist

Table 4 provides a list of reset straps that are multiplexed on the Peripheral Address Bus **A[24:0]**. These pins are latched on the rising edge of **P_RST#**. All reset strap signals are internally pulled to logic 1 by default. An external 4.7 KΩ 5% pull-down resistor is required to force a logic 0 on these pins.

Table 4. Reset Straps Checklist (Sheet 1 of 2)

Signal	Recommendations	Comments	Compliance	
			Yes	No
BOOT_WIDTH_8#	0 = 8 bits wide, 0 = 4.7 KΩ resistor pull down. 1 = 16 bits wide (Default mode internal pull-up).	***Note:*** Muxed onto signal **A[0]**.		
CFG_CYCLE_EN#	0 = Configuration Cycles enabled, 0 = 4.7 KΩ resistor pull down. 1 = Configuration Retry enabled (Default mode internal pull-up).	***Note:*** Muxed onto signal **A[1]**.		
HOLD_X0_IN_RST#	0 = Hold Scale in reset, 0 = 4.7 KΩ resistor pull down. 1 = Do not hold in reset (Default mode internal pull-up).	***Note:*** Muxed onto signal **A[2]**.		
HOLD_X1_IN_RST#	0 = Hold in reset, 0 = 4.7 KΩ resistor pull down. 1 = Do not hold in reset (Default mode internal pull-up).	***Note:*** Muxed onto signal **A[3]**.		
EXT_ARB#	Requires a 4.7 K ohms resistor pull down.	***Note:*** Muxed onto signal **A[6]**. ***Note:*** This signal must always be pulled down.		
INTERFACE_SEL_PCIX#	• For PCI Express -No connect. • For PCI-X - Requires a 4.7K ohms resistor pull down.	**Interface Select PCI-X:** determines which ATU is function 0. 0 = 4.7 KΩ resistor pull down. 1 = internal pull up. ***Note:*** Muxed onto signal **A[10].**		
PCIX_EP#	For PCI-X endpoint: **Requires a** 4.7 KΩ resistor pull down.	**413808 and 413812 operates as in PCI-X End Point mode.** ***Note:*** muxed onto signal **A[11].**		
PCIE_RC#	No connect.	**413808 and 413812 operates as in endpoint mode only (default with internal pull-up).** ***Note:*** muxed onto signal **A[12].**		
SMB_A5, **SMB_A3**, **SMB_A2**, **SMB_A1**	Refer to comments.	**SM Bus Address:** maps to address bits 5, 3, 2, and 1 where bits[7:0] represent the address the SMBus slave port will respond to when access is attempted. 0 = address bit will be low. 1 = address bit will be high (Default mode). ***Note:*** **SMB_A5** muxed onto signal **A[16]**. ***Note:*** **SMB_A3** muxed onto signal **A[15]**. ***Note:*** **SMB_A2** muxed onto signal **A[14]**. ***Note:*** **SMB_A1** muxed onto signal **A[13]**. 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
PCIX_PULLUP#	When pulled-low enables the following signal pull-ups: **P_AD[63:32]**, **P_C/BE[7:4]#**, **P_PAR64**, **P_REQ64#**, **P_ACK64#**, **P_FRAME#**, **P_IRDY#**, **P_TRDY#**, **P_STOP#**, **P_DEVSEL#**, **P_SERR#**, **P_PERR#**, **P_INT[D:A]#**	**PCI-X Pull Up:** 0 = enable PCI pull up resistors. 1 = disable PCI pull up resistors (Default mode). ***Note:*** Muxed onto signal **A[17].** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		

Table 4. Reset Straps Checklist (Sheet 2 of 2)

Signal	Recommendations	Comments	Compliance	
			Yes	No
PCIX_32BIT#	When 32 PCI-X bus enabled the following signals have internal pull-ups: **P_AD[63:32]**, **P_C/BE[7:4]#** and **P_PAR64** and can be left as **NC**.	**32-Bit PCI-X Bus:** 0 = 32 bit wide PCI-X bus. 1 = 64 bit wide PCI-X bus. (Default mode). ***Note:*** Muxed onto signal **A[18].** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
PCIXM1_100#	Refer to comments.	**PCI-X Mode 1 100 MHz Enable:** 0 = limit PCI-X mode 1 to 100 MHz 1 = 133 MHz enabled (Default mode) ***Note:*** Muxed onto signal **A[19].** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
HS_SM#	Refer to comments.	Hot-Swap **Startup Mode:** 0 = Hot-Swap mode enabled. 1 = Hot-Swap mode disabled (Default mode). ***Note:*** Muxed onto signal **A[21]** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
FW_TIMER_OFF#	Refer to comments.	**Firmware Timer Off:** 0 = firmware timer disabled. 1 = firmware timer enabled (Default mode). ***Note:*** Muxed onto signal **A[22]** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
CONTROLLER_ONLY#	4.7 KΩ resistor pull down.	Controller-Only Enable: 0 = Controller only, RAID disabled. 1 = RAID enabled (default mode) this is not supported in 413808 and 413812. **NOTE:** Muxed onto signal **A[23].**		
DF_SEL[2:0]	413808 and 413812 configurations: • Single-core 8-port DF_SEL[2:0] = 000. • Dual-core 8-port DF_SEL[2:0] = 100.	DF_SEL[2:0] configurations set as follows: 0 = 4.7 KΩ resistor pull down. 1 = internal pull up and can be **NC**.		
CLK_SRC_PCIE#	Refer to comments.	**Clock Source PCI-E:** selects the PCI Express Refclk pair as the input clock to the PLLs that control most internal logic. 0 = source clock is **REFCLKP/REFCLKN**. 1 = source clock comes from the active PCI interface (Default mode). ***Note:*** Muxed onto signal **PWE#** 0 = 4.7 KΩ resistor pull down. 1 = internal pull up.		
LK_DN_RST_BYPASS#	Use for PCI Express mode.	Link Down Reset Bypass: Disables the full chip reset that would normally be caused by a Link Down or hot reset. 0 = Do not reset on Link Down. 1 = Reset on Link Down (default mode). Muxed onto signal **A[24]**		
PCE[1:0]#	Pull up both these signals with 8.2K resistor.	These pins are muxed onto signal **PCE[1:0]#**.		

Table 5 provides the reset strap configuration for valid operational modes of the chip: PCI Express endpoint or PCI-X endpoint modes.

Table 5. PCI Express/PCI-X Strap Configuration Table

Endpoint Configuration	Strapping Settings			
	CONTROLLER_ONLY#	INTERFACE_SEL_PCIX#	PCIE_RC# (PCI Express root Complex strap)	PCIX_EP# (PCIX endpoint strap)
PCI Express endpoint	0	1	1	X
PCI-X endpoint	0	0	X	0

3.4 Analog Filter Checklist

This section describes filters needed for the PLL circuitry. Table 6 lists the PLLs that are required for this part.

Table 6. Required PLLs

Interface	Filtered Voltage	VCC PLL Balls	VSS PLL Balls	Layout Guideline Table
Storage	1.2 V	VCC1P2PLLS0	VSSPLLS0	Table 7
		VCC1P2PLLS1	VSSPLLS1	
PCI-X	1.2 V	VCC1P2PLLP	VSSPLLP	Table 8
Core Digital Logic	1.2 V	VCC1P2PLLD	VSSPLLD	Table 8
Intel XScale® michroarchitecture and internal bus logic	3.3 V	VCC3P3LLX	VSSPLLX	Table 9

3.4.1 VCC1P2PLLS0, VCC1P2PLLS1 Filter Requirements

The lowpass filter, as shown in Figure 1 reduces noise induced clock jitter and its effects on timing relationships in system designs. The Figure 1 filter circuit is recommended for the two PLL pairs:

- **VCC1P2PLLS0** - **VSSPLLS0**.
- **VCC1P2PLLS1** - **VSSPLLS1** pairs.

The filter has the following characteristics:

- the purpose of this filter is to achieve at least 10 dB rejection of frequencies between 1 and 20 MHz.
- the filter components are selected to achieve a corner frequency of 100 KHz.
- the minimum voltage into the filter must be ≥ 1.14 V.
- the current draw for these pins is less than 85 mA.

Figure 1. VCC1P2PLLS0, VCC1P2PLLS1 Configuration

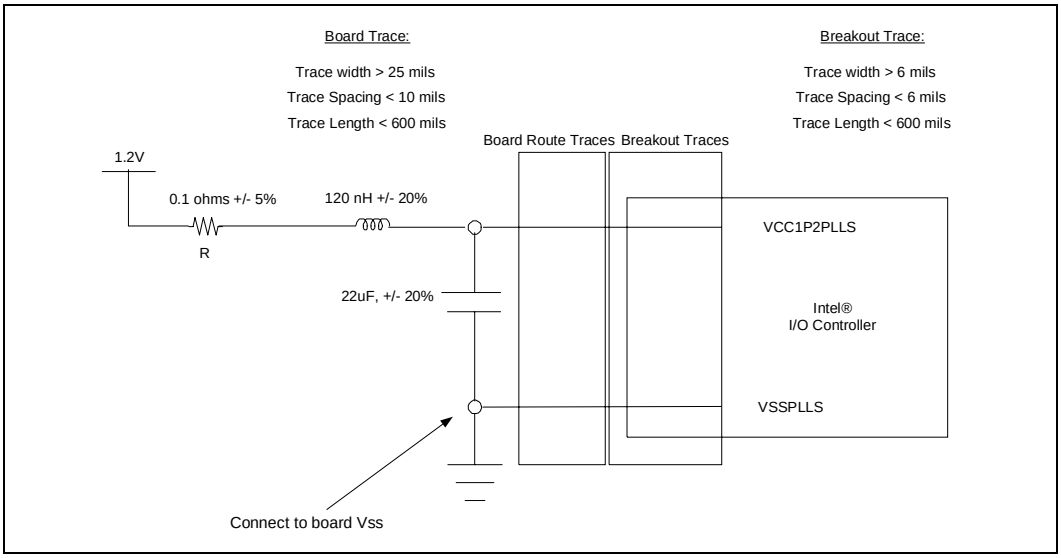


Table 7. $V_{CC1P2PLLS0}$, $V_{CC1P2PLLS1}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground. • **VCC1P2PLLS0**, **VSSPLLS0** and **VCC1P2PLLS1**, **VSSPLLS1** traces must be ground referenced (no V_{CC} references).
Inductor	• 120 nH +/- 20%. • L must be magnetically shielded. • ESR: max < 0.3 Ω. • rated at 45 mA.
Capacitor	• 22 µF +/- 20% (Capacitor). • ESR: max < 0.3 Ω. • ESL < 2.5 nH. • Place 22 µF capacitor as close as possible to package pin.
Resistor	• 0.1 +/- 5% (resistor). • resistor must be placed between V_{CC1P2} and L. • Note: when trace resistance is large enough a discrete resistor is not required.
Breakout Trace	• Trace Width > 6 mils. • Trace Spacing < 6 mils. • Trace Length < 600 mils.
Board Trace	• Trace Width > 25 mils. • Trace Spacing < 10 mils. • Trace Length < 600 mils.
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	1.2″
Routing Guideline 1	Route **VCC1P2PLLS** and **VSSPLL** as differential traces.
Routing Guideline 2	The nodes connecting **VCC1P2PLLS** and the capacitor must be as short as possible.
Routing Guideline 3	The 1.2 V supply regulator used for the PLL filter must have less than +/- 3% tolerance.

3.4.2 VCC1P2PLLP, VCC1P2PLLD Filter Requirements

The low-pass filter (as shown in Figure 2, "VCC1P2PLLD, VCC1P2PLL Low-Pass Filter Configuration" on page 20) reduces noise-induced clock jitter and its effects on timing relationships in system designs. The Figure 2 filter circuit is recommended for each of the PLL pairs:

- **VCC1P2PLLP–VSSPLLP**.
- **VCC1P2PLLD–VSSPLLD** pairs.

Note: **VCC1P2PLLP** and **VSSPLLP** pins can be connected to ground when PCI-X interface is not used.

Figure 2. VCC1P2PLLD, VCC1P2PLL Low-Pass Filter Configuration

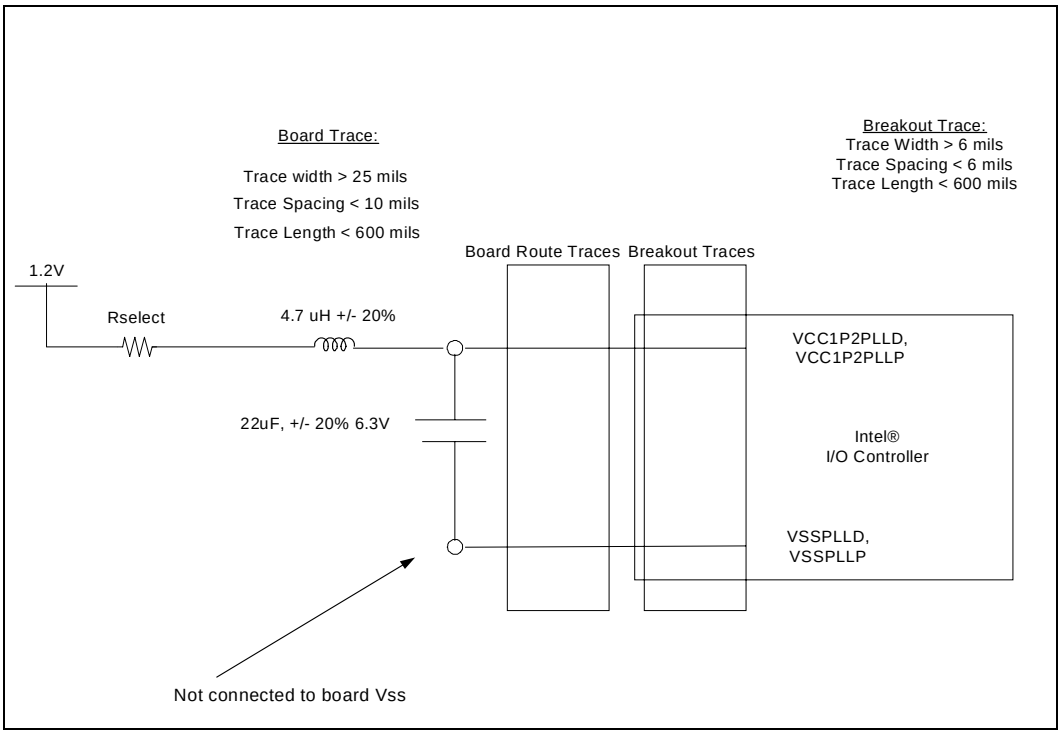


Table 8. $V_{CC1P2PLLP}$, $V_{CC1P2PLLD}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground. • **VCC1P2PLLP**, **VCC1P2PLLD** traces must be ground referenced (no V_{CC} references).
Inductor	• 4.7 µH +/- 25%. • L must be magnetically shielded. • ESR: max < 0.3 Ω. • rated at 45 mA.
Capacitor	• 22 µF +/- 20% 6.3 V (Capacitor). • ESR: max < 0.3 Ω. • ESL < 2.5 nH. • Place 22 µF capacitor as close as possible to package pin.
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 1.2 V plane to the top end of the capacitor is > 0.35 Ω (including board and component resistance). • 1.2 V plane to $V_{CC1P2PLL}$ < 1.5 Ω. • 1/16 W 6.3 V. • resistor must be placed between V_{CC1P2} and L. • Note: when trace and component resistance is large enough the discrete resistor is not required.
Breakout Trace	• Trace Width > 6 mils. • Trace Spacing < 6 mils. • Trace Length < 600 mils.
Board Trace	• Trace Width > 25 mils. • Trace Spacing < 10 mils. • Trace Length < 600 mils.
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	1.2″
Routing Guideline 1	Route **VCC1P2PLLD** and **VSSPLLD**, **VCC1P2PLLP** and **VSSPLLP** as differential traces.
Routing Guideline 2	The nodes connecting **VCC1P2PLLD** and the capacitor, **VCC1P2PLLP** and the capacitor must be as short as possible.
Routing Guideline 3	The 1.2 V supply regulator used for the PLL filter must have less than +/- 3% tolerance.

3.4.3 VCC3P3LLX PLL Requirements

To reduce clock skew, a PLL is implemented for Intel XScale® processor. The balls associated with this PLL are **VCC3P3LLX** and **VSSPLLX**. The lowpass filter, as shown in Figure 3, reduces noise induced clock jitter and its effects on timing relationships in system designs. The node connecting **VCC3P3LLX** and the capacitor must be as short as possible.

The filter has the following characteristics:

- The filter components must be able to handle a DC current of 30 mA.
- < 0.2 dB gain in pass band and < 0.5 dB attenuation in pass band < 1 Hz. Passband is DC through 1 Hz.
- > 34 dB attenuation from 1 MHz to 66 MHz.
- > 28 dB attenuation from 66 MHz to core frequency.

Figure 3. VCC3P3LL Filter Configuration

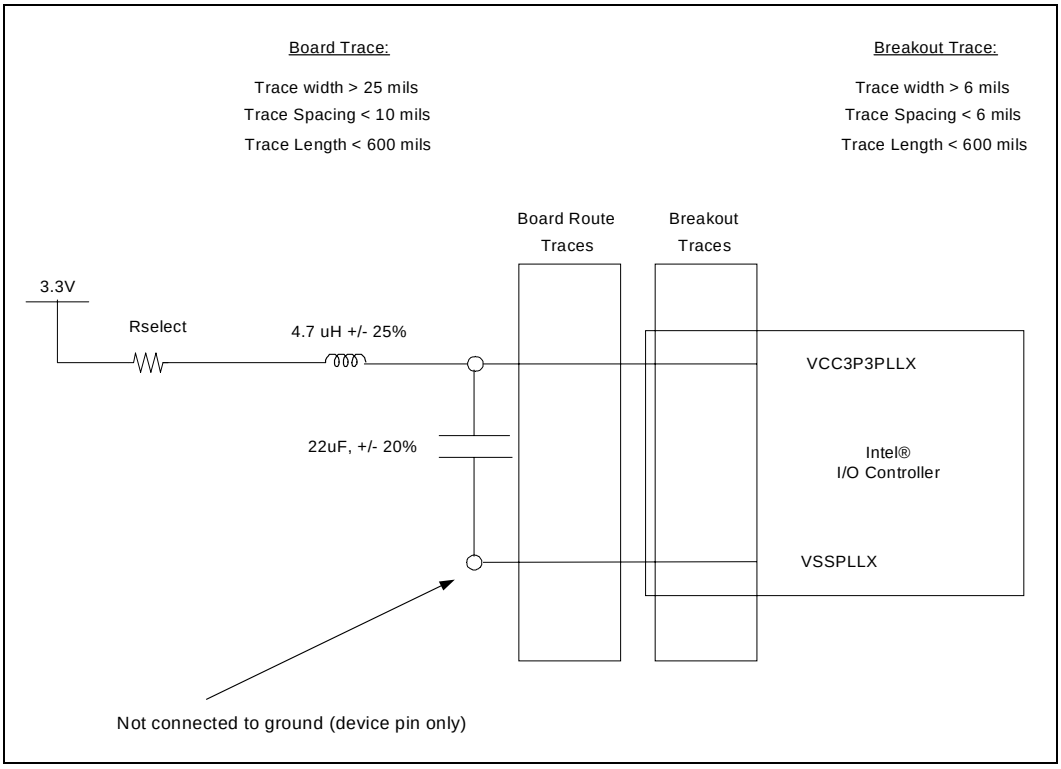


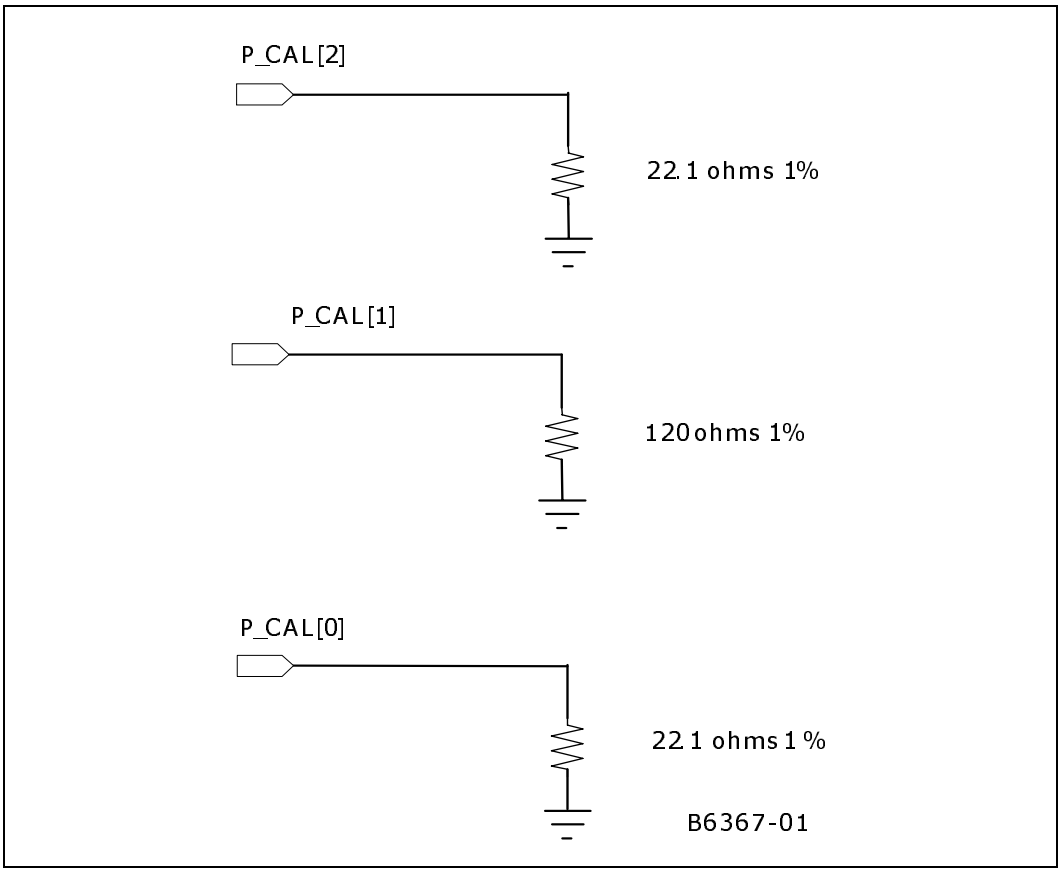
Table 9. $V_{CC3P3PLL}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground referenced. • **VCC3P3LL** and **VSSPLLX** traces must be ground referenced (no V_{CC} references).
Inductor	• 4.7 µH. • L must be magnetically shielded. • ESR: max < 0.4 Ω. • rated at 45 mA. • An example of this inductor is TDK part number MLZ2012E4R7P.
Capacitor	• 22 µF (Capacitor). • ESR: max < 0.4 Ω. • ESL < 3.0 nH. • Place 22 µF capacitor as close as possible to package pin.
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 3.3 V plane to the top end of the capacitor is > 0.35 Ω. • 3.3 V plane to $V_{CC3P3PLL}$ < 1.5 Ω. • resistor ratings: 1/16 W 6.3 V. • resistor must be placed between V_{CC3P3} and L. ***Note:*** When trace and component resistance is large enough the discrete resistor is not required.
Breakout Trace	• Trace Width > 6 mils. • Trace Spacing < 6 mils. • Trace Length < 600 mils.
Board Trace	• Trace Width > 25 mils. • Trace Spacing < 10 mils. • Trace Length < 600 mils.
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	1.2 inches
Routing Guideline 1	Route **VCC3P3LLX** and **VSSPLLX** as differential traces.
Routing Guideline 2	The nodes connecting **VCC3P3LL** and the capacitor must be as short as possible.

3.5 PCI Resistor Calibration

Figure 4 shows the termination required for the PCI calibration circuitry. PCI Calibration pins **P_CAL[1:0]** are connected to an external calibration resistors. The PCI output drivers can reference the resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations.

Figure 4. PCI Resistor Calibration



3.6 PCI Express Resistor Compensation

Figure 5 shows the termination required for the PCI Express RCOMP circuit.

Figure 5. PCI Express RCOMP

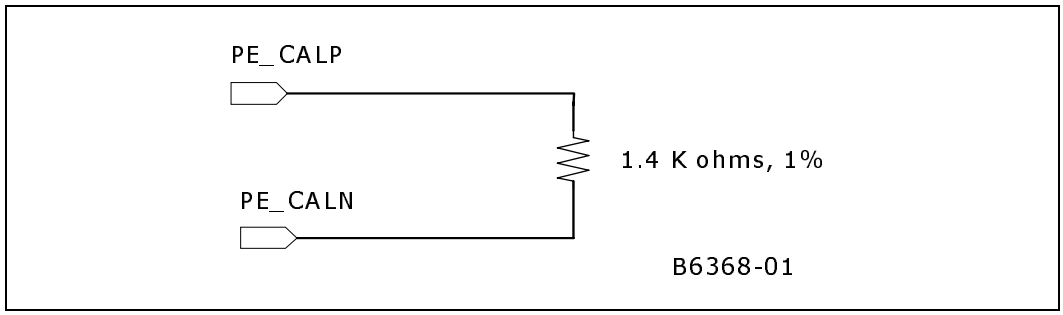


Figure 6. Memory Calibration Circuitry

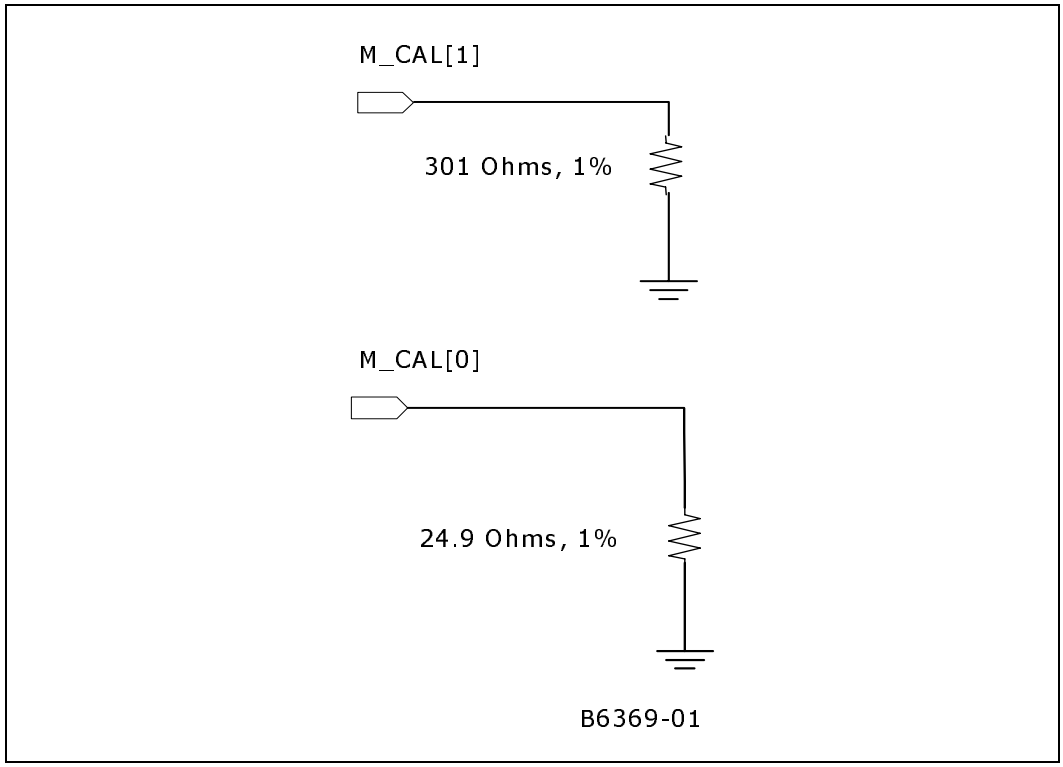


Figure 7 provides a diagram on how to connect the **RBIAS0** and **RBIAS_SENSE0** pins. **RBIAS1** and **RBIAS_SENSE1** must be connected in the same manner.

Figure 7. RBIAS0, RBIAS_SENSE0 Connections