Intel® 81348 I/O Processor

Design Guide

May 2007

Order Number: 315053-002US

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Revision History

Date	Revision	Description
May 2007	002	Updated product naming conventions and fixed links
September 2006	001	Initial release.

1.0 Introduction

1.1 About This Document

This document provides layout information and guidelines for designing platform or add-in board applications with Intel® 81348 I/O Storage Processor (81348).

It is recommended that this document be used as a guideline. Intel recommends employing best-known design practices using board-level simulation, signal integrity testing and validation to create a robust design. Designers note that this guide focuses on specific design considerations for this part and is not intended to be an all-inclusive list of good design practices. It is recommended that this guide is used in conjunction with empirical data to optimize the particular design.

The simulation conditions used for each of the interfaces are listed in the Appendix. The simulations were performed for motherboard and adapter card topologies. The impedance used for the motherboard is 50 ohm +/- 15% and the adapter card trace impedance is 60 ohm +/- 15%. These results are based on the six layer board stackup that is provided in Chapter 3.0.

1.2 Intel® 81348 I/O Storage Processor Document Details

This document is partitioned into the following chapters:

- The top level block diagram and package dimensions are provided in Chapter 2.0, "Package Information".
- The example stackups for a motherboards and adapter cards are provided in Chapter 3.0, "Board Layout Guidelines".
- The layout guidelines external interfaces are listed in the following chapters: Chapter 6.0, "PCI-X Layout Guidelines", Chapter 5.0, "PCI Express Layout", Chapter 4.0, "Memory Controller", Chapter 7.0, "SATA/SAS Bus Layout", and Chapter 8.0, "Peripheral Local Bus".
- The required terminations are listed in Chapter 12.0, "Terminations". This chapter also details the recommended filtering.
- The summary of the layout guidelines for each of the interfaces and the filters is listed in Chapter 13.0, "Layout Checklist".
- The details on power sequencing and decoupling recommendations are provided in Chapter 9.0, "Power Delivery".
- The JTAG information is listed in Chapter 10.0, "JTAG Circuitry for Debug". The details on test equipment are listed in Chapter 11.0, "Debug and Test".
- The references are listed in Chapter 14.0, "References".
- The definitions and the simulation conditions (used for all the simulations described in this document) are provided in Appendix A.
- The details on the recommended heatsink solutions are listed in the Thermal Application Note.

1.3 About the Intel® 81348 I/O Storage Processor

The 81348 is an I/O storage processor that integrates two Intel XScale® microarchitectures with intelligent peripherals including a PCI bus application bridge and eight Serial-Attached SCSI (SAS) Engines. 81348 also supports two internal busses: North XSI bus and South XSI bus. With the two internal busses, transactions takes place simultaneously on each bus. The north XSI bus provides the two Intel XScale® microarchitectures with low latency access to the DDR SDRAM Memory Controller, the on-chip SRAM Memory Controller, and the SAS Engines control registers. Peripherals that generate large burst transactions are located on the south XSI bus, thus allowing the two Intel XScale® microarchitectures exclusive access to the north XSI bus.

The 81348 consolidates the following features into a single system:

- Two Intel XScale® microarchitectures running at speed up to 1.2 GHz
- Eight Serial-Attached SCSI Links or Eight Serial ATA links
- PCI - Local Memory Bus Address Translation Unit, function 0 programming interface
- Messaging Unit, function 0 programming interface
- Third Party Messaging Interface (TPMI), function 1 programming interface
- Application Direct Memory Access (DMA) Controllers
- Transport DMA Controllers
- Peripheral Bus Interface Unit
- Integrated DDR2 Memory Controller
- Integrated SRAM Memory Controller
- Performance Monitor
- Application Accelerator
- Two Programmable Timers per Intel XScale® microarchitecture
- Watchdog Timer per Intel XScale® microarchitecture
- Three I^2C Bus Interface Units
- Two Serial Port Units
- Eight General Purpose Input Output (GPIO) ports
- Sixteen General Purpose Output - two per SAS Engine
- Internal North Bus-South Bus Bridge

This integrated processor addresses the needs of intelligent I/O Storage applications and helps reduce intelligent I/O system costs.

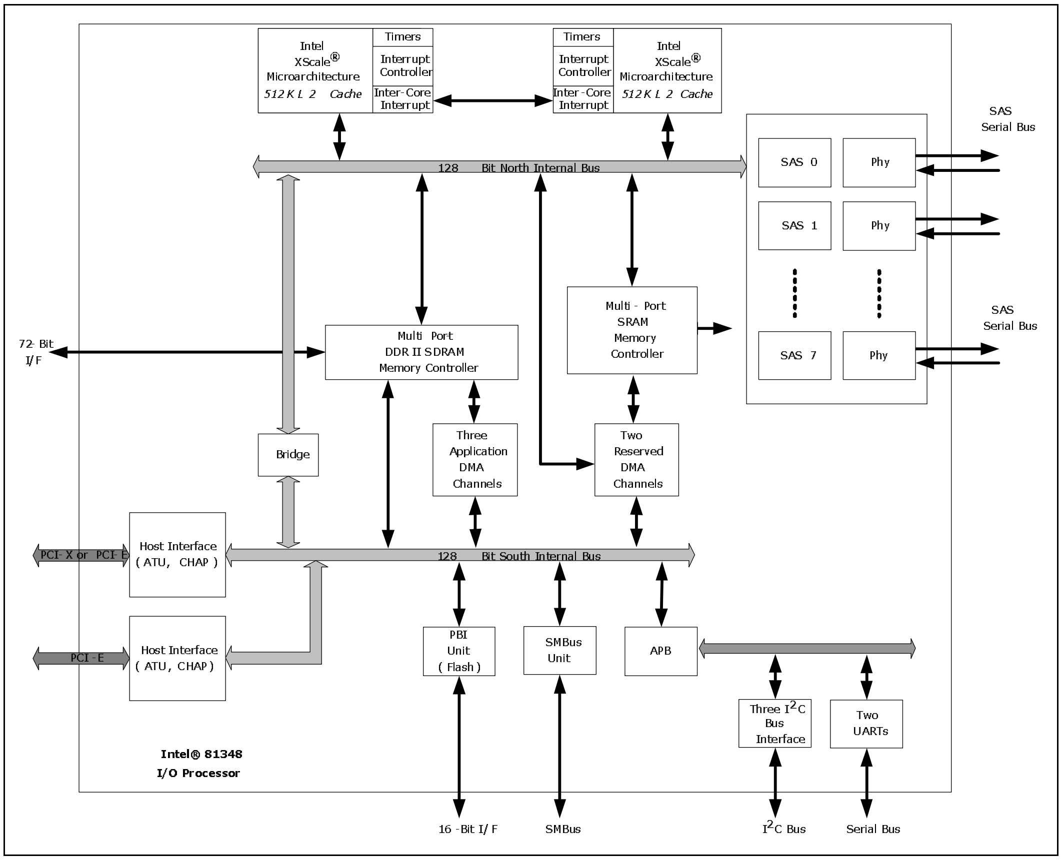
The 81348s PCI Bus is capable of 133 MHz operation in PCI-X mode as defined by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0b. Also, the processor supports a 66 MHz conventional PCI mode as defined by the *PCI Local Bus Specification* Revision 2.2. The 81348 supports PCI Express interface lane widths of x1, x2, x4 and x8.

The 81348 is available as a single interface or a dual interface version. The single interface version support either PCI-X 1.0b or PCI Express*. The interface is selected by using reset straps. The dual interface version supports both PCI-X 1.0b and PCI Express.

When PCI-X 1.0b is selected as the upstream (host) I/O interface, PCI Express is available as a private (not visible to the host), downstream I/O interface. Likewise, when PCI Express is selected as the upstream I/O interface, PCI-X 1.0b is available as a private, downstream I/O interface. The selection of the upstream I/O interface is a reset strap option.

Figure 1 is a block diagram of the 81348.

Figure 1. Intel® 81348 I/O Storage Processor Functional Block Diagram



2.0 Package Information

2.1 Package Introduction

Intel® 81348 I/O Processor is offered in a 1357-ball FCBGA5 package. This package is shown in Figure 2. Figure 3 shows the top view of the package with the interfaces labeled and color coded. This figure is helpful during board layout. The signals are located on the FCBGA package to simplify signal routing and system implementation.

Figure 2. Intel® 81348 I/O Processor 1357-ball FCBGA Package Diagram

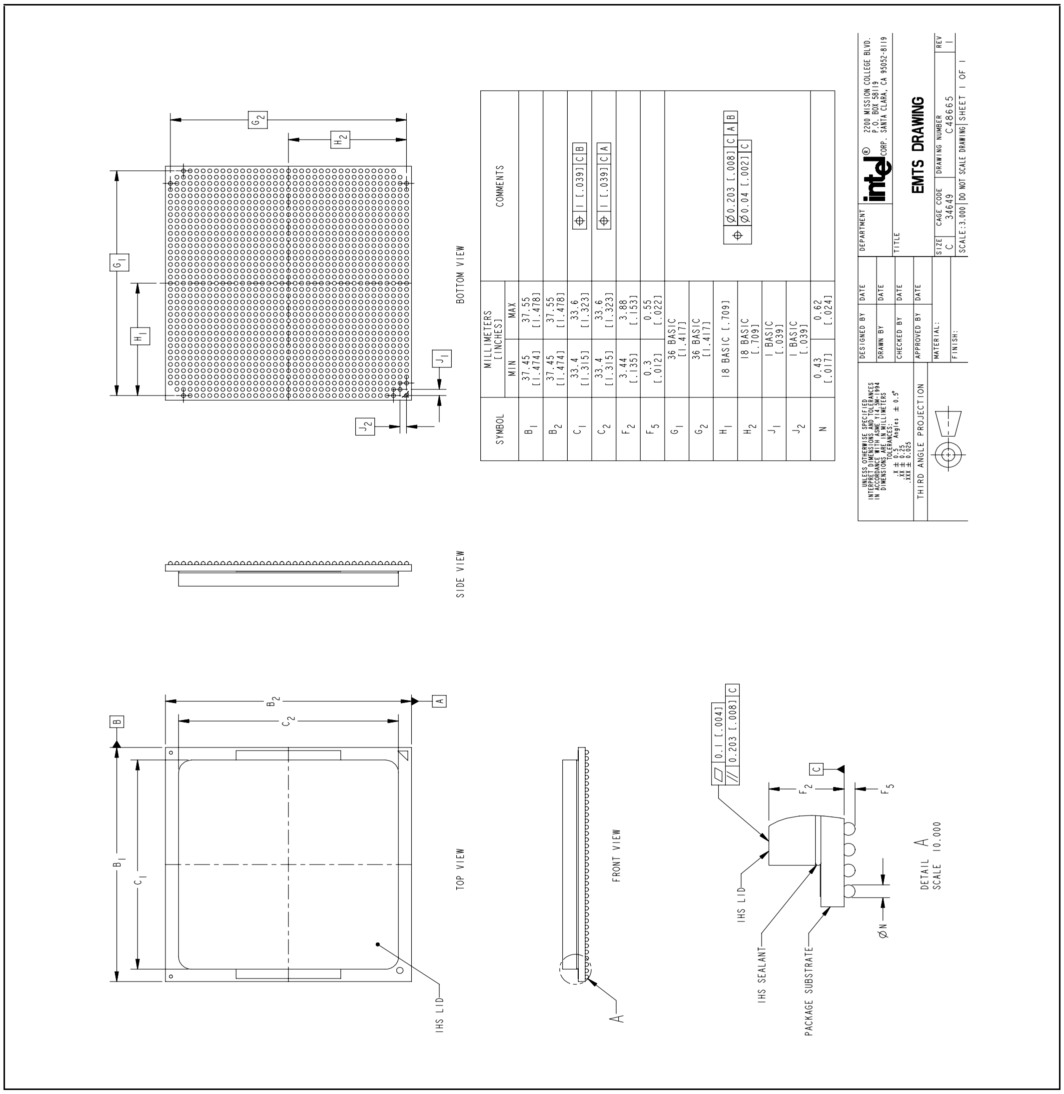
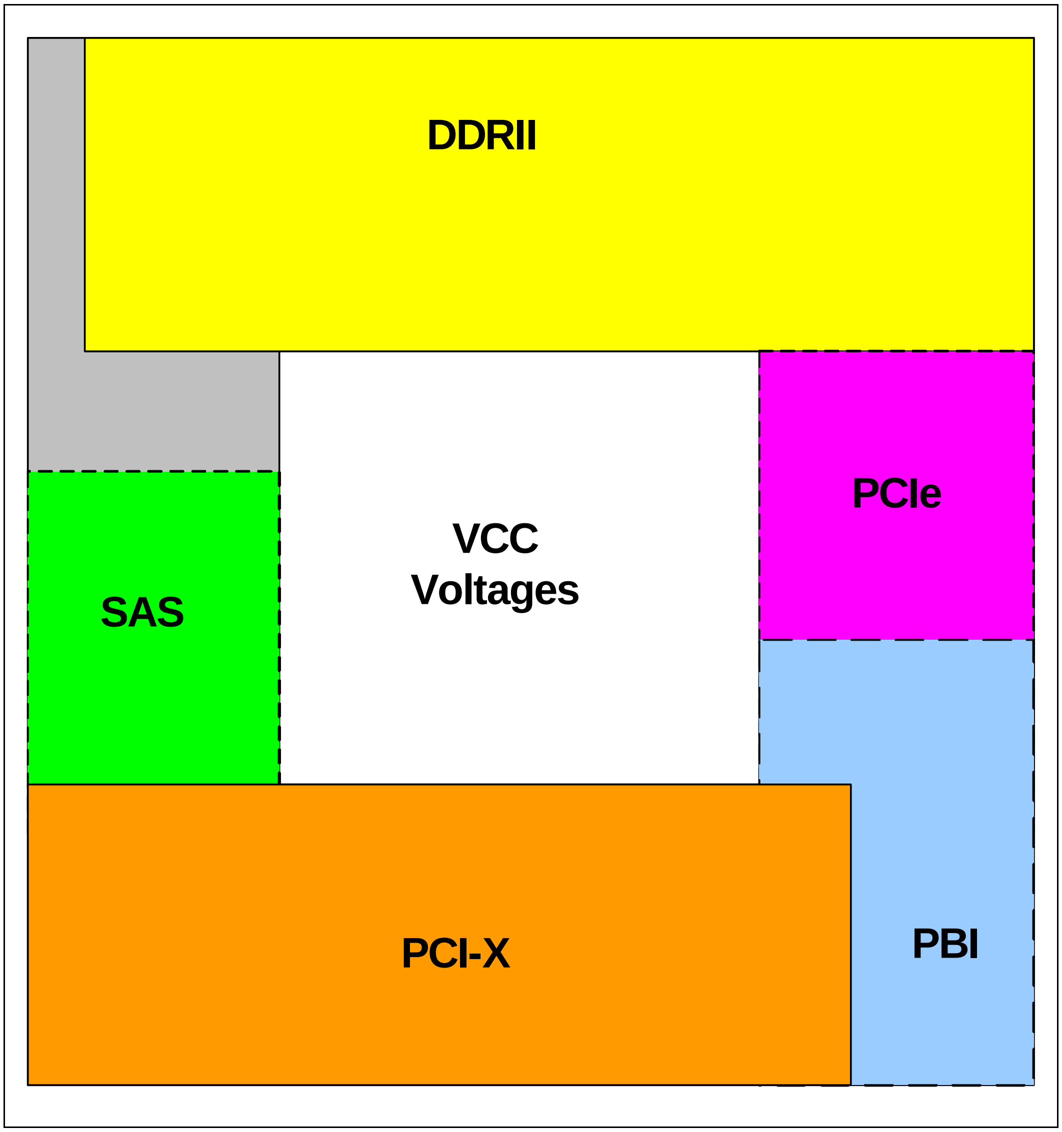


Figure 3. Top View Ball Map Interfaces



3.0 Board Layout Guidelines

This chapter provides an example of a motherboard and a adapter card stackup implementation. This stackup was used for all simulations listed in this design guide. It is highly recommended that signal integrity simulations be conducted to verify each PCB layout. This is especially true when the layout deviates from the recommendations listed in these design guidelines.

3.1 Motherboard Stack Up Information

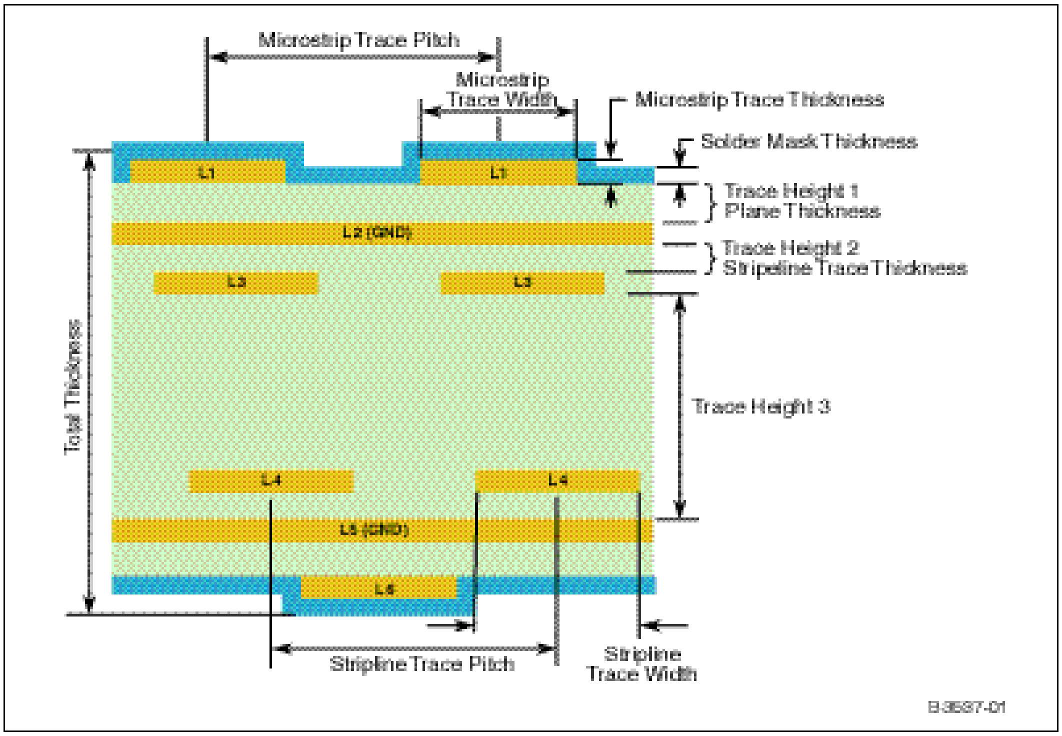
In this design guide the motherboard stack up example isIn this design guide the motherboard stack up example is when the Intel® 81348 I/O Processor is used in server and workstation Raid On Mother Board (ROMB) applications, the motherboard is implemented on six layers. The specified impedance range for all board implementations is 50ohms +/-15%. Adjustments are made for interfaces specified at other impedances. Table 1 defines the typical layer geometries for a six layer board.

The motherboard impedance guidelines are based on the typical server/workstation impedance for their processor and memory subsystem of 50-ohms. Dimensions and tolerances for the motherboard are listed in Table 1. Refer to Figure 4 for location of variables in Table 1.

Table 1. Motherboard Stack Up, Stripline and Microstrip

Variable	Type	Nominal	Minimum	Maximum	Notes
Solder Mask Thickness (mil)	N/A	0.8	0.6	1.0	
Solder Mask E_r	N/A	3.65	3.65	3.65	
Core Thickness (mil)	N/A	9.8	9.6	10	
Core E_r	N/A	4.30	3.75	4.85	2113 material
Plane Thickness (mil)	Power	2.7	2.5	2.9	
	Ground	1.35	1.15	1.55	
Trace Height (mil)	1	3.5	3.3	3.7	The trace height is determined to achieve a nominal 50 ohms.
	2	3.5	3.3	3.7	
	3	10.5	9.9	11.1	
Preg E_r	Microstrip	4.30	3.75	4.85	
	Stripline1	4.30	3.75	4.85	
	Stripline2	4.66	4.19	5.13	
Trace Thickness (mil)	Microstrip	1.75	1.2	2.3	
	Stripline	1.4	1.2	1.6	
Trace Width (mil)	Microstrip	5.0	3.5	6.5	
	Stripline	4.0	2.5	5.5	
Trace Spacing (mil)	Microstrip	15.0	-	-	Each interface sets the trace spacing based on its signal integrity of differential impedance requirements. For the purposes of the building the transmission line models, it is assumed the artwork is very accurate and therefore a constant. Thus, all the variability in the trace spacing is the result of the tolerances of the trace width.
	Stripline	12.0	-	-	
Total Thickness (mil)	FR4	62.0	56.0	68.0	
Trace Velocity (ps/in)	Microstrip		135	141	Velocity varies based on variation in Er. It cannot be controlled during the fab process.
	Stripline		167	178	
Trace Impedance (ohms)	Microstrip	50	42.5	57.5	
	Stripline	50	45	55	

Figure 4. Motherboard Stackup Recommendations



3.2 Adapter Card Topology

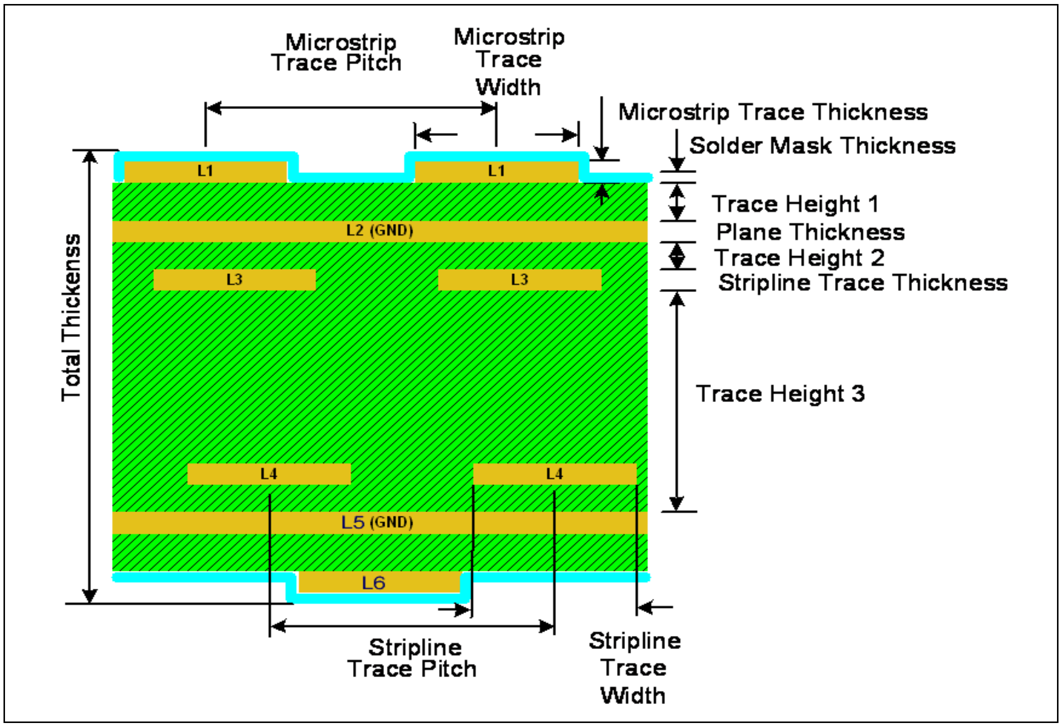
Intel® 81348 I/O Processor is implemented on PCI Express or PCI-X adapter cards with six layers. The specified impedance range for all adapter card implementations is 60ohms +/-15%. Table 2 defines the typical layer geometries for a six layer board. Note that the values are the same as the motherboard stack up with the exception of the impedance.

Table 2. Adapter Card Stack Up, Microstrip and Stripline

Variable	Type	Nominal	Minimum	Maximum	Notes
Solder Mask Thickness (mil)	N/A	0.8	0.6	1.0	
Solder Mask E_r	N/A	3.65	3.65	3.65	
Core Thickness (mil)	N/A	2.8	3.0	3.2	
Core E_r	N/A	4.3	3.75	4.85	2113 material
Plane Thickness (mil)	Power	2.7	2.5	2.9	
	Ground	1.35	1.15	1.55	
Trace Height (mil)	1	3.5	3.3	3.7	The trace height is determined to achieve a nominal 60 ohms.
	2	7.0	6.7	7.3	
	3	7.0	6.7	7.3	
Preg E_r	Microstrip	4.30	3.75	4.85	2113 material
	Stripline1	4.30	3.75	4.85	
	Stripline2	4.66	4.19	5.13	
Trace Thickness (mil)	Microstrip	1.75	1.2	2.3	
	Stripline	1.4	1.2	1.6	
Trace Width (mil)	Microstrip	4.0	2.5	5.5	
	Stripline	4.0	2.5	5.5	
Total Thickness (mil)	FR4	62.0	56.0	68.0	
Trace Velocity (ps/in)	Microstrip		135	141	Velocity varies based on variation in Er. It cannot be controlled during the fab process.
	Stripline		167	178	
Trace Impedance	Microstrip	60	51	69	
	Stripline	60	51	69	

Note: Each interface sets the trace spacing based on its signal integrity of differential impedance requirements. For the purposes of the building the transmission line models, it is assumed the artwork is very accurate and therefore a constant. Thus, all the variability in the trace spacing is the result of the tolerances of the trace width.

Figure 5. Adapter Card Stackup



3.3 PCB Impedance Targets

Table 3 and Table 4 provide impedance ranges and the associated trace dimensions for single-ended and differential traces. Figure 4 shows an example of a differential trace.

Table 3. Single-ended Trace Parameters

Single Line						
Topology	Ohms	Actual Impedance Range			Width (mils)	Spacing (mils)
		Min	Max	Nominal		
Stripline	50	44.17	57.47	50.82	4	N/A
Stripline	60	51.16	66.62	58.89	4	N/A
Microstrip	50	42.97	57.46	50.22	5	N/A
Microstrip	60	51.30	67.89	59.60	4	N/A

Table 4. Differential Trace Dimensions

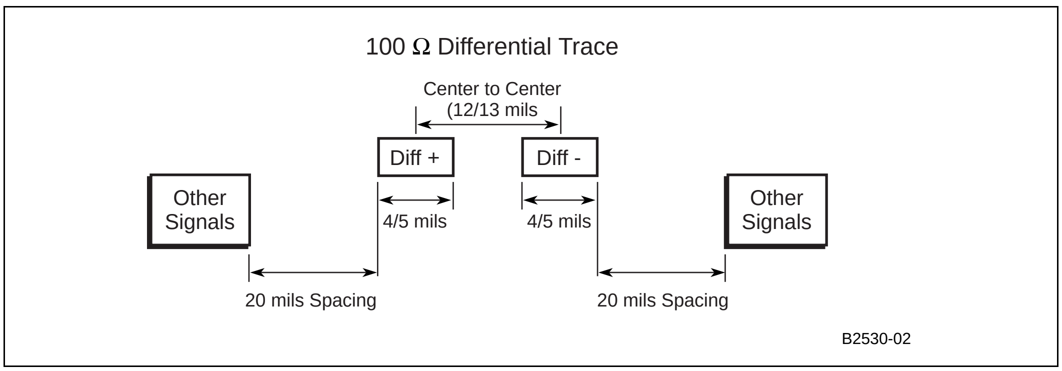
Differential Pair						
Topology	Ohms	Actual Impedance Range			Width (mils)	Edge to edge Spacing (mils)
		Min	Max	Nominal		
Stripline	85	74.24	102.28	92	4	8
Stripline	100	87.06	121.84	100	4	8
Microstrip	85	71.56	119.36	88	5	7
Microstrip	100	80.36	114.28	100	4	8

3.3.1 100 Ohm Differential Trace

The Figure 6 shows a 100 ohm differential trace constructed from various topologies based on the stackup listed in this chapter. These differential traces are used to route the DQS and clock lines.

1. Using two striplines of trace width 4 mils separated by 8 mils edge to edge (12 mils center to center).
2. Using two microstrips of trace width 5 mils separated by 8 mils edge to edge (13 mils center to center).

Figure 6. An Example of 100 Ohm Differential Trace



4.0 Memory Controller

This chapter describes how to layout the physical memory interface for Intel® 81348 I/O Processor.

4.1 Overview

The Intel® 81348 I/O Processor integrates a high performance, multi-ported memory controller to provide a direct interface between Intel® 81348 I/O Processor and its local memory subsystem. The Memory Controller supports:

- PC3200 and PC4300 Double Data Rate II (DDR2) Registered and Unbuffered DDR2 400MHz and DDR2 533MHz SDRAM
- 512 Mbit and 1 Gbit DDR2 SDRAM technology support
- Registered and Unbuffered DDR2 DIMM support
- Dedicated port for Intel XScale® microarchitectures to DDR2 SDRAM
- Between 256 MBytes and 2 GBytes of 64-bit DDR2 SDRAM
- 36-bit addressable
- Optimized core processor data processing 32-bit region
- Generation and/or Verification of Block Guard Data Integrity fields embedded in the data stream
- Single-bit error correction, multi-bit detection support (ECC)
- 32-, 40- and 64-, 72-bit wide Memory Interfaces (non-ECC and ECC support)
- The memory controller provides two chip enables to the memory subsystem. These two chip enables service the DDR2 SDRAM subsystem (one per bank).
- For 64-bit ECC memory, a 32-bit memory region are programmed to operate as 32-bit ECC memory for higher core write performance by avoiding Read-Modify-Write (RMW) operation of DDR2 SDRAM.
- One or two banks of DDR2 SDRAM (in the form of one two-bank dual inline memory module).

4.2 DDR2 533 Layout Guidelines

This section provides the DDR2 533 layout guidelines for both DIMM topology (for motherboard and adapter card topologies) and embedded memory down (for motherboard topology). For a DDR2 400 layout the same DDR2 533 layout guidelines are used.

- Section 4.2.2 provides details on the DDR2 533 DIMM routing guidelines.
- Section 4.2.3 provides details on the DDR2 533 embedded routing guidelines.

4.2.1 DDR2 533 DIMM Layout Guidelines

This section provides the layout guidelines for a DIMM topology for DDR2 533.

The DDR interface is divided up into three groups that each have special routing guidelines:

1. Source synchronous signal group: DQ/DQS/DQM/CB signals, Section 4.2.2.1.
2. Clocked: M_CLK signals, 6 clocks, three positive (**M_CK[2:0]**) and three negative (**M_CK[2:0]#**), Section 4.2.3.2.
   — The 72-bit 2-bank unbuffered DDR SDRAM DIMM specification requires 6 clocks to distribute the loading across eighteen x8 DDR SDRAM components.
3. Control signals: Address/RAS/CAS/CS/WE/CKE/ODT signals, Section 4.2.2.3.

The On Die Termination or ODT for DDR2 eliminates some of the termination resistors needed for the source synchronous signals.

The Table 5 and Table 6 list the DDR2 differential strobe alignment with each of the DQ groups.

Table 5. x64 DDR Memory Configuration

Data Group	Positive Strobe	Negative Strobe
DQ[7:0], **DM[0]**	**DQS0**	**DQS0#**
DQ[15:8], **DM[1]**	**DQS1**	**DQS1#**
DQ[23:16], **DM[2]**	**DQS2**	**DQS2#**
DQ[31:24], **DM[3]**	**DQS3**	**DQS3#**
DQ[39:32], **DM[4]**	**DQS4**	**DQS4#**
DQ[47:40], **DM[5]**	**DQS5**	**DQS5#**
DQ[55:48], **DM[6]**	**DQS6**	**DQS6#**
DQ[63:56], **DM[7]**	**DQS7**	**DQS7#**

Table 6. x72 DDR Memory Configuration

Data Group	Positive Strobe	Negative Strobe
DQ[7:0], **DM[0]**	**DQS0**	**DQS0#**
DQ[15:8], **DM[1]**	**DQS1**	**DQS1#**
DQ[23:16], **DM[2]**	**DQS2**	**DQS2#**
DQ[31:24], **DM[3]**	**DQS3**	**DQS3#**
DQ[39:32], **DM[4]**	**DQS4**	**DQS4#**
DQ[47:40], **DM[5]**	**DQS5**	**DQS5#**
DQ[55:48], **DM[6]**	**DQS6**	**DQS6#**
DQ[63:56], **DM[7]**	**DQS7**	**DQS7#**
CB[7:0], DM[8]	**DQS8**	**DQS8#**

4.2.2 DDR2 533 DIMM Layout Design

This section provides the source synchronous, clock and control layout guidelines for DDR2 533 unbuffered and registered DIMMs. The topologies that were simulated for this revision of the document include RAW Card A, B, C and registered DIMMs. Refer to the JEDEC specification for more details on these topology http://www.jedec.org.

4.2.2.1 DDR2 DIMM Source Synchronous Routing

This section lists the recommendations for the DDR2 Source Synchronous Routing. These signals include all the DQ/DQS/DM/CB signals.

- Refer to Figure 7 for a block diagram of the DQ and DQS group length matching relationship.
- Refer to Figure 8 for a block diagram of the DQ/DQS group and length matching relationship with respect to the clock M_CK/M_CK# signals.
- Refer to Figure 9 for segment lengths of the DQ lines and Figure 10 for the segment lengths of the DQS lines.
- Table 7 lists the routing recommendations for DQ/DQS lines. Table 8 lists the segment lengths for the DQ lines and Table 9 lists segment lengths for the DQS lines.

Figure 7. DDR2 DIMM Source Synchronous Routing

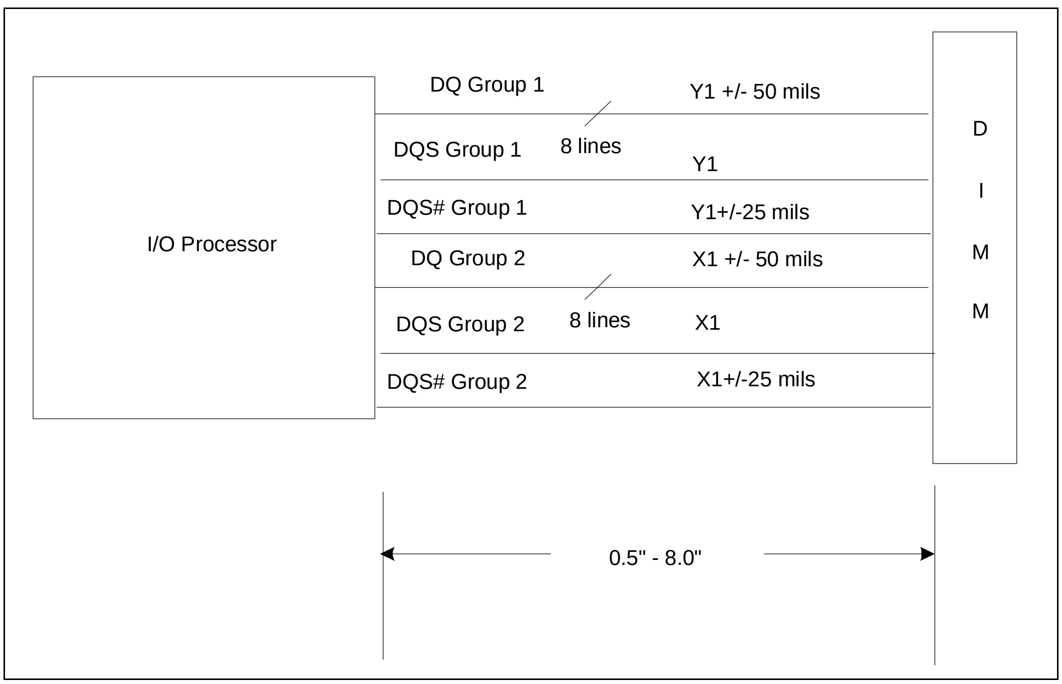


Figure 8. DDR2 DIMM Length Matching DQ/DQS Group with Respect to Clocks M_CK/M_CK#

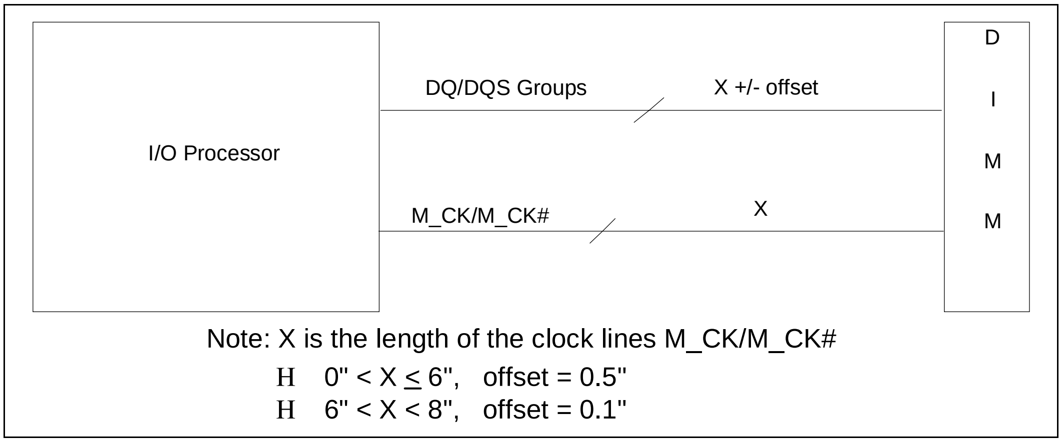


Table 7. DDR2 DIMM Source Synchronous Routing Recommendations

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane or unbroken power plane.
Preferred Layer	Stripline
Breakout	• 5 mils width • 5 mils spacing. • Maximum length of breakout region ≤ 500 mils microstrip
DQ signals Trace Impedance	Single ended stripline lines: • 50 ohms +/- 15% impedance for motherboards • 60 ohms +/- 15% impedance for Add-in cards
DQS Signals Trace Impedance	Differential stripline: • Differential 85ohm +/- 15% impedance for motherboards. • Differential 100 ohm +/-15% impedance for add-in cards
DQ Group Spacing (edge to edge)[1]	• Spacing within the same group: 12 mils minimum • Spacing from other DQ groups: 20 mils minimum • For DQS from any other signals: 20 mils minimum
Overall Trace Length: signal Ball to DIMM connector	0.5" minimum to 8" maximum (correlated with the clock length from ball to DIMM).
DQS Length Matching: • Trace Length Matching within DQS group • Within one DQS pair plus and minus	+/-0.05" within DQS group +/- 0.0250"
Length Matching:[1]DQS with respect to clock (from controller to DIMM connector)	Total Length: • 0" < total length ≤ 6", matching ≤ +/- 0.5" • 6" < total length ≤ 8", matching ≤ +/- 0.1"
Number of Vias	≤ 2 (for differential signals the number of vias on + and - signals must be the same)
DQ and DQS ODT	• 150 ohm ODT on Intel® 81348 I/O Processor • 75 ohm ODT on DRAM
Routing Guideline	Route all data signals and their associated strobes on the same layer.

Note: [1] For a right angle DDR connector consideration must be given to the lead length skew across the connector. Refer to Table 62.

Table 8. DDR2 DIMM DQ Lengths

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing (edge to edge)	Notes
TL0	Breakout	Microstrip	0″	0.5″		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Stripline	0.5″	8″	• 50 ohms +/- 15% impedance for motherboards • 60 ohms +/- 15% impedance for Add-in cards	• Within same group ≥ 12 mils • Between other groups ≥ 20 mils	

Figure 9. DDR2 DIMM DQ Topology

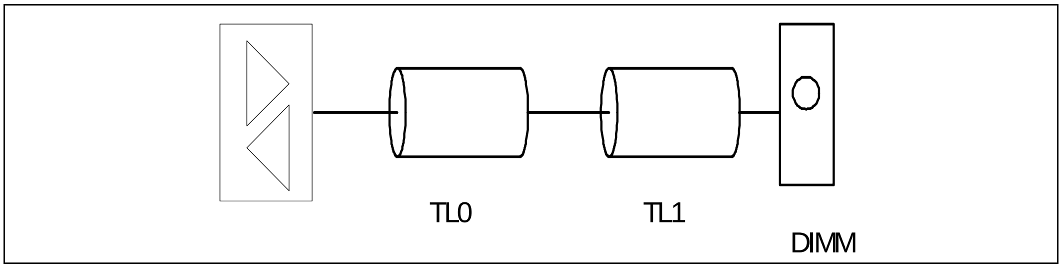
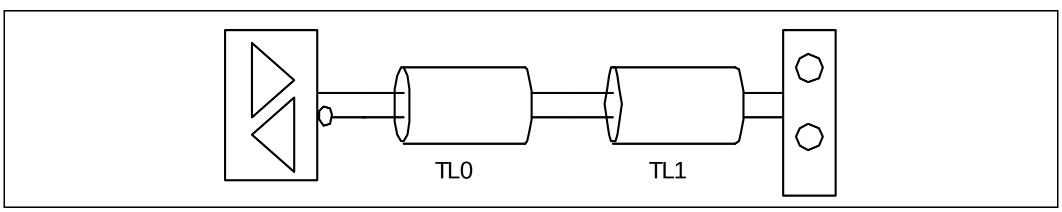


Table 9. DDR2 DIMM DQS Lengths

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing (edge to edge)	Notes
TL0	Breakout	Microstrip	0″	0.5″		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Stripline	0.5″	8″	• Differential 85ohm +/- 15% impedance for motherboards. • Differential 100 ohm +/-15% impedance for add-in cards	• 8 mils spacing (edge to edge) for 4 mil differential stripline trace. See Section 3.3 for details on differential routing. • ≥ 20 mils from other signals	Route as differential pair

Figure 10. DDR2 DIMM DQS Topology



4.2.2.2 DDR2 Clock Routing Guidelines

This section lists the recommendations for the DDR2 Clock signals.

- Table 10: DIMM clock routing guidelines
- Table 11: DIMM clock segment lengths.
- Figure 11: clock topology segment lengths.
- Figure 8: DQ/DQS group block diagram and length matching relationship with respect to clock signals.
- Figure 12: Address/Command length matching relationship with respect to clock signals.

Table 10. DDR2 DIMM Clock Routing Recommendations

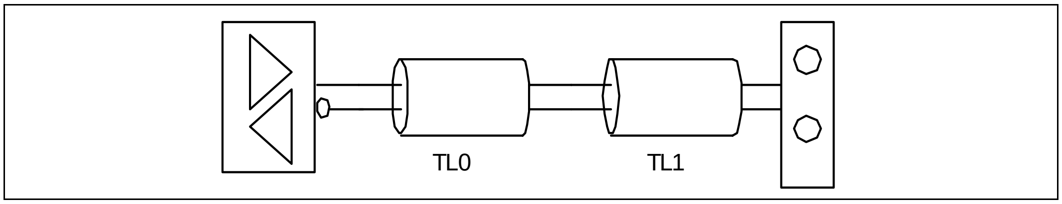
Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane preferred
Preferred Topology	Microstrip differential lines preferred
Breakout Trace Width and spacing	5 mils by 5 mils microstrip or stripline. Maximum length of breakout trace is 500 mils.
Trace Impedance	• Differential impedance of 85 ohms +/- 15% motherboard • Differential impedance of 100 ohms +/- 15% add-in card
Trace Spacing (edge to edge)[1]	• ≥ 25 mils between other signals.
Trace Length : TL0 + TL1: signal Ball to DIMM connector	0.5” min to 8.0” max
Length Matching:[2] Within M_CK/M_CK# (differential clock signals)	• +/- 0.0250” within pairs (intra-pair)
Length Matching:[2] With respect to DQS (from controller to DIMM connector) :	Total Length: • 0 < total length ≤ 6”, matching ≤ +/- 0.5” • 6” < total length ≤ 8”, matching ≤ +/- 0.1”
Length Matching: With respect to address/command group (from controller to DIMM connector)	• +8”/-3”[1] maximum for motherboard and +8”/-2” maximum for add-in card
Length Matching: With respect to CS/CKE group	• +/-2” maximum for motherboard and +1”/-3” maximum for add-in card
Routing Guideline 1	Maximum of 1 via/layer change for M_CK/M_CK# clocks. (use the same number of vias between + and - signals of differential clock)

Notes:
1. Length matching +8/-2 max means that for example address is routed up to 8 inches longer than clock and up to 2 inches shorter than clock.
2. For a right angle, DDR connector consideration must be given to the lead length skew across the connector. Refer to Table 62.

Table 11. DDR2 DIMM Clock Lengths

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing (edge to edge)	Notes
TL0	Breakout	Microstrip or stripline	0″	0.5″		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Microstrip	0.5″	8″	• Differential impedance of 85 ohms +/- 15% motherboard • Differential impedance of 100 ohms +/- 15% add-in card	• See Section 3.3 for details on differential routing. • Other groups ≥ 25 mils	

Figure 11. DDR2 DIMM Clock Topology



4.2.2.3 DDR2 Address/Command/Control Routing Guidelines

This section lists the recommendations for the DDR2 Address/Command and Control signals.

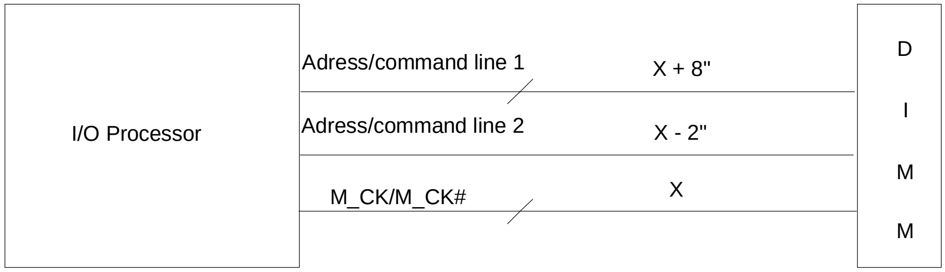
- Refer to Figure 12 for the Address/Command length matching relationship with respect to clock lines.
- Refer to Table 12 for a description of the Address/Command signals routing guidelines.
- Refer to Table 13 for the Address/Command signals segment length guidelines.

Table 12. DDR2 DIMM Address/Command/Control Routing Recommendation

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane preferred
Preferred Topology	Microstrip lines
Breakout Trace Width and Spacing	5 mils x 5mils. Microstrip or stripline is acceptable. Maximum length of the breakout trace is 500 mils.
Trace Spacing (edge to edge)[1]	• 5 mils acceptable between the pins and the breakout regions. • ≥ 12 mils within group • ≥ 20 mils from any other clock/DQ/DQS groups.
Trace Impedance	50 ohms +/- 15% for a motherboard 60 ohms +/- 15% for a add-in card
Trace Length: Overall length from signal Ball to DIMM Connector	0.5” min to 10” maximum Refer to Table 13 for segment lengths.
Length Matching: address/command group (except CS, ODT and CKE lines) with respect to clock (from controller to DIMM connector)	• +8”/-3”[1] maximum for motherboard and +8”/-2” maximum for add-in card
Length Matching: CS, ODT and CKE lines with respect to clock (from controller to DIMM connector)	• +/-2” maximum for motherboard and +1”/-3” maximum for add-in card
Single Parallel Termination or Split Termination	• 51.1 ohms +/- 1% to VTT • 100 ohms +/- 1% to ground and 100 ohms +/- 1% to 1.8V
Routing Guideline 1	Place the VTT terminations in the VTT island after the DIMM with a trace length of 0.15” to 0.5”
Routing Guideline 2	For split terminations place the VTT termination in their respective power islands
Number of vias	2 Vias or less

1. Length matching +8/-3 max means that for example address is routed up to 8 inches longer than clock and up to 3 inches shorter than clock.

Figure 12. DDR2 DIMM Length Matching Address/Command Group to Clocks M_CK/M_CK#



Example of length matching address lines to the clock lines: address/command lines can be a maximum of 8" greater or a minimum of 2" less then then average M_CK/M_CK# lengths for motherboards (+8/-3 for add-in cards).
.
Note: X is the length of the clock lines M_CK/M_CK#

Table 13. DDR2 DIMM Address/Command Lengths

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing (edge to edge)	Notes
TL0	Breakout	Microstrip	0"	0.5"		5 mils	5 mils trace width OK for breakout.
TL1	Lead-in	Microstrip	0.5"	10"	50 +/- 15%	• Within same group ≥ 12 mils • Between other groups ≥ 20 mils	
TL2	Vtt	Microstrip	0.15"	0.5"			

Figure 13. DDR2 DIMM Address/CMD Topology (Vtt Termination)

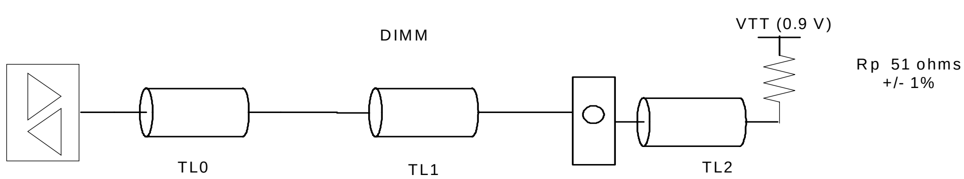
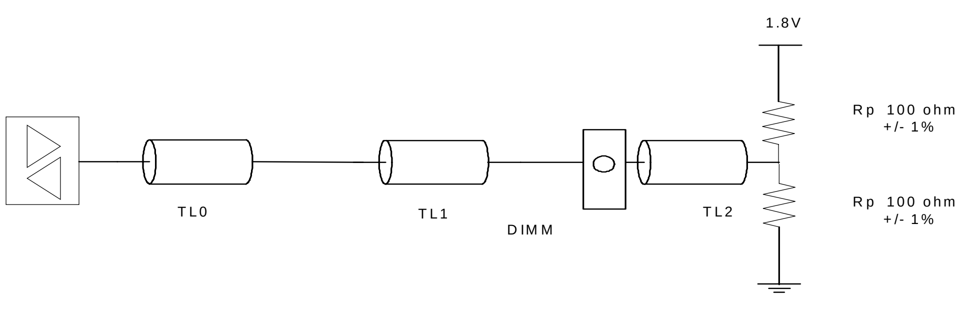


Figure 14. DDR2 DIMM Address/CMD Topology (Split Termination)



4.2.3 DDR2 533 Embedded Layout Design

This section provides the source synchronous, clock and control layout guidelines for separate DDR2 533 unbuffered memory chips placed on the board (without a DIMM). This analysis is also valid for an embedded DDR2 400 design. The topology that was simulated consisted of four memory chips x16 and one additional x8 for ECC. The simulations were based on 50 ohm +/- 15% motherboard stackup.

The embedded DDR2 interface is divided up into four groups that each have special routing guidelines:

1. Source synchronous signal group: DQ/DQS/DQM/CB signals, Section 4.2.3.1
2. Clocked: M_CLK signals, 6 clocks, three positive (**M_CK[2:0]**) and three negative (**M_CK[2:0]#**), Section 4.2.3.2.
3. Control signals: Address/RAS/CAS//WE, Section 4.2.3.3.
4. Control signals: CKE/CS/ODT signals, Section 4.2.3.4.

4.2.3.1 DDR2 Embedded Source Synchronous Routing

This section lists the recommendations for the DDR2 Source Synchronous Routing. These signals include all the DQ/DQS/DM/CB signals.

- Refer to Figure 15 for a block diagram of the DQ and DQS group length matching relationship.
- Refer to Figure 16 for a block diagram of the DQ/DQS group and length matching relationship with respect to the clock M_CK/M_CK# signals.
- Refer to Figure 17 for segment lengths of the DQ lines and Figure 18 for the segment lengths of the DQS lines.
- Table 14 lists the routing recommendations for DQ/DQS lines. Table 15 lists the segment lengths for the DQ lines and Table 16 lists segment lengths for the DQS lines.

Figure 15. DDR2 Embedded Source Synchronous Routing

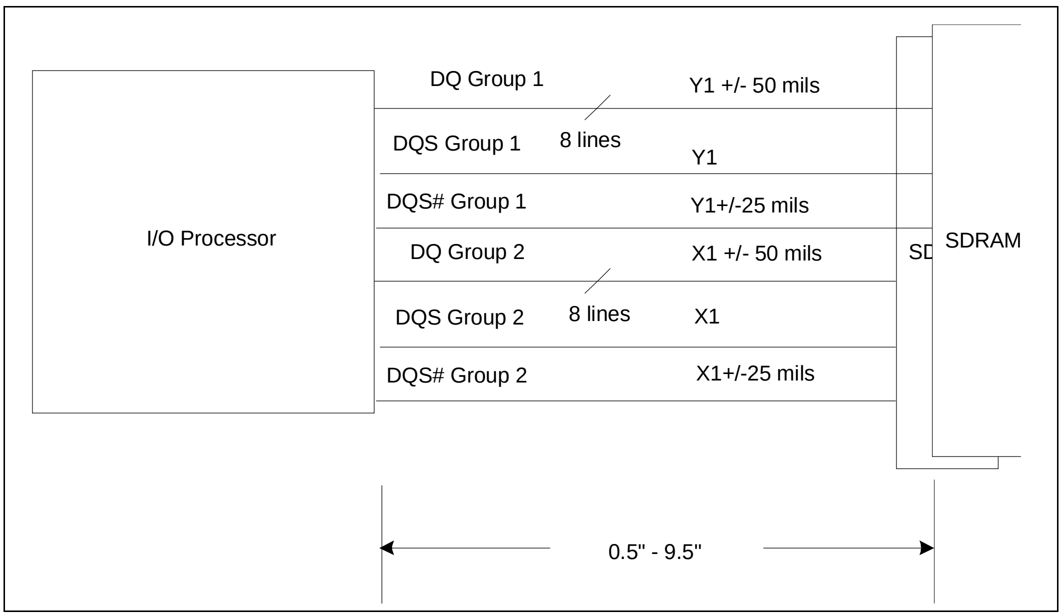


Figure 16. DDR2 Embedded Length Matching DQ/DQS Group with Clocks M_CK/M_CK#

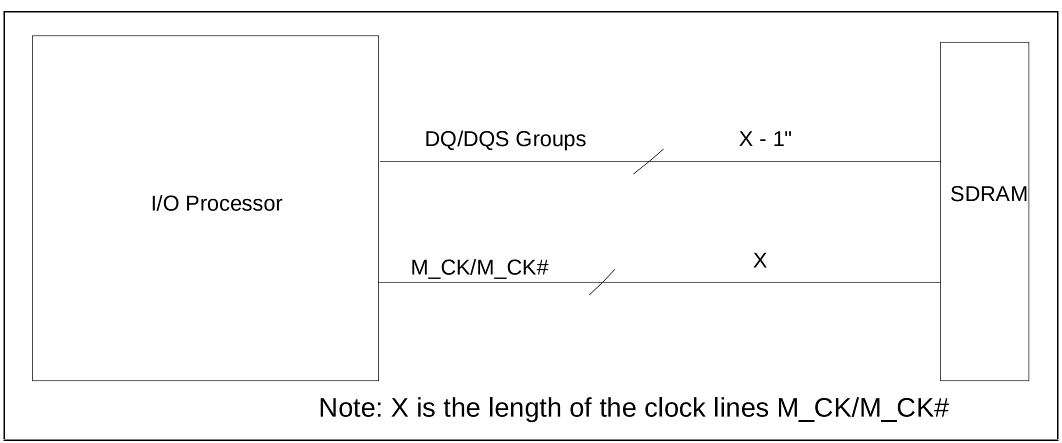


Table 14. DDR2 Embedded Source Synchronous Routing Recommendations

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane or unbroken power plane.
Preferred Layer	Stripline
Breakout	• 5 mils width • 5 mils spacing. • Maximum length of breakout region ≤ 500 mils microstrip
DQ signals Trace Impedance	Single ended stripline lines: • 50 ohms +/- 15% impedance for motherboards
DQS Signals Trace Impedance	Differential stripline: • Differential 85ohm +/- 15% impedance for motherboards.
DQ Group Spacing (edge to edge)	• Spacing within the same group: 12 mils minimum • Spacing from other DQ groups: 20 mils minimum • For DQS from any other signals: 20 mils minimum
Overall Trace Length: signal Ball to memory ball	0.5” minimum to 9.5” maximum (correlated with the clock length from ball to memory).
DQS Length Matching: • Trace Length Matching within DQS group • Within one DQS pair plus and minus	 +/-0.05” within DQS group +/- 0.0250”
Length Matching:DQS group with respect to clock (from controller to memory chip)	• DQS length = clock length - 1” (tolerance +/- 0.1”)
Number of Vias	≤ 4 (for differential signals the number of vias on + and - signals must be the same)
DQ and DQS ODT	• 150 ohm ODT on the Intel® 81348 I/O Processor • 75 ohm ODT on SDRAM
Routing Guideline	Route all data signals and their associated strobes on the same layer.

Table 15. DDR2 Embedded DQ Lengths

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing (edge to edge)	Notes
TL_BRK	Breakout	Microstrip	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL0	Lead-in	Microstrip	0.5”	8”	• 50 ohms +/- 15% impedance for motherboards	• Within same group ≥ 12 mils • Between other groups ≥ 20 mils	
TL1	SDRAM Lead-in	Microstrip	0.2”	0.75”	“	“	

Figure 17. DDR2 Embedded DQ Topology

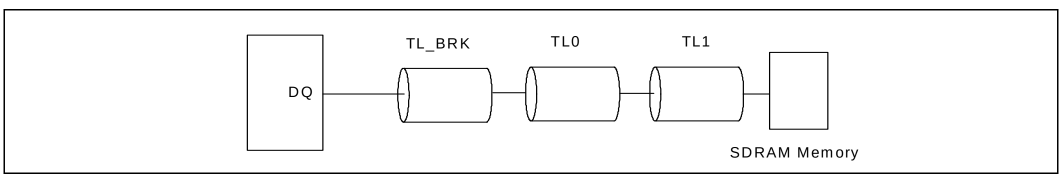
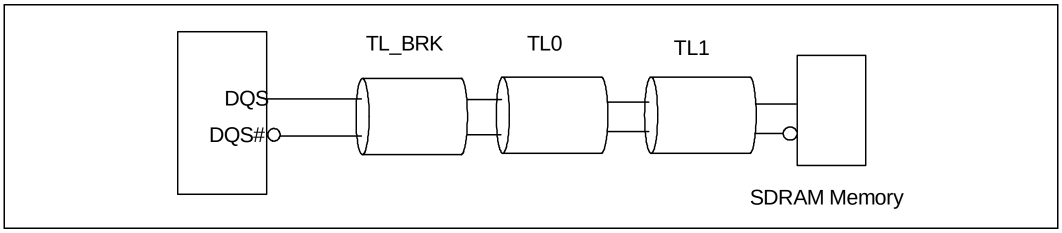


Table 16. DDR2 Embedded DQS Lengths

Traces	Description	Layer	Minimum Length	Maximum Length	Trace Impedance	Spacing (edge to edge)	Notes
TL_BRK	Breakout	Micro-strip	0"	0.5"		5 mils	5 mils trace width OK for breakout.
TL0	Lead-in	Microstrip	0.5"	8"	• Differential 85ohm +/- 15% impedance for motherboards.	• 8 mils spacing (edge to edge) for 4 mil differential stripline trace. See Section 3.3 for details on differential routing. • ≥ 20 mils from other signals • Route as differential pair	Length tolerance +/- 0.1"
TL1	SDRAM Lead-in	Microstrip	0.2"	0.75"	"	"	"

Figure 18. DDR2 Embedded DQS Topology



4.2.3.2 DDR2 Embedded Clock Routing

This section lists the recommendations for the DDR2 Clock signals.

- Refer to Table 17 for the embedded clock routing guidelines and Table 18 for the DIMM clock segment lengths.
- Refer to Figure 19 for the clock topology segment lengths.
- Refer to Figure 16 for the DQ/DQS group length matching relationship with respect to the clock signals.

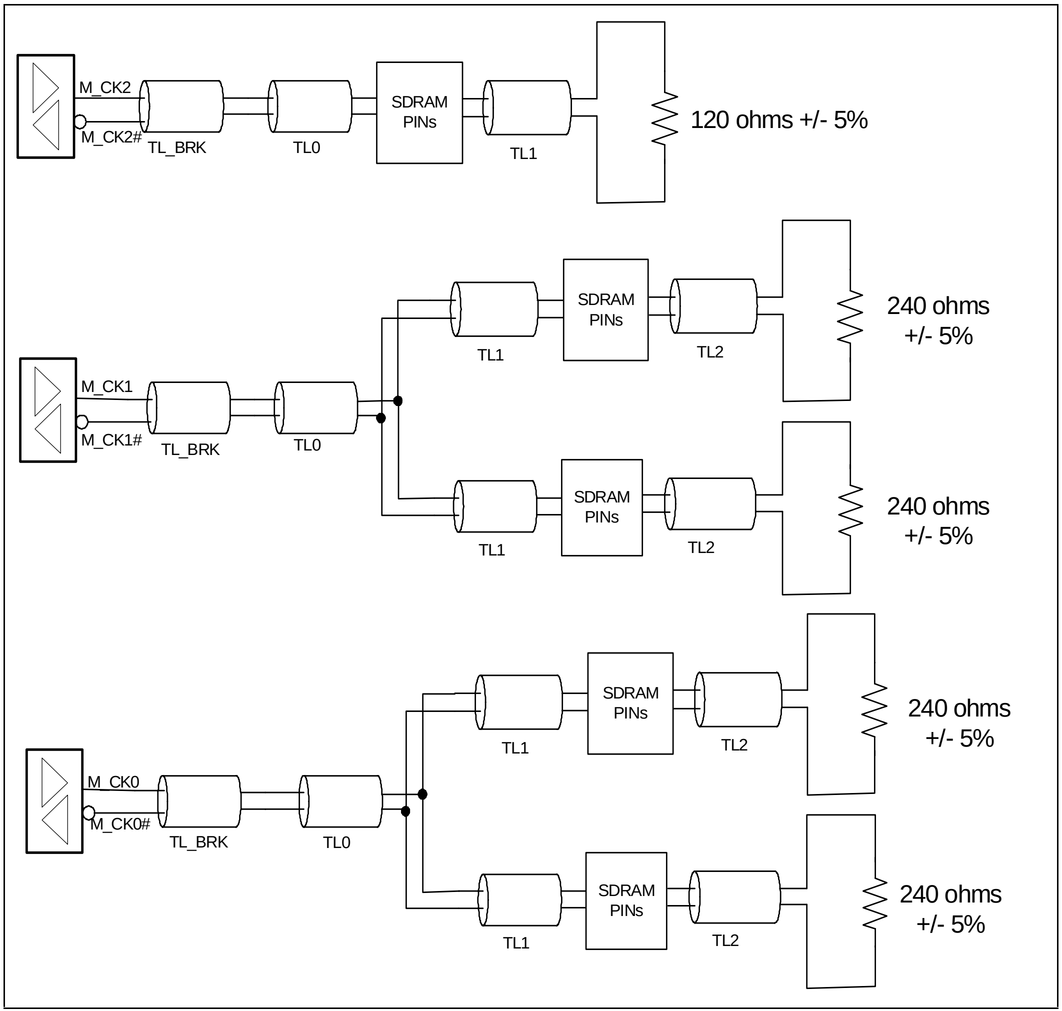
Table 17. DDR2 Embedded Clock Routing Recommendations

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane preferred
Preferred Topology	Microstrip differential lines preferred
Breakout Trace Width and spacing	5 mils by 5 mils microstrip or stripline. Maximum length of breakout trace is 500 mils.
Trace Impedance	• Differential impedance of 85 ohms +/- 15% motherboard
Trace Spacing (edge to edge)	• ≥ 25 mils between other signals.
Trace Length 1: signal Ball to memory ball	0.5” min to 10.5” max
Length Matching: Within M_CK/M_CK# (differential clock signals)	• +/- 0.0250” within pairs (intra-pair)
Length Matching: With respect to DQ/DQS group (from controller to memory ball)	• DQ/DQS length = clock length - 1”
Length Matching: With respect to address/command group (except CS, CKE, ODT) from controller to memory ball	• ADDR/CMD <= clock length + 2” • ADDR/CMD >= clock length - 1”
Length Matching: With respect to CS/CKE group	For daisy chain topology: • when CS/CKE group length is ≤ 4”: clock length + 1” • when CS/CKE group length is > 4”: clock length + 3” For balanced segment topology: • when CS/CKE group length is ≤ 2”: clock length + 1” • when CS/CKE group length is > 2”: clock length +/- 0.5”
Routing Guideline 1	Maximum of 2 via/layer change for M_CK/M_CK# clocks. (use the same number of vias between + and - signals of differential clock)

Table 18. DDR2 Embedded Clock Lengths

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing (edge to edge)	Notes
TL_BRK	Breakout	Microstrip or stripline	0”	0.5”		5 mils	5 mils trace width OK for breakout.
TL0	Lead-in	Microstrip	0.5”	10”	• Differential impedance of 85 ohms +/- 15% motherboard • Differential impedance of 100 ohms +/- 15% add-in card	• See Section 3.3 for details on differential routing. • Other groups ≥ 25 mils	Length Tolerance+/- 0.1”
TL1	Lead-in SDRAM	Microstrip	0.05”	0.2”	“	“	“
TL2	Lead-in resistor	Microstrip	0.05”	0.2”	“	“	“

Figure 19. DDR2 Embedded Clock Topology With Five SDRAMs



4.2.3.3 DDR2 Address/Command/Control Routing Guidelines

This section lists recommendations for DDR2 Address/Command and Control signals. (except for CS, ODT and CKE signals). Refer to Section 4.2.3.4, “DDR2 CS, ODT and CKE Routing Guidelines” on page 40 for details on routing CS, ODT and CKE signals.

- See Table 19 for a description of the Address/Command signals routing guidelines.

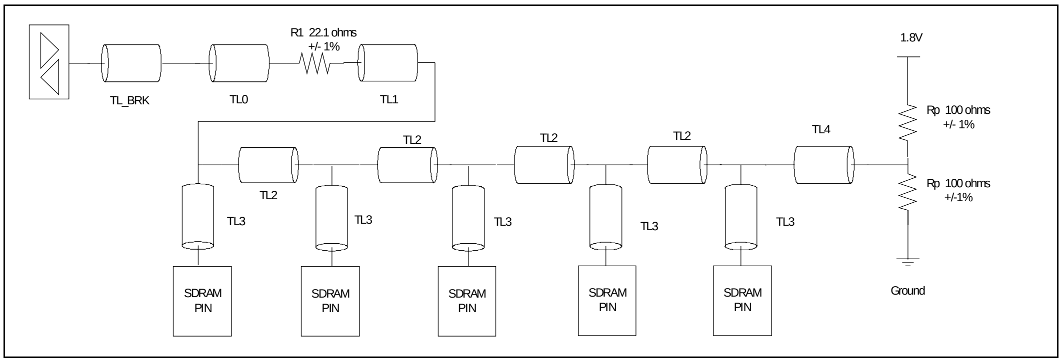
Table 19. DDR2 Embedded Address/Command/Control Routing Recommendation

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane preferred.
Preferred Topology	Microstrip lines.
Breakout Trace Width and Spacing	5mil x 5mil (Microstrip preferred)-Max length breakout trace (500 mil).
Trace Spacing (edge to edge)	• 5 mils acceptable between the pins and the breakout regions. • ≥ 12 mils within group. • ≥ 20 mils from any other clock/DQ/DQS groups.
Trace Impedance	50 ohms +/- 15% for a motherboard.
Trace Length: Overall length from signal Ball to SDRAM ball	1” min to 12” maximum. Refer to Table 20 for segment lengths.
Length Matching: address/command group (except CS, ODT and CKE lines) with respect to clock (from controller to SDRAM ball)	• ADDR/CMD <= clock length + 2”. • ADDR/CMD >= clock length - 1”.
Split Termination	• 100 ohms +/- 1% to ground and 100 ohms +/- 1% to 1.8V.
Routing Guideline 1	Place the VTT terminations in the VTT island after the DIMM with a trace length of 0.15” to 0.5”.
Routing Guideline 2	For split terminations place the VTT termination in their respective power islands.
Number of vias	6 Vias or less.

Table 20. DDR2 Embedded Address/CMD Lengths Topology

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing (edge to edge)	Notes
TL_BRK	Breakout	Microstrip	0.05″	0.5″		5 mils	5 mils trace width OK for breakout.
TL0	Lead-in Resistor	Microstrip	0.5″	9″	50 +/- 15% motherboard	≥ 12 mils within group, Other groups ≥ 20 mils	Length Tolerance+/- 0.1
TL1	Segment	Microstrip	0.2″	0.75″	"	"	"
TL2	Segment	Microstrip	0.2″	0.75″	"	"	"
TL3	Lead-in SDRAM	Microstrip	0.05″	0.2″	"	"	"
TL4	Lead-in VTT	Microstrip	0.05″	0.2″	"	"	"

Figure 20. DDR2 Embedded Address/CMD Topology (Split Termination)



4.2.3.4 DDR2 CS, ODT and CKE Routing Guidelines

This section lists the recommendations for the layout of the DDR2 CS, ODT and CKE signals.

- Refer to Table 21 for the segment lengths and for the CS, ODT and CKE balanced topology. This topology requires matching each of the branches going to the SDRAM chips. This topology is the preferred topology.
- Refer to Table 22 for the segment lengths and CS, ODT and CKE

Table 21. DDR2 Embedded CS, ODT and CKE Routing Recommendation

Parameter	Routing Guideline
Reference Plane	Route over unbroken ground plane preferred
Preferred Topology	Microstrip lines
Breakout Trace Width and Spacing	5 mils x 5mils. Microstrip preferred. Maximum length of the breakout trace is 500 mils.
Trace Spacing (edge to edge)	• 5 mils acceptable between the pins and the breakout regions. • ≥ 12 mils within group • ≥ 20 mils from any other clock/DQ/DQS groups.
Trace Impedance	50 ohms +/- 15% for a motherboard
Trace Lengths	Refer to Table 22 for segment lengths.
Length Matching: With respect to CS/CKE group	For daisy chain topology: • when CS/CKE group length is < 4”: CK length + 1” • when CS/CKE group length is > 4”: CK length + 3” For balanced segment topology: • when CS/CKE group length is < 2”: CK length + 1” • when CS/CKE group length is > 2”: CK length +/- 0.5”
Series Termination R1	• 22 +/-5%
Split Termination Rp	• 100 ohms +/- 1% to ground and 100 ohms +/- 1% to 1.8V
Routing Guideline 1	For split terminations place the VTT termination in their respective power islands
Number of vias	5 Vias or less

Table 22. DDR2 Embedded CS, ODT and CKE Lengths Balanced Topology

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing (edge to edge)	Notes
TL_BRK	Breakout	Microstrip	0.05”	0.5”		5 mils	5 mils trace width OK for breakout.
TL0	Lead-in Resistor	Microstrip	0.5”	8”	50 +/- 15% motherboard	≥ 12 mils within group, Other groups ≥ 20 mils	Length Tolerance+/- 0.050
TL1	Segment	Microstrip	0.2”	0.75”	"	"	"
TL2	Segment	Microstrip	0.2”	0.2”	"	"	"
TL3	Segment	Microstrip	0.2”	0.2”	"	"	"
TL4	Lead-in SDRAM	Microstrip	0.2”	0.2”	"	"	"
TL5	Lead-in SDRAM	Microstrip	0.4	0.4		"	"
TL6	Lead-in Vtt	Microstrip	0.05”	0.2”	"	"	"

Figure 21. DDR2 Embedded CS, ODT and CKE Balanced Topology

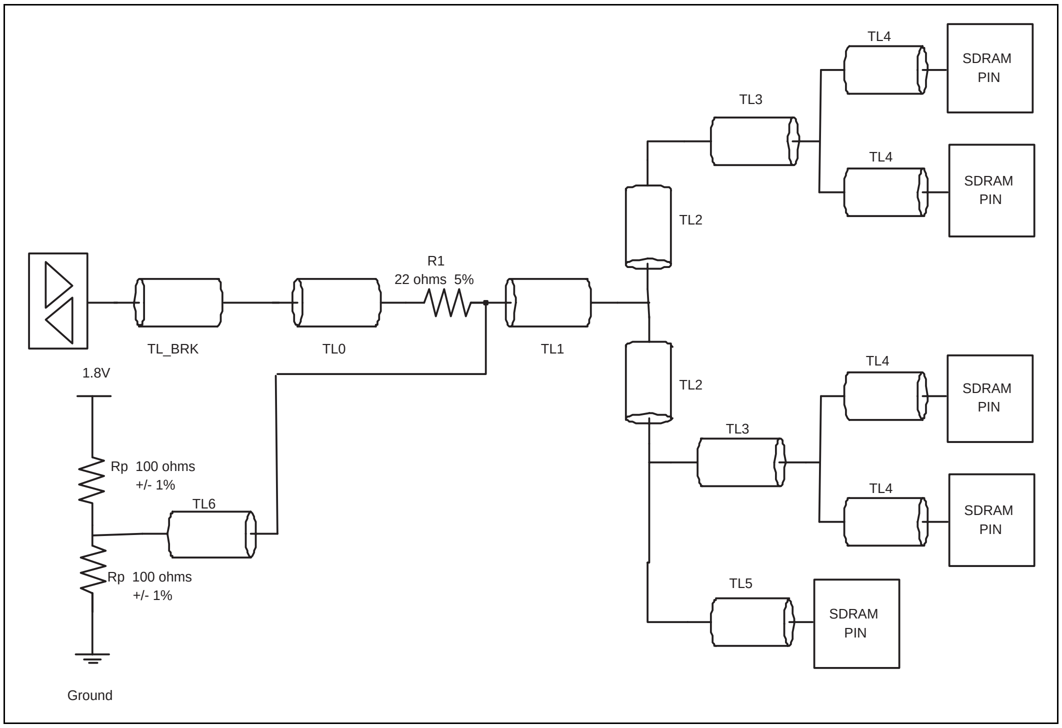
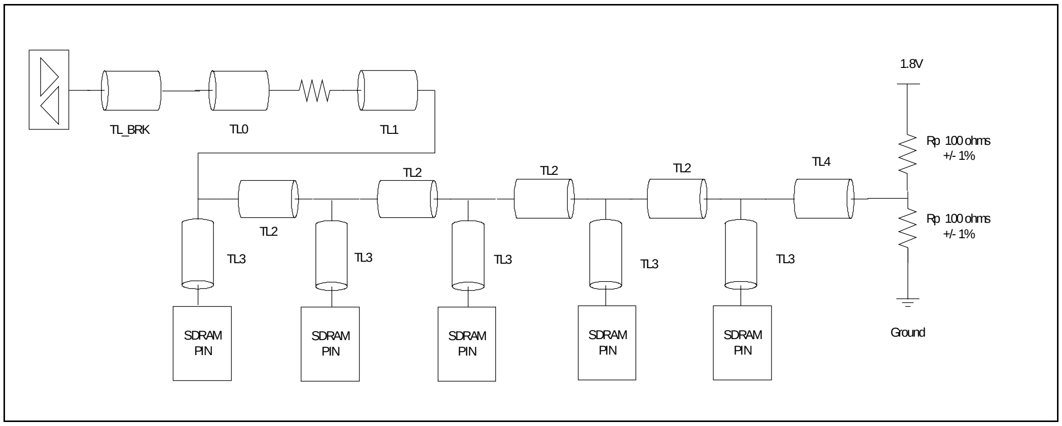


Table 23. DDR2 Embedded CS, ODT and CKE Lengths Daisy Chain Topology

Traces	Description	Layer	Min Length	Max Length	Trace Impedance	Spacing (edge to edge)	Notes
TL_BRK	Breakout	Microstrip	0.05”	0.5”		5 mils	5 mils trace width OK for breakout.
TL0	Lead-in Resistor	Microstrip	0.5”	8”	50 +/- 15% motherboard	≥ 12 mils within group, Other groups ≥ 20 mils	Length Tolerance+/- 0.05”
TL1	Segment	Microstrip	0.2”	0.75”	"	"	"
TL3	Lead-in SDRAM	Microstrip	0.05”	0.2”	"	"	"
TL4	Lead-in VTT	Microstrip	0.05”	0.2”	"	"	"

Figure 22. DDR2 Embedded CS, ODT and CKE Daisy Chain Topology



4.3 DDR2 Signal Termination

This section provides details on layout for DDR2 signal termination.

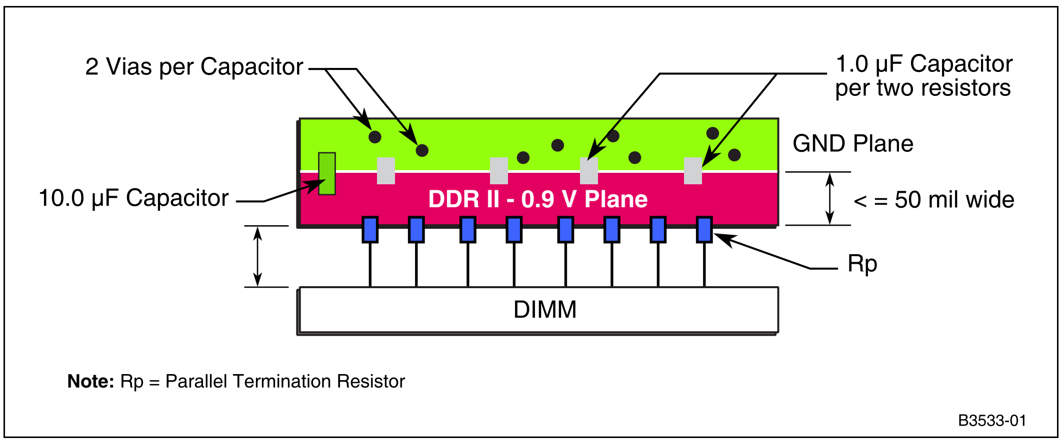
- Refer to Section 4.3.1 for details on laying out the VTT for a DIMM design.
- Refer to Section 4.4.1 for DDR Vref Volatage details.

4.3.1 DDR2 DIMM VTT Details

This section provides the suggested guidelines:

- Place a 0.9 V termination plane on the top layer or one of the inner layers, just beyond the DIMM connector.
- The $\mathbf{V_{TT}}$ island must be at least 50 mils wide.
- Use this termination plane to terminate all DIMM signals, using one termination resistor per signal.
- Decouple the $\mathbf{V_{TT}}$ plane using one 0.1 mF decoupling capacitor per two termination resistors.
- Each decoupling capacitor must have at least two vias between the top layer ground fill and the internal ground plane.
- In addition, place one 10 µF or larger (100 µF suggested) Tantalum capacitor on each end of the termination island for bulk decoupling.
- Figure 23 provides an example of how to route the termination resistors.

Figure 23. Routing Termination Resistors (Top View)



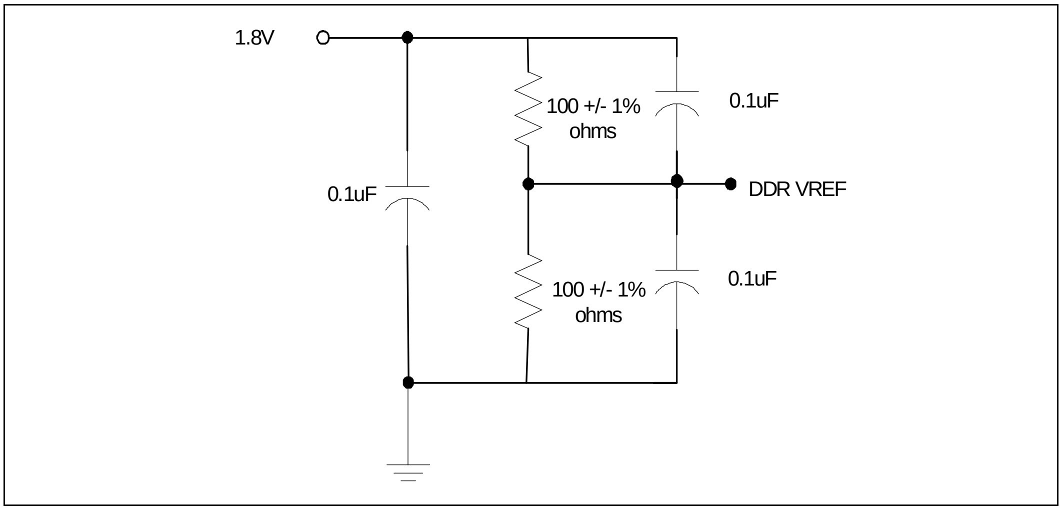
4.4 DDR2 Termination Voltage

The VTT DDR termination voltage must track the VDDQ (voltage for the DDR SDRAM DQ signals) and provide the termination voltage to the termination resistors. This tracking must be 50 percent of (VDDQ - VSSQ) over voltage, temperature, and noise. It must maintain less than 40 mV offset from VREF over these conditions. This voltage must be low-impedance and source-significant current. The source and sink DC current for signal termination is at its absolute maximum current of 2.6 A-2.9 A for a 64/72-bit DIMM.

4.4.1 DDR V_{REF} Voltage

The Figure 24 shows the DDR Vref voltage. The DDR VREF is a low-current source (supplying input leakage and small transients). It must track 50 percent of (VDDQ - VSSQ) over voltage, temperature, and noise. Use a single source for VREF to eliminate variation and tracking of multiple generators. Maintain 15-20 mils clearance around other nets. Use a distributed decoupling scheme. Use a simple resistor divider with 1% or better accuracy.

Figure 24. DDR V_{REF} Circuit



5.0 PCI Express Layout

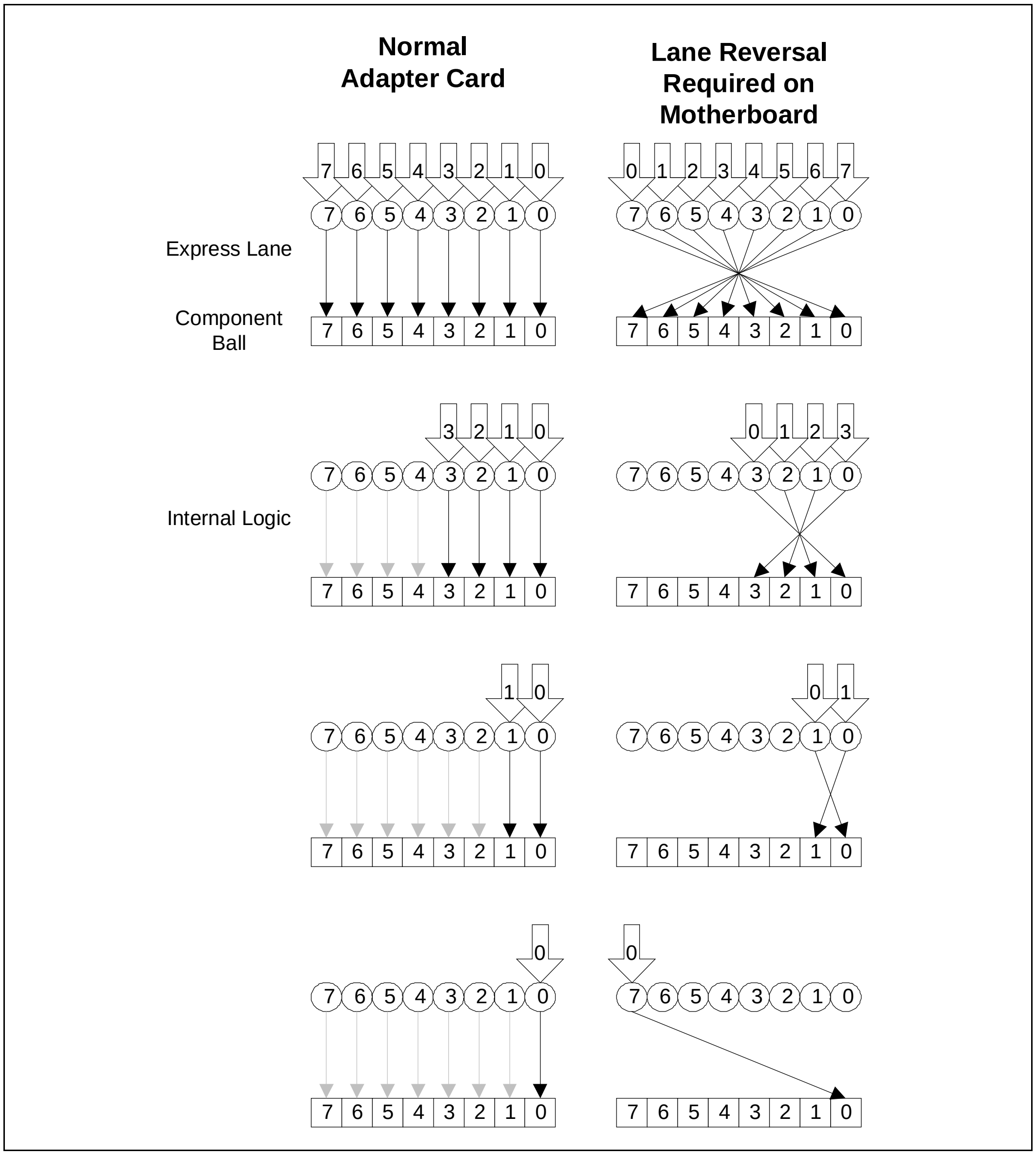
This section provides an overview of the PCI Express layout recommendation based on simulation results. PCI Express is a serial differential low-voltage point-to-point interconnect. The PCI Express was designed to support 20 inches between components with standard FR4.

For more information on the PCI Express standard refer to PCI Express Base Specification 1.0a and the *PCI Express Card Electromechanical Specification*, revision1.0a, found on the http://www.pcisig.com/home website.

5.1 Optional PCI Express Lane Reversal

The following Figure 25 describes the lane reversal which is considered when designing a PCI-E x8 motherboard slot or an adapter card to improve PCB routing. Note that the adapter card PCI-E pins map with a straight through connection but the motherboard implements lane reversal in x8, x4, x2 and x1 configurations as shown in Figure 25.

Figure 25. PCI Express Lane Reversal To Improve PCB Routing



5.2 PCI Express Layout recommendations

The following recommendations are summarized based on the presilicon simulation results for the following topologies:

1. motherboard topology with the PCI Express device on the board Section 5.2.1.
2. motherboard topology with a PCI Express connector and an adapter card topology with the device on the card Section 5.2.2.

The PCI Express clock layout recommendations are listed in Section 5.2.3.

5.2.1 PCI Express Motherboard Layout Guidelines

The following layout recommendations were determined for a motherboard application with the PCI Express device on the board.

Figure 26. Motherboard Topology

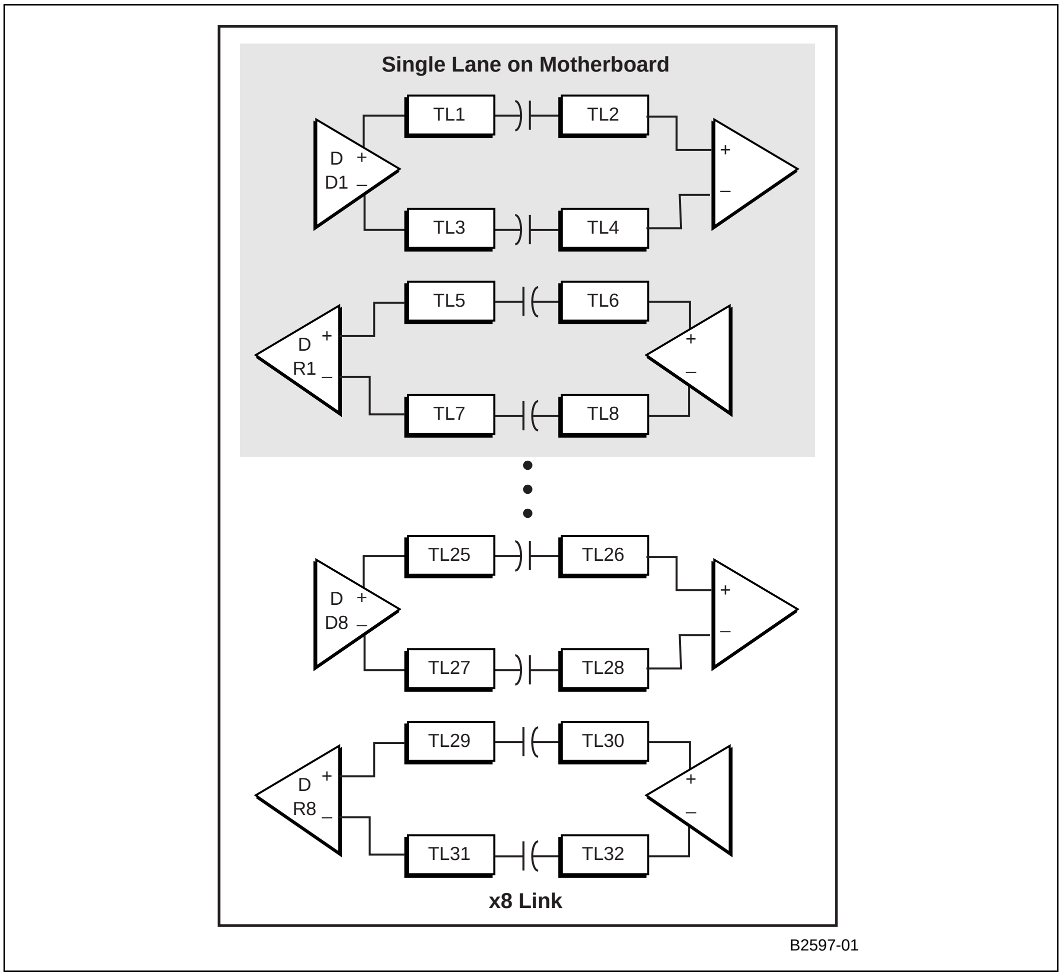


Table 24. PCI Express Layout for a Motherboard

Parameter	Routing Guidelines
Signal Group	Transmit and receive differential pairs
Reference Plane	Routing over unbroken ground plane is preferred. When unbroken ground plane is not available, route over unbroken voltage plane.
Characteristic Trace Impedance:	Single-ended: 50 ohms +/- 15% Differential: 85 ohms nominal +/-15%
Microstrip Trace Width	5 mils (Refer to Table Note)
Microstrip Trace Spacing	• Between + (P) and - (N) of pair: 7 mils edge to edge • Between other signals: ≥ 25 mils edge to edge • Transmit and receive pairs are interleaved. When interleaving is not possible, then the spacing between pairs (inter pair) are increased to ≥ 45 mils (edge to edge). Edge to Edge of inter pair is defined as edge of Positive of one pair to edge of Negative of the next pair or vice versa.
Stripline Trace Width	5 mils (Refer to Table Note below)
Stripline Trace Spacing	• Between + (P) and - (N) of pair: 7 mils edge to edge • Between other pairs : ≥ 25 mils edge to edge • Transmit and receive pairs are interleaved. When interleaving is not possible, then inter pair spacing is increased to 45 mils (edge to edge). Edge to Edge of inter pair is defined as edge of Positive of one pair to edge of Negative of the next pair or vice versa.
Group Spacing	Spacing from other groups: > 25 mils minimum from edge to edge for microstrip or stripline.
AC Coupling	AC Coupling capacitors must be located at the transmitter. Required values of 75 nF to 200 nF.
Total Trace Length - (Transmitter/Receiver) from device signal pin to AC coupling capacitor and AC coupling capacitor to PCI Express device pin	1.0" min. - 30.0" max
Length Matching Requirements	• Total allowable between pair (length skew between + and - signals of the pair) length mismatch on a system board must not exceed 10 mils. • Match length on a segment by segment basis. • Each routing segment to be matched as close as possible. • Total skew across all lanes must be less than 20 ns.
Number of Vias	4 max

Note: Width and Intra Pair (length skew between + and - signals of the pair) spacing recommendations need not be strictly adhered to, but it is very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendations.

5.2.2 PCI Express Layout Motherboard-Adapter Card Guidelines

This section provides the routing guidelines for the motherboard-adapter card topology as shown in Figure 27. Table 25 provides the routing guidelines for a motherboard with a PCI Express connector on it and the routing guidelines for an adapter card.

Figure 27. Motherboard-Adapter Card Topology

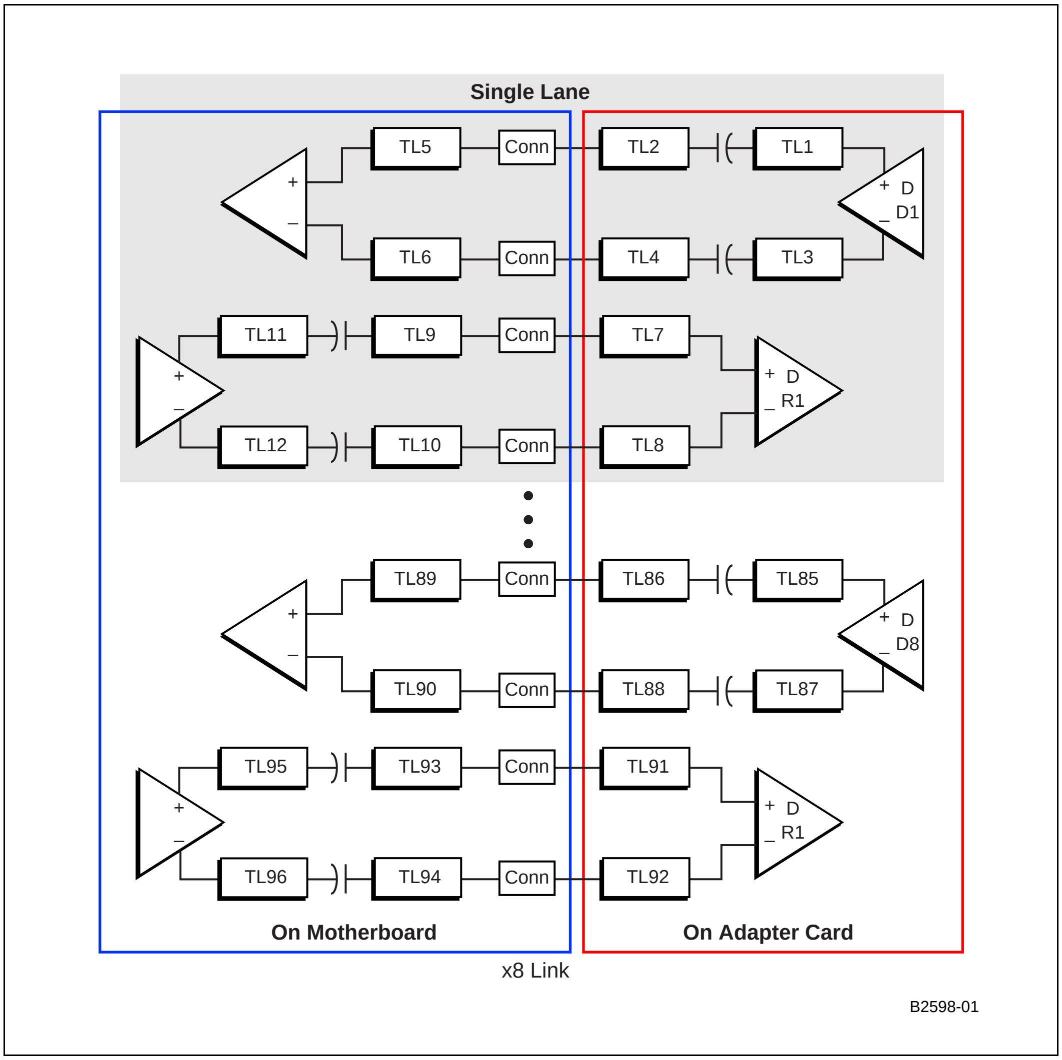


Table 25. PCI Express Layout for Motherboard-Adapter Card Topology

Parameter	Routing Guidelines
Signal Group	Transmit and Receive differential pairs
Reference Plane	Routing over unbroken ground plane is preferred. When unbroken ground plane is not available route over unbroken voltage plane.
Characteristic Trace Impedance motherboard	Single Ended: 50 +/-15% ohms nominal
	Differential: 85 +/-15% ohms nominal
Characteristic Trace Impedance adapter card	Single Ended: 60 +/-15% ohms nominal
	Differential: 100 +/-15% ohms nominal
Microstrip Trace Width	5 mils
Microstrip Trace Spacing	• Between intra-pair (between + (P) and - (N) of pair): 7 mils edge to edge (see Table Note) • Between other pairs : ≥ 25 mils edge to edge • Transmit and receive pairs are interleaved. When interleaving is not possible, then the spacing between pairs (inter pair) are increased to ≥ 45 mils (edge to edge). Edge to Edge of inter pair is defined as edge of the positive of one pair to edge of negative of the next pair or vice versa
Stripline Trace Width	5 mils (see Table Note)
Stripline Trace Spacing	• Between + (P) and - (N) of pair: 7 mils edge to edge • Between other pairs: ≥ 25 mils edge to edge • Transmit and Receive pairs are interleaved. When interleaving is not possible, then increase inter pair spacing to 45 mils (edge to edge). Edge to Edge of inter pair is defined as edge of the positive of one pair to edge of negative of the next pair or vice versa
Group Spacing	Spacing from other groups: > 20 mils minimum from edge to edge for microstrip or stripline.
AC Coupling	AC Coupling capacitors must be located at the transmitter. Required value of 75 nF to 200 nF.
Total Length: Topology 1: from device signal pin transmitter on motherboard with PCI-E device receiver on adapter card	1.0" min. - 27" max
Total Length: Topology 2: from device signal pin transmitter on adapter card and the PCI-E device receiver on motherboard.	1.0" min. - 25" max
Length Matching Requirements	• Total allowable intra-pair (length skew between + and - signals of the pair) trace mismatch for a lane that must not exceed 15 mils for the motherboard-adapter card combination (10 mils for the motherboard, 5 mils for the adapter card). • Match length on a segment by segment basis. • Total skew across all lanes must be less than 20 ns.
Number of Vias	4 max

Note: Width and Intra Pair Spacing (between + (P) and - (N) of pair) recommendations need not be strictly adhered to, but it is very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendations.

5.2.3 Clock Routing Guidelines

This section provides routing guidelines for the PCI Express Clocks in an application.T he *PCI Express Card Electromechanical Specification Rev 1.0a* states in that any terminations required by the clock are to be on the system board.

The termination in Figure 28 is only required on the system board when these resistors were not already provided.

- PCI Express adapter cards do not have to add Rs and Rt termination resistors.

Figure 28. PCI Express Clock Routing Topology

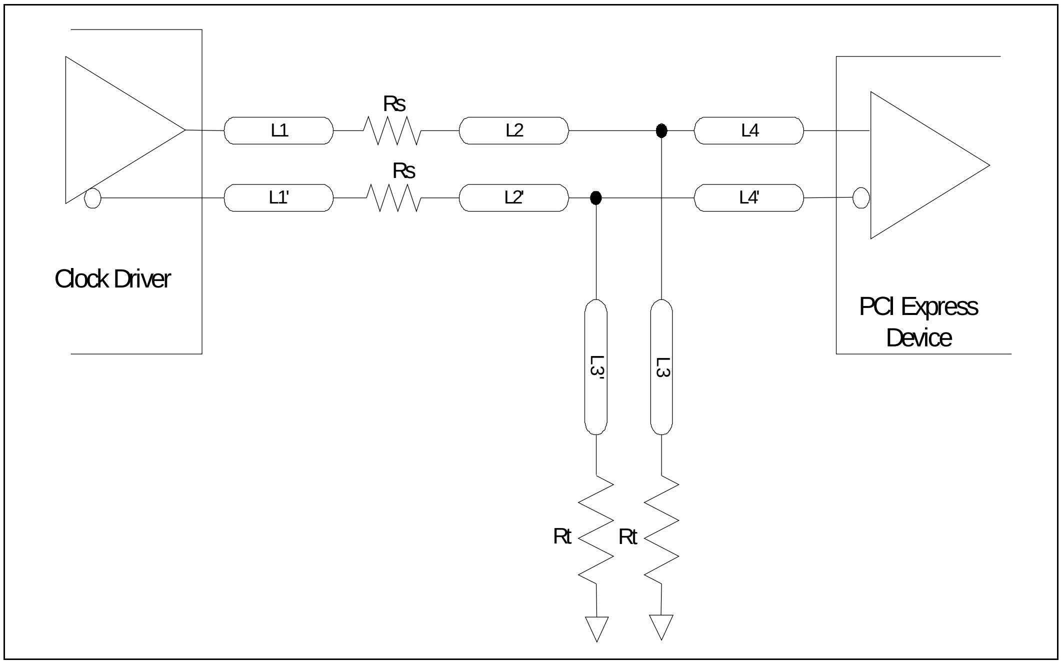


Table 26. PCI Express Layout for Clock Routing

Parameter	Routing Guidelines
Signal Group	REFCLKP, REFCLKN differential pairs
Reference Plane	Routing over unbroken ground plane is preferred. When unbroken ground plane is not available route over unbroken voltage plane.
Characteristic Trace Impedance	Single Ended: 50 +/-15% ohms nominal
	Differential: 100 +/-15% ohms nominal
Trace Width[1]	5 mils (see Table Note 2)
REFCLKP, REFCLKN differential clock Pair Spacing	< 1.4 x Space Width
Serpentine Spacing (spacing of a clock lines from itself)	> 25 mils
Clock to Other Signal Spacing	> 25 mils
Trace Lengths[2]	L1, L1: 0.5” max
	L2, L2: 0.2” max
	L3, L3: 0.2” max
	L4, L4 • Device down: 2” to 15.3” or • Connector: 2” to 11.3
	Total Length = L1+L2_+L4 • Device Down: 3” to 16” or • Connector: 3” to 12”
Length Matching Requirements within differential pair	+/- 5 mils
Rs Series Resistors	33 +/- 5%
Rt Shunt Resistors	49.9 +/- 1%
Number of Vias	4 max

Notes:

1. Termination resistors are only required on system boards when not already present. Adapter cards do not require Rs and Rt resistors)
2. Width and Intra Pair Spacing recommendations need not be strictly adhered to, but it is very important to meet the given differential target impedance and specified tolerance. It is also very important to follow the inter pair spacing recommendations.

6.0 PCI-X Layout Guidelines

This section provides an overview of the PCI-X layout recommendations based on Intel simulation results. The results were compiled for a motherboard with 50 ohm impedance and an adapter card with 60 ohm impedance.

- Section 6.1 provides details on the central resource mode details including: PCI-X Frequency control, interrupt routing and arbitration.
- Section 6.2 provides the layout recommendations for each of the topologies and PCI-X speeds.

For more information on the PCI-X standard refer to *PCI-X Addendum to the PCI Local Bus Specification,* Revision 1.0a on the www.pcisig.com website.

6.1 Central Resource/Endpoint Mode Details

The Intel® 81348 I/O Processor is enabled as a central resource or an endpoint with the external strapping signal **PCIX_EP#**. For the central resource mode **PCIX_EP#** = 1 is set by default with an internal pull-up. For the endpoint mode **PCIX_EP#** = 0 is set with a pull-down. The central resource dependent functions described in this section include:

- Section 6.1.1 PCI-X Frequency Control
- Section 6.1.2 Interrupt Routing
- Section 6.1.3 Internal Arbitration
- Section 6.1.4 External Arbitration

6.1.1 PCI/PCI-X Frequency Selection

When the central resource is enabled, the resultant mode and frequency is dependent upon the device capabilities reported as well as any system specific loading information. The following table lists the encoding of M66EN and PCIXCAP to determine the capability speed of the PCI/PCI-X bus.

Table 27. PCI/PCI-X Device Capability Reporting

M66EN	PCIXCAP	PCI Device Frequency Capability	PCI-X Device Frequency Capability
Ground	Ground	33 MHz	Not capable
8.2K pull-up[1]	Ground	66MHz	Not Capable
Ground	10K pull-down	33 MHz	PCI-X 66MHz
8.2 K pull-up[1]	10K pull-down	66 MHz	PCI-X 66MHz
Ground	NC	33MHz	PCI-X 133 MHz
8.2K pull-up[1]	NC	66 MHz	PCI-X 133MHz

1 M66EN maybe pulled high on the motherboard.

Table 28 describes the PCI-X bus mode and frequency initialization pattern that this part initiates on the PCI bus when coming out of reset as a central resource. Intel® 81348 I/O Processor decodes this initialization pattern to determine the bus frequency when it is set as an endpoint.

Table 28. PCI-X Initialization Pattern

DEVSEL#	STOP#	TRDY#	Mode	Clock Period (ns)		Clock Frequency (MHz)	
				Max	Min	Min	Max
Deasserted	Deasserted	Deasserted	PCI 33	60	30	16	33
			PCI 66	30	15	33	66
Deasserted	Deasserted	Asserted	PCI-X	20	15	50	66
Deasserted	Asserted	Deasserted	PCI-X	15	10	66	100
Deasserted	Asserted	Asserted	PCI-X	10	7.5	100	133

The ATU additionally limits the frequency of the output clocks. This maybe useful when in an application where the PCI bus is connected to individual devices or bus slots and the PCI bus system speed needs to be limited. In this case the designer terminates the M66EN, PCIXCAP and PCIXM1_100# (reset strap) to set the PCI clock frequency.

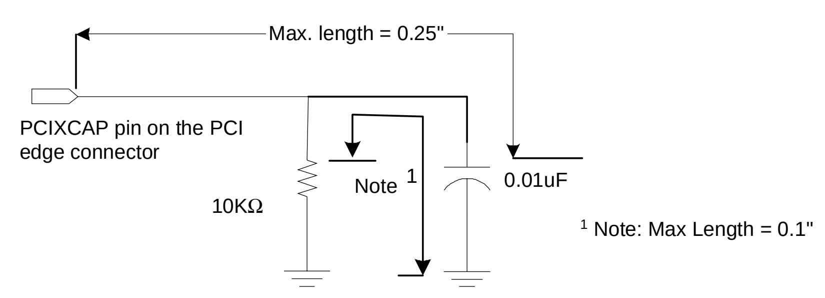
Table 29. PCI Bus Frequency Encoding

M66EN	PCIXCAP	PCIXM1_100#	PCI Device Frequency Capability	PCI-X Device Frequency Capability
Ground	Ground	-	33 MHz	Not capable
8.2K pull-up	Ground	-	66MHz	Not Capable
-	10K pull-down	-		PCI-X 66MHz
-	8.2K pull-up	GND		PCI-X 100MHz
-	8.2K pull-up	NC (internal pull-up)		PCI-X 133MHz

Note: '-' value is a do not care for computing the bus mode/frequency.

Figure 29 provides layout guidelines for locating the connections from the PCIXCAP pin on the card edge connector for an Intel® 81348 I/O Processor adapter card. With the Intel® 81348 I/O Processor on an adapter card, the P_PCIXCAP pin is pulled-up with an 8.2K resistor.

Figure 29. P_PCIXCAP Layout Guidelines with Intel® 81348 I/O Processor Adapter card

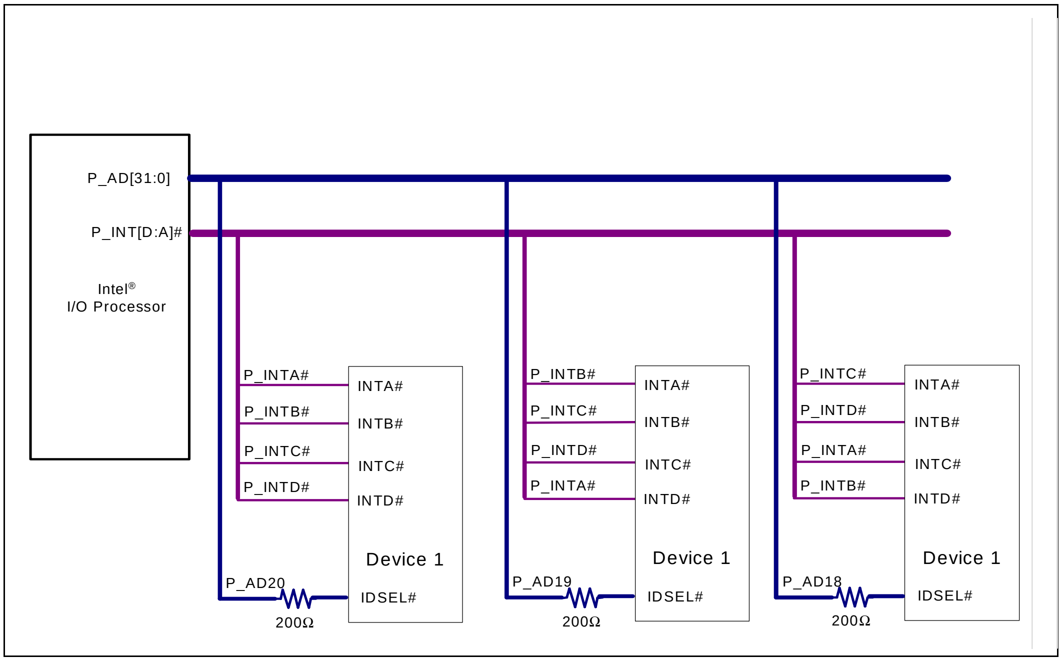


With Intel® 81348 I/O Processor in Central Resource mode PCIXCAP is pulled up 3.3K pulled up to 3.3V unless the bus speed is limited.

6.1.2 Interrupt Routing in Central Resource Mode

Figure 30 below shows the device running in central resource mode connected to three multifunction PCI devices. Notice that the interrupts are rotated for each device. The practice of rotating interrupts are used when connecting to PCI slots. The IDSEL lines acts as chip selects during the configuration cycles. The IDSEL lines are mapped to upper address lines which are unused during the configuration cycles. Each IDSEL line requires a 200 ohm series resistor on it as shown in Figure 30.

Figure 30. Interrupt and IDSEL Mapping



6.1.3 Internal Arbitration

Intel® 81348 I/O Processor has a internal PCI arbiter that supports up to four external masters. A hardware bootstrap method has been provided to enable or disable the internal arbiter at boot-up time. The internal arbiter is enabled when **EXT_ARB#**='1' at the rising edge of P_RST# signal. The request inputs into the internal arbiter include: 4 external request inputs P_REQ[3:0]#, and the Intel® 81348 I/O Processor Address Translation Unit.

6.1.4 External Arbitration

When the reset strap **EXT_ARB#**='0', then the internal arbiter in Intel® 81348 I/O Processor is disabled and an external arbiter is used instead for PCI bus arbitration.

When operating in the external arbiter mode, Intel® 81348 I/O Processor produces one P_REQ# output and receives one P_GNT# input. The P_REQ#/P_GNT# pair is for ATU transactions.

The Intel® 81348 I/O Processor arbitration pins switch modes between internal and external arbitration. **P_GNT[0]#** pin becomes the ATU request output P_REQ# to the external arbiter and **P_REQ[0]#** pin becomes the ATU grant input P_GNT# from the external arbiter.

6.2 PCI-X Layout Recommendations

This section provides the layout recommendations for PCI-X topologies in the following subsections:

- Section 6.2.1, "PCI-X Clock Routing Guidelines"
- Section 6.2.2, "Point-to-Point Signals (REQ#/GNT#)"
- Section 6.2.3, "133 MHz One Slot Topology"
- Section 6.2.4, "Embedded 133 MHz Topology"
- Section 6.2.5, "Mixed 133 MHz Topology"
- Section 6.2.6, "100 MHz Two Slot Topology"
- Section 6.2.7, "Embedded 100 MHz Topology"
- Section 6.2.8, "Mixed 100 MHz Topology"
- Section 6.2.9, "66 MHz PCI-X Four Slot Topology"
- Section 6.2.10, "Embedded 66 MHz Topology"
- Section 6.2.11, "Mixed 66 MHz Topology"
- Section 6.2.12, "Additional PCI Layout Notes"

6.2.1 PCI-X Clock Routing Guidelines

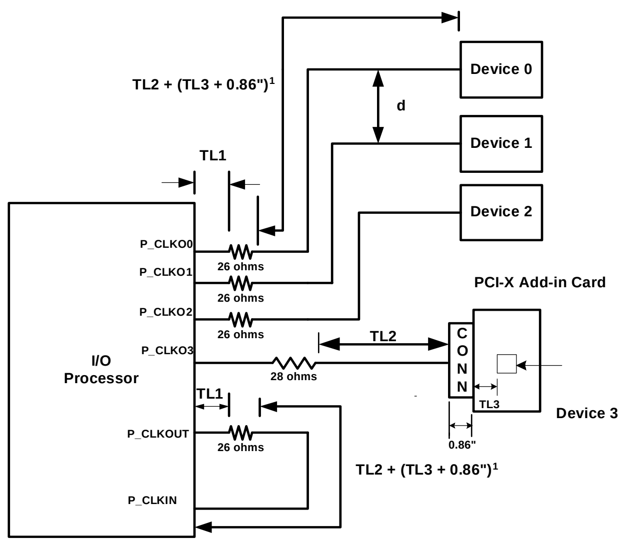
Intel® 81348 I/O Processor provides a clock buffer for up to four PCI-X devices when operating in central resource mode. Note that when the **P_CLKIN** is the primary clock source (**CLK_SRC_PCIE#** = 1), the PCI Clock outputs are unavailable and not be used as a clock source for any device.

- Refer to Table 30 for the listing of clock routing guidelines.
- Refer to Figure 31 with the clock topology. This figure shows three clocks connected to individual PCI-X devices, one slot with adapter card and the clock feedback signals.

The *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0b, allows a maximum of 0.5 ns clock skew timing for each of the PCI-X frequencies: 66 MHz, 100 MHz, and 133 MHz.

Figure 31 shows four clocks connected to individual PCI-X devices with P_CLKOUT fed back into P_CLKIN.

Figure 31. PCI Clock Distribution and Matching Requirements



Note: 1
- if the design does not have both connectors and embedded devices, remove the (TL3 + 0.86") term for length matching
- TL1 ≤ 0.5"
- TL3 = 2.4" to 2.6"
- Connector compensation length is 0.86"
- Clock lengths should be matched to ≤ 25 mils

Table 30. PCI-X Clock Layout Guidelines

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane.
Recommended Layer	Stripline
Trace Impedance: Motherboard	Microstrip: 50 ohm +/- 15%, stripline: 50 ohm +/- 10%
Trace Impedance: Adapter Card	Microstrip or stripline: 60 ohm +/- 15%
Trace Spacing (edge to edge)	• between two different clock lines $\geq$ 25 mils • between two segments of the same clock line $\geq$ 25 mils • between clock and other signals $\geq$ 50 mils
Series Resistors	28 ohms 1% for connectors 26 ohms 1% for embedded
Trace Length TL1 from buffer to the resistor	1.0” max
Total Trace Length: from device ball to device (including resistor segment)	11” max
Length Matching:	All clock lines including PCLKOUT to PCLKIN (feedback clock) must be matched to within 25 mils. Refer to Figure 31.
• Topologies with only embedded devices	Match clocks to within 25 mils
• Topologies with only connectors	• Match clocks to within 25 mils. • Rout feedback clock longer to compensate for the adapter card length (2.4” to 2.6”) + 0.85” (for the connector delay)
• Topologies with both slots and devices used in the design	• Match Clocks to within 25 mils • Rout feedback clock longer to compensate for the adapter card length (2.4” to 2.6”) + 0.85” (for the connector delay) • PCLKs going to the embedded devices must be compensate for the adapter card length (2.4” to 2.6”) + 0.85” (for the connector delay)
Vias	$\leq$ 2 vias

6.2.2 Point-to-Point Signals (REQ#/GNT#)

This section provides the layout guidelines for REQ# and GNT# lines. Topology in Figure 32 for 133 MHz slot design is the same as the one used for point-to-point signals.

Table 31. PCI-X REQ#/GNT# Layout Guidelines

Parameter	Routing Guidelines
Signal Group	REQ# and GNT# lines
Reference Plane	Route over unbroken reference plane.
Motherboard Impedance (microstrip)	50 ohm ± 15% microstrip and 50 ohm ± 10% stripline
Motherboard Trace Spacing	14 mils microstrip and 12 mils stripline
Add-in Card Impedance	60 ohm ± 15% microstrip and stripline
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline
Group Spacing: Spacing from other groups	25 mils minimum, edge to edge
Trace Length TL1 - from buffer to the connector	• 0.5” min to 4.5” max for 133MHz • 0.5” min to 12.0” max for 100MHz • 0.5” min to 15.0” max for 66MHz
Trace Length TL2 - from connector to the receiver	2.4” - 2.6” max
Vias	$\leq$ 3 vias

6.2.2.1 Point-to-Point Signals (REQ#/GNT#)

This section provides the layout guidelines for REQ# and GNT# lines. Topology in Figure 32 for 133MHz slot design is the same as the one used for point-to-point signals.

Table 32. PCI-X REQ#/GNT# Layout Guidelines

Parameter	Routing Guidelines
Signal Group	REQ# and GNT# lines
Reference Plane	Route over unbroken reference plane.
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline
Motherboard Trace Spacing	14 mils microstrip and 12 mils stripline
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline
Group Spacing: Spacing from other groups	25 mils minimum, edge to edge
Trace Length TL1 - from buffer to the connector	• 0.5” min to 4.5” max for 133MHz • 0.5”min to 12.0” max for 100MHz • 0.5” min to 15.0” max for 66MHz
Trace Length TL2 - from connector to the receiver	2.4” - 2.6” max
Vias	$\leq$ 3 vias

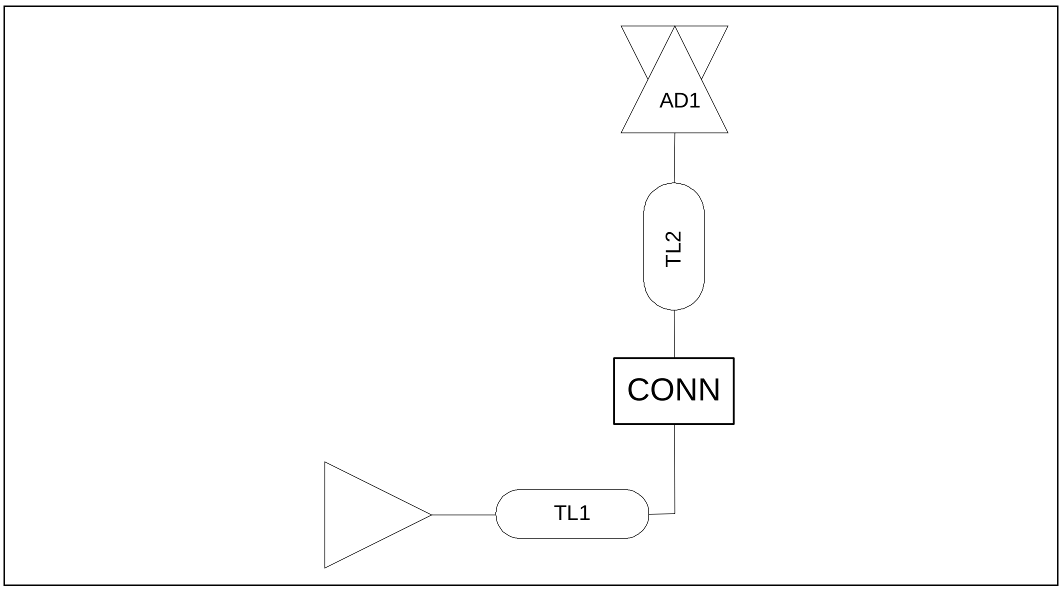
6.2.3 133 MHz One Slot Topology

This section lists the parameters used for the address/data and control lines for 133 MHz single slot design.

Table 33. 133 MHz Single-Slot Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	14 mils microstrip 12 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	14 mils microstrip and stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the connector	1.0” - 6.0” max	0.5” - 5.0” max
Trace Length TL2 - from connector to the receiver	0.75” - 1.5” Max	1.75” - 2.75” Max
Vias	< 3 vias	

Figure 32. 133 MHz One Slot Topology



6.2.4 Embedded 133 MHz Topology

This section lists the parameters used for the address, data and control signals for 133 MHz embedded design with two embedded devices.

Figure 33. Embedded 133 MHz Topology

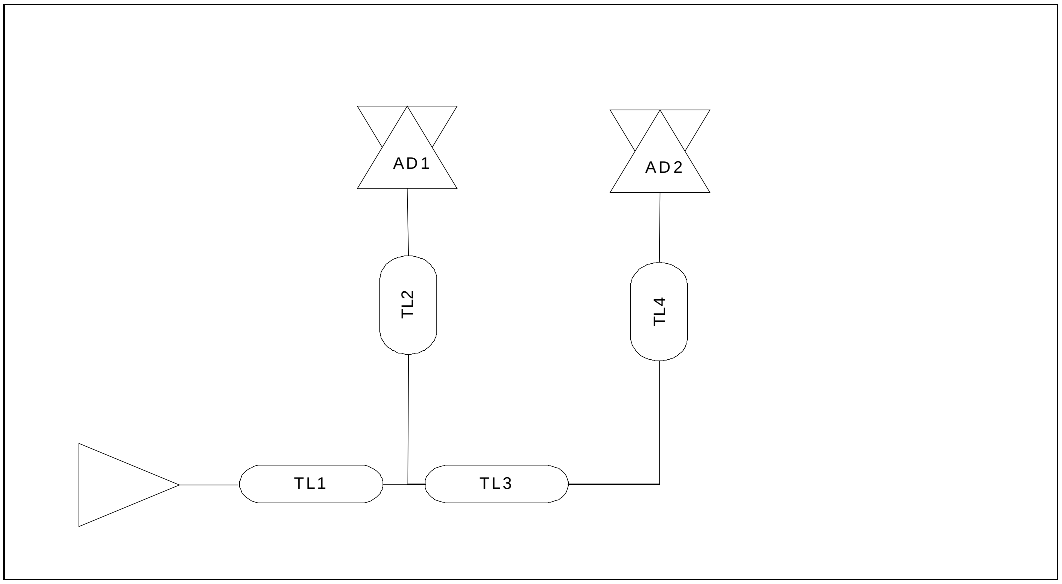


Table 34. Embedded 133 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, Data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (Stripline	50 ohm +/- 10%	
Motherboard Trace Spacing	14 mils microstrip, 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from ball to the junction	0.75" min. to 2.5" max	
Trace Length TL3 - from junction to junction	0.75" min. to 2.5" max	
Trace Length TL2, TL4, from junction to receiver	0.75" min. to 2.5" max	
Vias	< 3 vias	

6.2.5 Mixed 133 MHz Topology

This section lists the parameters used for the address, data and control signals for 133 MHz embedded design with one embedded load and one connector.

Figure 34. Mixed 133 MHz Topology

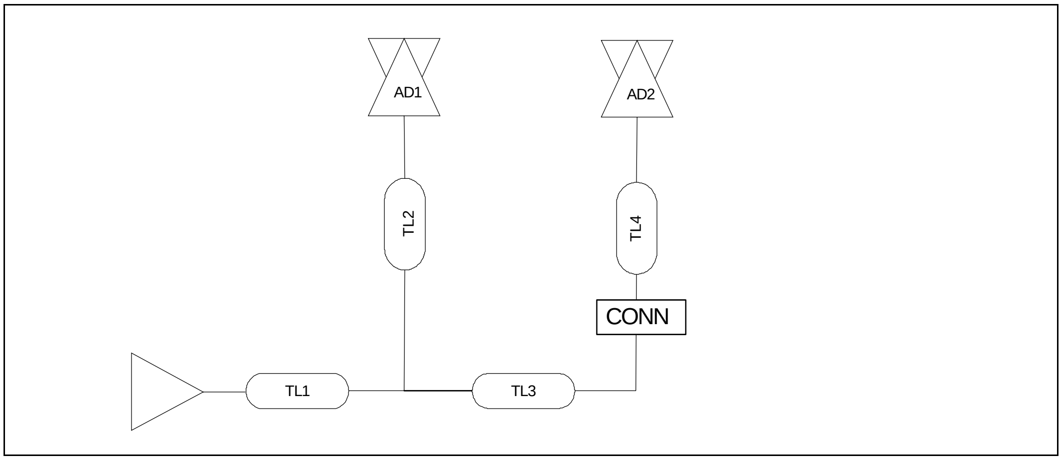


Table 35. Mixed 133 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.0″ max	0.5″ min. to 2.0″ max
Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	0.5″ min. to 2.0″ max
Trace Length TL3, from junction to CONN	0.5″ min. to 3.5″ max	0.5″ min. to 2.25″ max
Trace Length TL4, from CONN to adapter	0.75″ min. to 1.5″ max	1.75″ min. to 2.75″ max
Vias	< 3 vias	

6.2.6 100 MHz Two Slot Topology

This section lists the parameters used for the address, data and control signals for 100 MHz. This topology is shown in Figure 35.

Figure 35. 100 MHz Dual Slot Topology

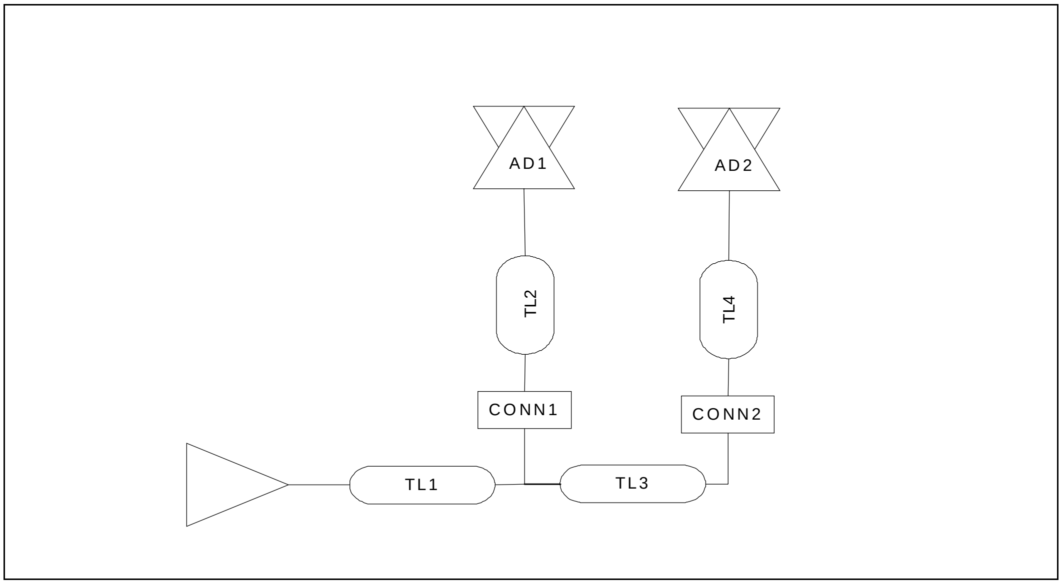


Table 36. 100 MHz Two Slot Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from ball to the connector	0.5” - 12.0” max	0.5” - 10.0” max
Trace Lengths TL3 - Between connectors	0.5” - 3.0” max	0.5” - 3.0” max
Trace Lengths TL2 - from connector to the first receiver, TL4 - from connector to the second receiver	0.75” - 1.50” max	1.75” - 2.75” max
Vias	< 3 vias	

6.2.7 Embedded 100 MHz Topology

This section lists the parameters used for the address, data and control signals for 100 MHz embedded design with five embedded loads.

Figure 36. Embedded 100 MHz Topology

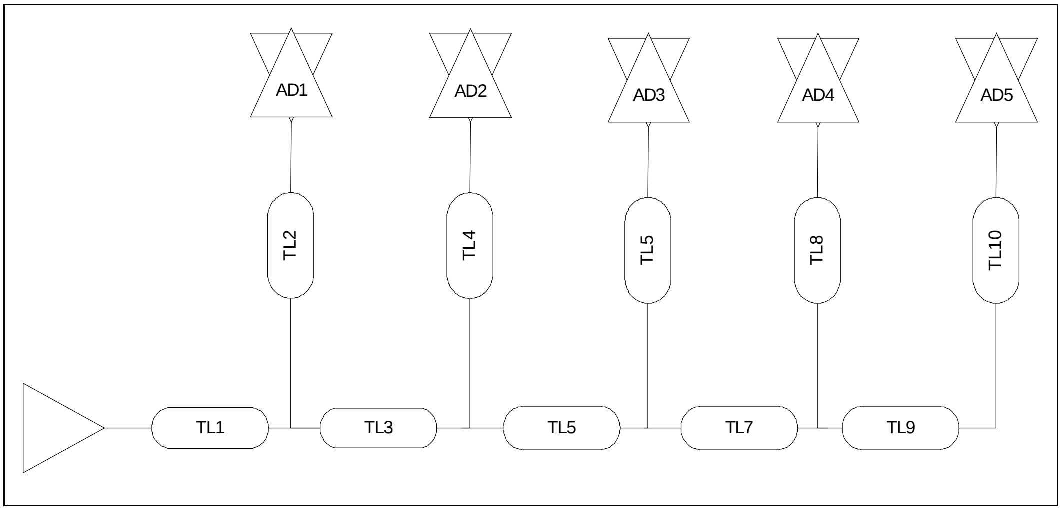


Table 37. Embedded 100 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Group Spacing	spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5" min. to 3.0" max (3 loads, 5 loads)	
Trace Length TL3, TL5, TL7, TL9: from junction to junction	0.5" min. to 2.0" max (3 loads) 0.5" min. to 1.0" max (5 loads)	
Trace Length TL2, TL4, TL6, TL8, TL10: from junction to receiver	0.5" min. to 3.0" max (3 loads) 0.5" min to 2.0" max (5 loads)	
Vias	≤ 4 vias	

6.2.8 Mixed 100 MHz Topology

This section lists the parameters used for the address, data and control signals for 100 MHz embedded design with one embedded load and two connectors.

Figure 37. Mixed 100 MHz Topology

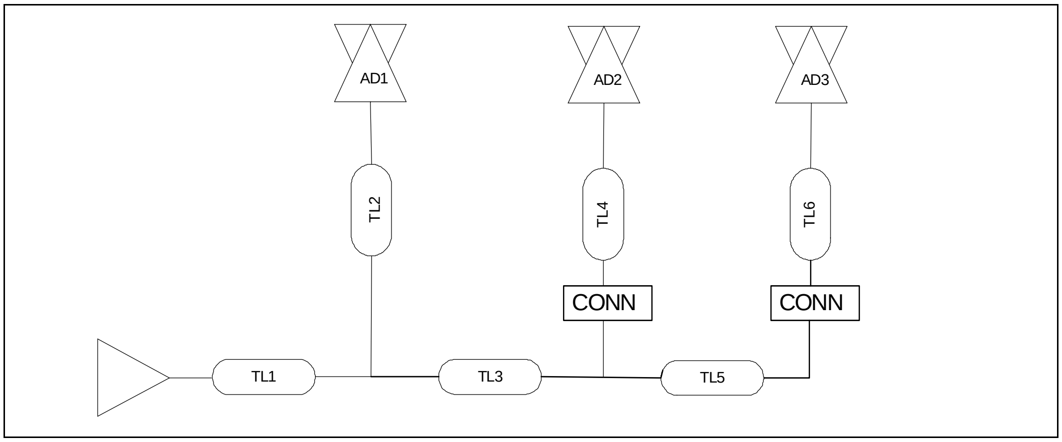


Table 38. Mixed 100 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.5″ max	0.5″ min. to 2.5″ max
Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	0.5″ min. to 2.0″ max
Trace Length TL3, from junction to first CONN	0.5″ min. to 3.5″ max	0.5″ min. to 3.0″ max
Trace Length TL5, from 1st CONN to 2nd CONN	0.5″ min. to 3.5″ max	0.5″ min. to 3.5″ max
Trace Length TL4, from 1st CONN to AD2 Trace Length TL6, from 2nd CONN to AD3	0.75″ min. to 1.5″ max	1.75″ min. to 2.75″ max
Vias	$\leq$ 3 vias	

6.2.9 66 MHz PCI-X Four Slot Topology

This section lists the parameters used for the address, data and control signals for 66 MHz. This topology is shown in Figure 38.

Figure 38. 66 MHz Four Slot Topology

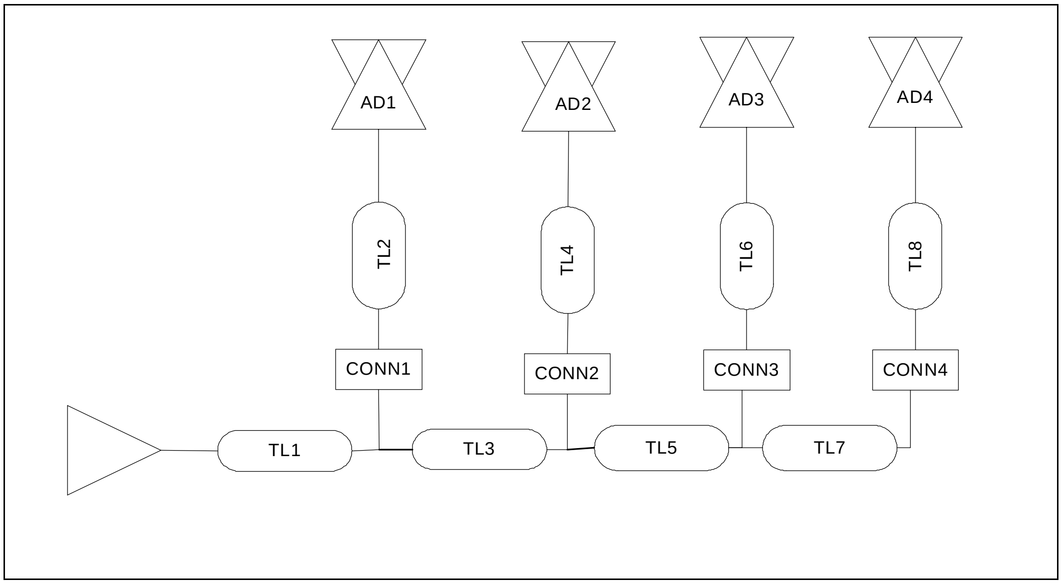


Table 39. 66 MHz Four Slot Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	12 mils microstrip and 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from ball to the connector	0.5" - 12.0" max	0.5" - 9.0" max
Trace Lengths TL3, TL5, TL7 - Between connectors	0.5" - 2.0" max	0.5" - 2.0" max
Trace Lengths TL2, TL4, TL6, TL8- from connector to the first receivers	0.75" - 1.50" max	1.75" - 2.75" max
Vias	$\leq$ 4 vias	

6.2.10 Embedded 66 MHz Topology

This section lists the parameters used for the address, data and control signals for 66 MHz embedded design with 8 embedded loads.

Figure 39. Embedded 66 MHz Topology

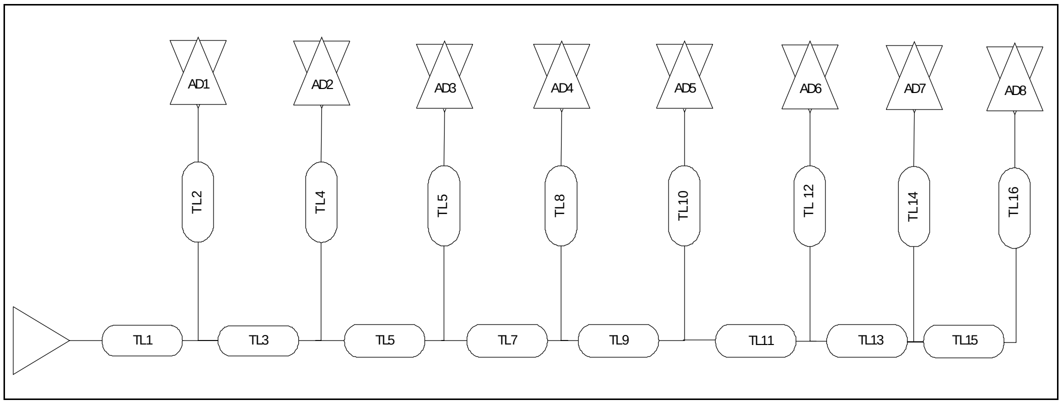


Table 40. Embedded 66 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5" min. to 3.0" max (8 loads) 0.5" min. to 3.5" max (6 loads)	
Trace Length TL3, TL5, TL7, TL9,TL11,TL13,TL15: from junction to junction	0.5" min. to 1.5" max (8 loads) 0.5" min. to 2.5" max (6 loads)	
Trace Length TL2, TL4, TL6, TL8, TL10,TL12,TL14,TL16: from junction to receiver	0.5" min. to 1.5" max (8 loads) 0.5" min to 2.0" max (6 loads)	
Vias	$\leq$ 4 vias	

6.2.11 Mixed 66 MHz Topology

This section lists the parameters used for the address, data and control signals for 66 MHz embedded design with one embedded load and two connectors.

Figure 40. Mixed 66 MHz Topology

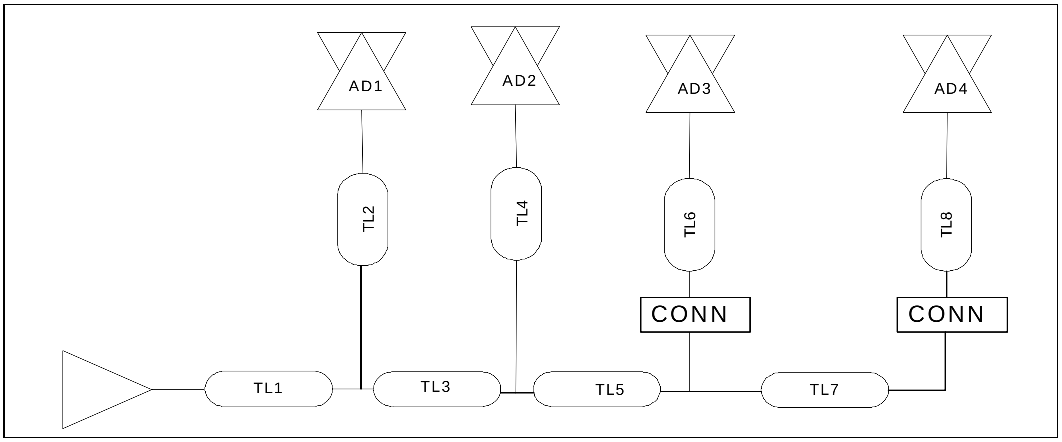


Table 41. Mixed 66 MHz Topology

Parameter	Routing Guidelines	
	Lower AD	Upper AD
Signal Group	Address, data and control line	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	12 mils microstrip and 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5″ min. to 11″ max	0.5″ min. to 10″ max
Trace Length TL2, TL4 - from junction to AD1, AD2	0.5″ min. to 4.5″ max	0.5″ min. to 4.0″ max
Trace Length TL3, TL5, TL7 from junction to junction	0.5″ min. to 4.0″ max	0.5″ min. to 4.0″ max
Trace Length TL6 from 1st CONN to AD3, TL8: from 2nd CONN to AD4	0.75″ min. to 1.5″ max	1.75″ min. to 2.75″ max
Vias	≤ 4 vias	

6.2.12 Additional PCI Layout Notes

- The **P_INT[D:A]#** signals do not have any length restrictions.
- When **PCIX_PULLUP#** is pulled-low, it enables internal pull-ups on the following PCI signals: **P_AD[63:32]**, **P_C/BE[7:4]#**, **P_PAR64**, **P_REQ64#**, **P_ACK64#**, **P_FRAME#**, **P_IRDY#**, **P_TRDY#**, **P_STOP#**, **P_DEVSEL#**, **P_SERR#**, **P_INT[D:A]#**, and **P_PERR#**.
- When application requires external pull-ups on the upper P_AD bus make sure that the location of the pull-up is less than ≤ 1″ from the ball.

7.0 SATA/SAS Bus Layout

This section provides an overview of the SAS and SATA layout recommendations. Due to the fact that the SAS standard supports the interoperability with SATA devices, the layout guidelines for SAS listed in this section are valid for SATA as well.

7.1 SAS/SATA General Recommendations

SATA is a serial differential point-to-point interconnect. For more information on the SATA standard refer to Serial ATA Specification 2.5 found at the www.serialata.org website.

SAS is also a serial differential low-voltage point-to-point interconnect. For more information on the SAS standard, refer to *Serial Attached SCSI 1.1* found at the www.t10.org website.

The analysis was performed for SAS compliant implementations. For more details on meeting the transmitter, receiver compliance and the transfer function (TCTF) refer to the SAS specification.

- Refer to the Table 42 for the for SAS compliant guidelines.
- The SAS inter-enclosure topology is shown in Figure 41 shown with an external cable connecting to a external storage system.
- A SAS intra-enclosure topology is shown in Figure 42 with a connection through the backplane to SAS drives. The intra-enclosure topologies also includes the storage controller directly attaching to the SAS drives.
- Table 43 provides maximum parallel lengths to minimize crosstalk effects.

Figure 41. SAS Inter-enclosure Topology

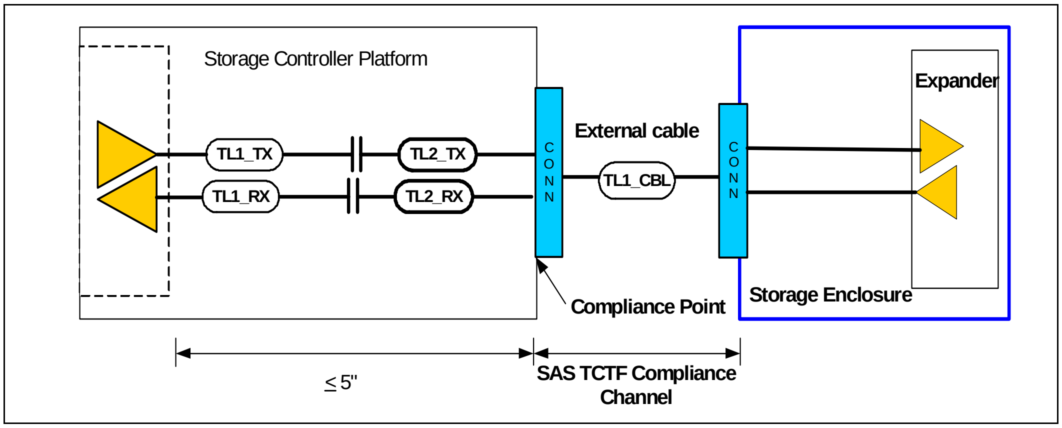


Figure 42. SAS Intra-enclosure Topology

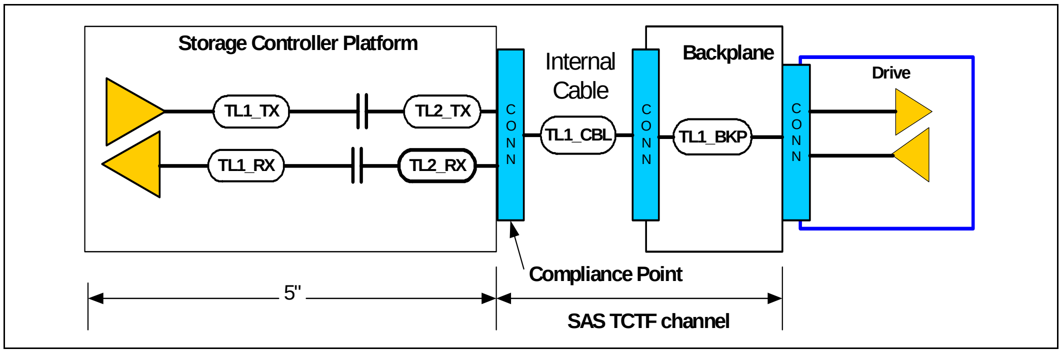


Table 42. SAS Compliant Guidelines

Parameter	Routing Guidelines
Signal Group	**S_TXP[7:0]**, **S_TXN[7:0]**, **S_RXP[7:0]**, **S_RXN[7:0]** Transmit and Receive differential pairs
Reference Plane	Unbroken ground plane preferred
Trace Impedance	100 ohms +/- 15% differential motherboard and adapter card
Trace Spacing	• breakout: SAS pair to pair spacing 20 mils ≤ 0.5” of the device ball • ≥ 50 mils from other types of signals • Refer to Table 43 for interpair spacing recommendations
Group Spacing (edge to edge)	• Keep SAS signals ≥ 50 mils away from the other types of signals. • SAS pair-to-pair spacing is reduced to ≥ 20 mils in the breakout region within 0.5” of the pin field as necessary
Maximum trace length: Motherboard or Add-in card (Intel® 81348 I/O Processor ball to first connector (compliance point))	≤ 5” (max)
Length Matching requirements intrapair (with differential pair)	• Must be matched to within 0.025 inches • Maintain consistent spacing between P and N signals for achieving differential trace impedance (takes precedence over length matching)
AC Coupling on TX+, TX- and RX+, RX-	• 10 nF with low ESR and ESL. • As close to the TX pad as possible
Vias	• Board thickness 0.062 inches max for though hole vias. • Drill width 20mils • No more than 2 vias per signal between device package ball and connector pin • Note: Reducing the number of vias takes precedence over the AC capacitor placement. • Impedance controlled vias (100% +/-15%) preferred

Table 43. Interpair (Between Pair) Spacing Requirements

Parallel Routed Length Next to Each Other	Microstrip/Stripline	Spacing Recommendation Between Lanes (edge to edge in mils)
0 - 2”	Microstrip	25
2 - 5”	Microstrip and Stripline	30

8.0 Peripheral Local Bus

This section provides the layout guidelines for the Peripheral Bus Interface Unit (PBI) of Intel® 81348 I/O Processor. The PBI bus is commonly used to interface Flash components to the Intel® 81348 I/O Processor Peripheral Bus.

The PBI unit includes two chip enables. The PBI chip enables activate the appropriate peripheral device when the address falls within one of the PBIs two programmable address ranges. Each chip enable supports up to 32 MBytes of addressability.

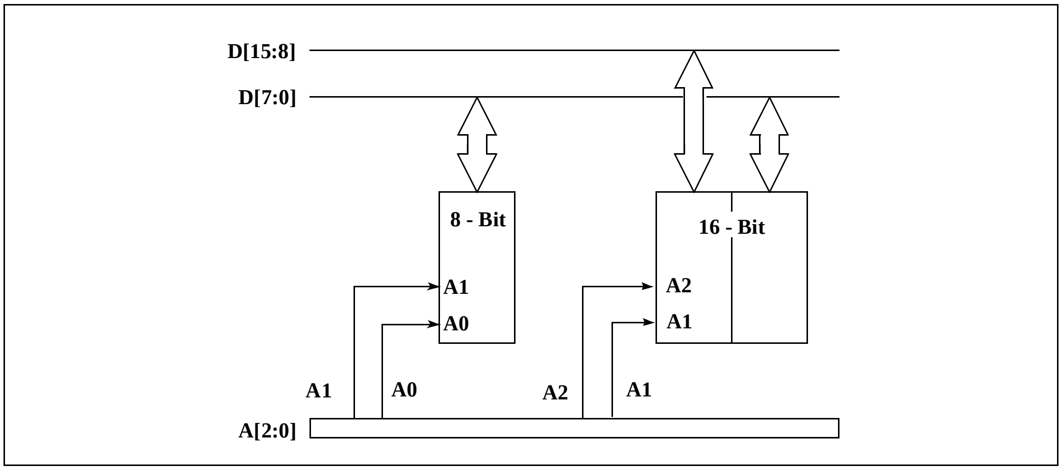
8.1 Peripheral Bus Signals

Bus signals consist of three groups: address A[24:0], data D[15:0], and control/status lines POE#, PWE#, PCE[1:0], PB_RSTOUT#.

8.2 PBI Bus Width

The PBI allows an 8-, or 16-bit data bus width for each range. The PBI places 8- and 16-bit data on low-order data signals, simplifying the interface to narrow bus external devices. As shown in Figure 43, 8-bit data is placed on lines **D[7:0]**; 16-bit data is placed on lines **D[15:0]**.

Figure 43. Data Width and Low Order Address Lines



The user needs to wire up the Flash memories in a manner consistent with the programmed bus width:

- 8-bit region: **A[1:0]** provide the demultiplexed byte address for a read burst.
- 16-bit region: **A[2:1]** provide the demultiplexed short-word address for a read burst.

8.3 Flash Memory Support

PBI peripheral bus interface supports 8-, or 16- bit Flash devices. Figure 45 shows two 8-bit Flash devices connect with the Intel® 81348 I/O Processor through the PBI Interface.

Figure 44. Sixty-Four Mbyte Flash Memory System

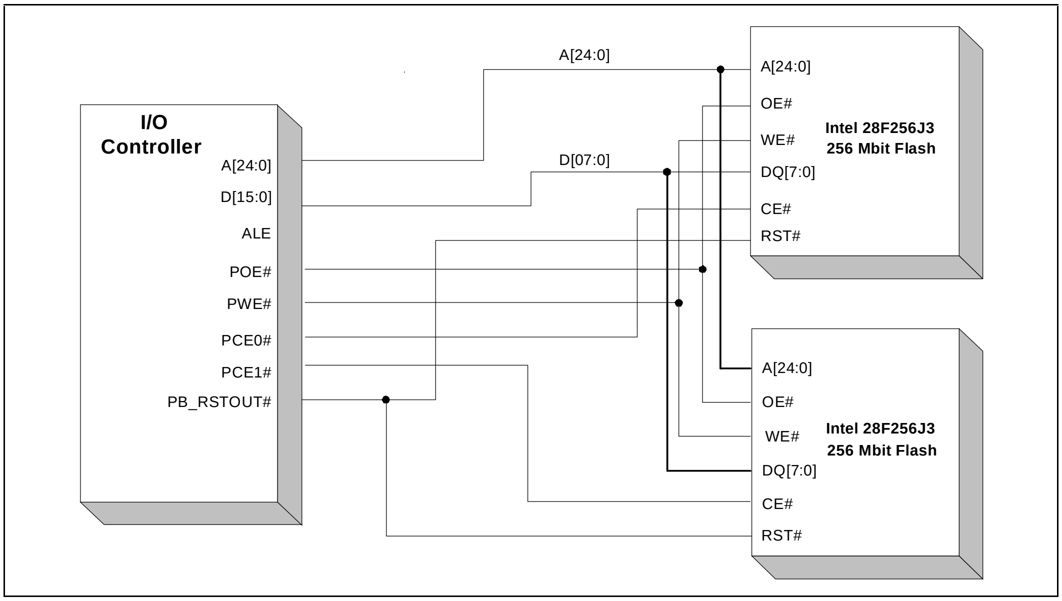
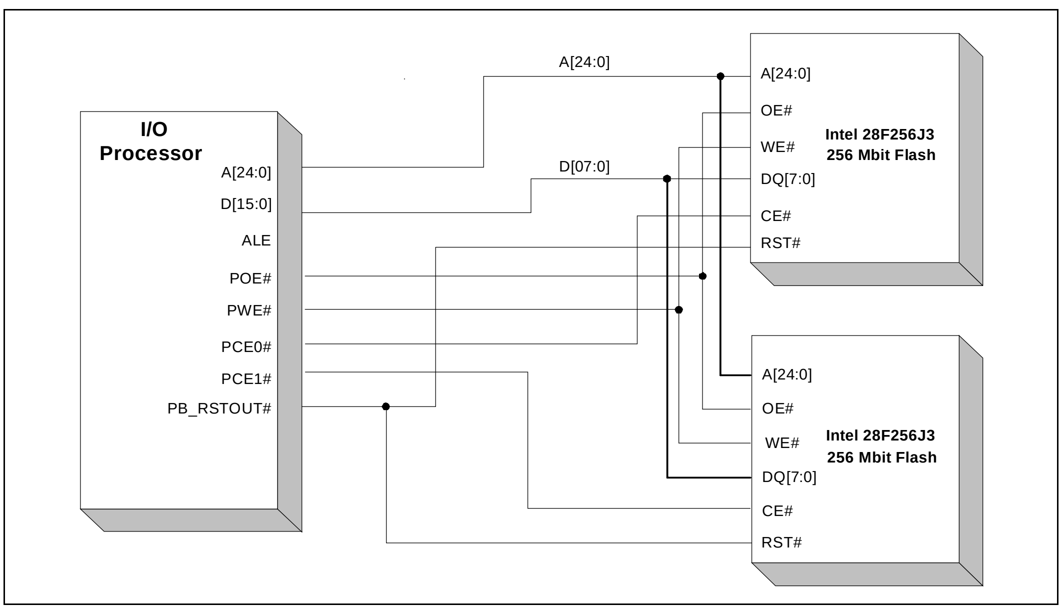


Figure 45. Sixty-Four Mbyte Flash Memory System



8.4 PBI Topology Layout Guidelines

This section provides the topologies for routing the Address and Data bus for single load, double load and three load topologies. Note that no length matching is required between the Address and Data lines.

Figure 46. Peripheral Bus Single Load Topology

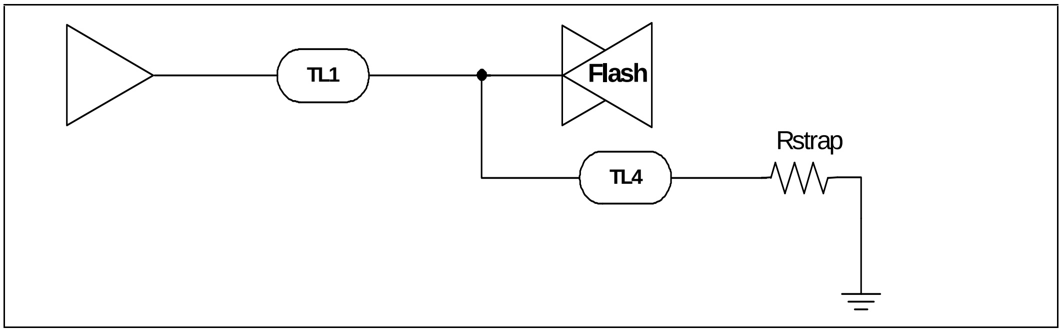


Table 44. PBI Routing Guideline Single Load

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane or unbroken power plane. When routing over power plane maintain this consistency throughout the topology.
Routing	Microstrip or stripline or combination of microstrip and stripline.
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%
Add-in card Impedance (for both microstrip and stripline)	60 ohms +/- 15%
Trace Spacing (edge to edge)	• $\geq$ 5 mils between all Address and Data lines • $\geq$ 20 mils must be maintained from all other signals or vias (for 5 mils trace width)
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Trace Length TL1	0” to 20.0”
Trace Length to strapping resistors TL4	0.5” to 3.0” from the last device on the bus.
Routing Recommendations	Number of vias $\leq$ 8
Routing Recommendations	Route as Daisy Chain

Figure 47. Peripheral Bus Dual Load Topology

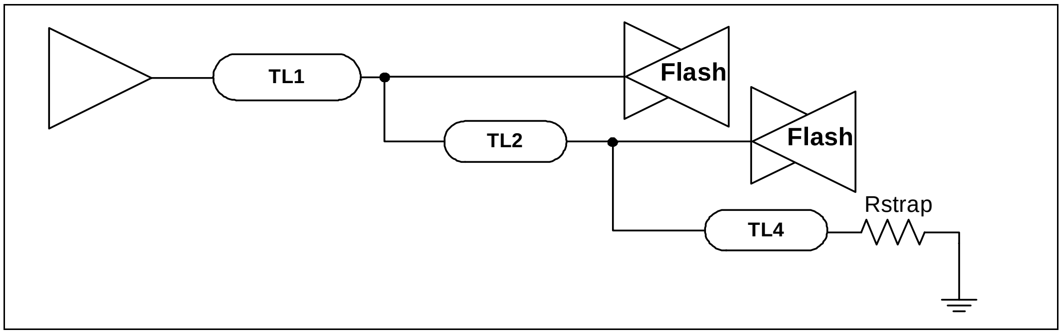


Table 45. PBI Routing Guidelines for Two Loads

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane or unbroken power plane. When routing over power plane maintain this consistency throughout the topology.
Routing	Microstrip or stripline or combination of microstrip and stripline
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%
Add-in card Impedance (for both microstrip and stripline)	60 ohms +/- 15%
Trace Spacing (edge to edge)	• ≥ 5 mils between all Address and Data lines • ≥ 20 mils must be maintained from all other signals or vias (for 5 mils trace width)
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils
Trace Length TL1	2.0" to 20.0"
Trace Length to TL2	0.5" to 2.0"
Trace Length to strapping resistor TL4	0.5" to 3.0" from the last device on the bus
Routing Recommendations	Number of vias for microstrip ≤ 8
	Route as daisy-chain only

Figure 48. Peripheral Bus Three Load Topology

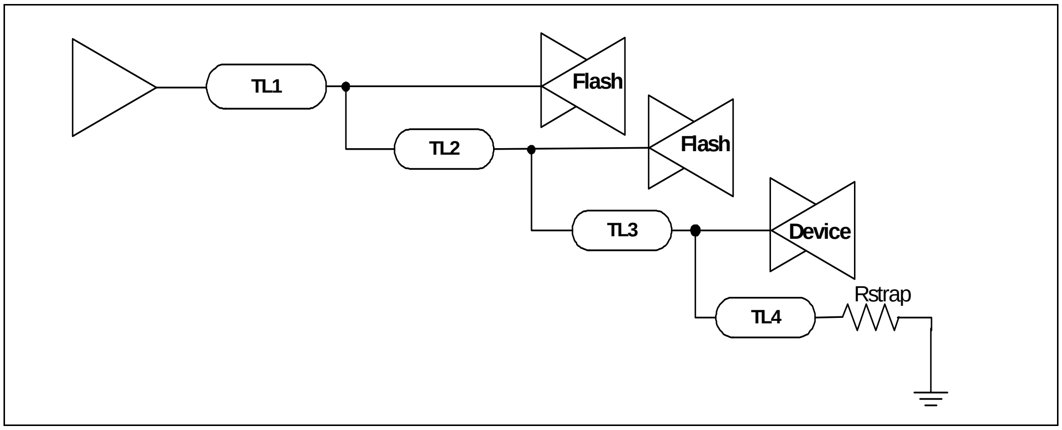


Table 46. PBI Routing Guideline for Three Loads

Parameter	Routing Guidelines
Reference Plane	Route over unbroken ground plane or unbroken power plane. When routing over power plane maintain this consistency throughout the topology.
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Routing	Microstrip or stripline minimize the layer changes.
Motherboard Impedance (for both microstrip and stripline)	50 ohms +/- 15%
Add-in card Impedance (for both microstrip and stripline)	60 ohms +/- 15%
Trace Spacing (edge to edge)	• ≥ 5 mils between all Address and Data lines • ≥ 20 mils must be maintained from all other signals or vias (for 5 mils trace width)
Breakout	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.
Trace Length TL1	2.0” to 20.0”
Trace Length TL2, TL3	0.5” to 2.0”
Trace Length to strapping resistor TL4	0.5” to 3.0” from the last device on the bus.
Routing Recommendations	Number of vias for microstrip ≤ 8
	Route as daisy-chain only

9.0 Power Delivery

This section provides information on the power delivery for this chip including:

- the different voltage domains that are required on the Intel® 81348 I/O Processor are provided in Table 47
- an example of the power plane layout used on the eight layer customer reference board Section 9.1
- decoupling recommendations Section 9.2
- required power sequencing Section 9.3
- the power failure recommendations Section 9.4

Table 47. Supply Voltages

Voltage Supply	Voltage	Minimum	Maximum
V_{CC3P3}	3.3 V supply voltage for PCI-X interface and general purpose I/Os	3.0	3.6
V_{CC1P8S}	1.8 V supply voltage for storage interface	1.71	1.89
V_{CC1P8E}	1.8 V supply voltage for PCI Express* interface	1.71	1.89
V_{CC1P8}	1.8 V supply voltage for DDR2 SDRAM memory interface I/Os	1.71	1.89
V_{CCVIO}	3.3 V supply voltage for PCI-X interface	3.0	3.6
V_{CC1P2X}	1.2 V supply voltage for Intel XScale® processors	1.164	1.236
V_{CC1P2}	1.2 V supply voltage for most digital logic	1.164	1.236
V_{CC1P2E}	1.2 V supply voltage for PCI Express* interface digital logic	1.164	1.236
$V_{CC1P2AE}$	1.2 V supply voltage for PCI Express* interface analog logic	1.164	1.236
$V_{CC1P2AS}$	1.2 V supply voltage for storage interface analog logic	1.164	1.236
$V_{CC1P2DS}$	1.2 V supply voltage for storage interface digital logic	1.164	1.236
VCC1P2PLLS0	1.2 V supply voltage for storage PLL 0	1.164	1.236
VCC1P2PLLS1	1.2 V supply voltage for storage PLL 1	1.164	1.236
VCC1P2PLLP	1.2 V supply voltage for PCI-X PLL	1.164	1.236
VCC1P2PLLD	1.2 V supply voltage for DDR2 SDRAM PLL	1.164	1.236
VCC3P3PLLX	3.3 V supply voltage for core logic PLL	3.0	3.6
M_VREF	Memory I/O reference voltage	$0.49V_{CC1P8}$	$0.51V_{CC1P8}$

— ESL for a 0603 package is 150pH, divide this by 6 = 25nH

— Total ESL: 25nH || 19 pH = ~ 18.9pH

9.1 Power Plane Layout

This section provides the layout of the power planes around the Intel® 81348 I/O Processor package on the eight-layer customer reference board (CRB).

These figures provide additional supplies required for the Intel® 81348 I/O Processor storage interface and are included in the Intel® 81348 I/O Processor design guide for reference purposes.

The voltage plane descriptions are listed in Table 48 and the stackup for the customer reference board is listed in Table 49. Figure 49 provides the voltage layout for layer 3, Figure 50 provides the voltage layout for layer 5, Figure 51 provides the voltage layout for layer 6 and Figure 52 provides the voltage layout for layer 8.

Note: That with careful power supply layout, 1.2V and 1.8V switching regulators are used to generate each of the 1.2V and 1.8V supplies. It is important to connect the +1_2V and +1_2VA supplies at a single point such as the 1.2V switching regulator output capacitor. This same recommendation applies to connecting the +1_8V and +1_8VA at a single point such as the 1.8V switching regulator output capacitor.

Table 48. Customer Reference Board Voltage Planes

CRB Voltage Plane	Package Voltage Planes	Voltage Source	Voltage Description	Notes
+1_2V	VCC1P2X, VCC1P2	1.2V Switching Regulator	1.2V digital voltage for core logic	Connect +1_2V and +1_2VA only at a single point.
+1_2VB[1]	VCC1P2DS		1.2V digital voltage for storage	
+1_2VA	VCC1P2AE, VCC1P2AS, VCC1P2E	1.2V Switching Regulator	1.2V analog voltage for PCI-E and storage interfaces	
+1_8VA	VCC1P8E, VCC1P8S	1.8V Switching Regulator	1.8V analog voltage for PCI-E and storage interfaces	Connect +1_8V and +1_8VA only at a single point.
+1_8V	VCC1P8	1.8V Switching Regulator	1.8V digital voltage for DRAM interface.	
+3_3V	VCC3P3, VCCVIO	System power	3.3V digital voltage for PCI-X and peripheral bus interfaces	

1. +1_2VA and +1_2VB are supplied from the same regulator on the CRB.

Table 49. Customer Reference Board Layer Stackup

Layer	Layer Description	Voltage Planes	Color Code
1	Primary side	none	
2	Ground plane 1		
3	Internal routing layer 1	+1_2V	Red
		+1_2VB	Blue
		+1_8VA	Yellow
		+1_2VA	Purple
		+3_3V	Pink
4	VCC split plane	+1_2V	Red
		+3_3V	Pink
5	Ground plane 2		
6	Internal routing layer 2	+1_2V	Red
		+1_2VB	Blue
		+1_2VA	Purple
		+3_3V	Pink
		+1_8V	Green
7	Ground plane 3		
8	Secondary layer	+1_8VA	Yellow
		+1_8V	Green

Figure 49. Split Voltage Planes for Layer 3 (Top View)

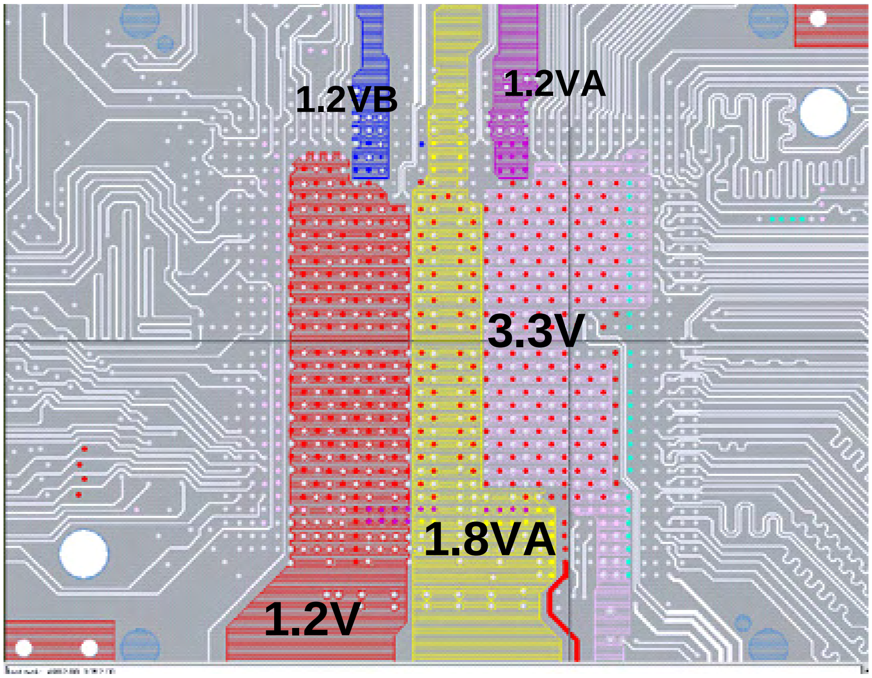


Figure 50. Split Voltage Planes for Layer 4 (Top View)

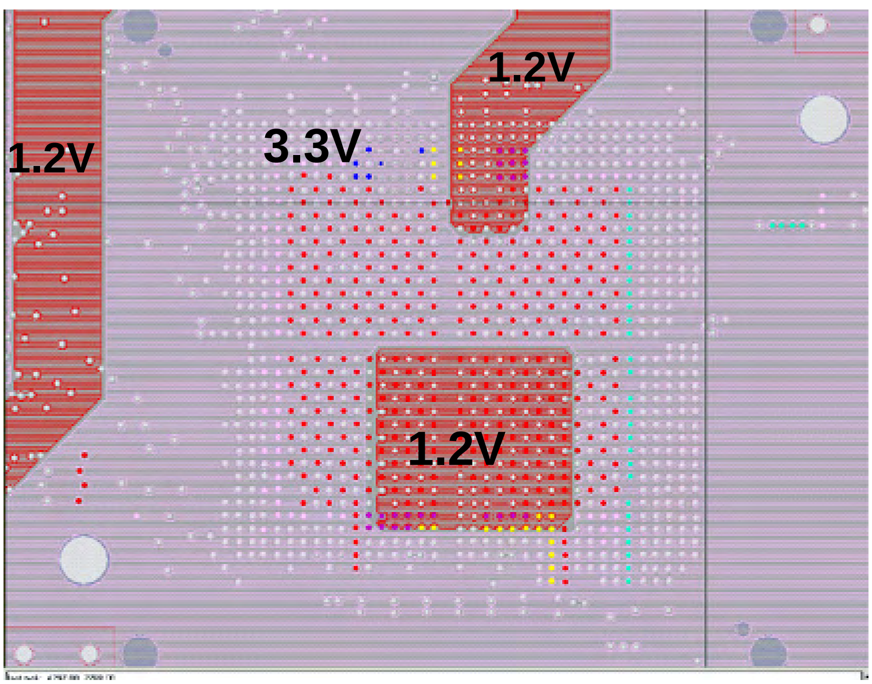


Figure 51. Split Voltage Planes for Layer 6 (Top View)

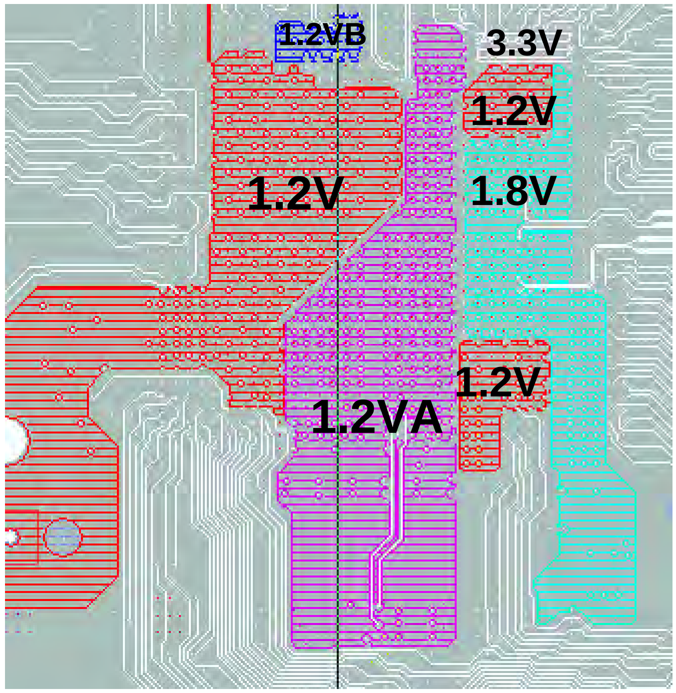
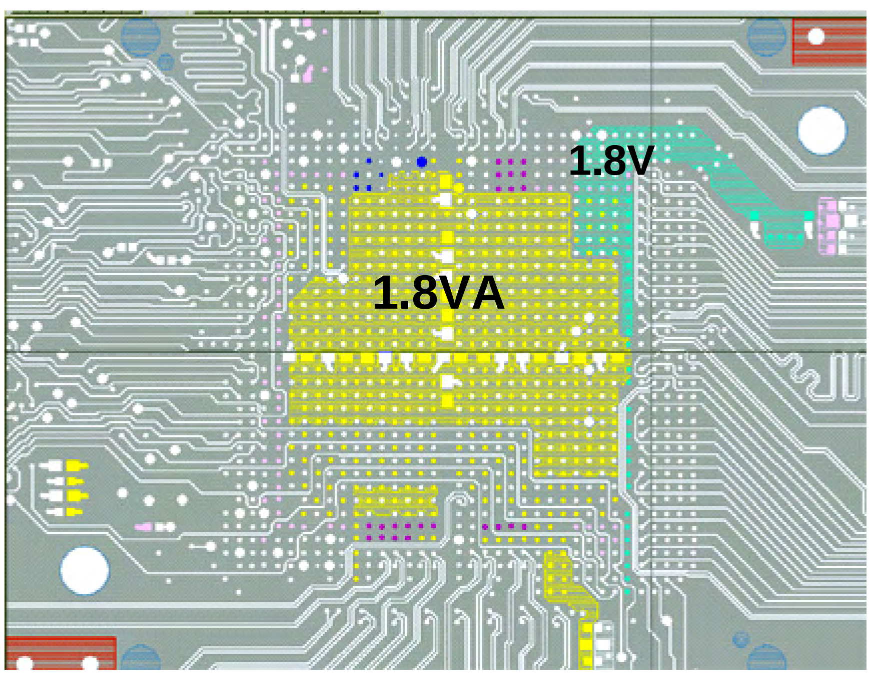


Figure 52. Split Voltage Planes for Layer 8 (Top View)



9.2 Decoupling Recommendations

Table 50 contains the decoupling recommendations for Intel® 81348 I/O Processor. Note that the recommendations provide the total minimum capacitance for each voltage plane. The recommended decoupling capacitance, ESR and ESL for each voltage plane is an minimum aggregate value that is achieved with adding multiple decoupling capacitors in parallel. An example of implementing these decoupling guidelines is provided with the customer reference board decoupling values listed in Section 9.2.1.

Each decoupling capacitor is placed with a single via to a voltage plane (or plane fill area) and solid ground plane, such that copper loss and inductance between the capacitor and nearby ball via is negligible. Distribute the capacitors so that all power ball vias have decoupling nearby. It is recommended that the distance from ball vias to decoupling be minimized.

Note: The 1.2V High Speed Voltage for the SAS/SATA and the PCI Express is generated from a regulator that is isolated from the 1.2V core regulator.

Table 50. Decoupling Recommendations

Voltage	Interface	Capacitors
1.2V Digital	Intel XScale® microarchitecture 1 Voltage	1 x 20uF min with < 150pH ESL, ~1mohm ESR
	Intel XScale® microarchitecture 2 Voltage	1 x 20uF min with < 150pH ESL, ~1mohm ESR
1.2V High Speed Serial	PCI Express	1 x 5 uF min with < 150pH ESL, ~3mohm ESR
	SAS/SATA	1 x 5 uF min with < 150pH ESL, ~3mohm ESR
1.2V Analog	SAS/SATA Serial Interface	1 x 5 uF min with < 150pH ESL, ~3mohm ESR
1.8V Digital	DDR2, SAS/SATA	1 x 10uF with < 100pH ESL, ~1mohm ESR
1.8V Analog	SAS/SATA	1 x 5 uF min with <150pH ESL, ~3mohm ESR
	PCI Express, SAS	1 x 5 uF min with <150pH ESL, ~3mohm ESR
3.3V	PCI-X	1 x 10 uF min with <150pH ESL, ~1mohm ESR

9.2.1 Customer Reference Board Decoupling Implementation

Table 51 provides the decoupling used on the Intel® 81348 I/O Processor customer reference board. The recommendation for a minimum of 20uF capacitance with a ESL of < 150pH and a ESR of ~1ohm for each of the core voltages are calculated with the capacitors provided in Table 51 as follows:

- Total capacitance = (6 x 4.7uF) + (14 x 1uF) = 42.2uF total for both cores
- Calculating equivalent ESR:
  - — ESR for a 0402 package is 15mOhms, divide this by 14 (number of caps) = 1.07mOhm
  - — ESR for a 0603 package is 10mOhms, divide this by 6 = 1.67mOhms
  - — Total ESR: 1.67mOhms || 1.07mOhms = ~0.65 mOhms
- Calculating equivalent ESL:
  - — ESL for a 0402 package is 278pH, divide this by 14 = 19pH
  - — ESL for a 0603 package is 150pH, divide this by 6 = 25pH
  - — Total ESL: 25pnH || 19 pH = ~ 10.8pH

Note: The symbol "||" represents inductors or resistors in parallel. The equivalent inductance is calculated as the product of the two inductances divided by the sum of the two inductances. The equivalent resistance is calculated as the product of the two resistances divided by the sum of the two resistances.

Table 51. Customer Reference Board Decoupling Example

Voltage	Interface	Quantity	Capacitors (uF)	Package
1.2V Digital	Intel XScale® microarchitecture Voltages	6	4.7	0603
		14	1	0402
1.2V High Speed	PCI Express and SAS/SATA	6	4.7	0603
		15	1	0402
1.8V Digital	DDR2 SAS/SATA	1	4.7	0603
		7	1	0402
1.8V High Speed	PCI Express SAS/SATA PHY	2	4.7	0603
		6	1	0402
3.3V	PCI-X	2	4.7	0603
		8	1	0402

9.3 Power Sequencing

The Intel® 81348 I/O Processor requires the following power sequence:

Power-up: 1.8V <= 1.2V

- 1.8V supply must not turn on before or any faster than the 1.2V supplies.

Power Down: 1.8V <= 1.2V

- 1.8V turns off first, or, 1.8V must reach 1.2V before 1.2V begins ramping down.

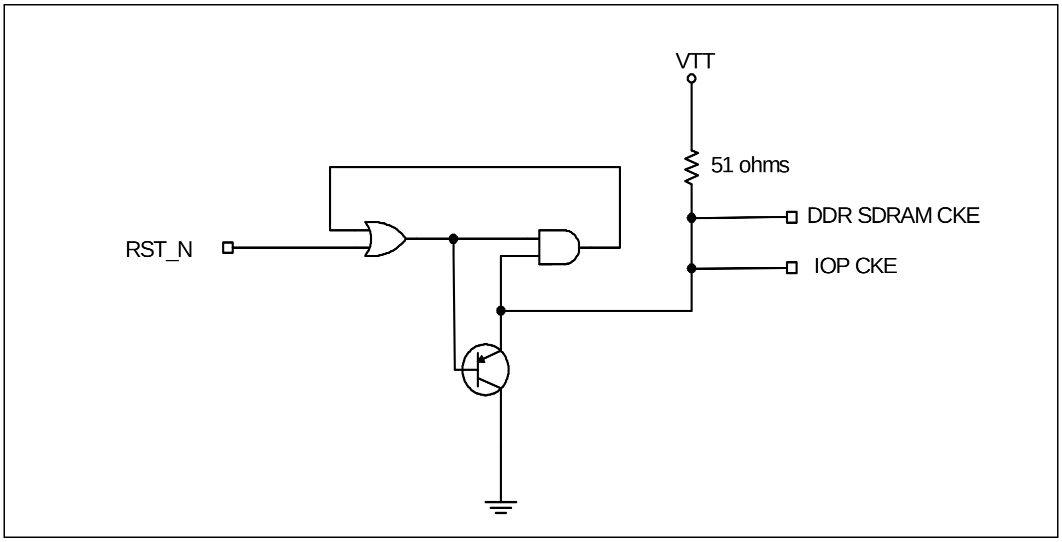
9.4 Power Failure

The following list provides details on the power failure mode:

- Intel® 81348 I/O Processor always attempts to the put the DRAM in the self refresh mode whenever power is lost.
- During battery backup mode it is recommended that power to the Intel® 81348 I/O Processor be isolated and only the DRAM be powered in order to reduce battery power drain.
- CKE[1:0] must remain deasserted regardless of the state of V_{CC} powering the Intel® 81348 I/O Processor during the battery backup mode. Figure 53 shows an implementation of the CKE latching circuit to maintain the DRAM in self refresh. Note that the 51 ohms pull-up to VTT is shown as the typical termination for the CKE lines. Additional information on terminating the CKE lines is detailed in Section 4.2.2.3.

VTT is turned off battery backup needs to maintain power on DDR voltages $\mathbf{V_{DD}}$, $\mathbf{V_{DDQ}}$ and $\mathbf{V_{REF}}$ to prevent data loss.

Figure 53. SCKE Circuit



9.4.1 Non-Battery Backup Circuits

For applications not supporting battery back-up, the circuit in Figure 53 is not required. Instead the following is recommended:

- Connect **CKE** pins directly from Intel® 81348 I/O Processor to the CKE pins on the SDRAM.

10.0 JTAG Circuitry for Debug

Certain restrictions exist in order to use JTAG based debuggers with the Intel XScale® microarchitecture. This is primarily due to the Tap Controller reset requirements of the Intel XScale® microarchitecture and the reset requirements of specific JTAG debuggers. The following outlines these requirements along with suggestions for circuitry to alleviate potential problems

10.1 Requirements

The Intel® 81348 I/O Processor, requires that TRST# (Tap Reset) is asserted during power-up. This is to ensure a fully initialized boundary scan chain. Failure to comply with this requirement results in spurious behavior of the application.

The ARM* Multi-ICE* JTAG debugger requires that TRST# is always weakly pulled high. This requirement stems from the fact that the debugger only asserts TRST# (drive low). Both reset signals coming from the Multi-ICE™ (TRST# and SRST#) are open collector and must be weakly pulled high in order to avoid unintentional resets (System or TAP).

JTAG Board Layout Tips:

- Make the connector easily accessible with a debugger by positioning it near the edge of the board.
- Label the debug connector and pin 1 on the silk-screen of the PCB.
- The debug connector is at the end of the JTAG chain nets, not in the center of the nets.
- **TCK**, **TDI**, **TDO**, **TRST#** and **TMS** signals do not have length restrictions but keep these signals as short as possible and close to equal in length.

10.2 JTAG Signals / Header

Figure 54 provides the pin definition (20-pin standard ARM connector) for JTAG. Figure 55 is the pin out for a smaller profile 10 pin connector. Note that the nTRST is equivalent to the TRST# and the nSRST is equivalent to the SRST#. The connector in Figure 55 is provided as an alternative to the 20 pin to save on board space. This connector is implemented on the customer reference board. This part is a 10 pin, 2 x 5, surface mounted header with 2 mm spacing.

Figure 54. JTAG Header Pin Out

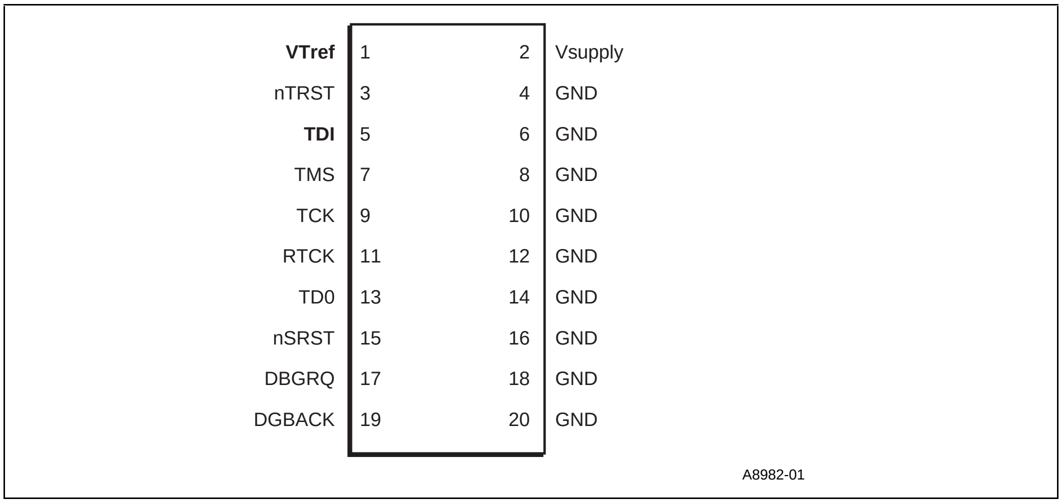
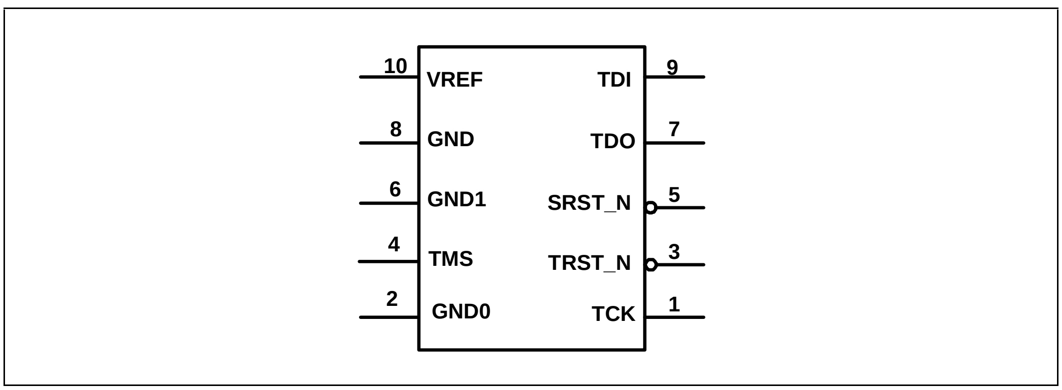


Figure 55. Mini JTAG Header Pin Out



The ARM Multi-ICE debugger along with the Macraigor Raven* and WindRiver Systems* visionPROBE / visionICE utilize this connector. The main difference is the specific implementation of TRST# for each debugger. The Macraigor Raven implementation actively drives TRST# (high and low). The WindRiver Systems* visionPROBE / visionICE configures TRST# active or open collector (only drive low). ARM Multi-ICE is configured as open collector only.

10.3 System Requirements

In order to successfully invoke a debug session, the JTAG debug unit must be able to control TRST# and SRST# independently. The TRST# signal allows the debugger to get the TAP controller in a known state. The SRST# signal allows the debugger to control system/processor reset in order to download the debug handler via the JTAG interface.

Figure 56 and Figure 57 are used as examples without reflecting actual signal timings.

Figure 56. JTAG Signals at Powerup

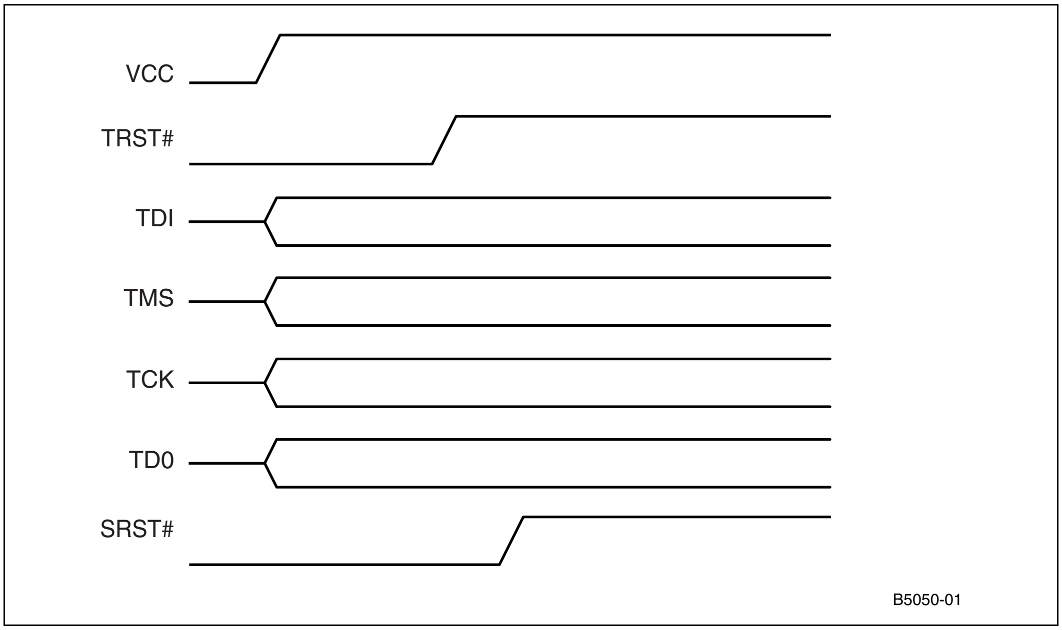
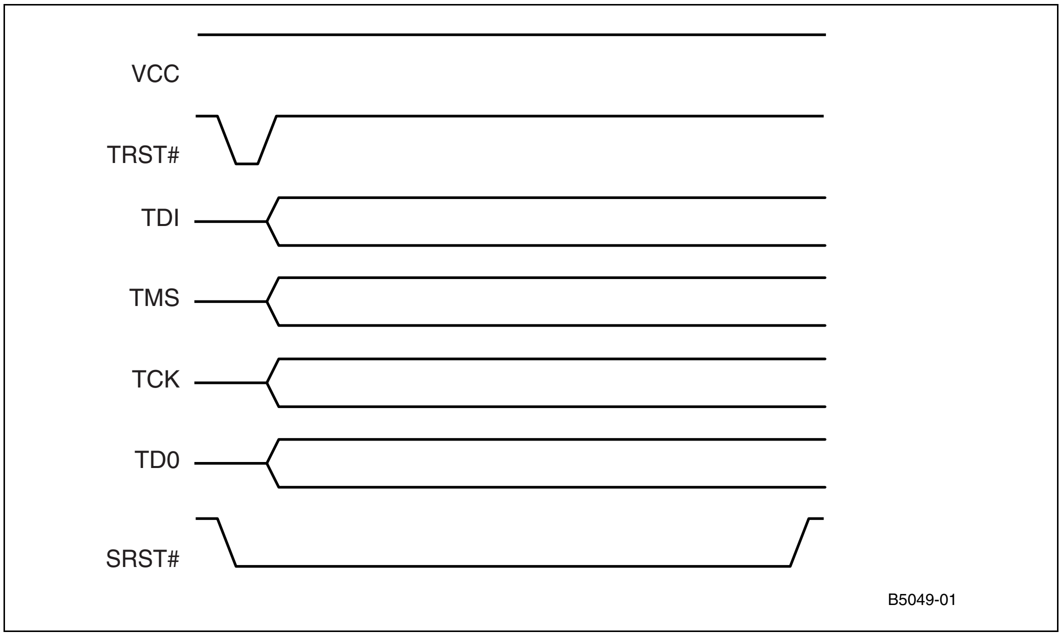


Figure 57. JTAG Signals at Debug Startup



10.4 JTAG Hardware Requirements

Due to the conflicting requirements of Multi-ICE* and the Intel XScale® microarchitecture, it is necessary to incorporate a circuit that drives **TRST#** low at power-up and weakly pull it high at all other times. The following section details the circuits required for the Macraigor Raven*, WindRiver Systems* visionPROBE*/visionICE*, and ARM* Multi-ICE*. Figure 58 provides the JTAG section from the customer reference board. Note that for JTAG debuggers that actively drive the JTAG signals resistor MR_N must be installed. For debuggers that have open collector outputs this resistor MR_N is removed.

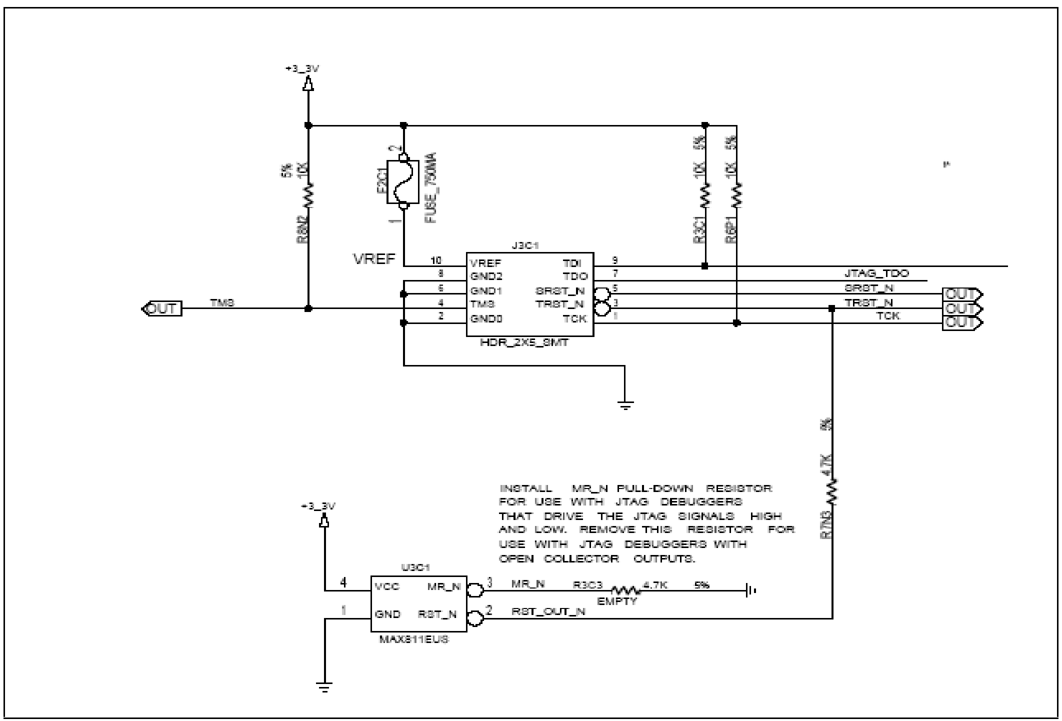
10.4.1 Macraigor Raven and WindRiver Systems visionPROBE/visionICE

Both the Macraigor Raven and WindRiver Systems visionPROBE/visionICE (when configured as active) do not require any special power-up circuitry. The requirement is that TRST# is weakly pulled down at the processor. It is suggested that the value of the pull-down resistor is 10 KΩ or greater. The value of this resistor needs to be confirmed with the JTAG debugger manufacturer to ensure optimal performance.

10.4.2 ARM Multi-ICE

The ARM Multi-ICE debugger requires special power-up circuitry due to the open collector implementation of the TRST# signal. This power-up circuit must ensure that TRST# is asserted (low) at power on and weakly pulled high thereafter. Refer to Figure 58 for an example of the Power-Up Circuit for TRST# based on the customer reference board.

Figure 58. Example Power-Up Circuit for TRST#



11.0 Debug and Test

This chapter provides information on test equipment that is used to test the PCI-X, PCI Express and SAS/SATA interfaces of this part. It is recommended to check the bus interface and manufacturer websites for the latest test techniques and test equipment.

11.1 PCI-X Debugging

There are several tools available that aid in the debug and development of PCI-X bus based systems and cards. Agilent Technologies*, VMetro* and Catalyst Enterprises* make analyzer/exercisers cards for capturing and generating PCI-X transactions. These cards also provide capability to trigger on errors, emulate an initiator or target, invoke errors, measure performance, and check for protocol and compliance issues. For pure analysis of the PCI-X bus, both Tektronix and Agilent make passive interposer probe cards that plug into the PCI-X slot of the device under test to capture PCI-X traffic. An example of an interposer card that works with the Agilent logic analyzers is the FuturePlus Systems* FS2007. Another method to capture the PCI-X bus signals with a logic analyzer is to place AMP* Mictor-38 connectors or Agilent Soft Touch Connectorless Probes on the PCB. For the pinout of the connectors that work with the Agilent logic analyzer refer to the FuturePlus Systems* website www.futureplus.com.

11.2 PCI Express Debugging

Debugging a PCI Express design requires analysis at the physical layer to verify the layout and the data link/transaction layer to ensure that the read and write request packets are being transmitted correctly.

11.2.1 Physical Layer Debugging

For PCI Express, the fundamental signaling frequency is 1.25GHz (half the bit rate) and the specified 20-80% rise-time is 100 ps. The Tektronix™TDS6604 Real-Time Digital Storage Oscilloscope and the Agilent Technologies ™ 54855A provides an analog bandwidth of 6 GHz (with a 20GSa/sec. sampling rate) sufficient to measure the PCI Express differential signals with their respective differential probes.

The alternative equipment to the high speed oscilloscopes include Vector Network Analyzers or Time Domain Reflectometry (TDR) scopes which help pinpoint signal integrity issues with the PCBs and connectors. This test equipment allows checking the lane-to-lane skew, analyzing jitter and measuring drive strength and receiver tolerance for verification of the physical layer. For more information on using TDR analysis, the application note from Tektronix is useful:

TDR Impedance Measurements: A Foundation for Signal Integrity.

11.2.2 Data Link and Transaction Layer Testing

The Data Link/Transaction layer is debugged and validated with PCI Express protocol analyzers or PCI Express analyzer/exerciser tools. Companies that make protocol analyzers for PCI Express include: Catalyst Enterprises, LeCroy (formerly CATC), Agilent, Tektronix and Finisar (formerly DataTransit). For more information on the PCI Express test equipment refer to Intel's PCI Express Developer's website http://www.pciexpressdevnet.org/kshowcase/. The probing solutions for the PCI Express bus include an interposer card and a mid-bus probing solution.

Agilent Technology has a PCI Express Packet Analysis Probe N4220B which works in conjunction with their 16700 family of logic analyzers. The Agilent slot interposer part numbers that work with the 16700 logic analyzer include: N4224A for a x8 slot, N4225A for a x4 slot and N4227A for a x1 slot. The Tektronix slot interposer solution that works with their TLA700 logic analyzer is the TMS817.

11.2.3 PCI Express Analyzer/Exercisers

Agilent E2960A, Catalyst Enterprises SPX-8E and LeCroy PETRacer/PETrainer provide the ability to capture and exercise the PCI Express bus.

11.2.4 Mid-bus Probing

The mid-bus probe provides probing between two devices without PCI Express connector. Catalyst Enterprises, Agilent and Tektronix support mid-bus PCI Express probing. Agilent makes a protocol analyzer/exerciser, E2960A, which uses the Soft touch mid-bus probe e2941A. The Agilent solution that works with the 16700 analyzer is the N4221A. The Tektronix solution is the TMSIC6. The PCB must be designed with the PCI Express mid-bus footprint to allow probing between two devices. Refer to the following paper for more information on PCI Express mid-bus probing and the layout of the mid-bus probe.

http://www.tek.com/Measurement/logic_analyzers/contact/_notes/probe_design_guide_pci.pdf.

11.3 SAS Debugging

Debugging the SAS bus is aided with SAS protocol analyzer. There are several companies that have SAS test tools including: Catalyst Enterprises, Finisar (formerly Data Transit) and LeCroy (formerly CATC). Most of these protocol analysis tools provide multi-level triggering, filtering, state configuration and post-capture filtering of SAS packets. The Catalyst Enterprises solution STX-430 provides both protocol analysis and exerciser capability for SAS/SATA links running at 3.0Gbps. LeCroy also provides both analysis and exerciser capability with their *SASTracer/Trainer* for links up to 3.0Gbps.

11.4 SATA Debugging

Debugging the SATA bus is aided with a SATA protocol analyzer. There are several companies that make SATA test tools including: Catalyst Enterprises, Finisar (formerly Data Transit) and LeCroy (formerly CATC). Refer to the www.serialata.org website for more test manufacturer information. Most of these protocol analysis tools provide multi-level triggering, filtering, state configuration and post-capture filtering of Serial ATA packets. The Catalyst Enterprises solution STX-430 provides both protocol analysis and exerciser capability for SAS/SATA links running at 3.0Gbps. LeCroy also provides both analysis and exerciser capability with their *SASTracer/Trainer* for links up to 3.0Gbps.

12.0 Terminations

This chapter provides the recommended pull-up and pull-down terminations for a Intel® 81348 I/O Processor layout. Table 53 lists these Intel® 81348 I/O Processor termination values. Additional information is made available in future revisions.

12.1 Important Design and Debug Requirements

The following details are required for all Intel® 81348 I/O Processor designs. Note that these table is not an inclusive list. It is recommended that design guide is referenced for additional details.

Note: Without implementing the debug requirements Intel is extremely limited in its ability to assist with debug issues involving the transport firmware and device driver.

Table 52. Design and Debug Checklist

Recommendations	Comments	Compliance	
		Yes	No
Debug Requirements			
• The connection from serial console port0 connector to the UART0 port must be implemented to assist in debug of Intel transport firmware.	UART 0 is dedicated as the debug port for the transport FW. This port is also implemented on Intel development boards. UART 1 is a general purpose port. Without the UART0 port the debug of the transport firmware is extremely limited. ***Note:*** This port is depopulated on production boards.		
• The connection from the serial console port1 connector to the UART1 port is implemented when the application core needs a UART.	UART 1 is a general purpose port but it is useful for debugging the firmware on the application core1.		
• The JTAG port must be implemented on the board to assist in debug of third party device drivers.	A JTAG port provides the ability to connect a 3rd party debugger to Intel® 81348 I/O Processor. Using a debugger is the only way to pinpoint potential device driver and transport firmware issues. ***Notes:*** 1. JTAG port is required even when the customer has no plans to utilize this connector in their debug process. Without the JTAG port, the debug of the device driver is extremely limited. 2. A low profile 10 pin JTAG port is now recommended to save on board space. Refer to the JTAG chapter of the design guide for implementation recommendations. This port is depopulated on production boards.		
Design Notes			
• The SAS PLL filtering must be connected to ground. All the other PLL filters are not connected ground.	Refer to Section 12.5.1 of this document		
• Maximum SAS trace lengths (TX and RX) from controller ball to first connector	≤ 5"		
• 1.2V must be up before the 1.8V. The 1.2V must be down after the 1.8V.	Refer to the power delivery chapter of the design guide for additional details.		
• JTAG TRST_N must be asserted at power-on	A reset supervisor to pulse TRST_N low on power-on and pull high after power-on. Refer to the JTAG section of the design guide.		
• In PCI-X central resource mode: (using the P_CLK[3:0] outputs): REFCLKP, REFCLKN must have a 100 MHz differential clock input and **CLK_SRC_PCIE#**=0 strapping resistor pulled low.	The 100MHz clock input is needed to generate PCI clock outputs.		

12.2 Termination Checklist

Table 53 lists these Intel® 81348 I/O Processor termination values. Additional information is made available in future revisions.

Table 53. Terminations: Pull-up/Pull-down (Sheet 1 of 8)

Signal	Recommendations	Comments
S_TXP[7:0], S_TXN[7:0]	• connect each of **S_TXP[7:0]**, **S_TXN[7:0]** lines with a 10 nF series capacitor with low ESR • Unused ports are left unconnected	**Storage Transmit: carries** the differential output serial data and embedded clock for the **SAS/SATA** interface.
S_RXP[7:0], S_RXN[7:0]	• connect each of **S_RXP[7:0]**, **S_RXN[7:0]** lines with a10 nF series capacitor with low ESR • Unused ports are left unconnected	**Storage Receive: carries** the differential input serial data and embedded clock for the **SAS/SATA** interface.
S_CLKN0, S_CLKP0	• connect to differential 125 MHz ±100 ppm or a 150 MHz ±100 ppm oscillator. • use a 0.1uF AC coupling series capacitor on S_CLKN0 and S_CLKP0.	Differential storage clock
RBIAS[1:0]	6.49KΩ 1% to GND. Refer to Figure 65	
RBIAS_SENSE[1:0]	Connect to the same GND point of the **RBIAS[1:0]** resistors. Refer to Figure 65.	
S_ACT0/SCLOCK0, S_STAT0/SLOAD0	• NC when not used • SGPIO[0] is disabled: connect to LED with series resistor to VCC to indicate activity and status for storage engine[0]	These signals are open drain.
S_ACT1, S_STAT1	• NC when not used. • SGPIO[0] is disabled: these signals are connected to an LED with series resistor to VCC to indicate activity and status for storage engine[1]	These signals are open drain.
S_ACT2/SDATAIN0, S_STAT2/SDATAOUT 0	• NC when not used. • SGPIO[0] is disabled: these signals are connected to an LED with series resistor to to VCC in order to indicate activity or status for storage engine[2]	These signals are open drain.
S_ACT3, S_STAT3	• NC when not used. • SGPIO[0] is disabled: these signals are connected to an LED with series resistor to VCC in order to indicate activity and status for storage engine[3]	These signals are open drain.
S_ACT4/SCLOCK1, S_STAT4/SLOAD1	• NC when not used • SGPIO[1] is disabled: these signals are connected to an LED with series resistor to VCC in order to indicate activity/status for storage engine[4]	TThese signals are open drain.
S_ACT5, S_STAT5	• NC when not used • SGPIO[1] is disabled: these signals are connected to an LED with series resistor to VCC in order to indicate activity/status for storage engine[5]	TThese signals are open drain.
S_ACT6/SDATAIN1, S_STAT6/SDATAOUT 1	• NC when not used. • SGPIO[1] is disabled: these signals are connected to an LED with series resistor to VCC in order to indicate activity/status for storage engine[6]	These signals are open drain.
S_ACT7, S_STAT7	• NC when not used • SGPIO[1] is disabled: these signals are connected to an LED with series resistor to VCC in order to indicate activity/status for storage engine[7]	TThese signals are open drain.

Table 53. Terminations: Pull-up/Pull-down (Sheet 2 of 8)

Signal	Recommendations	Comments
REFCLKP, REFCLKN	• For PCI Express interface: connect to a 100MHz oscillator. • When using PCI-X (**CLK_SRC_PCIE#** = 0) and using the P_CLK[3:0] outputs: connect to these pins to a 100 MHz oscillator. • For PCI-X end point: connect the REFCLKP to a resistor divider such that the REFCLKP node is connected to both a 17.4K to VCC3P3 and a 4.7K connected to GND. REFCLKN must be connected to GND.	100 MHz oscillator is required for the PCI Express differential clock and to generate the P_CLKs.
PETP[7:0], PETN[7:0]	• Series capacitors with value of 75nF to 200nF (low ESR) on each of the lines. • NC when not used	
PERP[7:0], PERN[7:0]	• No series capacitor needed • NC when not used	
P_AD[63:32], P_CBE[7:4]#, P_PAR64	• When only PCI Express interface active these signals are internally pulled-up and are left as a NCs. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • When the PCIX_32BIT# is enabled (32 bit bus width), these signals are internally pulled-up and are left as a NCs.	
P_AD[31:0], P_CBE[3:0]#	When only PCI Express interface active these signals are internally pulled-up and are left as a NCs.	
P_GNT[0]# / P_REQ#	• PCI Express: **P_GNT[0]#** / **P_REQ#** has an internal pull-up and are left as a NC. • In Central Resource mode (internal arbiter) with PCIX_EP# = 1: **P_GNT[0]#** is output grant signal 0. • PCI Endpoint mode (external arbiter) PCIX_EP# = 0: This is the output request signal for the ATU and needs to connect to the external arbiter P_REQ# lines.	
P_REQ[0]# / P_GNT#	• PCI Express: **P_REQ[0]#** / **P_GNT#** has an internal pull-up and are left as a NC. • In Central Resource mode (internal arbiter) with PCIX_EP# = 1: **P_REQ[0]#** is input request signal to the ATU. • PCI Endpoint mode (external arbiter) PCIX_EP# = 0: **P_GNT#** is input grant signal for the ATU. This pin is pulled up to V_{CC3P3} with an 8.2K resistor.	
P_GNT[3:1]#	• When PCI Express interface only: **P_GNT[3:1]#** is left as a NC. • In Central Resource mode (internal arbiter) with PCIX_EP# = 1: These are three output grant signals. Unused signals are left as NCs. • In endpoint mode (external arbiter) with PCIX_EP# = 0: These signals are not used and are left as NCs	

Table 53. Terminations: Pull-up/Pull-down (Sheet 3 of 8)

Signal	Recommendations	Comments
P_REQ[3:1]#	• When PCI Express interface only: **P_REQ[3:1]#** is left as a NC. • In Central Resource mode (internal arbiter) with PCIX_EP# = 1: These are three input request signals to the internal arbiter. Unused signals are left as NCs. • In endpoint mode (external arbiter) with PCIX_EP# = 0: These signals are not used and are left as NCs	
P_REQ64#	• When only PCI Express interface is active these signals are internally pulled-up and are left as a NC. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • When the device is PCI endpoint then the width of the bus is indicated by the state of REQ64# at the rising edge of RST#.	
P_ACK64#, P_PAR P_SERR#, P_PERR#, P_INT[D:A]#	• When only PCI Express interface is active these signals are internally pulled-up and are left as a NC. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up.	
P_FRAME#, P_IRDY#, P_TRDY#, P_STOP#, P_DEVSEL#	• When only PCI Express interface is active these signals are internally pulled-up and are left as a NC. • When the **PCIX_PULLUP#** is enabled (pulled to 0), these signals are internally pulled-up. • When the device is PCI endpoint **PCIX_EP#** = 0 state of these signals are used for PCI-X initialization pattern at the rising edge of RST#.	Refer to the *PCI-X Specification 1.0b* for more information on the PCI-X Initialization pattern.
P_M66EN	PCI Express**: P_M66EN** has an internal pull-up and is left as a NC. **PCI-X Central Resource mode (PCIX_EP# = 1):** • **CLK_SRC_PCIE#** = 0 (**using the P_CLK[3:0] clock outputs):** Pull-up signal with 8.2 KΩ**.** • **CLK_SRC_PCIE#** = 1: **(P_CLKIN primary clock source):** Refer to PCI-X Frequency Selection Section of the *design guide*. **PCI Endpoint mode (PCIX_EP# = 0):** Refer to PCI-X Frequency Selection Section of the *design guide*.	
P_IDSEL	• PCI Express: P_IDSEL has an internal pull-up and is left as a NC. • Central Resource mode **PCIX_EP#** = 1: pull down with 1K resistor. • PCI Endpoint mode **PCIX_EP#** = 0: connect to AD lines; refer to Section 6.1.2	

Table 53. Terminations: Pull-up/Pull-down (Sheet 4 of 8)

Signal	Recommendations	Comments
P_CLKIN	For PCI Express only this signal is connected to GND. **PCI Central Resource mode (PCIX_EP# = 1):** • **CLK_SRC_PCIE#** = 0: Connect to P_CLKOUT through a 26 ohm +/- 1% resistor. Refer to the PCI-X chapter for length match details. • **CLK_SRC_PCIE#** = 1 **(P_CLKIN** is the primary clock source): connect to the system PCI clock **PCI Endpoint mode (PCIX_EP# = 0)**: connect to the system PCI clock.	• REFCLKP, REFCLKN must have 100 MHz clock to generate the P_CLKO[3:0] outputs. • When the **P_CLKIN** is the primary clock source (**CLK_SRC_PCIE#** = 1), the PCI Clock outputs are unavailable and is not used as a clock source for any device.
P_CLKOUT	For PCI Express only these signals are unconnected. **PCI Central Resource mode (PCIX_EP# = 1):** • **CLK_SRC_PCIE#** = 0 (**using the P_CLKO[3:0] outputs):** Connect to the **P_CLKIN** through a 26 ohm +/- 1% resistor (see PCI-X chapter of the design guide for length match details) • **CLK_SRC_PCIE#** = 1: this signal is left unconnected. PCI Endpoint mode **(PCIX_EP# =0)**: this signal is left unconnected.	REFCLKP, REFCLKN must have 100 MHz clock to generate the P_CLKO[3:0] outputs.
P_CLKO[3:0]	• Connect to PCI device **P_CLK** inputs through a 28 ohm +/- 1% series resistor for each slot and a 26 ohm +/- 1% for each embedded device. Refer to the PCI-X chapter of the design guide for length match details. • Any unused **P_CLKO**s are left unconnected.	REFCLKP, REFCLKN must be have 100 MHz clock to generate the P_CLKO[3:0] outputs.
P_PCIXCAP	When PCI Express only: • GND this pin. When PCI Central Resource mode is enabled **PCIX_EP#** = 1: • CLK_SRC_PCIE# = 0 using P_CLK[3:0] outputs: connect signal with 3.3 KW pull-up to 3.3 V. • CLK_SRC_PCIE# = 1 (P_CLKIN primary clock source): refer to Frequency Selection section in the PCI-X Chapter of the design guide. When PCI Endpoint mode: **PCIX_EP#** = 0: • Pull-up signal with 8.2K resistor. • Refer to Frequency Selection section in the PCI-X Chapter of the design guide for termination for the PCIXCAP pin on the edge connector.	Refer to Section 6.1 ***Note:*** This signal has been defeatured. Refer to non-core Erratum 69 in the *Intel® 81348 Specification Update* for more information.
P_BMI	• When PCI Express only: this signal is left as a no connect. • For PCI-X : no connect when not used.	
P_CAL[0], **P_CAL[2]**	• When PCI-X interface is used: This pin is connected to a separate 22.1 Ω 1% resistor to GND. See Section 12.6 for more information. • When PCI-X interface is not used: These pins are left as NCs	**PCI** Calibration: is connected to an external calibration resistor to dynamically adjust their slew rate and drive strength to compensate for voltage and temperature variations.

Table 53. Terminations: Pull-up/Pull-down (Sheet 5 of 8)

Signal	Recommendations	Comments
P_CAL[1]	• When PCI-X is used: This pin is connected to a separate 121Ω 1% resistor to GND. See Section 12.6 for more information. • When PCI-X interface is not used: These pins are left as NCs	**PCI** Calibration: is connected to an external calibration resistor such that the output drivers reference the resistor to dynamically adjust the ODT resistance to compensate for voltage and temperature variations.
PE_CALP **PE_CALN**	Connect PE_CALP ball through 1.4K 1% resistor to the PE_CALN ball. Refer to Figure 63. Note: this is required even when the PCI-Express interface is not used.	
M_CAL[0]	Connect to 24.9 ohm 1% resistor ground. Refer to Figure 64	
M_CAL[1]	Connect to 301 ohm 1% resistor to ground. Refer to Figure 64.	
ODT[1:0]	• NC when not used • When On-Die DDR2 termination used connect to the ODT inputs on the DDR2 SRAM.	Follow the same layout guidelines for CS# signals.
M_CK[2:0], M_CK[2:0]#	Unused M_CK/M_CK#s are left unconnected When used with Registered DIMMs: • connect **M_CK[0]/M_CK[0]#** pair, **M_CK[1]/M_CK[1]#**, **M_CK[2]/M_CK[2]#** are left unconnected When used with unbuffered DIMMs: • Connect M_CK[2:0]/M_CK[2:0]# to the DDR2 CK/CK# inputs.	These DDR2 clock signals are used to provide the three differential clock pairs. Refer to Section 4.2.2.2 for more details.
M_RST#	NC when not used	This Reset signal asynchronously forces all registered outputs LOW on the registered DDR2 DIMM
MA[13:0]	• Unused address lines are left unconnected. • When used refer to Section 4.2.2.3 for DDR2 termination recommendations.	DDR2 address signals
RAS#, CAS#, WE#, CS[1:0]#, CKE[1:0]	• Unused lines are left unconnected. • When used refer to Section 4.2.2.3 for DDR2 termination recommendations.	DDR2 control signals
DQ[63:0], DM[8:0], CB[7:0], DQS[8:0], DQS[8:0]#	• Unused pins are left unconnected. • When used refer to Section 4.2.2.1 for DDR2 termination recommendations.	Source Synchronous signals
M_VREF	Connect to the memory VREF voltage 0.9V refer to Section 4.4.1 for DDR2 termination recommendations.	
A[24:0], POE#, PB_RSTOUT#	• Unused pins are left unconnected. • When used refer to Section 8.3 for PBI bus connection recommendations.	
D[15:0], PCE[1:0]#, PWE#	• PCE[1:0]# are used for reset straps refer to the Reset Strap Table 54. • Also refer to Section 8.3 for PBI bus connection recommendations.	
HS_ENUM#	Leave unconnected when hot swap not used.	
HS_LSTAT	When Compact PCI Hot Swap is not supported, this signal must be tied to GND.	Hot Swap Latch Status: An input indicating the state of the ejector switch. 0 = Indicates the ejector switch is closed. 1 = Indicates the ejector switch is open. 1 = 8.2K pull-up to VCC 0 = connect to GND.

Table 53. Terminations: Pull-up/Pull-down (Sheet 6 of 8)

Signal	Recommendations	Comments
HS_LED_OUT	• Connect to Hot Swap blue LED. • When Compact PCI Hot Swap is not supported this signal is left unconnected.	
HS_FREQ[1:0] / CR_FREQ[1:0]	See comments	Hot Swap Frequency: While in Hot Swap mode, (these are only valid when **PCIX_EP#** = 0 and **HS_SM#** = 0). 00 = 133MHz PCI-X 01 = 100MHz PCI-X 10 = 66MHz PCI-X 11 = 33 or 66MHz. PCI (frequency depends on **P_M66EN**) Central Resource Frequency: While in Central Resource mode,.(these are only valid when **PCIX_EP#** = 1). 00 = 133 MHz 01 = 100 MHz 10 = 66MHz 11 = 33 MHz ***Note:*** 1 = internal pull-up 0 = connect to GND
P_INT[D:A]# / XINT[3:0]# / GPIO[11:8]	• when PCIX_EP#=0: act as outputs no termination is required • when PCIX_EP#=1: 8.2 K pull-ups required • When used as GPIOs these signals need 8.2 K pull-up	**When PCIX_EP# = 0:** • **PCI Interrupt requests an interrupt from the central resource.** **When PCIX_EP# = 1:** • External **Interrupt** requests are used by external devices to request interrupt service. • **General Purpose I/O** pins general-purpose inputs or outputs. The default mode is a general-purpose input.
HPI#, NMI0#, NMI1#, XINT[7:4]#	8.2 K pull-ups	
GPIO[7:0] / XINT[15:8]# / CHAPOUT	8.2 K pull-ups	• General Purpose I/O (default mode). • **External Interrupt**: These pins are level-detects and are internally synchronized. • CHAPOUT: **GPIO[7]** When enabled it overrides the normal **GPIO[7]** function.
SCL0, SDA0, SCL1, SDA1, SCL2, SDA2	• When used external pull-up to VCC is required. Refer to the I^2C specification for information on calculating the pull-up. ***Note:*** I^2C port is only used for SEP enclosure management. • 2K pull-up when unused.	The pull-up value is dependent on the bus loading. Refer to the I^2C specification at: http://www.semiconductors.philips.com/acrobat_download/literature/9398/39340011.pdf
SMBCLK	For PCI Express adapter cards: • When the SMBus is used, there is isolation device such as the LTC4301 between this signal and PE_SMCK on the PCI Express connector. For PCI Express motherboard applications: • When SMBus is used a pull-up is required (value is dependent on the loading). • When SMBus is unused, a 8.2K pull-up is required.	LTC4301 is a hotswappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website http://www.linear.com/pc/downloadDocument.do?navId=H0,C1,C1007,C1070,P2460,D3045 Refer also to the http://www.smbus.org/ for the latest specification.

Table 53. Terminations: Pull-up/Pull-down (Sheet 7 of 8)

Signal	Recommendations	Comments
SMBDAT	For PCI Express adapter cards: • When the SMBus is used, there is isolation device such as the LTC4301 between this signal and PE_SMDAT on the PCI Express connector. For PCI Express motherboard applications: • When SMBus is used a pull-up is required (value is dependent on the loading). • When SMBus is unused, a 8.2K pull-up is required.	LTC4301 is a hotswappable 2-wire bus buffer that allows card insertion without corruption of the data and clock buses. Refer to the Linear Technology website http://www.linear.com/pc/downloadDocument.do?navId=H0,C1,C1007,C1070,P2460,D3045 Refer also to the http://www.smbus.org/ for the latest specification.
U0_RXD, U1_RXD	• The serial console port connector to the UART0 port must be implemented to assist in debug of Intel transport firmware. • When unused connect to GND	***Note:*** UART 0 is dedicated as the debug port for the transport FW as implemented on Intel development boards. UART 1 is a general purpose port.
U0_TXD, U0_RTS#, U1_TXD, U1_RTS#	• The serial console port connector to the UART0 port must be implemented to assist in debug of Intel transport firmware. • Leave unconnected when unused.	***Note:*** UART 0 is dedicated as the debug port for the transport FW as implemented on Intel development boards. UART 1 is a general purpose port.
U0_CTS#, U1_CTS#	• The serial console port connector to the UART0 port must be implemented to assist in debug of Intel transport firmware. • When unused 8.2K pull-up	***Note:*** UART 0 is dedicated as the debug port for the transport FW as implemented on Intel development boards. UART 1 is a general purpose port.
TCK	• The JTAG port must be implemented on the board to assist in debug of third party device drivers. • 8.2 K pull-up when used. Refer to the JTAG chapter. • GND when unused.	Test Clock: provides clock input for IEEE 1149.1 Boundary Scan Testing (JTAG).
TDI	• The JTAG port must be implemented on the board to assist in debug. • 8.2 K pull-up when used. Refer to the JTAG chapter. • NC when unused has weak pull-up.	Test Data Input: is the JTAG serial input pin.
TDO	• The JTAG port must be implemented on the board to assist in debug. • When used refer to the JTAG chapter. • NC when unused	Test Data Output: is the serial output pin for the JTAG feature.
TRST#	• The JTAG port must be implemented on the board to assist in debug. • When used refer to the JTAG chapter. • GND when unused.	Test Reset: This pin has a weak internal pull-up.
TMS	• The JTAG port must be implemented on the board to assist in debug. • 8.2 K pull-up when used. Refer to the JTAG chapter. • NC when unused has weak pull-up.	Test Mode Select: This pin has a weak internal pull-up.

Table 53. Terminations: Pull-up/Pull-down (Sheet 8 of 8)

Signal	Recommendations	Comments
WARM_RST#	• When PCI-X interface is used: 1K pull-up. • When PCI-Express used: This pin is used when the sticky bit functionality is required. In this scenario, the WARM_RST# pin must be tied to the system reset PCI_RST# signal while the P_RST# pin is tied to the system power good signal.	**Warm Reset** is the same as a cold reset, except sticky configuration bits are ***not*** reset. Notes: - When the PCI Express interface is used as an endpoint, the PCI Express in-band Hot Reset Mechanism is also used to provide the sticky bit functionality. - On the customer reference board, WARM_RST# is tied to the SRST_N to provide a JTAG debugger reset. -Driving WARM_RST# using any other methods than suggested above results in unpredictable behavior of the device.
NC	No Connect: pins have no usable function and must not be connected to any signal, power or ground.	
THERMDA	• Connect to the anode of the thermal diode. • NC when unused	
THERMDC	• Connect to the cathode of the thermal diode. • NC when unused	
VCCVIO	• When using the PCI-Express interface only: connect to ground. • When using the PCI-X interface: Connect to 3.3 V.	
PUR1	This pin must be pulled up to VCC3P3 with an external 8.2 KΩ 5%, resistor for proper operation.	

12.3 Reset Straps

The following table provides a list of reset straps which are multiplexed on the Peripheral Address Bus A[24:0]. These pins are latched on the rising edge of **P_RST#**. All reset strap signals are internally pulled to logic 1 by default.

An external 4.7KΩ 5% pull-down resistor is required to force a logic 0 on these pins.

Table 54. Reset Straps (Sheet 1 of 3)

Signal	Recommendations	Comments
BOOT_WIDTH_8#	0 = 8 bits wide, 0 = 4.7K ohms resistor pull down 1 = 16 bits wide (Default mode internal pull-up)	Muxed onto signal **A[0]**.
CFG_CYCLE_EN#	0 = Configuration Cycles enabled, 0 = 4.7K ohms resistor pull down 1 = Configuration Retry enabled (Default mode internal pull-up)	Muxed onto signal **A[1]**
HOLD_X0_IN_RST#	0 = Hold Scale in reset, 0 = 4.7 K ohms resistor pull down 1 = Do not hold in reset (Default mode internal pull-up)	Muxed onto signal **A[2:0]**
HOLD_X1_IN_RST#	0 = Hold in reset, 0 = 4.7K ohms resistor pull down 1 = Do not hold in reset (Default mode internal pull-up).	Muxed onto signal **A[3]**
MEM_FREQ[1:0]	10 = 533MHz 11 = 400MHz (Default mode). 0 = 4.7K ohms resistor pull down 1 = internal pull-up.	**MEM_FREQ[1:0]** muxed onto signal **A[5]** and A[4] respectively 0 = 4.7K ohms resistor pull down 1 = internal pull-up.
EXT_ARB#	0 =) External arbiter, 0 = 4.7K ohms resistor pull down 1 =) Internal arbiter (Default mode internal pull-up)	Muxed onto signal **A[6]**
INTERFACE_SEL_PCIX#	0 = ATU-X is function 0 (4.7 KΩ pull-down resistor) and ATUE is function 5. 1 = ATU-E is function 0 and ATUX is function 5. Refer to comments.	**Interface Select PCI-X:** determines which ATU is function 0. 0 = 4.7 KΩ resistor pull down 1 = internal pull up. ***Note:*** Muxed onto signal **A[10]**
PCIX_EP#	Refer to comments.	PCI-X End Point: 0 = Endpoint, 4.7K ohms resistor pull down 1 = Central Resource (Default mode) internal pull up. ***Note:*** muxed onto signal **A[11]**
DF_SEL[2:0]	Intel® 81348 I/O Processor 8 port mode each **DF_SEL[2:0]** must be pulled low.	**Device Function Select: DF_SEL[2:0]** ***Note:*** **DF_SEL[2]** muxed onto signal **A[9]** ***Note:*** **DF_SEL[1]** muxed onto signal **A[8]** ***Note:*** **DF_SEL[0]** muxed onto signal **A[7]** 0 = 4.7K ohms resistor pull down.
PCIE_RC#	Refer to comments.	PCI-E Root Complex: 0 = Root Complex 1 = Endpoint (Default mode) 0 = 4.7 K ohms resistor pull down 1 = internal pull up. NOTE: muxed onto signal **A[12]**

Table 54. Reset Straps (Sheet 2 of 3)

Signal	Recommendations	Comments
SMB_A5, SMB_A3, SMB_A2, SMB_A1	Refer to comments.	SM Bus Address: maps to address bits 5,3,2, and 1 where bits 7- 0 represent the address the SMBus slave port responds to when access is attempted. 0 = address bit is low 1 = address bit is high (Default mode) ***Note:*** **SMB_A5** muxed onto signal **A[16]** ***Note:*** **SMB_A3** muxed onto signal **A[15]** ***Note:*** **SMB_A2** muxed onto signal **A[14]** ***Note:*** **SMB_A1** muxed onto signal **A[13]** 0 = 4.7K ohms resistor pull down 1 = internal pull up.
PCIX_PULLUP#	When pulled-low enables the following signal pull-ups: **P_AD[63:32]**, **P_C/BE[7:4]#**, **P_PAR64**, **P_REQ64#**, **P_ACK64#**, **P_FRAME#**, **P_IRDY#**, **P_TRDY#**, **P_STOP#**, **P_DEVSEL#**, **P_SERR#**, **P_PERR#**, **P_INT[D:A]#**	PCI-X Pull Up: 0 = enable PCI pull up resistors 1 = disable PCI pull up resistors (Default mode) ***Note:*** Muxed onto signal **A[17]** 0 = 4.7K ohms resistor pull down 1 = internal pull up.
PCIX_32BIT#	When 32 PCI-X bus enabled the following signals have internal pull-ups: **P_AD[63:32]**, **P_C/BE[7:4]#** and **P_PAR64** and left as NCs.	32-Bit PCI-X Bus: 0 = 32 bit wide PCI-X bus. 1 = 64 bit wide PCI-X bus. (Default mode) ***Note:*** Muxed onto signal **A[18]** 0 = 4.7K ohms resistor pull down 1 = internal pull up.
PCIXM1_100#	Refer to comments.	PCI-X Mode 1 100MHz Enable: 0 = limit PCI-X mode 1 to 100MHz 1 = 133MHz enabled (Default mode) ***Note:*** Muxed onto signal **A[19]** 0 = 4.7K ohms resistor pull down 1 = internal pull up.
HS_SM#	Refer to comments	Hot Swap Startup Mode: 0 = Hot Swap mode enabled 1 = Hot Swap mode disabled (Default mode) ***Note:*** Muxed onto signal **A[21]** 0 = 4.7K ohms resistor pull down 1 = internal pull up.
FW_TIMER_OFF#	Refer to comments.	Firmware Timer Off: 0 = firmware timer disabled 1 = firmware timer enabled (Default mode) ***Note:*** Muxed onto signal **A[22]** 0 = 4.7K ohms resistor pull down 1 = internal pull up.
CONTROLLER_ONLY#	Refer to comments.	Controller-Only Enable: 0 = Controller only, RAID disabled 1 = RAID enabled (default mode) **NOTE:** Muxed onto signal A[23]

Table 54. Reset Straps (Sheet 3 of 3)

Signal	Recommendations	Comments
CLK_SRC_PCIE#	Refer to comments.	Clock Source PCI-E: selects the PCI Express Refclk pair as the input clock to the PLLs that control most internal logic. 0 = source clock is **REFCLKP**/**REFCLKN** 1 = source clock comes from the active PCI interface (Default mode) ***Note:*** Muxed onto signal **PWE#** 0 = 4.7K ohms resistor pull down 1 = internal pull up.
LK_DN_RST_BYPASS#	Use for PCI Express mode	Link Down Reset Bypass: Disables the full chip reset that is normally caused by a Link Down or hot reset. 0 = Do not reset on Link Down 1 = Reset on Link Down (default mode) Muxed onto signal **A[24]**
PCE[1:0]#	Pull up both these signals with 8.2K resistor	

12.4 Configuration Details

The following table provides the reset strap configuration for valid operational modes of the chip: PCI Express root complex or endpoint , PCI-X endpoint or central resource or dual interface configuration modes. Note that the dual interface chip is a different sku (not strapping option) and has a unique part number.

Note: The **PCIXCAP** feature has been defeatured. Refer to Non-Core Erratum #69 in the *Intel® 81348 I/O Processor Specification Update* for more information. THis erratum overrides **PCIXCAP** references throughout this document.

Table 55. PCI Express/PCI-X Strap Configuration Table

Application	Dual Interface (PCI-X and PCI Express)	Endpoint Configuration	Strapping Settings		
			INTERFACE_SEL_PCIX#	PCIE_RC# (PCI Express root Complex strap)	PCIX_EP# (PCIX endpoint strap)
HBA or Motherboard	Yes	PCI Express endpoint with PCI-X Central Resource (default)	1	1 (PCIE Endpoint)	1 (Central Resource)
HBA or Motherboard	Yes	PCI-X endpoint with PCI Express Root Complex	0	0 (PCI Root Complex)	0 (PCIX Endpoint
HBA or Motherboard	No	PCI Express endpoint	1	1	X
HBA or Motherboard	No	PCI-X endpoint	0	X	0
Motherboard	Yes	PCI Express Root Complex and PCI-X Central Resource	0 (ATU-X is function 0, ATU-E is function 5) 1 (ATU-E is function 0, ATU-X is function 5)	0	1
Motherboard	No	PCI-X Central Resource	0	X	1
Motherboard	No	PCI Express Root Complex	1	0	X

12.4.1 PCI-E Mode Only

PCI-E active refer to the Table 54 for **INTERFACE_SEL_PCIX#**, **PCIE_RC#** and **PCIX_EP#** straps for the following modes:

1. PCI-E root complex Section 12.4.3.1
2. PCI-E end point Section 12.4.3.2

12.4.1.1 PCI-E Root Complex

- REFCLKP, **REFCLKN** differential pins must be connected to 100MHz oscillator.
- **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75nF to 200nF and then to corresponding RX lane pins on device or connector. Unused lanes are NCs.
- **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector.
- PE_CALP, PE_CALN - Connect PE_CALP ball through 1.4K 1% resistor to the PE_CALN ball.
- **INTERFACE_SEL_PCIX#** = 1 - Reset Strap NC (default)
- **PCIE_RC#** = 0, Reset Strap 4.7K pull-down
- CLK_SRC_PCIE# = 0
- P_CLKIN: GND
- P_PCIXCAP: GND
- P_INT[D:A]/XINT[3:0]: 8.2K pull-up
- VCCVIO: ground
- VCC1P2PLLP and VSSPLLP filter pins are grounded.
- All other PCI-X pins are NCs

12.4.1.2 PCI-E endpoint

- REFCLKP, **REFCLKN** differential pins must be connected to 100MHz oscillator.
- **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75nF to 200nF and then to corresponding RX lane pins on device or connector. Unused lanes are NCs.
- **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector. Unused lanes are NCs.
- PE_CALP, PE_CALN - Connect PE_CALP ball through 1.4K 1% resistor to the PE_CALN ball.
- **INTERFACE_SEL_PCIX#** = 1 - Reset Strap NC (default)
- **PCIE_RC#** = 0, Reset Strap 4.7K pull-down
- CLK_SRC_PCIE# = 0
- P_CLKIN: GND
- P_PCIXCAP: GND
- P_INT[D:A]/XINT[3:0]: 8.2K pull-up
- VCCVIO: ground
- VCC1P2PLLP and VSSPLLP filter pins are grounded.
- All other PCI-X pins are NCs.

12.4.2 PCI-X Mode Only

When the PCI-X interface is used and PCI Express is not used the following provisions must be made:

- REFCLKP/REFCLKN must have the 100 MHz differential signal on it to generate the P_CLKOs.
- PE_CALP, PE_CALN - Connect PE_CALP ball through 1.4K 1% resistor to the PE_CALN ball.
- **INTERFACE_SEL_PCIX#** = 0 - Reset Strap NC (default)
- **PCIE_RC#** = 1, Reset Strap 4.7K pull-down
- CLK_SRC_PCIE# strap: Make sure strapping reflects whether clock source is the REFCLKP/REFCLKN CLK_SRC_PCIE# = 0 or PCI clock in CLK_SRC_PCIE# = 1 (default).
- All other PCI Express pins are no connects. Make sure configuration strapping options are set correctly for operation mode refer to Table 53 for additional details.

12.4.2.1 Central Resource Mode: (PCIX_EP# = 1)

1. P_PCIXCAP:
   — CLK_SRC_PCIE# = 0, (using P_CLK[3:0] outputs): P_PCIXCAP connect signal with 3.3 K ohms pull-up to 3.3 V.
   — CLK_SRC_PCIE# = 0, (using P_CLK[3:0] outputs but limiting the PCI clock frequency): refer to Table 29. Note that strapping **PCIXM1_100#** is pulled low to limit frequency to 100MHz.
   — CLK_SRC_PCIE# = 1, (P_CLKIN primary clock source): refer to Section 6.1.1.
2. P_M66EN:
   — CLK_SRC_PCIE# = 0, (using P_CLK[3:0] outputs): pull-up the signal 8.2K ohms pull-up to 3.3 V.
   — CLK_SRC_PCIE# = 0, (using P_CLK[3:0] outputs but limiting the PCI clock frequency): refer to Table 29. Note that strapping **PCIXM1_100#** is pulled low to limit frequency to 100MHz.
   — CLK_SRC_PCIE# = 1, (P_CLKIN primary clock source): Refer to the Section 6.1.1.
3. P_IDSEL: pull-down the signal 1K ohm resistor.
4. P_REQ[0]#/P_GNT#: This is an input request signal and has a 8.2K pull-up resistor.
5. P_GNT[0]#/P_REQ#: (internal arbiter): This is an output grant signal.
6. P_GNT[3:1]#: (internal arbiter) - These are output grant signals and unused signals are NCs.
7. P_REQ[3:1]#: (internal arbiter) - These are input request signals and unused signals are NCs.
8. P_CLKIN:
   — CLK_SRC_PCIE# = 0, Connect to P_CLKOUT through a 26 ohm +/- 1% resistor.
   — CLK_SRC_PCIE# = 1, (P_CLKIN primary clock source) connect to system clock.
9. P_CLKOUT:
   — CLK_SRC_PCIE# = 0, Connect to P_CLKIN through a 26 ohm +/- 1% resistor.
   — CLK_SRC_PCIE# = 1, (P_CLKIN primary clock source) signal is left unconnected.

12.4.2.2 PCI-X Endpoint Mode (PCIX_EP# = 0)

1. P_PCIXCAP:
   — Pull-up signal with 8.2K resistor and refer to Frequency Selection Section 6.1.1 *for termination for the PCIXCAP pin on the edge connector*.
   — CLK_SRC_PCIE# = 1, P_CLKIN primary clock source: refer to Frequency Selection Section 6.1.1.
2. P_M66EN: connect to the M66EN on the board and refer to Frequency Selection Section 6.1.1.
3. P_IDSEL: connect to one of the AD lines
4. P_REQ[0]#/P_GNT#: This is an input grant signal and has a 8.2K pull-up resistor.
5. P_GNT[0]#/P_REQ#: (external arbiter): This is an output request signal and connects to the external arbiter P_REQ# line.
6. P_GNT[3:1]#: (external arbiter): These signals are unused signals are NCs.
7. P_REQ[3:1]#: (external arbiter): These signals are unused signals are NCs.
8. P_CLKIN: Connect to system PCI clock.
9. P_CLKOUT: this signal is left unconnected.
10. REFCLKP connect to a resistor divider such that the REFCLKP node is connected to both a 17.4K to VCC3P3 and a 4.7K connected to GND. REFCLKN must be connected to GND.

12.4.3 Dual Interface Mode

For dual interface mode with PCI-E and PCI-X interfaces active refer to the Table 54 for **INTERFACE_SEL_PCIX#**, **PCIE_RC#** and **PCIX_EP#** straps for the following modes:

1. PCI-E root complex with PCI-X endpoint mode Section 12.4.3.1
2. PCI-X central resource with PCI-E endpoint mode Section 12.4.3.2
3. PCI-E root complex with PCI-X central resource mode Section 12.4.3.3

12.4.3.1 PCI-E Root Complex with PCI-X Endpoint Mode

- PCI-E Root complex:
  - REFCLKP, **REFCLKN** differential pins must be connected to 100MHz oscillator.
  - **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75nF to 200nF and then to corresponding RX lane pins on device or connector. Unused lanes are NCs.
  - **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector.
  - PE_CALP, PE_CALN - Connect PE_CALP ball through 1.4K 1% resistor to the PE_CALN ball.
- PCI-X endpoint mode follow recommendations in Section 12.4.2.2

12.4.3.2 PCI-E endpoint with PCI-X Central Resource

- PCI-E Endpoint
  - REFCLKP, **REFCLKN** differential pins must be connected to 100MHz oscillator.
  - **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75nF to 200nF and then to corresponding RX lane pins on device or connector. Unused lanes are NCs.
  - **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector. Unused lanes are NCs.
  - PE_CALP, PE_CALN - Connect PE_CALP ball through 1.4K 1% resistor to the PE_CALN ball.
- PCI-X central resource mode follow recommendations in Section 12.4.2.1

12.4.3.3 PCI-E Root Complex with PCI-X Central Resource

- PCI-E Root complex:
  - REFCLKP, **REFCLKN** differential pins must be connected to 100MHz oscillator.
  - **PETP[7:0]**, **PETN[7:0]** differential transmit pair pins lanes 0 through 7 connect to series capacitors with value of 75nF to 200nF and then to corresponding RX lane pins on device or connector. Unused lanes are NCs.
  - **PERP[7:0]**, **PERN[7:0]** differential receiver pairs lanes 0 through 7 these connect to the corresponding TX lane pins on device or connector. Unused lanes are NCs.
  - PE_CALP, PE_CALN - connect PE_CALP ball through 1.4K 1% resistor to the PE_CALN ball.
- PCI-X central resource mode follow recommendations in Section 12.4.2.1

12.5 Analog Filters

This section describes filters needed for the PLL circuitry. Figure 56 lists the PLLs that are required for this part.

Table 56. Required PLLs

Interface	FilteredVoltage	VCC PLL Balls	VSS PLL Balls	Layout Guideline Table
Storage	1.2V	VCC1P2PLLS0	VSSPLLS0	Table 57
		VCC1P2PLLS1	VSSPLLS1	
PCI-X	1.2V	VCC1P2PLLP	VSSPLLP	Table 58
Core Digital Logic	1.2V	VCC1P2PLLD	VSSPLLD	Table 58
Intel XScale® microarchitecture and internal bus logic	3.3V	VCC3P3LLX	VSSPLLX	Table 59

12.5.1 $V_{CC1P2PLLS0}$, $V_{CC1P2PLLS1}$ Filter Requirements

The lowpass filter, as shown in Figure 59 reduces noise induced clock jitter and its effects on timing relationships in system designs. The Figure 59 filter circuit is recommended for the two PLL pairs: VCC1P2PLLS0 - VSSPLLS0 and VCC1P2PLLS1 - VSSPLLS1 pairs.

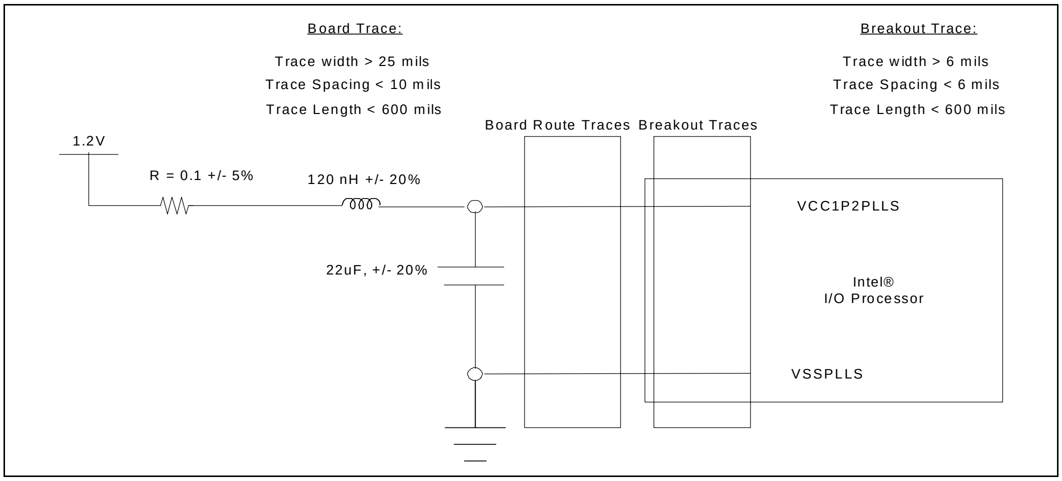
The filter has the following characteristics:

- the purpose of this filter is to achieve at least 10 dB rejection of frequencies between 1 and 20 MHz
- the filter components are selected to achieve a corner frequency of 100KHz
- the minimum voltage into the filter must be $\geq$ 1.14V
- the current draw for these pins is less than 85mA

Table 57. $V_{CC1P2PLLS0}$, $V_{CC1P2PLLS1}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground • VCC1P2PLLS0, VSSPLLS0 and VCC1P2PLLS1, VSSPLLS1 traces must be ground referenced (no V_{CC} references)
Inductor	• 120 nH +/- 20% • L must be magnetically shielded • ESR: max < 0.3 Ω • rated at 45 mA
Capacitor	• 22 µF +/- 20% (Capacitor) • ESR: max < 0.3 Ω • ESL < 2.5 nH • Place 22 µF capacitor as close as possible to package pin.
Resistor	• 0.1 +/- 5% (resistor) • resistor must be placed between V_{CC1P2} and L. • Note: when trace resistance is large enough a discrete resistor is not required
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils
Trace Spacing	• $\geq$ 30 mils from any other signals.
Trace Length maximum	1.2”
Routing Guideline 1	Route VCC1P2PLLS and VSSPLL as differential traces.
Routing Guideline 2	The nodes connecting VCC1P2PLLS and the capacitor must be as short as possible.
Routing Guideline 3	The 1.2 V supply regulator used for the PLL filter must have less than +/- 3% tolerance

Figure 59. VCC1P2PLLS0, VCC1P2PLLS1 Configuration



12.5.2 $V_{CC1P2PLLP}$, $V_{CC1P2PLLD}$ Filter Requirements

The lowpass filter, as shown in Figure 59 reduces noise induced clock jitter and its effects on timing relationships in system designs. The Table 58 filter circuit is recommended for each of the PLL pairs: VCC1P2PLLP-VSSPLLP and VCC1P2PLLD - VSSPLLD.

The filter has the following characteristics:

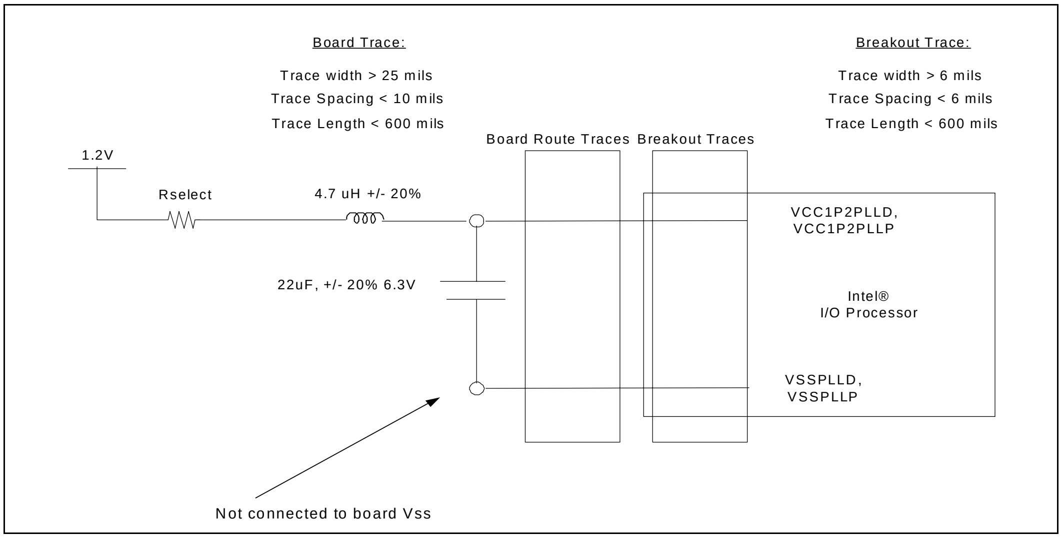
- The filter components must be able to handle a DC current of 30mA.
- < 0.2dB gain in pass band and < 0.5dB attenuation in pass band < 1Hz. The passband is DC through 1Hz.
- > 34dB attenuation from 1MHz to 66MHz
- > 28dB attenuation from 66MHz to core frequency

Note: When the PCI-X interface is not used the VCC1P2PLLP and VSSPLLP pins are grounded.

Table 58. $V_{CC1P2PLLP}$, $V_{CC1P2PLLD}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground • VCC1P2PLLP, VCC1P2PLLD traces must be ground referenced (no V_{CC} references)
Inductor	• 4.7 uH +/- 25% • L must be magnetically shielded • ESR: max < 0.3 Ω • rated at 45 mA
Capacitor	• 22 µF +/- 20% 6.3V (Capacitor) • ESR: max < 0.3 Ω • ESL < 2.5 nH • Place 22 µF capacitor as close as possible to package pin.
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 1.2V plane to the top end of the capacitor is > 0.35 Ω (ινχλυδινγ βοαρδ ανδ χομπονεντ resistance) • 1.2V plane to $V_{CC1P2PLL}$ < 1.5 Ω • 1/16 W 6.3 V • resistor must be placed between V_{CC1P2} and L. • Note: when trace and component resistance is large enough the discrete resistor is not required
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	1.2”
Routing Guideline 1	Route VCC1P2PLLD and VSSPLLD, VCC1P2PLLP and VSSPLLP as differential traces.
Routing Guideline 2	The nodes connecting VCC1P2PLLD and the capacitor, VCC1P2PLLP and the capacitor must be as short as possible.
Routing Guideline 3	The 1.2 V supply regulator used for the PLL filter must have less than +/- 3% tolerance

Figure 60. VCC1P2PLLD, VCC1P2PLL Lowpass Filter Configuration



12.5.3 $V_{CC3P3PLLX}$ PLL Requirements

To reduce clock skew, a PLL is implemented for Intel XScale® microarchitecture. The balls associated with this PLL are VCC3P3PLLX and VSSPLLX. The lowpass filter, as shown in Figure 61, reduces noise induced clock jitter and its effects on timing relationships in system designs. The node connecting VCC3P3PLLX and the capacitor must be as short as possible.

The filter has the following characteristics:

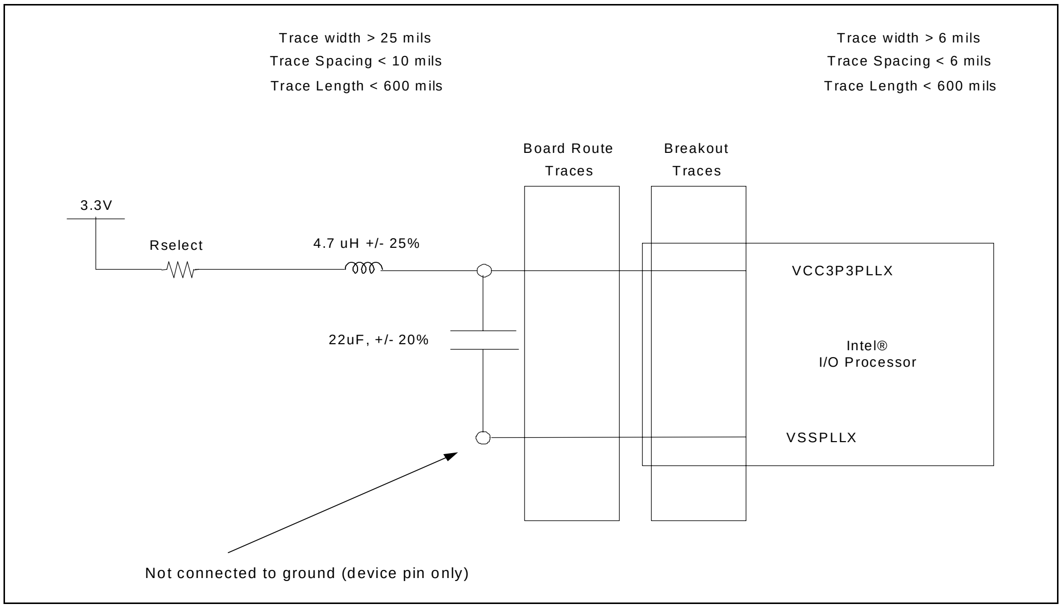
- The filter components must be able to handle a DC current of 30mA.
- < 0.2dB gain in pass band and < 0.5dB attenuation in pass band < 1Hz. Passband is DC through 1Hz.
- > 34dB attenuation from 1MHz to 66MHz
- > 28dB attenuation from 66MHz to core frequency

The following notes list the layout guidelines for this filter:

Table 59. $V_{CC3P3PLL}$ Layout Guideline

Parameter	Specification
Reference Plane	• Ground referenced • VCC3P3PLL and VSSPLLX traces must be ground referenced (no V_{CC} references)
Inductor	• 4.7 µH • L must be magnetically shielded • ESR: max < 0.4 Ω • rated at 45 mA • An example of this inductor is TDK part number MLZ2012E4R7P.
Capacitor	• 22 µF (Capacitor) • ESR: max < 0.4 Ω • ESL < 3.0 nH • Place 22 µF capacitor as close as possible to package pin.
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 3.3V plane to the top end of the capacitor is > 0.35 Ω • 3.3V plane to $V_{CC3P3PLL}$ < 1.5 Ω • resistor ratings: 1/16 W 6.3 V • resistor must be placed between V_{CC3P3} and L. • Note: when trace and component resistance is large enough the discrete resistor is not required
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils
Trace Spacing	• ≥ 30 mils from any other signals.
Trace Length maximum	1.2”
Routing Guideline 1	Route VCC3P3PLLX and VSSPLLX as differential traces.
Routing Guideline 2	The nodes connecting VCC3P3PLL and the capacitor must be as short as possible.

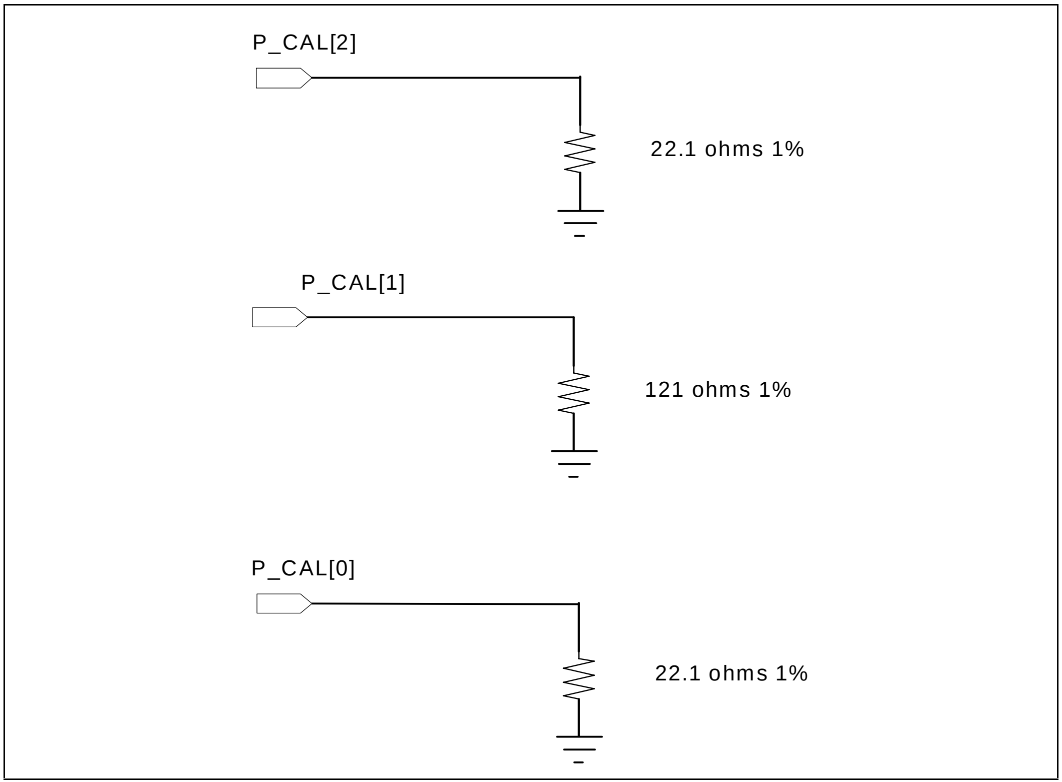
Figure 61. VCC3P3PLL Filter Configuration



12.6 PCI Resistor Calibration

Figure 62 shows the termination required for the PCI calibration circuitry. **PCI** Calibration pins P_CAL[1:0] are connected to an external calibration resistors. The PCI output drivers reference the resistor for dynamic adjustment of slew rate and drive strength to compensate for voltage and temperature variations.

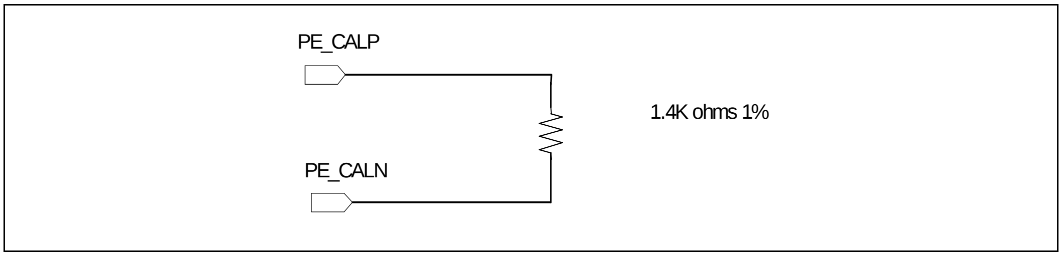
Figure 62. PCI Resistor Calibration



12.7 PCI Express Resistor Compensation

Figure 63 shows the termination required for the PCI Express RCOMP circuit.

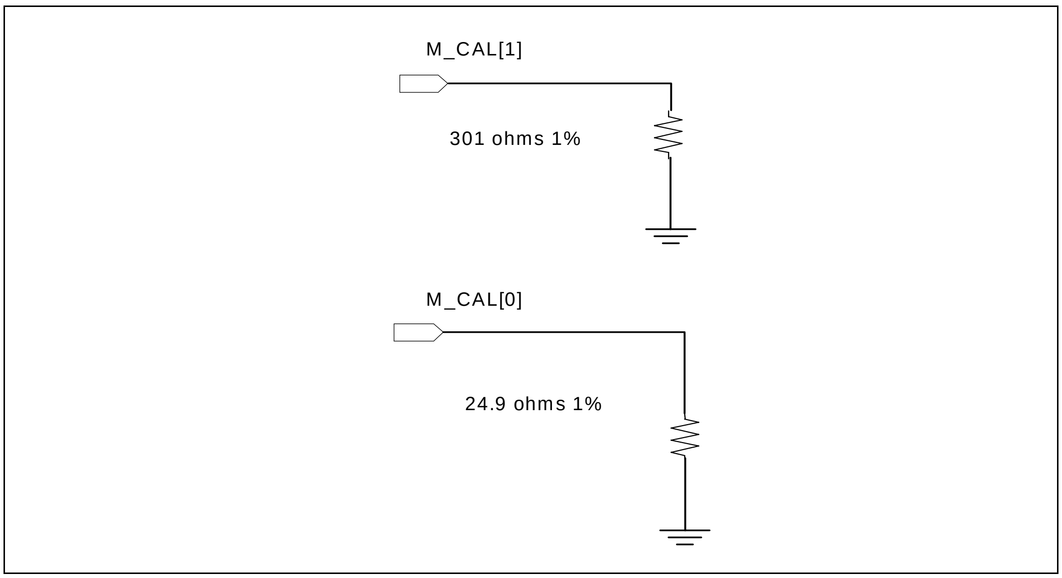
Figure 63. PCI Express RCOMP



12.8 Memory Calibration Circuitry

The Figure 64 shows the memory calibration pins M_CAL[1] and M_CAL[0] connected to external calibration resistors to ground. The memory output drivers reference the resistor for dynamic adjustment of the drive strength to compensate for temperature and voltage variations.

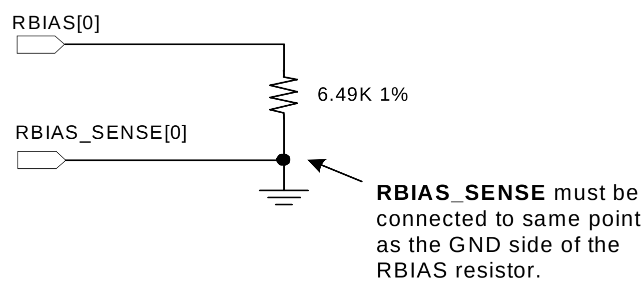
Figure 64. Memory Calibration Circuitry



12.9 RBIAS Circuit

Figure 65 provides a diagram on how to connect the RBIAS0 and RBIAS_SENSE0 pins. RBIAS1 and RBIAS_SENSE1 must be connected in the same manner.

Figure 65. RBIAS[0], RBIAS_SENSE[0] Connections



13.0 Layout Checklist

13.1 Intel® 81348 I/O Processor Layout Checklist

The Table 60 provides a summary of layout guidelines for each of the Intel® 81348 I/O Processor interfaces described in detail in the previous sections. The spacing and width specifications are based on the stackup provided in Section 3.0.

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 1 of 20)

Checklist Items	Recommendations	Comments
DDR2 Synchronous (DQ/DQS/DM/CB) DIMM		
Reference Layer	Route over unbroken ground plane.	
Preferred Layer	Stripline	
Impedance	DQ Stripline Trace Impedance: 50 ohms +/- 15% motherboard and 60 ohms +/- 15% adapter card	
	DQS Differential Stripline Trace Impedance: 85 ohms +/- 15% and 100 ohms +/- 15% adapter card	Refer to stackup Section 3.0
Spacing (edge to edge)	• Spacing with-in the same group ≥ 12 mils min • Spacing from other DQ groups ≥ 20 mils min. • Spacing of DQS to other signals ≥ 20 min.	
Length Matching DQS pair and group	Trace Length Matching: • within DQS group: +/- 0.05” • within one pair DQS +/-: =/- 0.0250” • all DQS lines with respect to the clock signal: +/- 0.05”	
Length Matching: DQS with respect to clock	When total length: • 0” < total length ≤ 6”, matching < +/- 0.5” • 6” < total length ≤ 8”, matching < +/- 0.1”	
DQ Break out Exception	Microstrip • spacing: 5 mils, • width 5 mils • Length 0” - 0.5”	
DQ Lead-in Length	0.5” to 8”	
DQS Break out Exception	Microstrip: • spacing: 5 mils, • width: 5 mils • length 0” - 0.5”	
DQS Lead-in Length	0.5” to 8”	
Via counts	≤ 2 (for differential signals the number of vias on + and - signals must be the same)	
DQ and DQS ODT	• 150 ohms ODT enabled on memory for reads • 75 ohms ODT enabled on IOP for writes	
Routing Guideline	Route all data signals and their associated strobes on the same layer	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 2 of 20)

Checklist Items	Recommendations	Comments
DDR2 DIMM Clock Routing (M_CK[2:0]/M_CK#[2:0])		
Reference Plane	Route over unbroken ground plane	
Preferred Topology	Microstrip	
Trace Impedance	Microstrip differential impedance: 85 ohms +/- 15% for motherboard and 100 +/- 15% for add-in card.	Refer to stackup Chapter 3.0
Trace Spacing (edge to edge)	Between other groups ≥ 25 mils	
Length Matching	• Within M_CK/M_CK# differential clock + /- pair: +/- 0.0250" • With respect to DQS group: when total length: 0 < total length ≤ 6", matching ≤ +/- 0.5" when total length: 6" < total length ≤ 8", matching ≤ +/- 0.1" • With respect to address/command group +8"/-3" motherboard and +8/-2" add-in card • With respect to CS/CKE group +/-2" motherboard and +1/-3" add-in card	
Breakout:	Microstrip or Stripline • spacing: 5 mils, • width: 5 mils • Length 0" - 0.5"	
Lead-in Length	Microstrip: • 0.5" to 8"	
Via Count	Maximum of 1 via/layer change for M_CK/M_CK# differential clocks. Use the same number of vias for + and - lines.	
DDR2 DIMM Address/Command Routing (MA[13:0], CS[1:0],CKE[1:0], ODT[1:0])		
Reference Plane	Route over unbroken ground plane or unbroken voltage plane.	
Preferred Topology	Microstrip	
Trace Impedance	Impedance: 50 ohms +/- 15% for motherboard and 60 +/- 15% for add-in card.	
Trace Spacing (edge to edge)	• Within the group ≥ 12 mils • Between other groups ≥ 20 mils	
Breakout	Microstrip • spacing: 5 mils, • width: 5 mils • Length 0" - 0.5"	
Lead-in Length	• 0.5" - 10"	
Length Matching: address/ command group (except CS, ODT and CKE lines) with respect to clock (from controller to DIMM connector)	• +8"/-3"[1] maximum for motherboard and +8"/-2" maximum for add-in card	
Length Matching: CS, ODT and CKE lines with respect to clock (from controller to DIMM connector)	• +/-2" maximum for motherboard and +1"/-3" maximum for add-in card	
Length to Parallel Termination	Microstrip: • 0.15" - 0.5"	Place terminations in VTT island.
Parallel Termination: single	• 51.1 ohms +/- 1% to VTT. Refer to Figure 31	
Parallel Termination: split	• 100 ohms +/- 1% to 1.8V and 100ohms +/-1% to ground. Refer to Figure 32	
Via counts	2 vias or less	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 3 of 20)

Checklist Items	Recommendations	Comments
Embedded DDR2 Synchronous (DQ/DQS/DM/CB)		
Reference Layer	Route over unbroken ground plane.	
Preferred Layer	Stripline	
Impedance	DQ Stripline Trace Impedance: 50 ohms +/- 15%	
	DQS Differential Stripline Trace Impedance: 85 ohms +/- 15%	Refer to stackup Chapter 3.0
Spacing (edge to edge)	• Spacing with-in the same group ≥ 12 mils min • Spacing from other DQ groups ≥ 20 mils min. • Spacing of DQS to other signals ≥ 20 min.	
Length Matching DQS pair and group	Trace Length Matching: • within DQS group: +/- 0.05” • within one pair DQS +/-: =/- 0.0250”	
Length Matching DQS group with respect clock	• DQS length = clock length - 1” (tolerance +/- 0.1”)	
DQ/DQS Break out Exception	Microstrip • spacing: 5 mils, • width 5 mils • Length 0” - 0.5”	
Overall Trace Length	0.5” to 9.5”	
Via counts	≤ 4 (for differential signals the number of vias on + and - signals must be the same)	
DQ and DQS ODT	• 150 ohms ODT enabled on IOP for reads • 75 ohms ODT enabled on SDRAM	
Routing Guideline	Route all data signals and their associated strobes on the same layer	
Embedded DDR2 Clock Routing (M_CK[2:0]/M_CK#[2:0])		
Reference Plane	Route over unbroken ground plane	
Preferred Topology	Microstrip	
Trace Impedance	Microstrip differential impedance: 85 ohms +/- 15%	Refer to stackup Chapter 3.0
Trace Spacing (edge to edge)	Between other groups ≥ 25 mils	
Length Matching: With respect to DQ/DQS group (from controller to memory ball)	• DQ/DQS length = clock length - 1”	
Length Matching: With respect to address/command group (except CS, CKE, ODT) from controller to memory ball	• ADDR/CMD <= clock length + 2” • ADDR/CMD >= clock length - 1”	
Length Matching with respect to CS/CKE group	For Daisy chain Topology: • when CS/CKE length is ≤ 4”: clock length + 1” • when CS/CKE length is > 4”: clock length + 3” For balanced segment topology: • when CS/CKE length is ≤ 2”: clock length + 1” • when CS/CKE length is > 2”: clock length +/- 0.5”	
Breakout:	Microstrip or Stripline • spacing: 5 mils, • width: 5 mils • Length 0” - 0.5”	
Lead-in Length	Microstrip: • 0.5” to 10.5”	
Routing Guideline	Maximum of 2 via/layer changes for M_CK/M_CK# clocks (same number of vias between + and - signals of the differential clock).	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 4 of 20)

Checklist Items	Recommendations	Comments
Embedded DDR2 Address/CMD Routing		
Reference Plane	Route over unbroken ground plane preferred	
Preferred Topology	Microstrip lines	
Trace Spacing (edge to edge)[1]	• 5 mils acceptable between the pins and the breakout regions. • $\geq$ 12 mils within group • $\geq$ 20 mils from any other clock/DQ/DQS groups.	
Trace Impedance	50 ohms +/- 15% for a motherboard	
Trace Length: Overall length from signal Ball to SDRAM ball	1” min to 12” maximum	
Trace Length	• TL Break out: $\leq$ 0.5”	
	• TL0: 0.5” to 9”	
	• TL1: 0.2” to 0.75”	
	• TL2: 0.2” to 0.75”	
	• TL3: 0.05” to 0.2	
	• TL4: 0.05” to 0.2	
Length Matching: address/ command group (except CS, ODT and CKE lines) with respect to clock (from controller to SDRAM ball)	• ADDR/CMD <= clock length + 2” • ADDR/CMD >= clock length - 1”	
Breakout Trace Width and Spacing	5 mils x 5mils. Microstrip is preferred. Maximum length of the breakout trace is 500 mils.	
Split Termination	• 100 ohms +/- 1% to ground and 100 ohms +/- 1% to 1.8V	
Routing Guideline 1	Place the VTT terminations in the VTT island after the DIMM with a trace length of 0.15” to 0.5”	
Routing Guideline 2	For split terminations place the VTT termination in their respective power islands	
Routine Guideline 3	6 Vias or less	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 5 of 20)

Checklist Items	Recommendations	Comments
Embedded DDR2 CS, ODT, CKE Routing Topology		
Reference Plane	Route over unbroken ground plane preferred	
Preferred Topology	Microstrip lines	
Trace Spacing (edge to edge)[1]	• 5 mils acceptable between the pins and the breakout regions. • ≥ 12 mils within group • ≥ 20 mils from any other clock/DQ/DQS groups.	
Trace Impedance	50 ohms +/- 15% for a motherboard	
Trace Length: Overall length from signal Ball to SDRAM ball	1” min to 12” maximum Refer to Table 2 for segment lengths.	
Trace Length Routing	Balanced Load Topology	
	• TL Break out: ≤ 0.5”	
	• TL0: 0.5” to 8”	
	• TL1: 0.2” to 0.2”	
	• TL3: 0.2” to 0.2”	
	• TL4: 0.2” to 0.2”	
	• TL5: 0.4” to 0.4”	
	• TL6: 0.05” to 0.2”	
	Daisy Chain Topology:	
	• TL Break out: ≤ 0.5”	
	• TL0: 0.5” to 8”	
	• TL1: 0.2” to 0.75”	
	• TL3: 0.05” to 0.2”	
	• TL4: 0.05” to 0.2”	
Length Matching: With respect to CS/CKE group	For daisy chain topology: • when CS/CKE group length is < 4”: CK length + 1” • when CS/CKE group length is > 4”: CK length + 3” For balanced segment topology: • when CS/CKE group length is < 2”: CK length + 1” • when CS/CKE group length is > 2”: CK length +/- 0.5”	
Breakout Trace Width and Spacing	5 mils x 5mils. Microstrip is preferred. Maximum length of the breakout trace is 500 mils.	
Split Termination	• 100 ohms +/- 1% to ground and 100 ohms +/- 1% to 1.8V	
Routing Guideline 1	Place the VTT terminations in the VTT island after the DIMM with a trace length of 0.15” to 0.5”	
Routing Guideline 2	For split terminations place the VTT termination in their respective power islands	
Routine Guideline 3	6 Vias or less	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 6 of 20)

Checklist Items	Recommendations	Comments
Embedded DDR2 CS, ODT, CKE Routing Daisy Chain Topology		
Reference Plane	Route over unbroken ground plane preferred	
Preferred Topology	Microstrip lines	
Trace Spacing (edge to edge)[1]	• 5 mils acceptable between the pins and the breakout regions. • ≥ 12 mils within group • ≥ 20 mils from any other clock/DQ/DQS groups.	
Trace Impedance	50 ohms +/- 15% for a motherboard	
Trace Length: Overall length from signal Ball to SDRAM ball	1” min to 12” maximum Refer to Table 2 for segment lengths.	
Trace Length	• TL Break out: ≤ 0.5”	
	• TL0: 0.5” to 8”	
	• TL1: 0.2” to 0.75”	
	• TL3: 0.05” to 0.2”	
	• TL4: 0.05” to 0.2”	
Length Matching: With respect to CS/CKE group	For daisy chain topology: • when CS/CKE group length is < 4”: CK length + 1” • when CS/CKE group length is > 4”: CK length + 3” For balanced segment topology: • when CS/CKE group length is < 2”: CK length + 1” • when CS/CKE group length is > 2”: CK length +/- 0.5”	
Breakout Trace Width and Spacing	5 mils x 5mils. Microstrip is preferred. Maximum length of the breakout trace is 500 mils.	
Split Termination	• 100 ohms +/- 1% to ground and 100 ohms +/- 1% to 1.8V	
Routing Guideline 1	Place the VTT terminations in the VTT island after the DIMM with a trace length of 0.15” to 0.5”	
Routing Guideline 2	For split terminations place the VTT termination in their respective power islands	
Routine Guideline 3	6 Vias or less	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 7 of 20)

Checklist Items	Recommendations	Comments
PCI Express for Motherboard Layout Recommendations (PETP[7:0]/ PETN[7:0],PERP[7:0],PERN[7:0])		Refer to Section 5.2.1
Reference Plane	Routing over unbroken ground plane is preferred. When unbroken ground plane is not available route over unbroken voltage plane.	
Trace Impedance	• Single-ended: 50 ohms +/- 15% • Differential: 85 ohms +/- 15%	
Microstrip Trace Width	5 mils	
Microstrip Trace Spacing (edge to edge)	• between + and - : 7 mils • Between other signals $\geq$ 25 mils • Transmit and Receive pairs are interleaved. • For non interleaved pairs interpair spacing $\geq$ 45 mils.	
Stripline Trace Width	5 mils	
Stripline Trace Spacing (edge to edge)	• between + and - : 7 mils • Between other signals $\geq$ 25 mils • Transmit and Receive pairs are interleaved. • For non interleaved pairs interpair spacing $\geq$ 45 mils.	
Length Matching	• Total allowable pair mismatch on system board $\leq$ 10 mils • Total allowable interpair trace mismatch for a lane that consists of system board and an add-in card < 15 mils • Length matched on a segment by segment basis.	
AC coupling capacitor	• 75 nF - 200 nF located at the transmitter	
Total Trace Length - (Transmitter/Receiver) from device signal pin to AC coupling capacitor and AC coupling capacitor to PCI Express device pin	• 1” - 30“ max.	
Via counts	4 vias or less	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 8 of 20)

Checklist Items	Recommendations	Comments
PCI Express Baseboard (for Motherboard-Adapter Card) Layout Recommendations (PETP[7:0]/PETN[7:0],PERP[7:0],PERN[7:0])		Refer to Section 5.2.2
Reference Plane	Routing over unbroken ground plane is preferred. When unbroken ground plane is not available route over unbroken voltage plane.	
Trace Impedance motherboard	• Single -ended: 50 ohms +/- 15% • Differential microstrip: 85 ohms +/- 15%	
Trace Impedance adapter card	• Single Ended: 60 +/-15% ohms nominal • Differential: 100 +/-15% ohms nominal	
Microstrip Trace Width	5 mils	
Microstrip Trace Spacing (edge to edge)	• between + and - : 7 mils • Between other signals ≥ 25 mils • Transmit and Receive pairs are interleaved. When interleaving • For non interleaved pairs interpair spacing ≥ 45 mils.	
Stripline Trace Width	5 mils	
Stripline Trace Spacing (edge to edge)	• Between + (P) and - (N) of pair: 7 mils • Between other signals ≥ 25 mils • Transmit and Receive pairs are interleaved. • For non interleaved pairs interpair spacing ≥ 45 mils.	
Length Matching	• Total allowable length skew between + and - signals of the pair length mismatch on a base board must not exceed 25 mils. • Total allowable length skew between + and - signals of the pair trace mismatch for a lane that consists of a base board and an add-in card must not exceed 15 mils. • Total skew across all lanes must be less than 20 ns.	
AC coupling capacitor	• 75nF - 200 nF located at the transmitter	
Total Trace Length - (Transmitter/Receiver) from device signal pin to AC coupling capacitor and AC coupling capacitor to PCI Express device pin	• 1.0” - 27“ max	
Total Length: Topology 2: Intel® 81348 I/O Processor transmitter on adapter card and the PCI-E device receiver on motherboard	• 1.0” min. - 25” max.	
Via counts	4 vias or less	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 9 of 20)

Checklist Items	Recommendations	Comments
PCI Express Clock Layout Recommendations (REFCLKP, REFCLKN)		Refer to Section 5.2.3
Reference Plane	Routing over unbroken ground plane is preferred. When unbroken ground plane is not available route over unbroken voltage plane.	
Trace Impedance	Differential target: 100 ohm, tolerance +/-15% Single Ended: 50 ohms +/- 15%	
Trace Width	5 mils	
REFCLKP, REFCLKN **d**ifferential Clock Pair Spacing	< 1.4 x Space Width	
Serpentine Spacing (spacing of clock lines from itself)	spacing $\geq$ 25 mils.	
Clock to Other Spacing (edge to edge)	Spacing from clock to other groups $\geq$ 25 mils.	
Trace Lengths[2]	L1, L1: 0.5" max	
	L2, L2: 0.2" max	
	L3, L3: 0.2" max	
	L4, L4 • Device down: 2" to 15.3" or • Connector: 2" to 11.3	
	Total Length = L1+L2_+L4 • Device Down: 3" to 16" or • Connector: 3" to 12"	
Length Matching Requirements within differential pair	+/- 5 mils	
Rs Series Resistor	33 +/- 5% ohms	
Rt Shunt Resistor	49.9 +/- 1% ohms	
Number of Vias	4 max	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 10 of 20)

Checklist Items	Recommendations	Comments
SAS Interface for Compliant Implementations (S_TXP[7:0], S_TXN[7:0], S_RXP[7:0], S_RXN[7:0])		Refer to Section 7.0
Reference Plane	Route over unbroken ground plane.	
Trace Impedance	Differential 100 ohms +/- 15%	
Trace Width	• Microstrip: 5 mils nominal • Stripline: 4 mils nominal	
Trace Spacing edge to edge	• breakout: SAS pair to pair spacing 20 mils ≤ 0.5" of the device ball • Refer to Table 43 for interpair spacing recommendations	• Refer to stackup Chapter 3.0
Group Spacing (edge to edge)	• Keep SAS signals ≥ 50 mils away from the other types of signals. • SAS pair to pair spacing is reduced to ≥ 20 mils in the breakout region within 0.5" of the pin field as necessary	
Compliant: maximum trace length: Motherboard (Intel® 81348 I/O Processor ball to first connector)	≤ 5" (max)	
Length Matching (between TX+ and TX-) and (between RX+ and RX-)	• ≤ 25 mils • Maintain consistent spacing between P and N signals for achieving differential trace impedance (takes precedence over length matching)	
AC Coupling on TX+, TX- and RX+, RX-	10 nF (low ESR) as close to the pad as possible.	
Vias	• 2 vias per signal between device package ball and connector pin • Board thickness 0.062 inches max for though hole vias. • Drill width 20mils • Note: Reducing the number of vias takes precedence over the AC capacitor placement. • Impedance controlled vias (100% +/-15%) preferred	
PBI Interface (A[24:0], D[15:0]) One, Two and Three Loads		Refer to Section 8.0
Reference Plane	Route over unbroken ground plane or unbroken power plane.	
Recommended Layer	Microstrip or stripline or combination	
Trace Impedance	Motherboard: 50 ohms +/- 15% Add-in Card: 60 ohms +/- 15%	
Trace Spacing (edge to edge)	• ≥ 5 mils between all Address and Data lines • ≥ 20 mils must be maintained from all other signals or vias.	
Breakout TL0	5 mils on 5 mils spacing. Maximum length of breakout region is 500mils.	
Trace LengthTL1 single load	0" to 20.0"	
Trace Length TL1 multiple loads	2" to 20.0"	
Trace Length TL2, TL3	0.5" to 2.0" from the last device on the bus.	
Trace Length to strapping resistors TL4	0.5" to 3.0" from the last device on the bus.	
Routing Guideline	Route as daisy-chain only.	
Via counts	8 vias or less	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 11 of 20)

Checklist Items	Recommendations	Comments
PCI-X Routing Recommendations (Clocks P_CLK[0-3], PCLKIN, PCLKOUT)		Refer to Section 6.0
Reference Plane	Route over unbroken ground plane.	
Recommended Layer	Stripline	
Trace Impedance: Motherboard	Microstrip: 50 ohm +/- 15%, stripline: 50 ohm +/- 10%	
Trace Impedance: Adapter Card	Microstrip or stripline: 60 ohm +/- 15%	
Trace Spacing (edge to edge)	• between two different clock lines ≥ 25 mils • between two segments of the same clock line≥ 25 mils • between clock and other signals ≥ 50 mils	
Series Resistors	28 ohms 1% for connectors 26 ohms 1% for embedded	
Trace Length TL1 from buffer to the resistor	1.0” max	
Total Trace Length: from device ball to device (including resistor segment)	11” max	
Length Matching:	All clock lines including PCLKOUT to PCLKIN (feedback clock) must be matched to within 25 mils. Refer to Figure 49.	
• Topologies with only embedded devices.	Match clocks to within 25 mils	
• Topologies with only connectors .	• Match clocks to within 25 mils. • Rout feedback clock longer to compensate for the adapter card length (2.4” to 2.6”) + 0.85” (for the connector delay)	
• Topologies with both slots and devices used in the design	• Match Clocks to within 25 mils • Rout feedback clock longer to compensate for the adapter card length (2.4” to 2.6”) + 0.85” (for the connector delay) • PCLKs going to the embedded devices must be compensate for the adapter card length (2.4” to 2.6”) + 0.85” (for the connector delay)	
Vias	≤ 2 vias	
PCI-X Point to Point Signals (REQ#, GNT#)		
Signal Group	REQ# and GNT# lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15% microstrip and 50 ohm +/- 10% stripline	
Motherboard Trace Spacing	14 mils microstrip and 12 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline	
Group Spacing: Spacing from other groups	25 mils minimum, edge to edge	
Trace Length TL1 - from buffer to the connector	• 0.5” min - 4.5” max for 100MHz • 0.5” - 12.0” for 100MHz • 0.5” - 15.0” for 66MHz	
Trace Length TL2 - from connector to the receiver	2.4” - 2.6” max	
Vias	≤ 3 vias	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 12 of 20)

Checklist Items	Recommendations	Comments
PCI-X 133 MHz Single Slot Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	14 mils microstrip 12 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	14 mils microstrip and 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Lower AD: Trace Length TL1 - from SL ball to the connector	1.0" - 6.0" max	
Lower AD: Trace Length TL2 - from connector to the receiver	0.75" - 1.5" Max	
Upper AD: Trace Length TL1 - from SL ball to the connector	0.5" - 5.0" max	
Upper AD: Trace Length TL2 - from connector to the receiver	1.75" - 2.75" Max	
Vias	$\leq$ 2 vias	
PCI-X 133 MHz Embedded Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	14 mils microstrip 12 mils stripline	
Group Spacing edge to edge	Spacing from other groups: 25 mils minimum	
Trace Length TL1 - from SL ball to the junction	0.75" min - 2.5" max	
Trace Length TL2, TL4 from connector to the receiver	0.75" min - 2.5" Max	
Trace Length TL3 from junction to junction	0.75 "min. to 2.5" max	
Vias	$\leq$ 3 vias	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 13 of 20)

Checklist Items	Recommendations	Comments
PCI-X 133 MHz Mixed Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	• 60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 stripline	
Group Spacing edge to edge	Spacing from other groups: 25 mils minimum	
Lower AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.0″ max	
Lower AD: Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	
Lower AD: Trace Length TL3, from junction to CONN	0.5″ min. to 3.5″ max	
Lower AD: Trace Length TL4, from CONN to adapter	0.75″ min. to 1.5″ max	
Upper AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.0″ max	
Upper AD: Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	
Upper AD: Trace Length TL3, from junction to CONN	0.5″ min. to 2.25″ max	
Upper AD: Trace Length TL4, from CONN to adapter	1.75″ min. to 2.75″ max	
Vias	< 3 vias	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 14 of 20)

Checklist Items	Recommendations	Comments
PCI-X 100 MHz Slot Topology (AD lines)		
Signal Group	Address/data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	• 60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 stripline	
Group Spacing edge to edge	Spacing from other groups: 25 mils minimum	
Lower AD: Trace Length TL1 - from ball to the junction	0.5” - 12.0” max	
Lower AD: Trace Lengths TL3 - Between connectors	0.5” - 3.0” max	
Lower AD: Trace Lengths TL2 - from connector to the first receiver, TL4 - from connector to the second receiver	0.75” - 1.50” max	
Upper AD: Trace Length TL1 - from ball to the junction	0.5” - 10.0” max	
Upper AD: Trace Lengths TL3 - Between connectors	0.5” - 3.0” max	
Upper AD: Trace Lengths TL2 - from connector to the first receiver, TL4 - from connector to the second receiver	1.75” - 2.75” max	
Vias	< 3 vias	
PCI-X 100 MHz Embedded Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	• 60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	14 mils microstrip and stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5” min. to 3.0” max (3 loads, 5 loads)	
Trace Length TL3, TL5, TL7, TL9: from junction to junction	0.5” min. to 2.0” max (3 loads) 0.5” min. to 1.0” max (5 loads)	
Trace Length TL2, TL4, TL6, TL8, TL10: from junction to receiver	0.5” min. to 3.0” max (3 loads) 0.5” min to 2.0” max (5 loads)	
Vias	≤ 4 vias	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 15 of 20)

Checklist Items	Recommendations	Comments
PCI-X 100 MHz Mixed Topology (AD lines)		
Signal Group	Address, data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip and 14 mils stripline	
Add-in Card Impedance	• 60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	18 mils microstrip and 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Lower AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.5″ max	
Lower Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	
Lower Trace Length TL3, from junction to first CONN and TL5, from junction to second CONN	0.5″ min. to 3.5″ max	
Lower Trace Length TL4, from 1st CONN to AD2 Lower AD: Trace Length TL6, from 2nd CONN to AD3	0.75″ min. to 1.5″ max	
Upper AD: Trace Length TL1 - from SL ball to the junction	0.5″ min. to 2.5″ max	
Upper AD: Trace Length TL2 - from junction to AD1	0.5″ min. to 2.0″ max	
Upper AD: Trace Length TL3, from 1st junction to first CONN	0.5″ min. to 3.0″ max	
Upper AD: From 2nd junction to second CONN	0.5″ min. to 3.5″ max	
Upper AD: Trace Length TL4, from 1st CONN to AD2 Upper AD: Trace Length TL6, from 2nd CONN to AD3	1.75″ min. to 2.75″ max	
Vias	$\leq$ 3 vias	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 16 of 20)

Checklist Items	Recommendations	Comments
PCI-X 66 MHz Slot Topology (AD lines)		
Signal Group	Address/data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Add-in Card Impedance	60 ohm +/- 15% microstrip and stripline	
Add-in Card Trace Spacing	12 mils microstrip and 12 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Lower AD: Trace Length TL1 - from ball to the connector	0.5” - 12.0” max	
Lower AD: Trace Lengths TL3, TL5, TL7 - Between connectors	0.5” - 2.0” max	
Lower AD: Trace Lengths TL2, TL4, TL6, TL8- from connector to the receivers	0.75” - 1.50” max	
Upper AD: Trace Length TL1 - from ball to the connector	0.5” - 9.0” max	
Upper AD: Trace Lengths TL3, TL5, TL7 - Between connectors	0.5” - 2.0” max	
Upper AD: Trace Lengths TL2, TL4, TL6, TL8- from connector to the receivers	1.75” - 2.75” max	
Vias	≤ 4 vias	
PCI-X 66 MHz Embedded Topology (AD lines)		
Signal Group	Address/data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip 14 mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Trace Length TL1 - from SL ball to the junction	0.5" min. to 3.0” max (8 loads) 0.5" min. to 3.5” max (6 loads)	
Trace Length TL3, TL5, TL7, TL9,TL11,TL13,TL15: from junction to junction	0.5" min. to 1.5” max (8 loads) 0.5" min. to 2.5” max (6 loads)	
Trace Length TL2, TL4, TL6, TL8, TL10,TL12,TL14,TL16: from junction to receiver	0.5" min. to 1.5” max (8 loads) 0.5” min to 2.0” max (6 loads)	
Vias	≤ 4 vias	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 17 of 20)

Checklist Items	Recommendations	Comments
PCI-X 66 MHz Mixed Topology (AD lines)		
Signal Group	Address/data and control lines	
Reference Plane	Route over unbroken reference plane.	
Motherboard Impedance (microstrip)	50 ohm +/- 15%	
Motherboard Impedance (stripline)	50 ohm +/- 10%	
Motherboard Trace Spacing	18 mils microstrip and 14 mils stripline	
Adapter Card Trace Impedance	60 ohm +/- 15% (microstrip and stripline)	
Adapter Card Trace Spacing	12 mils microstrip and mils stripline	
Group Spacing	Spacing from other groups: 25 mils minimum, edge to edge	
Lower AD: Trace Length TL1 - from SL ball to the junction	0.5” min. to 11” max	
Lower AD: Trace Length TL2, TL4 - from junction to AD1, AD2	0.5” min. to 4.5” max	
Lower AD: Trace Length TL3, TL5, TL7 from junction to junction	0.5” min. to 4.0” max	
Lower AD: Trace Length TL6 from 1st CONN to AD3, TL8: from 2nd CONN to AD4	0.75” min. to 1.5” max	
Upper AD: Trace Length TL1 - from SL ball to the junction	0.5” min. to 10” max	
Upper AD: Trace Length TL2, TL4 - from junction to AD1, AD2	0.5” min. to 4.0” max	
Upper AD: Trace Length TL3, TL5, TL7 from junction to junction	0.5” min. to 4.0” max	
Upper AD: Trace Length TL6 from 1st CONN to AD3, TL8: from 2nd CONN to AD4	1.75” min. to 2.75” max	
Vias	$\leq$ 4 vias	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 18 of 20)

Checklist Items	Recommendations	Comments
VCC1P2PLLS0 - VSSPLLS0, VCC1P2PLLS1 - VSSPLLS0 Storage PLL Filters		
Reference Plane	• Ground • VCC1P2PLLS0, VSSPLLS0 and VCC1P2PLLS1, VSSPLLS1 traces must be ground referenced (no V_{CC} references)	
Inductor	• 120 nH +/- 20%, • L must be magnetically shielded • RDC: max < 0.3 ohms • rated at 45 mA	
Capacitor	• 22 µF +/- 20% 6.3V (Capacitor) • ESR: max < 0.3 ohms • ESL < 2.5 nH • Place 22 µF capacitor as close as possible to package pin.	
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 1.2V plane to the top end of the capacitor is > 0.35 Ω (ινχλυδινγ βοαρδ ανδ χομπονεντ ρεσιστανχε) • 1.2V plane to $V_{CC1P2PLL}$ < 1.5 Ω (ινχλυδινγ βοαρδ ανδ χομπονεντ ρεσιστανχε) • resistor must be placed between V_{CC1P2} and L. • Note: when trace and component resistance is large enough a discrete resistor is not required	
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils	
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils	
Trace Spacing	• ≥ 30 mils from any other signals.	
Trace Length maximum	1.2”	
Routing Guideline 1	Route VCC1P2PLLS and VSSPLLS as differential traces.	
Routing Guideline 2	The nodes connecting VCC1P2PLLS and the capacitor must be as short as possible.	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 19 of 20)

Checklist Items	Recommendations	Comments
VCC1P2PLLD - VSSPLLP PCI-X PLL Filters		
Reference Plane	• Ground • VCC1P2PLLP, VCC1P2PLLD traces must be ground referenced (no V_{CC} references)	
Inductor	• 4.7 uH +/- 25% 45 mA • L must be magnetically shielded • ESR: max < 0.3 ohms • rated at 45 mA	
Capacitor	• 22 µF +/- 20% 6.3V (Capacitor) • ESR: max < 0.3 ohms • ESL < 2.5 nH • Place 22 µF capacitor as close as possible to package pin.	
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 1.2V plane to the top end of the capacitor is > 0.35 Ω (ινχλυδινγ βοαρδ ανδ χομπονεντ ρεσιστανχε) • 1.2V plane to $V_{CC1P2PLL}$ < 1.5 Ω (ινχλυδινγ βοαρδ ανδ χομπονεντ ρεσιστανχε) • 1/16 W 6.3 V • resistor must be placed between V_{CC1P2} and L. • Note: when trace and component resistance is large enough a discrete resistor is not required	
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils	
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils	
Trace Spacing	• ≥ 30 mils from any other signals.	
Trace Length maximum	1.2”	
Routing Guideline 1	Route VCC1P2PLLD and VSSPLLD, VCC1P2PLLP and VSSPLLP as differential traces.	
Routing Guideline 2	The nodes connecting VCC1P2PLLD and the capacitor, VCC1P2PLLP and the capacitor must be as short as possible.	
Routing Guideline 3	The 1.2 V supply regulator used for the PLL filter must have less than +/- 3% tolerance	

Table 60. Intel® 81348 I/O Processor Layout Checklist (Sheet 20 of 20)

Checklist Items	Recommendations	Comments
VCC3P3PLLX - VSSPLLX PLL Filters		
Reference Plane	• Ground referenced • VCC3P3PLL and VSSPLLX traces must be ground referenced (no V_{CC} references)	
Inductor	• 4.7 µH • L must be magnetically shielded • ESR: max < 0.4 ohms • rated at 45 mA • An example of this inductor is TDK part number MLZ2012E4R7P.	
Capacitor	• 22 µF 20% 6.3V (Capacitor) • ESR: max < 0.4 ohms • ESL < 3.0 nH • Place 22 µF capacitor as close as possible to package pin.	
Resistor	• Rselect: choose resistor such that both of the following conditions are met: • 3.3V plane to the top end of the capacitor is > 0.35 Ω • 3.3V plane to $V_{CC3P3PLL}$ < 1.5 Ω • resistor ratings: 1/16 W 6.3 V • resistor must be placed between V_{CC3P3} and L. • Note: when trace and component resistance is large enough the discrete resistor is not required	
Breakout Trace	• Trace Width > 6 mils • Trace Spacing < 6 mils • Trace Length < 600 mils	
Board Trace	• Trace Width > 25 mils • Trace Spacing < 10 mils • Trace Length < 600 mils	
Trace Length Max	• 1.2”	
Trace Spacing	• ≥ 30 mils from any other signals.	

14.0 References

The following manuals and specifications are helpful in designing an application using the Intel® 81348 I/O processor (81348).

14.1 Relevant Documents

- *Intel® 81348 I/O Processor Developer's Manual Developer's*, Intel Corporation
- *Intel® 81348 I/O Processor Datasheet*, Intel Corporation
- *Intel® 81348 I/O Processor Thermal Application Note*, Intel Corporation
- *PCI Express Specification*, Revision 1.0a
- PCI Express Base Specification 1.0a
- PCI Express Card Electromechanical Specification 1.0a
- *PCI Local Bus Specification*, Revision 2.3 - PCI Special Interest Group
- *PCI-X Specification,* Revision 1.0b - PCI Special Interest Group
- *PCI Hot-Plug Specification,* Revision 1.0 - PCI Special Interest Group
- *PCI Bus Power Management Interface Specification*, Revision 1.1 - PCI Special Interest Group
- IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE JTAG-1149.1-1990)
- The I2C Bus Specification version 2.1: http://www.semiconductors.philips.com/acrobat/literature/9398/39340011.pdf
- The SMBus Specification: http://www.smbus.org/specs/

Table 61. Intel Related Documentation

Document Title	Order #
Intel® Packaging Databook	240800

14.2 Design References

Table 62. Design References (Sheet 1 of 2)

Design References
Transmission Line Design Handbook, Brian C. Wadell
Microstrip Lines and Slotlines, K. C. Gupta. Et al.
Design, Modeling and Simulation Methodology for High Frequency PCI-X Subsystems, Moises Cases, Nam Pham, Dan Neal www.pcisig.com

Table 62. Design References (Sheet 2 of 2)

Design References
High-Speed Digital Design "A Handbook of Black Magic" Howard W. Johnson, Martin Graham
"Terminating Differential Signals on PCBs", Steve Kaufer, Kelee Crisafulli, Printed Circuit Design, March 1999
"Board Design Guidelines for PCI Express™ Interconnect", http://www.intel.com/technology/pciexpress/downloads/PCI_EI_PCB_Guidelines.pdf

14.3 Literature Resources

Intel documentation is available from the local Intel Sales Representative or Intel Literature Sales.

To obtain Intel literature write to or call:

Intel Corporation
Literature Sales
P.O. Box 5937
Denver, CO 80217-9808
(1-800-548-4725) or visit the Intel website at http://www.intel.com

14.4 Electronic Information

Table 63. Electronic Information

The Intel World-Wide Web (WWW) Location:	http://www.intel.com/
Customer Support (US and Canada):	800-628-8686

Appendix A Appendix

A.1 Terminology

To aid the discussion of the 81348, Table 64 provides the terminology used in this document.

Table 64. Terminology and Definitions (Sheet 1 of 3)

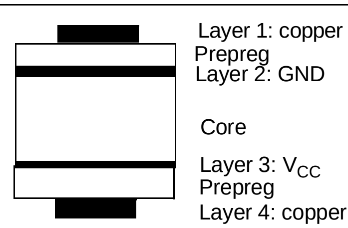
Term	Definition
Stripline	 Stripline in a PCB is composed of the conductor inserted in a dielectric with GND planes to the top and bottom. ***Note:*** An easy way to distinguish stripline from microstrip is to strip away layers of the board to view the trace on stripline.
Microstrip	 Microstrip in a PCB is composed of the conductor on the top layer above the dielectric with a ground plane below
Prepreg	Material used for the lamination process of manufacturing PCBs. It consists of a layer of epoxy material that is placed between two cores. This layer melts into epoxy when heated and forms around adjacent traces.
Core	Material used for the lamination process of manufacturing PCBs. This material is two sided laminate with copper on each side. The core is an internal layer that is etched.
PCB	 Example of a Four-Layer Stack Printed circuit board. Example manufacturing process consists of the following steps: • Consists of alternating layers of core and prepreg stacked • The finished PCB is heated and cured. • The via holes are drilled • Plating covers holes and outer surfaces • Etching removes unwanted copper • Board is tinned, coated with solder mask and silk screened
DDR	Double Data Rate Synchronous DRAM. Data clocked on both rising and falling edges of clock.
DDR2	DDR2 is backward compatible with DDR I. It allows 4.3GBytes/sec. for a clock rate of 533MHz and 3.2GB/sec. for a clock rate of 400 MHz.
DIMM	Dual Inline Memory Module
Source Synchronous DDR	With source-synchronous DDR interfaces, data and clock transport from a transmitter to a receiver, and the receiver interface uses the clock to latch the accompanying data.
SSTL_2	Series Stub Terminated Logic for 2.5 V
JEDEC	Provides standards for the semiconductor industry.
DLL	Delay Lock Loop - DDR feature used to provide appropriate strobe delay to clock in data.
PLL	Phase Lock Loop - A phase-locked loop (PLL) is an electronic circuit with a voltage- or current-driven oscillator that is constantly adjusted to match in phase (and thus lock on) the frequency of an input signal.

Table 64. Terminology and Definitions (Sheet 2 of 3)

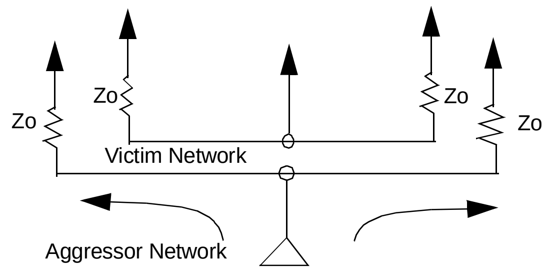
Term	Definition
Aggressor	A network that transmits a coupled signal to another network is aggressor network. 
Victim	A network that receives a coupled cross-talk signal from another network is a victim network.
Network	The trace of a PCB that completes an electrical connection between two or more components.
Stub	Branch from a trunk terminating at the pad of an agent.
ISI	Intersymbol Interference (ISI). This occurs when a transition that has not been completely dissipated, interferes with a signal being transmitted down a transmission line. ISI impacts both the timing and signal integrity. It is dependent on frequency, time delay of the line and the refection coefficient at the driver and receiver. Examples of ISI patterns used in testing at the maximum allowable frequencies are the sequences shown below: 0101010101010101 0011001100110011 000111000111000111
CRB	Customer Reference Board
PC1600	JEDEC Names for DDR based on peak data rates. PC1600= clock of 100 MHz * 2 data words/clock * 8 bytes = 1600 MB/sec.
PC2100	JEDEC Names for DDR based on peak data rates. PC2100= clock of 133 MHz * 2 data words/clock * 8 bytes = 2128 MB/sec.
PC2700	JEDEC Names for DDR2 based on peak data rates. PC2700= clock of 167 MHz * 2 data words/clock * 8 bytes = 2672 MB/sec
PC3200	JEDEC Names for DDR2 400 based on peak data rates. PC3200= clock of 200 MHz * 2 data words/clock * 8 bytes = 3200 MB/sec clock of 266 * 2 data words/clock * 8 bytes =
PC4300	JEDEC Names for DDR2 533 based on peak data rates. PC4300= clock of 266 MHz * 2 data words/clock * 8 bytes = 4256 MB/sec
Host processor	Processor located upstream from the Intel® 81348 I/O Processor
Local processor	Intel XScale® microarchitecture within Intel® 81348 I/O Processor
Downstream	• PCI Express: At or toward a PCI Express port directed away from root complex (to a bus with a higher number). • PCI-X: At or toward a PCI bus with a higher number (after configuration) away from host processor.
Upstream	• PCI Express: At or toward a PCI Express port directed to the PCI Express root complex (to a bus with a lower number). • PCI-X: At or toward a PCI bus with a higher number (after configuration) toward host processor.
Local memory	Memory subsystem on the Intel XScale® microarchitecture DDR SDRAM or Peripheral Bus Interface busses.
WORD	16-bits of data.
DWORD	32-bit data word.
QWORD	64-bit data word
Local bus	Internal Bus.
Outbound	At or toward the PCI interface of the ATU from the Internal Bus.
Inbound	At or toward the Internal Bus from the PCI interface of the ATU.
Core processor	Intel XScale® microarchitecture within the part.

Table 64. Terminology and Definitions (Sheet 3 of 3)

Term	Definition
Flip Chip	FC-BGA (flip chip-ball grid array) chip packages are designed with core flipped up on the back of the chip, facing away from the PCB. This allows more efficient cooling of the package.
Mode Conversion	Mode Conversions are due to imperfections on the interconnect which transform differential mode voltage to common mode voltage and common mode voltage to differential voltage.
ROMB	Raid on motherboard
ODT	On Die Termination - eliminates the need for termination resistors by placing the termination at the chip.

A.2 Right Angle Connector DDR2 Skews for Length Matching

Use Table 65 to compensate for the length differences for the right angle connector when performing length matching. Refer to Section 4.2.2.1 for additional information.

For example when compensating for the length difference between CB0, CB1 two choices either:

1. CB0 length is not adjusted but subtract 75 from CB1 length.
2. add a constant value of 285 to CB0 and a constant value of 210 to CB1

When chosen method was number 1 then the entire "Shorter by" column is used to compensate for length for the entire connector. When the choose method was number 2 then the entire "Longer by" column is used to compensate for length for the entire connector.

Note: The rows that are shaded in Table 65 are not critical signals and do not have to be length compensated.

Table 65. Right Angle Connector Skews (length matching compensation) (Sheet 1 of 7)

Connector Pin	Signal Name	Length Skews (choose one column below)	
		Shorter by (mils)	Longer by (mils)
42	CB0	0	285
43	CB1	75	210
48	CB2	0	285
49	CB3	75	210
161	CB4	285	0
162	CB5	210	75
167	CB6	285	0
168	CB7	210	75
185	CK0	285	0
186	CK0_N	210	75
137	CK1_RFU	285	0
138	CK1_RFU_N	210	75
220	CK2_RFU	210	75
221	CK2_RFU_N	285	0
125	DM0_DQS9	285	0
134	DM1_DQS10	210	75
146	DM2_DQS11	210	75
155	DM3_DQS12	285	0
202	DM4_DQS13	210	75
211	DM5_DQS14	285	0
223	DM6_DQS15	285	0
232	DM7_DQS16	210	75
164	DM8_DQS17	210	75
3	DQ0	75	210
4	DQ1	0	285

Table 65. Right Angle Connector Skews (length matching compensation) (Sheet 2 of 7)

Connector Pin	Signal Name	Length Skews (choose one column below)	
		Shorter by (mils)	Longer by (mils)
21	DQ10	75	210
22	DQ11	0	285
131	DQ12	285	0
132	DQ13	210	75
140	DQ14	210	75
141	DQ15	285	0
24	DQ16	0	285
25	DQ17	75	210
30	DQ18	0	285
31	DQ19	75	210
9	DQ2	75	210
143	DQ20	285	0
144	DQ21	210	75
149	DQ22	285	0
150	DQ23	210	75
33	DQ24	75	210
34	DQ25	0	285
39	DQ26	75	210
40	DQ27	0	285
152	DQ28	210	75
153	DQ29	285	0
10	DQ3	0	285
158	DQ30	210	75
159	DQ31	285	0
80	DQ32	0	285
81	DQ33	75	210
86	DQ34	0	285
87	DQ35	75	210
199	DQ36	285	0
200	DQ37	210	75
205	DQ38	285	0
206	DQ39	210	75
122	DQ4	210	75
89	DQ40	75	210
90	DQ41	0	285
95	DQ42	75	210
96	DQ43	0	285
208	DQ44	210	75
209	DQ45	285	0

Table 65. Right Angle Connector Skews (length matching compensation) (Sheet 3 of 7)

Connector Pin	Signal Name	Length Skews (choose one column below)	
		Shorter by (mils)	Longer by (mils)
214	DQ46	210	75
215	DQ47	285	0
98	DQ48	0	285
99	DQ49	75	210
123	DQ5	285	0
107	DQ50	75	210
108	DQ51	0	285
217	DQ52	285	0
218	DQ53	210	75
226	DQ54	210	75
227	DQ55	285	0
110	DQ56	0	285
111	DQ57	75	210
116	DQ58	0	285
117	DQ59	75	210
128	DQ6	210	75
229	DQ60	285	0
230	DQ61	210	75
235	DQ62	285	0
236	DQ63	210	75
129	DQ7	285	0
12	DQ8	0	285
13	DQ9	75	210
7	DQS0	75	210
6	DQS0_N	0	285
16	DQS1	0	285
15	DQS1_N	75	210
28	DQS2	0	285
27	DQS2_N	75	210
37	DQS3	75	210
36	DQS3_N	0	285
84	DQS4	0	285
83	DQS4_N	75	210
93	DQS5	75	210
92	DQS5_N	0	285
105	DQS6	75	210
104	DQS6_N	0	285
114	DQS7	0	285
113	DQS7_N	75	210

Table 65. Right Angle Connector Skews (length matching compensation) (Sheet 4 of 7)

Connector Pin	Signal Name	Length Skews (choose one column below)	
		Shorter by (mils)	Longer by (mils)
46	DQS8	0	285
45	DQS8_N	75	210
193	S0_N	285	0
76	S1_N	0	285
188	A0	210	75
183	A1	285	0
70	A10_AP	0	285
57	A11	75	210
176	A12	210	75
196	A13	210	75
174	A14	210	75
173	A15	285	0
54	A16_BA2	0	285
63	A2	75	210
182	A3	210	75
61	A4	75	210
60	A5	0	285
180	A6	210	75
58	A7	0	285
179	A8	285	0
177	A9	285	0
71	BA0	75	210
190	BA1	210	75
74	CAS_N	0	285
52	CKE0	0	285
171	CKE1	285	0
135	NC_DQS10_N	285	0
147	NC_DQS11_N	285	0
156	NC_DQS12_N	210	75
203	NC_DQS13_N	285	0
212	NC_DQS14_N	210	75
224	NC_DQS15_N	210	75
233	NC_DQS16_N	285	0
165	NC_DQS17_N	285	0
126	NC_DQS9_N	210	75
19	NC0	75	210
68	NC1	0	285
102	NC2	0	285
195	ODT0	285	0

Table 65. Right Angle Connector Skews (length matching compensation) (Sheet 5 of 7)

Connector Pin	Signal Name	Length Skews (choose one column below)	
		Shorter by (mils)	Longer by (mils)
77	ODT1	75	210
192	RAS_N	210	75
55	RC0	75	210
18	RESET_N	0	285
239	SA0	285	0
240	SA1	210	75
101	SA2	75	210
120	SCL	0	285
119	SDA	75	210
53	VDD0	75	210
59	VDD1	75	210
197	VDD10	285	0
64	VDD2	0	285
67	VDD3	75	210
69	VDD4	75	210
172	VDD5	210	75
178	VDD6	210	75
184	VDD7	210	75
187	VDD8	285	0
189	VDD9	285	0
194	VDDQ0	210	75
51	VDDQ1	75	210
191	VDDQ10	285	0
56	VDDQ2	0	285
62	VDDQ3	0	285
72	VDDQ4	0	285
75	VDDQ5	75	210
78	VDDQ6	0	285
170	VDDQ7	210	75
175	VDDQ8	285	0
181	VDDQ9	285	0
238	VDDSPD	210	75
1	VREF	75	210
2	VSS0	0	285
5	VSS1	75	210
32	VSS10	0	285
35	VSS11	75	210
38	VSS12	0	285
41	VSS13	75	210

Table 65. Right Angle Connector Skews (length matching compensation) (Sheet 6 of 7)

Connector Pin	Signal Name	Length Skews (choose one column below)	
		Shorter by (mils)	Longer by (mils)
44	VSS14	0	285
47	VSS15	75	210
50	VSS16	0	285
65	VSS17	75	210
66	VSS18	0	285
79	VSS19	75	210
8	VSS2	0	285
82	VSS20	0	285
85	VSS21	75	210
88	VSS22	0	285
91	VSS23	75	210
94	VSS24	0	285
97	VSS25	75	210
100	VSS26	0	285
103	VSS27	75	210
106	VSS28	0	285
109	VSS29	75	210
11	VSS3	75	210
112	VSS30	0	285
115	VSS31	75	210
118	VSS32	0	285
121	VSS33	285	0
124	VSS34	210	75
127	VSS35	285	0
130	VSS36	210	75
133	VSS37	285	0
136	VSS38	210	75
139	VSS39	285	0
14	VSS4	0	285
142	VSS40	210	75
145	VSS41	285	0
148	VSS42	210	75
151	VSS43	285	0
154	VSS44	210	75
157	VSS45	285	0
160	VSS46	210	75
163	VSS47	285	0
166	VSS48	210	75
169	VSS49	285	0

Table 65. Right Angle Connector Skews (length matching compensation) (Sheet 7 of 7)

Connector Pin	Signal Name	Length Skews (choose one column below)	
		Shorter by (mils)	Longer by (mils)
17	VSS5	75	210
198	VSS50	210	75
201	VSS51	285	0
204	VSS52	210	75
207	VSS53	285	0
210	VSS54	210	75
213	VSS55	285	0
216	VSS56	210	75
219	VSS57	285	0
222	VSS58	210	75
225	VSS59	285	0
20	VSS6	0	285
228	VSS60	210	75
231	VSS61	285	0
234	VSS62	210	75
237	VSS63	285	0
23	VSS7	75	210
26	VSS8	0	285
29	VSS9	75	210
73	WE_N	75	210

A.3 Simulation Conditions

This section provides the simulation conditions that were used in the analysis for each of the interfaces.

A.3.1 DDR2 Simulation Conditions

The following list provides the DDR2 simulation conditions used in this analysis:

- Motherboard 50 ohm single ended impedance stackup +/- 15% tolerance and 60 ohm single ended impedance stackup +/- 15%
- Motherboard clock target differential impedance 85 ohms +/- 15% and adapter card differential impedance of 100 ohms +/- 15%
- One Die Termination - ODT value of 75W was assumed for all DDR2 simulations.
- Generic DDR2 memory model
- DIMM models and topologies used the JEDEC model as a reference.
- JEDEC standard recommendations were used as a reference.
- Vias are modeled for all topologies with equal number of vias for differential pairTiming analysis was conducted.
- ISI Pattern was simulated.
- Signal Quality analysis covered for Rising flight time, Falling flight time, Low to high ring-back (noise margin high), High to Low ring-back (noise margin Low), and Low and High Overshoot.
- Frequency: 266MHz (DDR2 533MT/s)
- DIMM card microstrip routing is specified by JESD21-C.
- The ODT value used for simulations was 75Ω. Note that this value must be programmed for both the IOP and the SDRAM locations.
- Timing analysis was conducted.
- ISI Pattern was simulated.
- Signal Quality analysis covered for Rising flight time, Falling flight time, Low to high ring-back (noise margin high), High to Low ring-back (noise margin Low), and Low and High Overshoot.
- Frequency: 266MHz (DDR2 533MT/s)
- DIMM card microstrip routing is specified by JESD21-C.
- The ODT value used for simulations was 75Ω.. Note that this value must be programmed for both the IOP and the SDRAM locations.

A.3.2 DDR2 Simulation Conditions

The following list provides the DDR2 simulation conditions used in this analysis:

- Motherboard 50 ohm single ended impedance stackup +/- 15% tolerance and 60 ohm single ended impedance stackup +/- 15%
- Motherboard clock target differential impedance 85 ohms +/- 15% and adapter card differential impedance of 100 ohms +/- 15%
- One Die Termination - ODT value of 75Ω was assumed for all DDR2 simulations.
- Generic DDR2 memory model
- DIMM models and topologies used the JEDEC model as a reference.
- JEDEC standard recommendations were used as a reference.
- Vias are modeled for all topologies with equal number of vias for differential pair
- Timing analysis was conducted.
- ISI Pattern was simulated.
- Signal Quality analysis covered for Rising flight time, Falling flight time, Low to high ring-back (noise margin high), High to Low ring-back (noise margin Low), and Low and High Overshoot.
- Frequency: 266MHz (DDR2 533MT/s)
- DIMM card microstrip routing is specified by JESD21-C.
- The ODT value used for simulations was 75Ω. Note that this value must be programmed for both the IOP and the SDRAM locations.

A.3.3 PCI-X Simulation Conditions

The following list provides the PCI-X simulation conditions used in this analysis:

- Simulations were done for 133 MHz, 100 MHz and 66MHz.
- Various combinations of stripline and microstrip routing were analyzed.
- Vias and connectors were modeled using some estimated L and C parasitic values based on previous projects, or commonly used values from the literature.
- Connector Model: distributed PCI/PCI-X connector model
- PCI-X Package Model - Generic PCI-X spec device model
- SL Package Model: ball (RLC) + 1 via (RLC) + Stripline (W element) + 3 via + 1PTH (plated through hole RLC) + 4 via + 1 Ball.
- Motherboard trace: Impedance 50 ohm +/- 15% for stripline.
- Adapter Card Trace: Impedance 60 ohm +/- 15% for both microstrip and stripline.

A.3.4 SAS/SATA Simulation Conditions

The following list provides the SAS/SATA simulation conditions used in this analysis:

- Estimated Package parasitics were modeled as part of the topology.
- Power and ground parasitics are not included in the simulations.
- Stackups were set for nominal spacing, and then tolerance was applied to the line width (Spacing= nominal_line_pitch – actual_line_width).
- Various combinations of stripline and microstrip routing were analyzed.
- Vias and connectors were modeled using some estimated L and C parasitic values based on previous projects, or commonly used values from the literature.
- The HSPICE simulator was used to perform all simulation runs.
- SAS Package Model - package traces modeled using short transmission line segments and estimated minimum and maximum impedance values. Two package trace lengths were modeled, 0.1 inch and 0.75 inch.
- ISI Analysis -A test pattern was chosen that has been shown to be very close to worst case for ISI.

A.3.5 PCI Express Simulation Conditions

The following list provides the SAS simulation conditions used in this analysis:

- Jitter and insertion loss budgets used as per PCI Express Specifications
- AC coupling capacitors 75 nF with low ESL and ESR
- Both receiver and transmitter eyes were evaluated for the PCI Express mask specifications
- Modified worst case ISI pattern (8b/10b was used)
- Both near end and far end crosstalk were taken into consideration
- SSO simulated but the impact was found to be not significant.

A.3.6 PBI Simulation Conditions

The following list provides the PBI simulation conditions used in this analysis:

- System Board Stack up: 50 ohm +/- 15%, single ended impedance
- Add-In Card Stack up: 60 ohm +/- 15% single ended impedance
- Flash Model: RC128J3A
- Latch Model: 74LVC573A
- CPLD Model: XC9500XL TQFP package
- NVRAM Model: Same as Flash
- Lossy un-coupled transmission lines were used in simulations.
- Trace spacings were set to three times the height of the trace over the reference plane to avoid crosstalk
- Up to 200ns of cycles for AD lines are examined for every topology and are assumed to be equivalent to subsequent cycles.