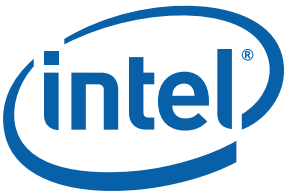

External Storage Design Schematics for Intel(R) 8134x I/O Processors

September 2006

Order Number: 315366-001US

Contents

September 2006
Order Number: 315366-001US

Revision History

Date	Revision	Description
September 2006	001	Initial release

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1.0 Schematics Overview

This manual provides the External Storage Design schematics for Intel(R) 8134x I/O Processors.

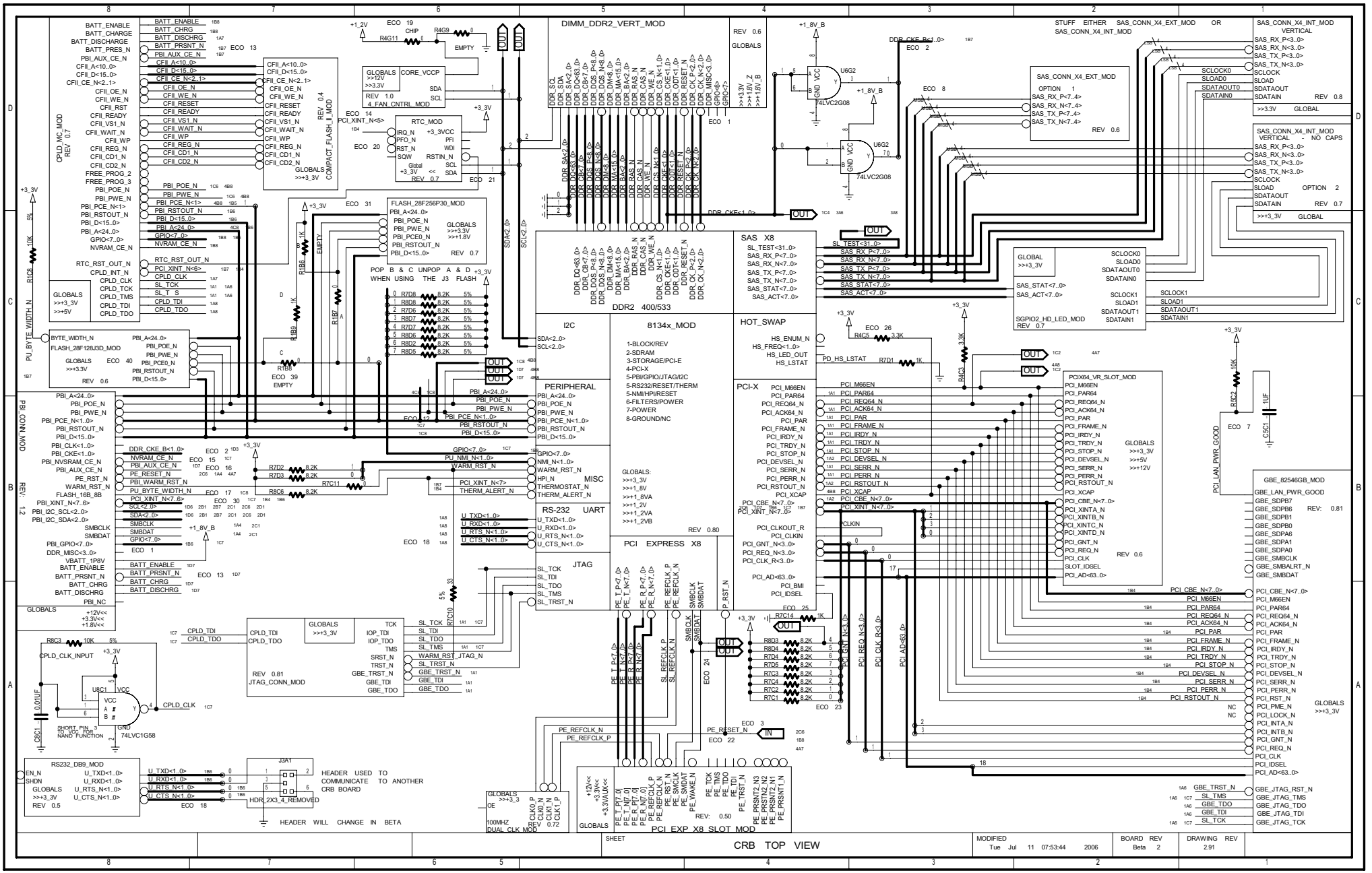
1.1 Product Descriptions

The products available from Intel in the 8134x family include:

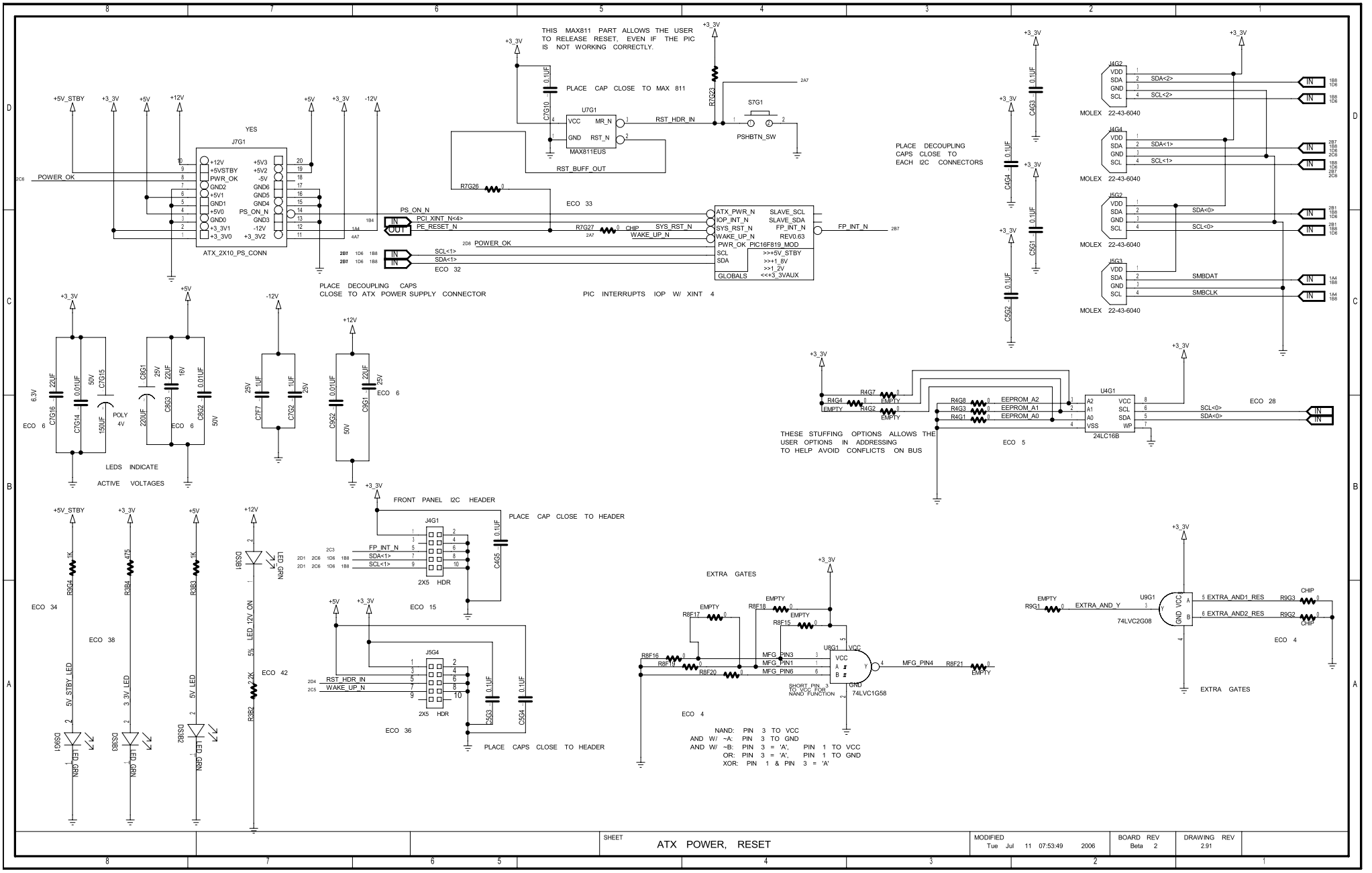
- Intel® 81348 I/O Processor-based host bus adapter with 8-port SAS/SATA controller.
- Intel® 81341 I/O Processor-based host bus adapter with one processing core.
- Intel® 81342 I/O Processor-based host bus adapter with two processing cores.
- Intel® 413808 I/O Controller-based host bus adapter with 8-port SAS/SATA controller and 800 MHz SAS engine
- Intel® 413812 I/O Controller-based host bus adapter with 8-port SAS/SATA controller and 1200 MHz SAS engine

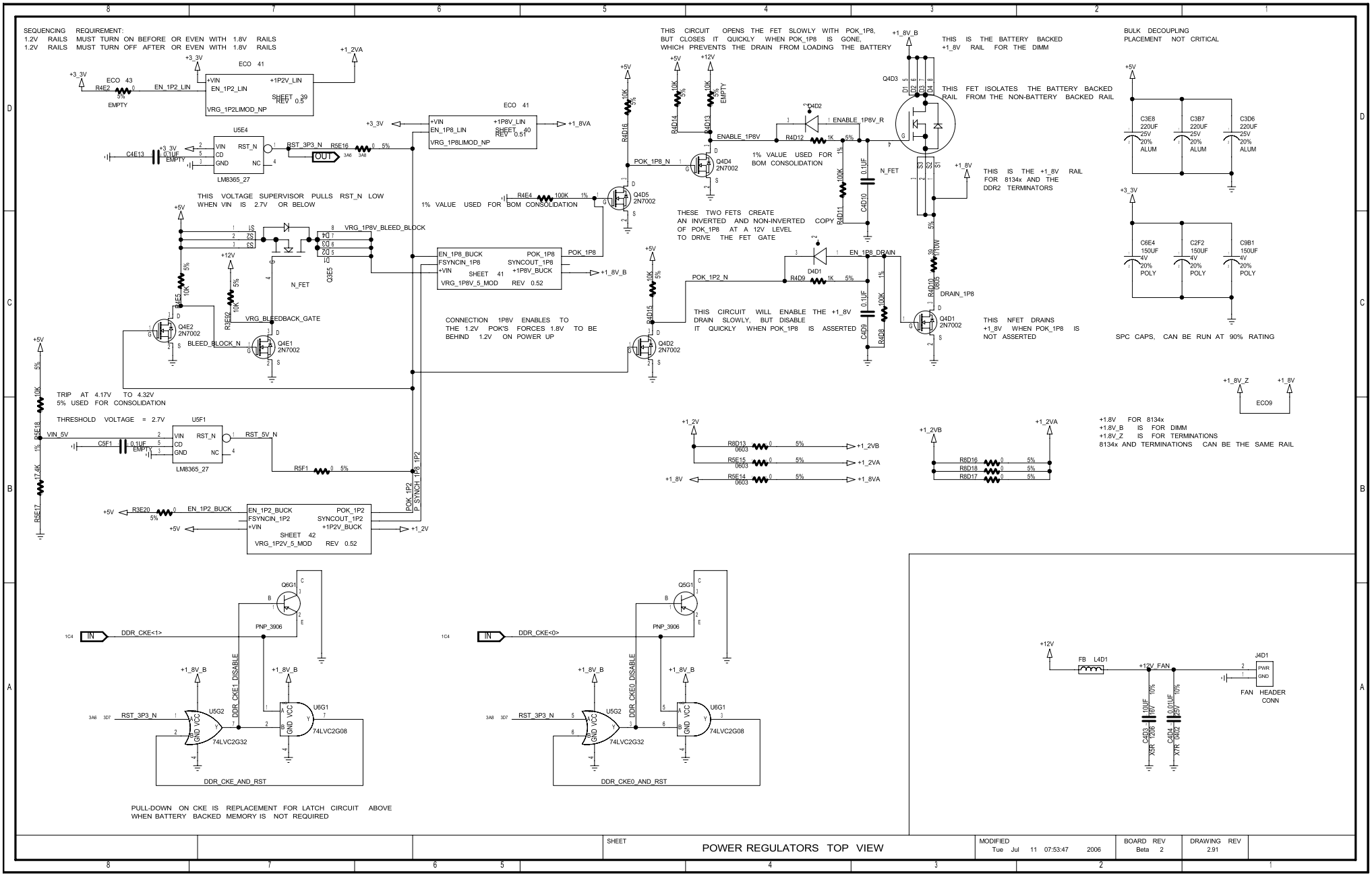
Note: The Intel® 81348 and Intel® 81341 and Intel® 81342 products are I/O Processors. The Intel® 413808 and Intel® 413812 products are I/O Controllers. In this manual for simplicity, we refer to all products as “processors”.

Contact your Intel Representative for more product information.



External Storage Design Schematics for Intel(R) 8134x I/O Processors
Order number: 315366-001US
8


THIS MAX811 PART ALLOWS THE USER TO RELEASE RESET, EVEN IF THE PIC IS NOT WORKING CORRECTLY.
PLACE CAP CLOSE TO MAX 811
MAX811EUS
RST_BUFF_OUT
PSHBTN_SW
RST_HDR_IN
ATX_2X10_PS_CONN
POWER_OK
PS_ON_N
PCI_XINT_N<4>
PE_RESET_N
SYS_RST_N
WAKE_UP_N
FP_INT_N
PIC16F819_MOD
SCL<1>
SDA<1>
ECO 32
ECO 33
PLACE DECOUPLING CAPS CLOSE TO ATX POWER SUPPLY CONNECTOR
PIC INTERRUPTS IOP W/ XINT 4
PLACE DECOUPLING CAPS CLOSE TO EACH I2C CONNECTORS
MOLEX 22-43-6040
SMBDAT
SMBCLK
LEDS INDICATE ACTIVE VOLTAGES
FRONT PANEL I2C HEADER
PLACE CAP CLOSE TO HEADER
2X5 HDR
PLACE CAPS CLOSE TO HEADER
EXTRA GATES
74LVC1G58
74LVC2G08
EEPROM_A2
EEPROM_A1
EEPROM_A0
24LC16B
THESE STUFFING OPTIONS ALLOWS THE USER OPTIONS IN ADDRESSING TO HELP AVOID CONFLICTS ON BUS
ECO 5
ECO 28
NAND: PIN 3 TO VCC
AND W/ ~A: PIN 3 TO GND
AND W/ ~B: PIN 3 = 'A', PIN 1 TO VCC
OR: PIN 3 = 'A', PIN 1 TO GND
XOR: PIN 1 & PIN 3 = 'A'
SHEET
ATX POWER, RESET
MODIFIED
Tue Jul 11 07:53:49 2006
BOARD REV
Beta 2
DRAWING REV
2.91



External Storage Design Schematics for Intel(R) 8134x I/O Processors
Order number: 315366-001US
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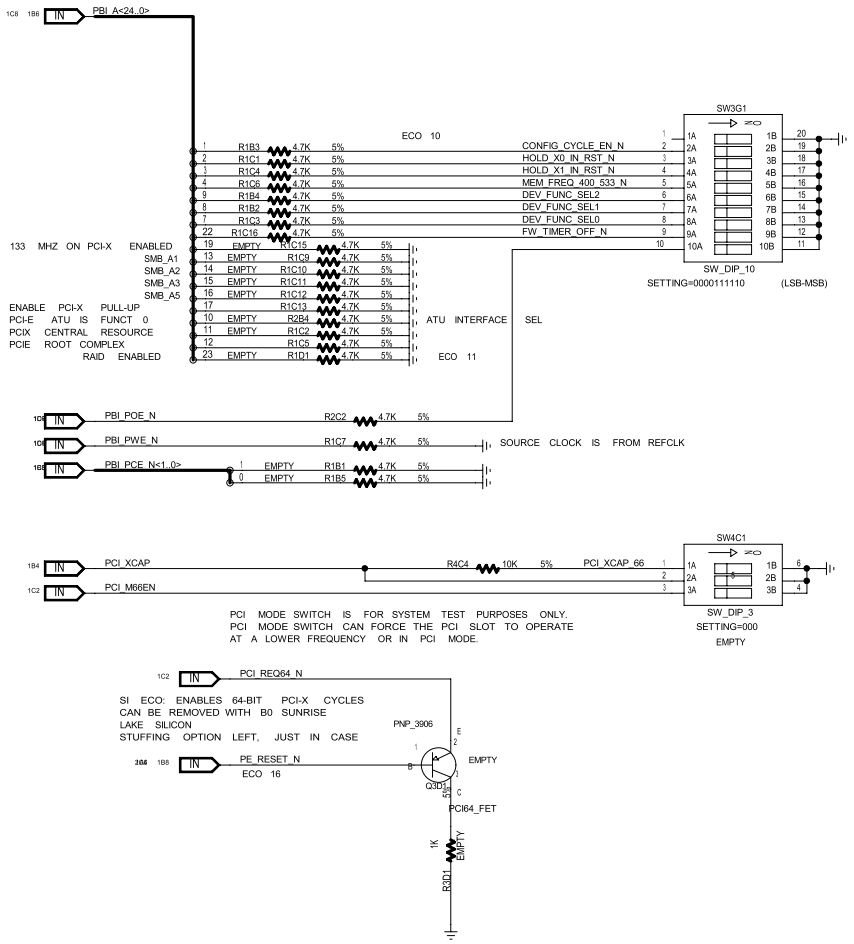


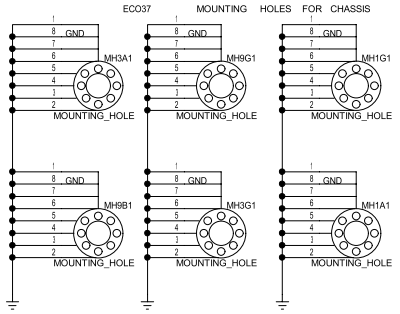
SWITCH SETTINGS

10 POSITION SWITCH

SWITCH #	ON	OFF
1	NOT CONNECTED	NOT CONNECTED
2	PCI CONFIGURATION ENABLED	PCI CONFIGURATION DISABLED (RETRY)
3	HOLD CPU X0 IN RESET	X0 CPU ACTIVE AFTER RESET
4	HOLD CPU X1 IN RESET	X1 CPU ACTIVE AFTER RESET
5	533 MHZ DDRII SDRAM INTERFACE	400 MHZ DDRII SDRAM INTERFACE
6	6 ON, 7 ON, 8 ON = ATU: 8 PORTS, TPMI: 0 PORTS	6 OFF, 7 ON, 8 ON = ATU: 4 PORTS, TPMI: 4 PORTS
7	6 ON, 7 ON, 8 OFF = ATU: 7 PORTS, TPMI: 1 PORT	6 OFF, 7 OFF, 8 OFF = ATU: 0 PORTS, TPMI: 8 PORTS
8	6 ON, 7 OFF, 8 ON = ATU: 6 PORTS, TPMI: 2 PORTS	ALL OTHER DEVICE FUNCTION SELECT CONFIGS RESERVED
9	FIRMWARE TIMER DISABLED	FIRMWARE TIMER ENABLED
10	RESERVED	DEFAULT

3 POSITION SWITCH - PCI MODE

SWITCH #			MAXIMUM PCI BUS SPEED
1	2	3	
ANY	ON	ON	PCI 33 MHZ MODE
ANY	ON	OFF	PCI 66MHZ MODE
ON	OFF	ANY	PCI-X 66MHZ MODE
OFF	OFF	ANY	PCI-X 100/133MHZ MODE



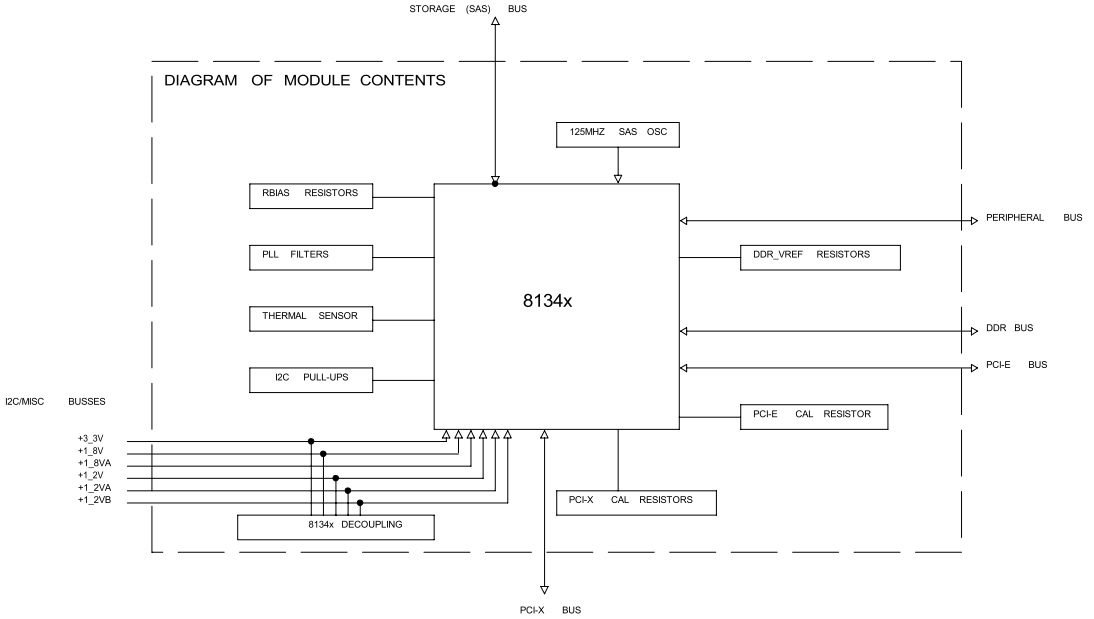
		SHEET: DIP SWITCHES	MODIFIED: Tue Jul 11 07:53:51 2006	BOARD REV: Beta 2	DRAWING REV: 2.91

8134x MODULE

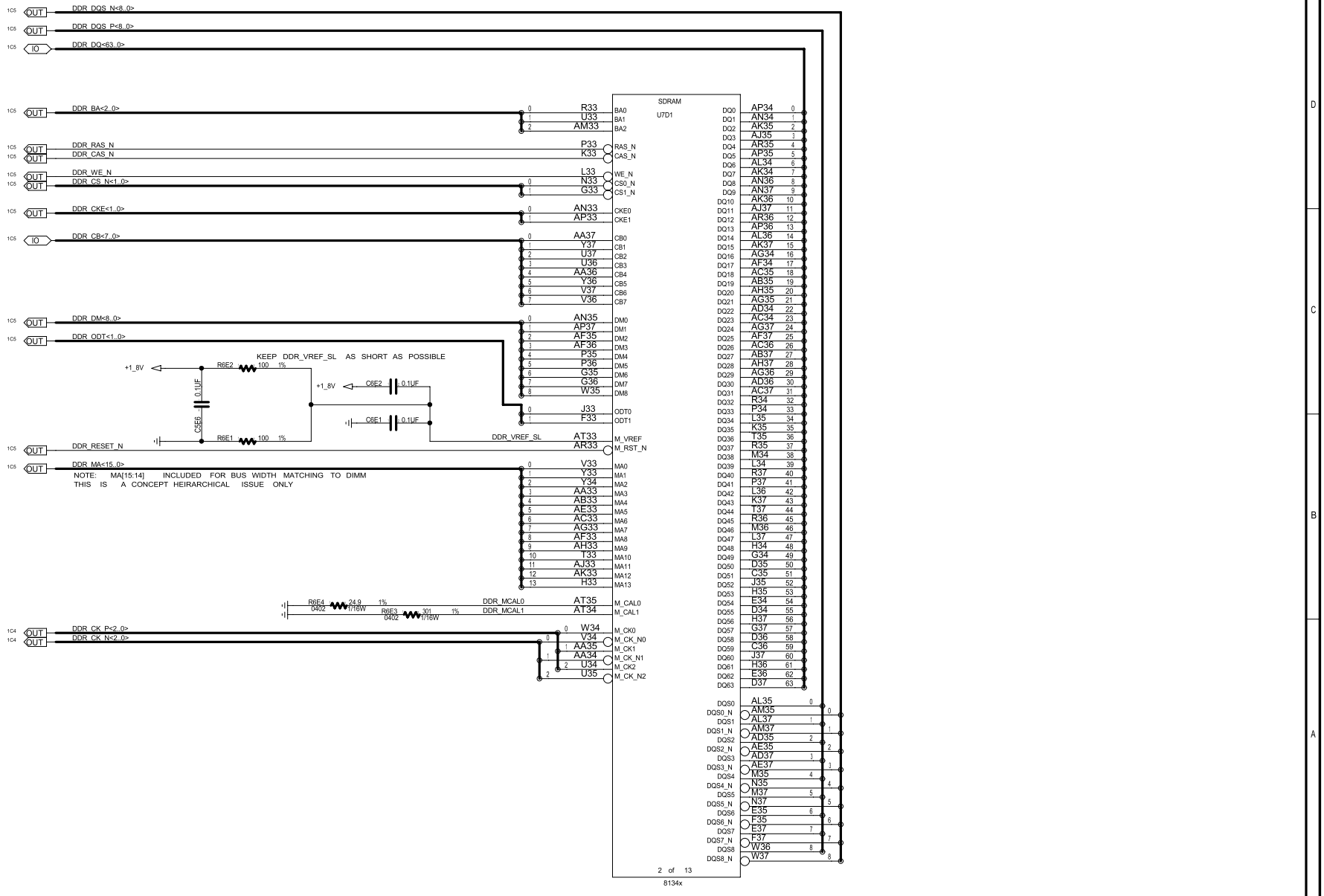
2 - SDRAM
3 - STORAGE/PCI-EXPRESS
4 - PCI-X BUS
5 - PERIPHERAL BUS/MISC
6 - POWER/FILTERS
7 - POWER
8 - GROUND/NO CONNECTS

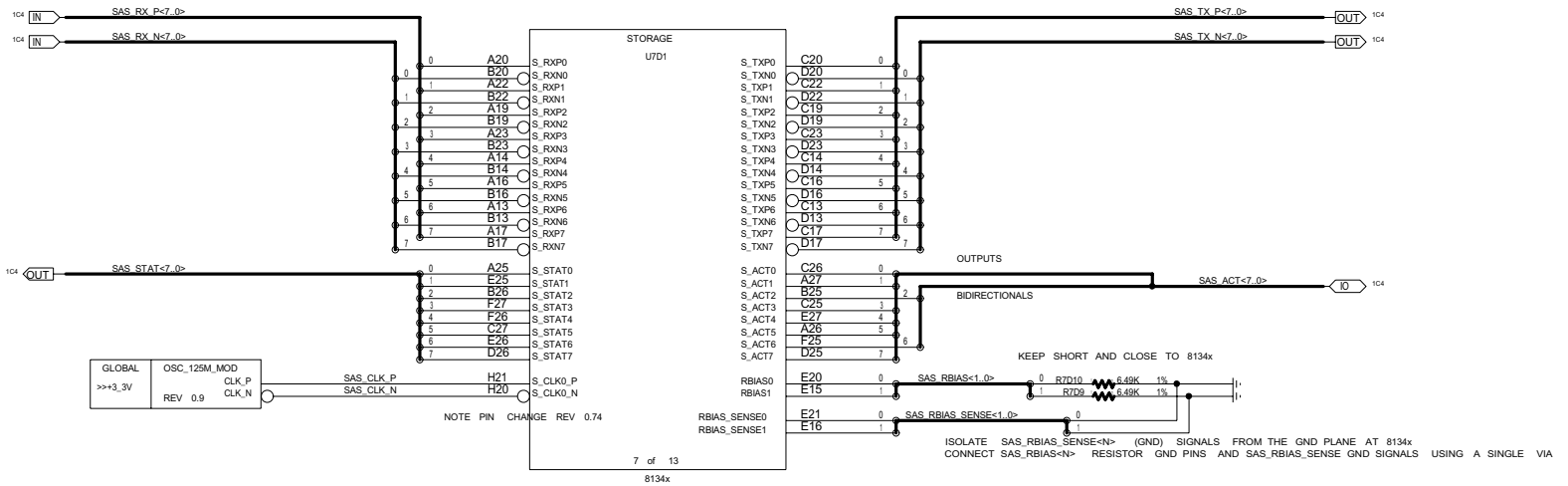
REVISIONS

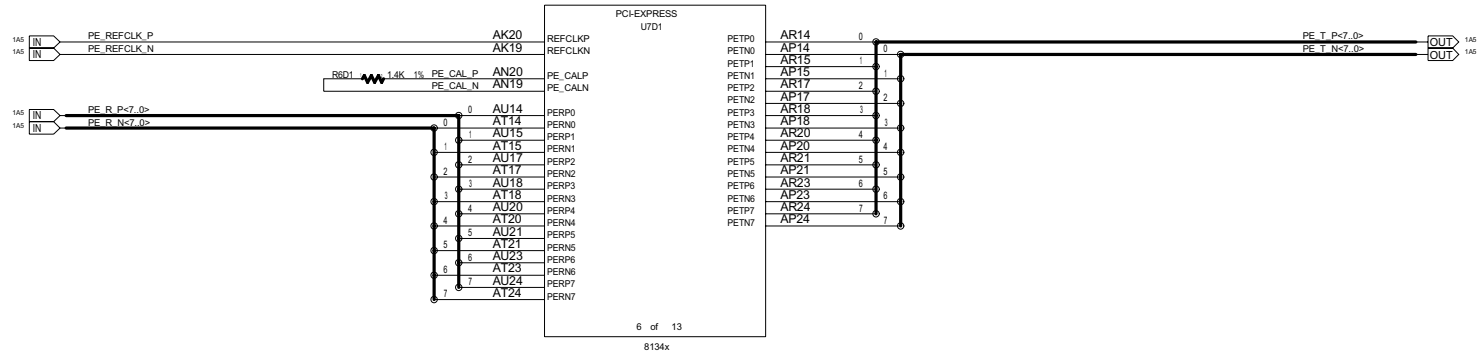
0.3 - SEP 18: PINOUT CHANGES INCORPORATED
0.4 - SEP 29: PORT NAME CHANGES, CORRECT DDR CLOCK SWAPPING
0.5 - SEP 29: RELEASE FOR CHECK
0.51- OCT 01: PCI_REQ64 -> PCI_REQ64_N
0.52- OCT 05: MOST OF THE BLOCK REVIEW FEEDBACK INC.
0.53- OCT 12: FIX REQ0 AND GNT0 DIRECTIONS
0.54 OCT 12: RESIZED MODULE SYMBOL
0.55 OCT 19: REMOVED SOME DECOUPLING, CHANGED SOME TO 0603
0.56 OCT 28: CHANGED DDR_MCAL1 SIZE TO 0402
0.57 OCT 29: ADDED PULLUPS ON SMB SIGNALS AND WARM_RST_N
0.58 NOV 1: ADJUSTED DECOUPLING TO NEW RECOMMENDATIONS
0.59 NOV 10: ADDED SL_TEST<31..0>
0.60 DEC 9: CHANGED 4.7NH IND TO -024
0.70 DEC 14: ADDED PCI_CLKOUT_R AND PCI_CLKIN
MOVED P_RST_N PIN, FIXED TABLE OF CONTENTS
0.71 JAN 7: ADDED 5PF CAP TO PCI_CLKIN
GROUNDED VSSPLLS0 AND VSSPLLS1
CHANGED PIN AN8 TO PUR1
CHANGED I2C PULLUPS TO 3.3K
0.72 FEB 28: ECO8: RENAMED VECTORED NETS TO HAVE VECTOR LAST
0.73 MAR 08: RENAMED PLL_VCC13P3_L_X NET TO PLL_VCC3P3_L_X
CHANGED 14 DECOUPLING CAPS TO EMPTY (NOT POPULATED)
0.74 APR 11: RENAMED S_CLK_N/P TO S_CLK0_N/P, SWAPPED ASSIGNMENTS OF PINS
H15 WITH H20(S_CLK0_N WITH VSS) AND H16 WITH H21 (S_CLK0_P WITH VSS)
0.75 OCT 14: UPGRADED IOP TO A1 IPN
0.76 DEC 23: DEPOPULATED P_CLKIN CAP
ADDED PULL-DOWN RESISTOR OPTION TO PUR1 PIN
0.80 FEB 10: MODIFIED SL PART FOR 800MHZ B0 VERSION



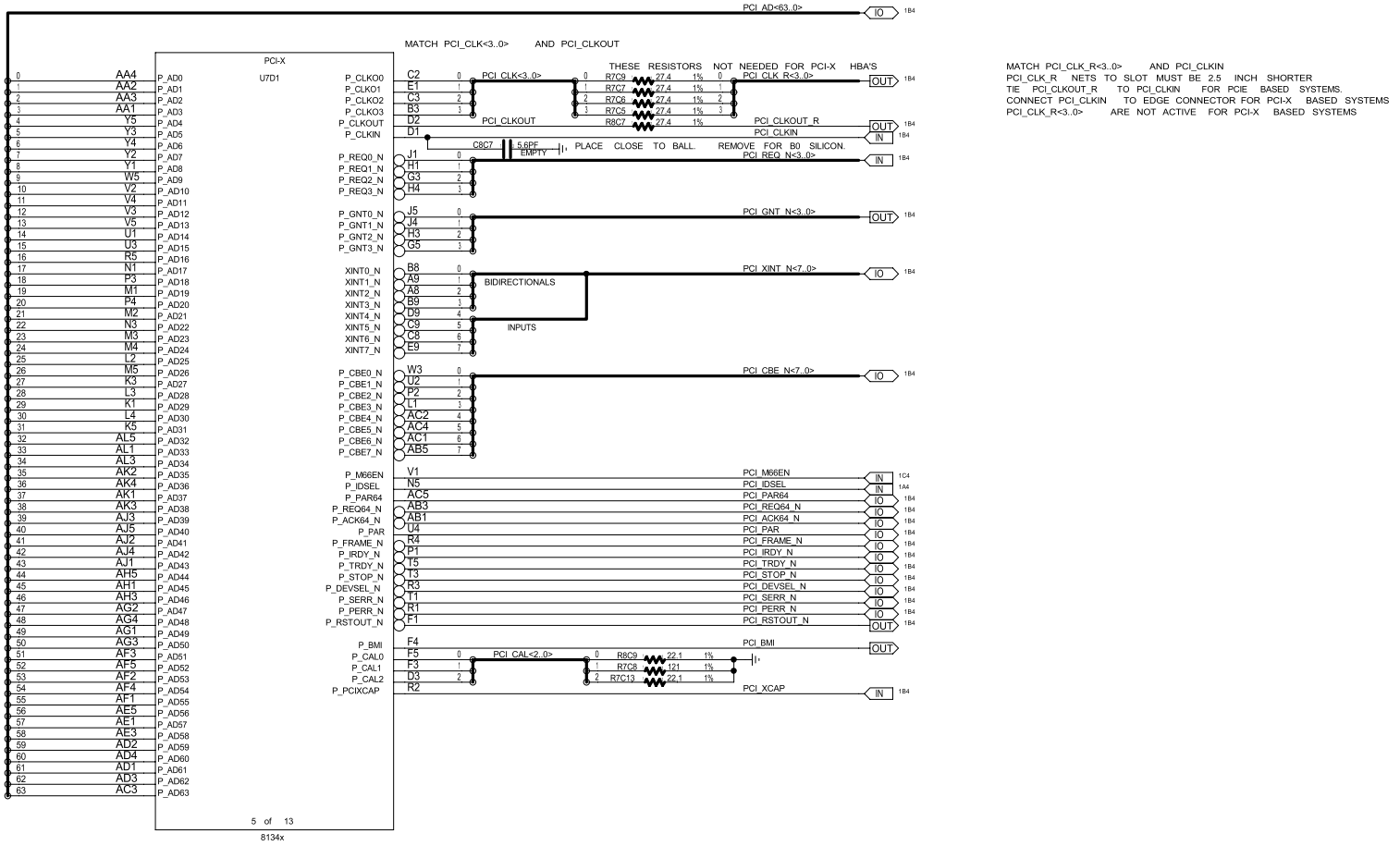
			SHEET	8134x MODULE CONTENTS	MODIFIED	BOARD REV	DRAWING REV	
					Fri Feb 10 08:54:38 2006	Beta 2	2.91	


DDR_DQS_N<8..0>
DDR_DQS_P<8..0>
DDR_DQ<63..0>
DDR_BA<2..0>
DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_CS_N<1..0>
DDR_CKE<1..0>
DDR_CB<7..0>
DDR_DM<8..0>
DDR_ODT<1..0>
KEEP DDR_VREF_SL AS SHORT AS POSSIBLE
+1_8V
R6E2 100 1%
R6E1 100 1%
C6E2 0.1UF
C6E1 0.1UF
C5E6 0.1UF
DDR_VREF_SL
DDR_RESET_N
DDR_MA<15..0>
NOTE: MA[15:14] INCLUDED FOR BUS WIDTH MATCHING TO DIMM
THIS IS A CONCEPT HEIRARCHICAL ISSUE ONLY
R6E4 24.9 1% 0402 1/16W
R6E3 301 1% 0402 1/16W
DDR_MCAL0
DDR_MCAL1
DDR_CK_P<2..0>
DDR_CK_N<2..0>
SDRAM
U7D1
BA0
BA1
BA2
RAS_N
CAS_N
WE_N
CS0_N
CS1_N
CKE0
CKE1
CB0
CB1
CB2
CB3
CB4
CB5
CB6
CB7
DM0
DM1
DM2
DM3
DM4
DM5
DM6
DM7
DM8
ODT0
ODT1
M_VREF
M_RST_N
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
MA12
MA13
M_CAL0
M_CAL1
M_CK0
M_CK_N0
M_CK1
M_CK_N1
M_CK2
M_CK_N2
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
DQ40
DQ41
DQ42
DQ43
DQ44
DQ45
DQ46
DQ47
DQ48
DQ49
DQ50
DQ51
DQ52
DQ53
DQ54
DQ55
DQ56
DQ57
DQ58
DQ59
DQ60
DQ61
DQ62
DQ63
DQS0
DQS0_N
DQS1
DQS1_N
DQS2
DQS2_N
DQS3
DQS3_N
DQS4
DQS4_N
DQS5
DQS5_N
DQS6
DQS6_N
DQS7
DQS7_N
DQS8
DQS8_N
2 of 13
8134x
SHEET
8134x SDRAM
MODIFIED
Fri Feb 10 08:52:07 2006
BOARD REV
Beta 2
DRAWING REV
2.91

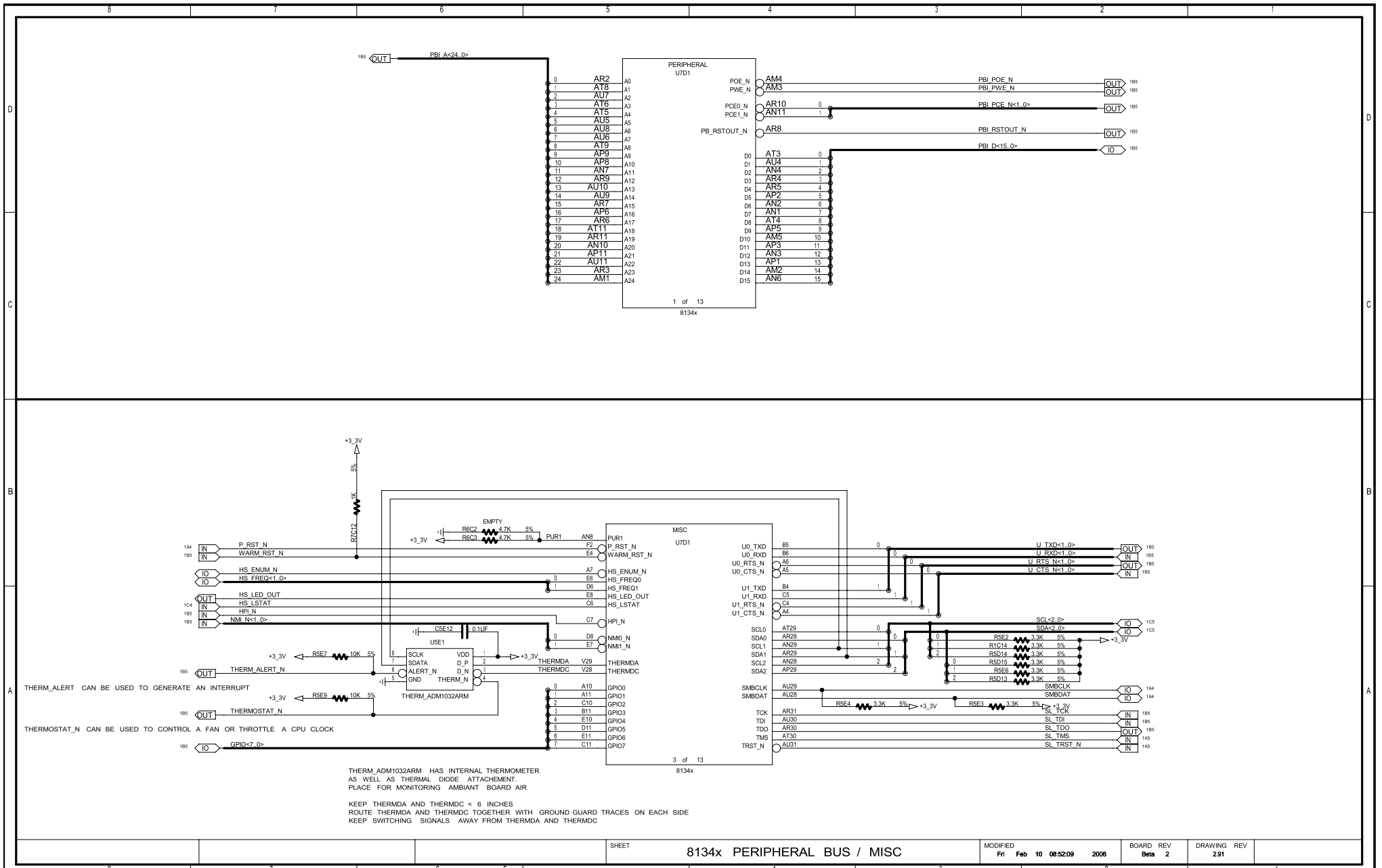


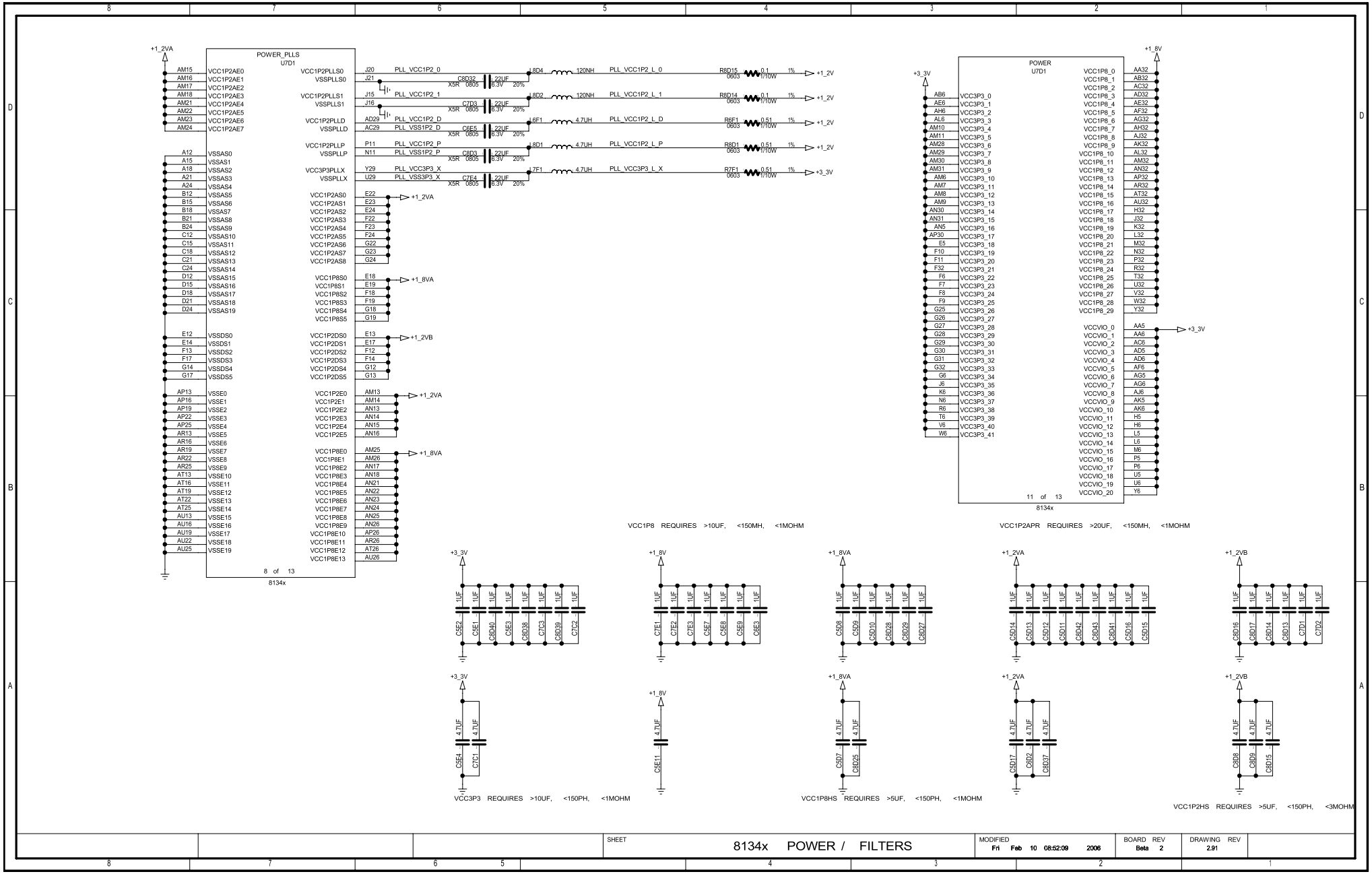


				SHEET		MODIFIED	BOARD REV	DRAWING REV
				8134x STORAGE / PCI-EXPRESS		Fri Feb 10 06:52:08 2006	Beta 2	2.91

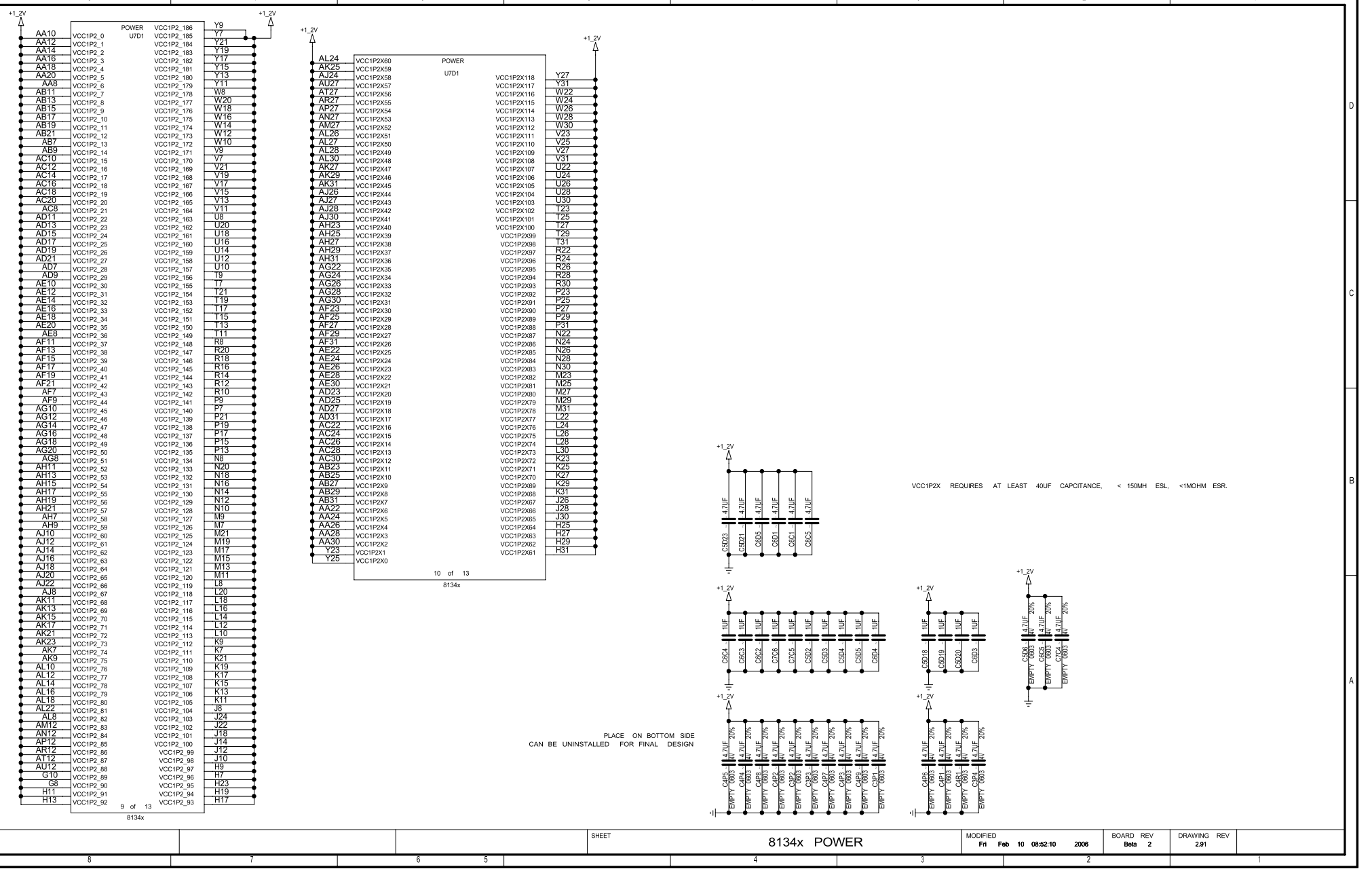


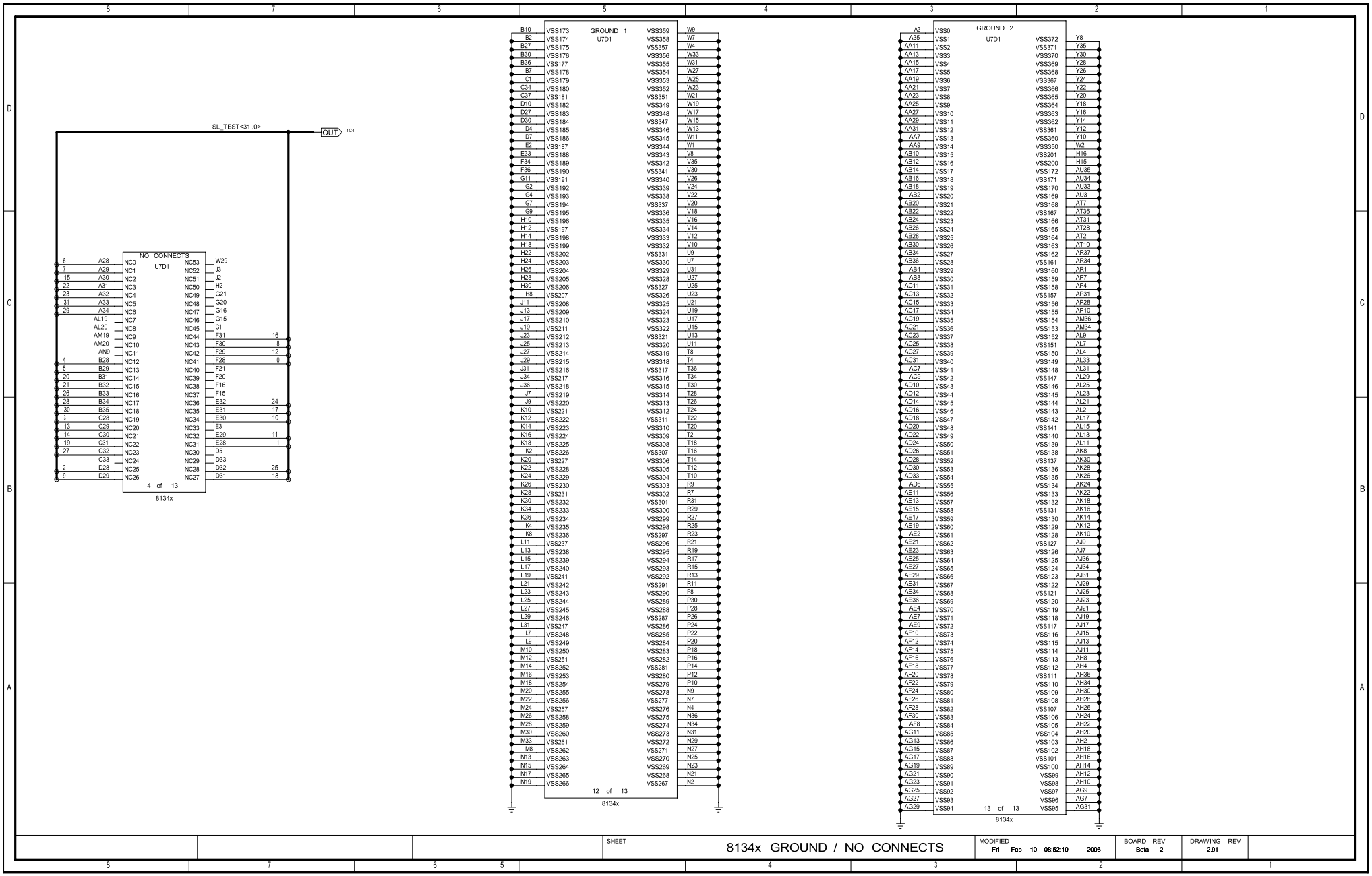
SHEET	MODIFIED	BOARD REV	DRAWING REV
8134x PCI-X BUS	Fri Feb 10 08:52:08 2006	Beta 2	2.91

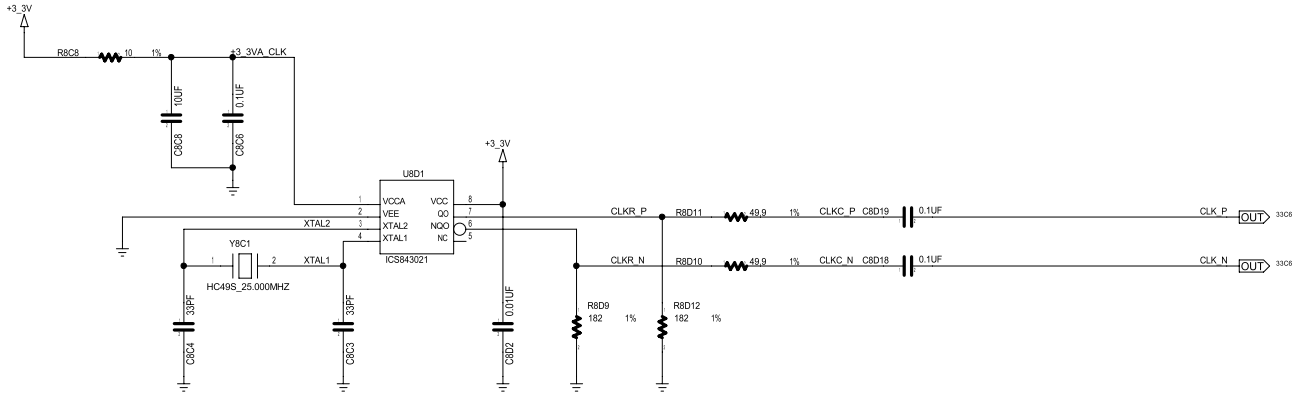

PERIPHERAL
U7D1
1 of 13
8134x
PBI_A<24..0>
PBI_POE_N
PBI_PWE_N
PBI_PCE_N<1..0>
PBI_RSTOUT_N
PBI_D<15..0>
MISC
U7D1
3 of 13
8134x
U5E1
THERM_ADM1032ARM
P_RST_N
WARM_RST_N
HS_ENUM_N
HS_FREQ<1..0>
HS_LED_OUT
HS_LSTAT
HPI_N
NMI_N<1..0>
THERM_ALERT_N
THERMOSTAT_N
GPIO<7..0>
U_TXD<1..0>
U_RXD<1..0>
U_RTS_N<1..0>
U_CTS_N<1..0>
SCL<2..0>
SDA<2..0>
SMBCLK
SMBDAT
SL_TDI
SL_TDO
SL_TMS
SL_TRST_N
SL_TCK
THERM_ALERT CAN BE USED TO GENERATE AN INTERRUPT
THERMOSTAT_N CAN BE USED TO CONTROL A FAN OR THROTTLE A CPU CLOCK
THERM_ADM1032ARM HAS INTERNAL THERMOMETER
AS WELL AS THERMAL DIODE ATTACHEMENT.
PLACE FOR MONITORING AMBIANT BOARD AIR
KEEP THERMDA AND THERMDC < 6 INCHES
ROUTE THERMDA AND THERMDC TOGETHER WITH GROUND GUARD TRACES ON EACH SIDE
KEEP SWITCHING SIGNALS AWAY FROM THERMDA AND THERMDC
SHEET
8134x PERIPHERAL BUS / MISC
MODIFIED
Fri Feb 10 08:52:09 2006
BOARD REV
Beta 2
DRAWING REV
2.91



External Storage Design Schematics for Intel(R) 8134x I/O Processors
Order number: 315366-001US
17


POWER
U7D1
9 of 13
8134x
POWER
U7D1
10 of 13
8134x
VCC1P2X REQUIRES AT LEAST 40UF CAPCITANCE, < 150MH ESL, <1MOHM ESR.
PLACE ON BOTTOM SIDE
CAN BE UNINSTALLED FOR FINAL DESIGN
SHEET
8134x POWER
MODIFIED
Fri Feb 10 08:52:10 2006
BOARD REV
Beta 2
DRAWING REV
2.91

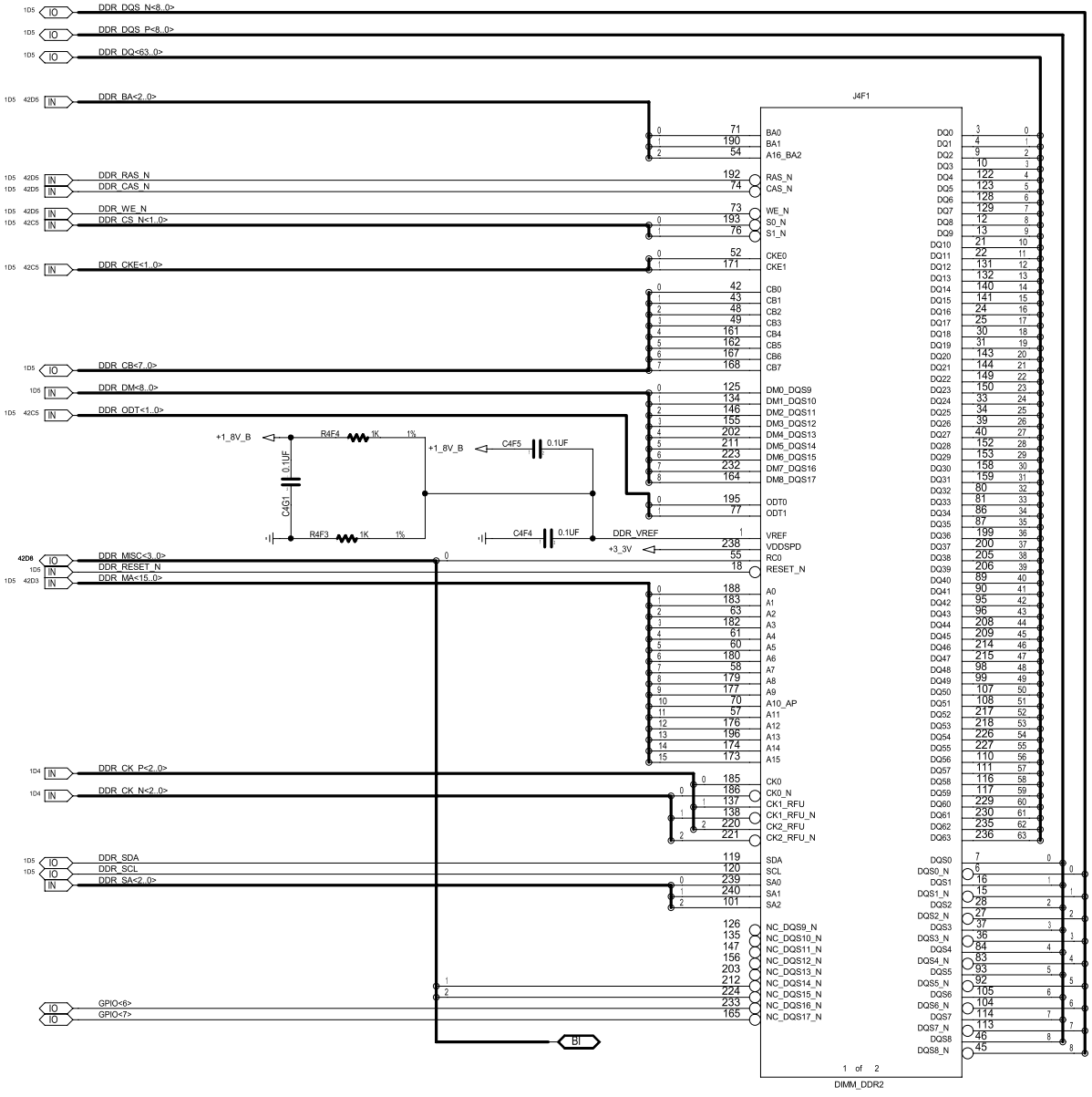

SL_TEST<31..0>
OUT
1C4
NO CONNECTS
U7D1
4 of 13
8134x
GROUND 1
U7D1
12 of 13
8134x
GROUND 2
U7D1
13 of 13
8134x
SHEET
8134x GROUND / NO CONNECTS
MODIFIED
Fri Feb 10 08:52:10 2006
BOARD REV
Beta 2
DRAWING REV
2.91



LAYOUT NOTES:
PLACE COMPONENTS AS CLOSE TO 843021 AS POSSIBLE.
SEE 843021 DATA SHEET FOR COMPONENT PLACEMENT EXAMPLE.
ROUTE CLK_P, CLK_N, CLKC_P, CLKC_N, CLKR_P, CLKR_N AS DIFFERENTIAL PAIRS.

REVISIONS
0.5: INITIAL RELEASE
0.6: CHANGED XTAL AND LOAD CAPACITOR TO MORE AVAILABLE COMPONENTS.
0.7: CHANGED SERIES CAPS TO COMMON PARTS, MADE REFDES HARD
0.8: CHANGED 10 OHM RESISTOR TO 0402.
0.9: CHANGED REFDES TO SOFT. ADDED DIFF PAIR LAYOUT NOTE.

			SHEET		MODIFIED	BOARD REV	DRAWING REV	
			DIFFERENTIAL OSCILLATOR 125 MHZ		Sun Apr 10 17:33:10 2005	Beta 2	2.91	


DDR_DQS_N<8..0>
DDR_DQS_P<8..0>
DDR_DQ<63..0>
DDR_BA<2..0>
DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_CS_N<1..0>
DDR_CKE<1..0>
DDR_CB<7..0>
DDR_DM<8..0>
DDR_ODT<1..0>
DDR_MISC<3..0>
DDR_RESET_N
DDR_MA<15..0>
DDR_CK_P<2..0>
DDR_CK_N<2..0>
DDR_SDA
DDR_SCL
DDR_SA<2..0>
GPIO<6>
GPIO<7>
+1_8V_B
R4F4 1K 1%
R4F3 1K 1%
C4G1 0.1UF
C4F5 0.1UF
C4F4 0.1UF
DDR_VREF
+3_3V
BI
J4F1
BA0
BA1
A16_BA2
RAS_N
CAS_N
WE_N
S0_N
S1_N
CKE0
CKE1
CB0
CB1
CB2
CB3
CB4
CB5
CB6
CB7
DM0_DQS9
DM1_DQS10
DM2_DQS11
DM3_DQS12
DM4_DQS13
DM5_DQS14
DM6_DQS15
DM7_DQS16
DM8_DQS17
ODT0
ODT1
VREF
VDDSPD
RC0
RESET_N
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10_AP
A11
A12
A13
A14
A15
CK0
CK0_N
CK1_RFU
CK1_RFU_N
CK2_RFU
CK2_RFU_N
SDA
SCL
SA0
SA1
SA2
NC_DQS9_N
NC_DQS10_N
NC_DQS11_N
NC_DQS12_N
NC_DQS13_N
NC_DQS14_N
NC_DQS15_N
NC_DQS16_N
NC_DQS17_N
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
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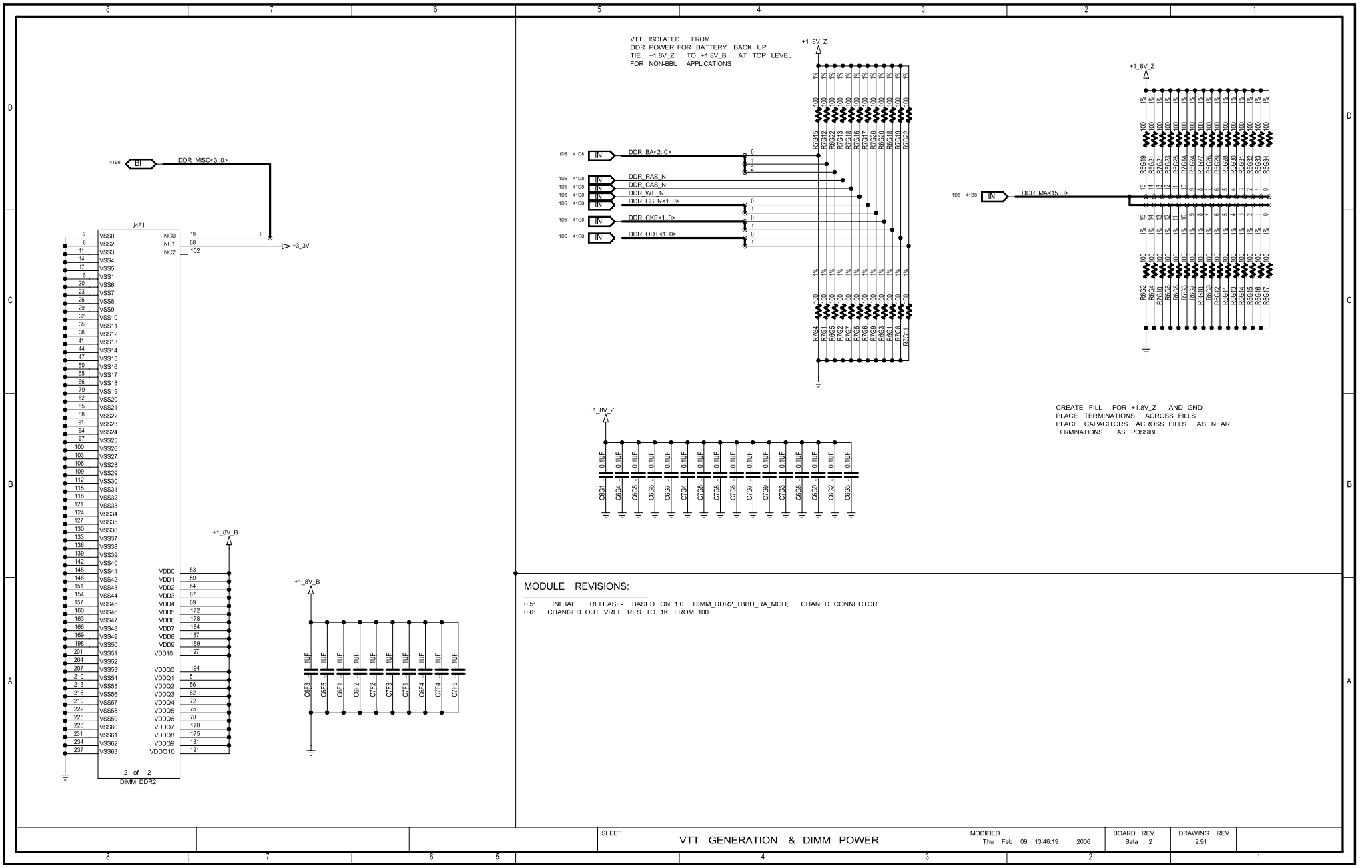
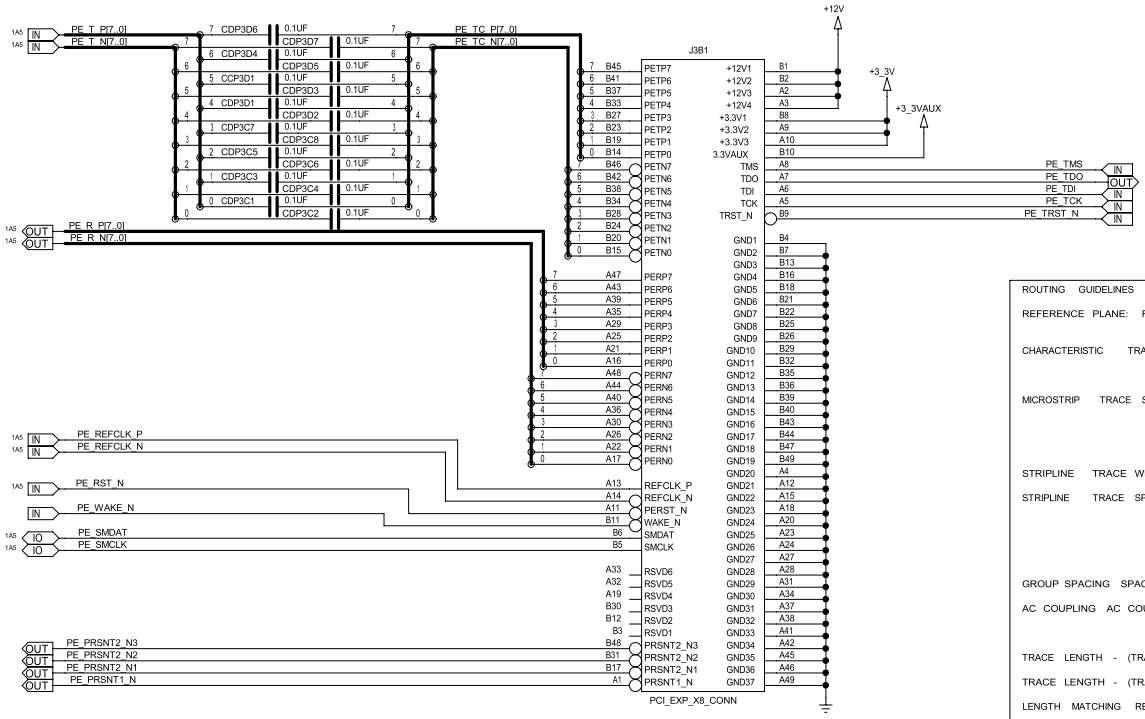
DQ56
DQ57
DQ58
DQ59
DQ60
DQ61
DQ62
DQ63
DQS0
DQS0_N
DQS1
DQS1_N
DQS2
DQS2_N
DQS3
DQS3_N
DQS4
DQS4_N
DQS5
DQS5_N
DQS6
DQS6_N
DQS7
DQS7_N
DQS8
DQS8_N
1 of 2
DIMM_DDR2
SHEET
DDR2 DIMM SOCKET
MODIFIED
Thu Feb 09 13:44:18 2006
BOARD REV
Beta 2
DRAWING REV
2.91


VTT ISOLATED FROM DDR POWER FOR BATTERY BACK UP TIE +1.8V_Z TO +1.8V_B AT TOP LEVEL FOR NON-BBU APPLICATIONS
+1_8V_Z
DDR_BA<2..0>
DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_CS_N<1..0>
DDR_CKE<1..0>
DDR_ODT<1..0>
DDR_MA<15..0>
BI
DDR_MISC<3..0>
+3_3V
J4F1
DIMM_DDR2
+1_8V_B
CREATE FILL FOR +1.8V_Z AND GND
PLACE TERMINATIONS ACROSS FILLS
PLACE CAPACITORS ACROSS FILLS AS NEAR TERMINATIONS AS POSSIBLE
MODULE REVISIONS:
0.5: INITIAL RELEASE- BASED ON 1.0 DIMM_DDR2_TBBU_RA_MOD, CHANED CONNECTOR
0.6: CHANGED OUT VREF RES TO 1K FROM 100
SHEET
VTT GENERATION & DIMM POWER
MODIFIED
Thu Feb 09 13:46:19 2006
BOARD REV
Beta 2
DRAWING REV
2.91



MODULE REVISIONS:

0.50: INITIAL RELEASE BASED ON PCI_EXP_X8_EDGE_MOD REV 0.53

ROUTING GUIDELINES

REFERENCE PLANE: ROUTING OVER UNBROKEN GROUND PLANE IS PREFERRED. IF UNBROKEN GROUND PLANE IS NOT AVAILABLE ROUTE OVER UNBROKEN VOLTAGE PLANE.

CHARACTERISTIC TRACE IMPEDANCE: SINGLE-ENDED: 50 OHMS +/- 15%
DIFFERENTIAL: 85 OHMS NOMINAL +/-15%
MICROSTRIP TRACE WIDTH 5 MILS (REFER TO TABLE NOTE)

MICROSTRIP TRACE SPACING
- BETWEEN + (P) AND - (N) OF PAIR: 7 MILS EDGE TO EDGE
- BETWEEN OTHER SIGNALS : > 25 MILS EDGE TO EDGE
- TRANSMIT AND RECEIVE PAIRS SHOULD BE INTERLEAVED. IF INTERLEAVING NOT POSSIBLE, THEN THE SPACING BETWEEN PAIRS (INTER PAIR) SHOULD BE INCREASED TO > 45 MILS (EDGE TO EDGE). EDGE TO EDGE OF INTER PAIR IS DEFINED AS EDGE OF POSITIVE OF ONE PAIR TO EDGE OF NEGATIVE OF THE NEXT PAIR OR VICE VERSA

STRIPLINE TRACE WIDTH 4 MILS

STRIPLINE TRACE SPACING
- BETWEEN + (P) AND - (N) OF PAIR: 6 MILS EDGE TO EDGE
- BETWEEN OTHER PAIRS : > 26 MILS EDGE TO EDGE
- TRANSMIT AND RECEIVE PAIRS SHOULD BE INTERLEAVED. IF INTERLEAVING NOT POSSIBLE, THEN INTER PAIR SPACING SHOULD BE INCREASED TO 46 MILS (EDGE TO EDGE). EDGE TO EDGE OF INTER PAIR IS DEFINED AS EDGE OF POSITIVE OF ONE PAIR TO EDGE OF NEGATIVE OF THE NEXT PAIR OR VICE VERSA

GROUP SPACING SPACING FROM OTHER GROUPS: > 20 MILS MINIMUM FROM EDGE TO EDGE FOR MICROSTRIP OR STRIPLINE.

AC COUPLING AC COUPLING CAPACITORS MUST BE LOCATED AT THE TRANSMITTER. REQUIRED VALUES OF 75 NF TO 200 NF.

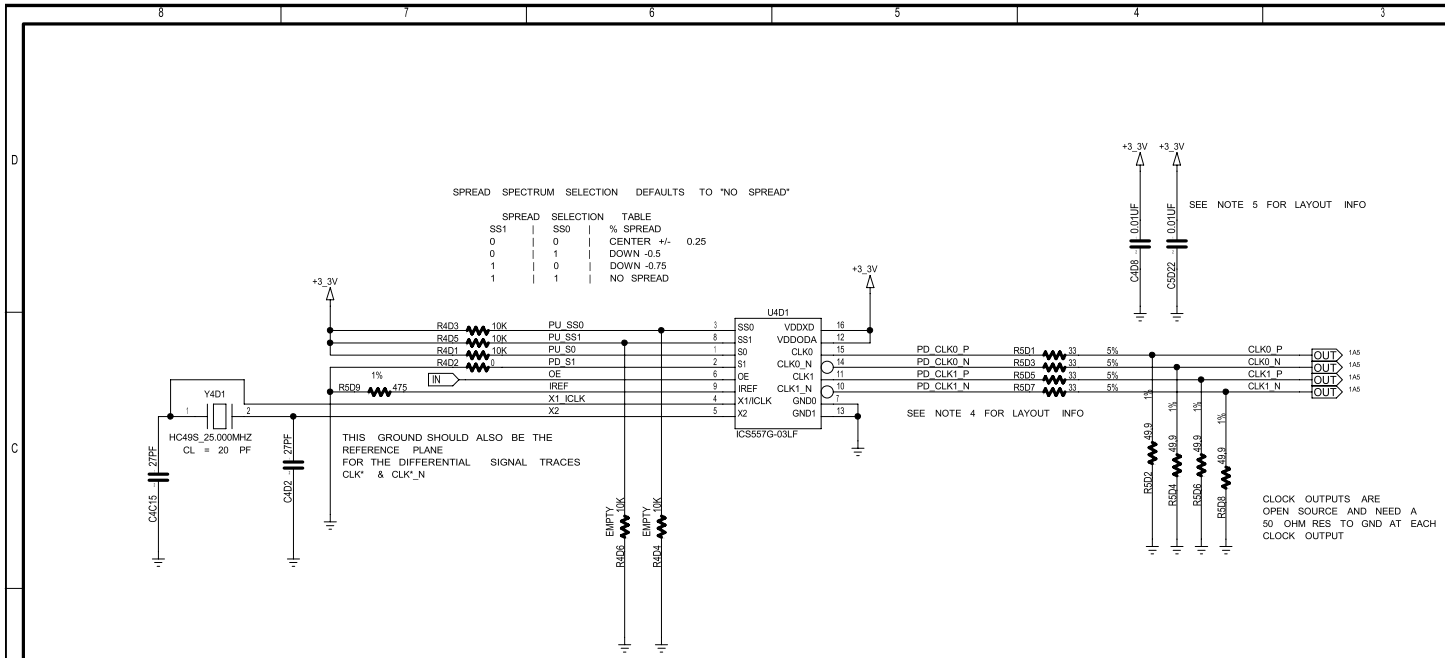
TRACE LENGTH - (TRANSMITTER/RECEIVER) DEVICE SIGNAL PIN TO AC COUPLING CAPACITOR 0.25ï MIN. - 11.0ï MAX

TRACE LENGTH - (TRANSMITTER/RECEIVER) FROM AC COUPLING CAPACITOR TO PCI EXPRESS CONNECTOR PIN 1.0ï MIN. - 13.85ï MAX

LENGTH MATCHING REQUIREMENTS
- TOTAL ALLOWABLE BETWEEN PAIR (LENGTH SKEW BETWEEN + AND - SIGNALS OF THE PAIR) LENGTH MISMATCH ON A SYSTEM BOARD MUST NOT EXCEED 10 MILS.
- LENGTH SHOULD BE MATCHED ON A SEGMENT BY SEGMENT BASIS.
- EACH ROUTING SEGMENT TO BE MATCHED AS CLOSE AS POSSIBLE.
- TOTAL SKEW ACROSS ALL LANES MUST BE LESS THAN 20 NS.

NUMBER OF VIAS 4 MAX

SHEET	MODIFIED	BOARD REV	DRAWING REV
PCI-EXPRESS EDGE CONNECTOR	Mon Aug 16 14:43:35 2006	Beta 2	2.91



REVISION HISTORY

0.1 INITIAL RELEASE
0.2 ADDED RESISTOR OPTION TO ADJUST SPREAD SPECTRUM CLOCKING
0.5 FIXED LAYOUT NOTES, ADDED 10K RESISTORS, FIXED SQUISHY TEXT
0.6 UPDATED NOTE 1, ADDED NOTE 7 AND CORRECTED SPREAD SPECTRUM TABLE.
0.7 PER ICS' RECOMMENDATIONS. CHANGED S1 RES FROM 10K TO 0 OHMS.
0.71 NET NAME CHANGE TO PD_S1
0.72 CHANGED OUT 33 OHM TOLERANCE TO 5% FOR LEAD-FREE CONVERSION.

NOTES:

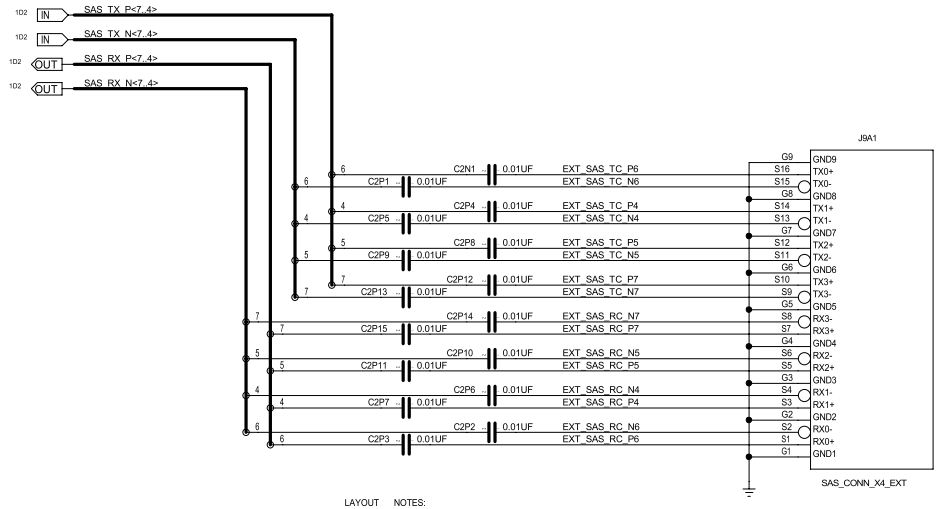
1) MODULE DESIGNED FOR NOMINAL SINGLE ENDED TRACE IMPEDANCE OF 50 OHMS.
2) OPTIMUM LAYOUT IS ONE WITH ALL COMPONENTS ON THE SAME SIDE OF THE BOARD
3) OTHER SIGNAL TRACES SHOULD BE ROUTED AWAY FROM THE ICS557-03. THIS INCLUDES SIGNALS TRACES JUST UNDERNEATH THE DEVICE, OR ON LAYERS ADJACENT TO THE GROUND PLANE LAYER USED BY THE DEVICE
4) LENGTH ROUTING FOR CLK* & CLK*_N ARE AS FOLLOWS:
   A) FROM ICS557-03 TO 33 OHM RES IS 0.5 INCH MAX
   B) FROM 33 OHM RES TO TOP OF 49.9 OHM RES IS 0.2 INCH MAX
   C) FROM 49.9 OHM RES TO GROUND IS 0.2 INCH MAX
   D) FROM TOP OF 49.9 OHM RES TO PCI EXPRESS CONNECTOR, ROUTE AS COUPLED 100 OHM DIFF TRACE
      IF USING MICROSTRIP: 0.25 MIN TO 14 INCH MAX
      ELSE IF USING STRIPLINE,: 0.225 MIN TO 12.6 INCH MAX
   E) FROM TOP OF 49.9 OHM RES TO COMPONENTS ON THE SAME PCB, ROUTE AS COUPLED 100 OHM DIFF TRACE
      IF USING MICROSTRIP: 2 MIN TO 16 INCH MAX
      ELSE IF USING STRIPLINE: 1.8 MIN TO 14.4 INCH MAX
5) DECOUPLING CAPS: PLACE CAPS AS CLOSE TO VDD AS POSSIBLE. ALSO KEEP TRACES AS SHORT AS POSSIBLE. NO VIAS SHOULD BE USED BETWEEN DECOUPLING CAPS & VDD PIN
6) MODULE IS HARD CODED TO OUTPUT 100 MHZ
7) OUTPUT ENABLE INPUT HAS INTERNAL 100K OHM PULLUP. DEFAULTS TO OUTPUT ENABLED IF LEFT UNCONNECTED

SHEET
100 MHZ DUAL DIFFERENTIAL CLOCK GENERATOR

MODIFIED
Fri Jan 27 09:38:32 2006

BOARD REV
Beta 2

DRAWING REV
2.91

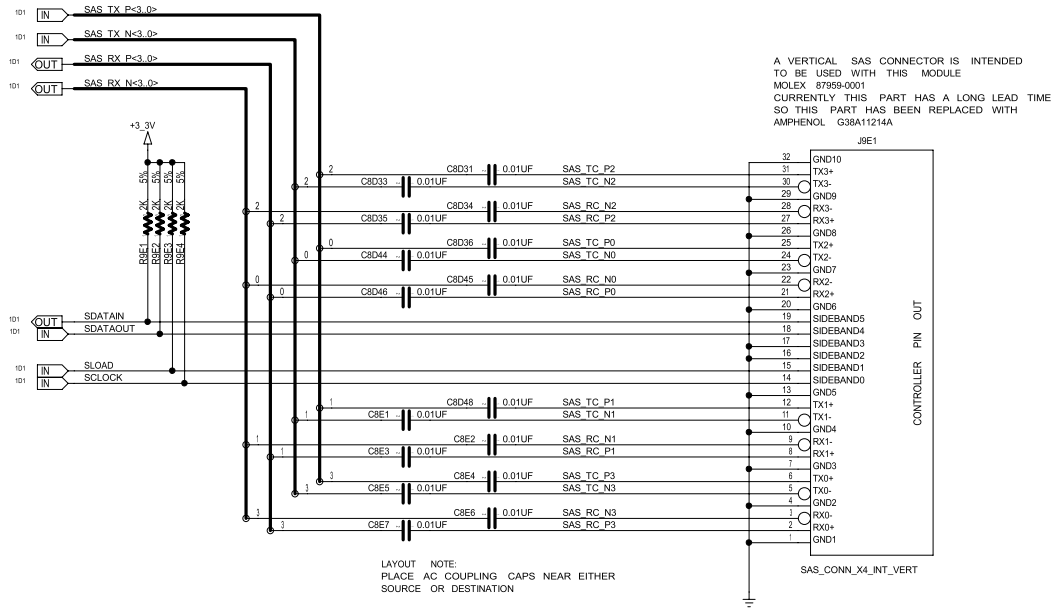


LAYOUT NOTES:
PLACE AC COUPLING CAPS NEAR EITHER SOURCE OR DESTINATION.

SAS LANES SWAPPED TO MINIMIZE VIAS.

REVISIONS
0.5: INITIAL RELEASE
0.6: FIXED BIT TAP SEQUENCING - BM

SHEET		MODIFIED	BOARD REV	DRAWING REV
SAS CONNECTOR X4 EXTERNAL		Sat Feb 25 16:06:42 2006	Beta 2	2.91



A VERTICAL SAS CONNECTOR IS INTENDED TO BE USED WITH THIS MODULE
MOLEX 87959-0001
CURRENTLY THIS PART HAS A LONG LEAD TIME SO THIS PART HAS BEEN REPLACED WITH AMPHENOL G38A11214A

LAYOUT NOTE:
PLACE AC COUPLING CAPS NEAR EITHER SOURCE OR DESTINATION

SAS SIGNALS FROM 8134x IO PROCESSOR TO X4 INTERNAL SAS CONNECTOR SWAPPED TO MINIMIZE VIAS. 8134x B0 WILL ENABLE REORDERING SGPIO TRANSMIT ORDER TO MATCH LANE SWAPS ON BOARD.

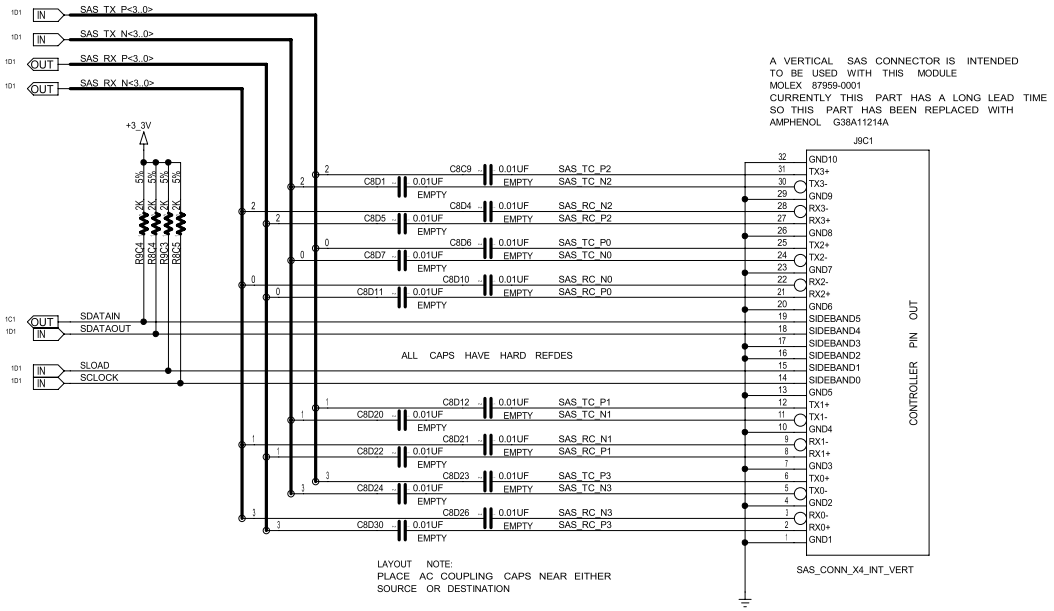
SAS LANE CONNECTIONS

8134x	X4 INTERNAL SAS CONNECTOR
LANE 0	LANE 2
LANE 1	LANE 1
LANE 2	LANE 3
LANE 3	LANE 0

REVISIONS
0.5: INITIAL RELEASE
0.6: SWAPPED SAS LANES TO IMPROVE ROUTING.
0.7: CHANGED OUT CONN FOR A VERTICAL ONE (HM)
0.71: TEMPORARY PART CHNAGE DUE TO AVAILABILITY (HM)
0.72: CORRECTED CONNECTOR ORIENTATION AND PIN CONNECTIONS (RP)
0.8: PART CHANGE: CONNECTOR NOW VERTICAL

SHEET	MODIFIED	BOARD REV	DRAWING REV
SAS CONNECTOR X4 INTERNAL - VERTICAL	Fri Sep 30 12:04:29 2005	Beta 2	2.91

REVISIONS
0.5: INITIAL RELEASE
0.6: HARD CODED REFDES FOR NO STUFF
0.7: PART CHANGED TO VERTICAL CONN



A VERTICAL SAS CONNECTOR IS INTENDED TO BE USED WITH THIS MODULE
MOLEX 87959-0001
CURRENTLY THIS PART HAS A LONG LEAD TIME SO THIS PART HAS BEEN REPLACED WITH AMPHENOL G38A11214A

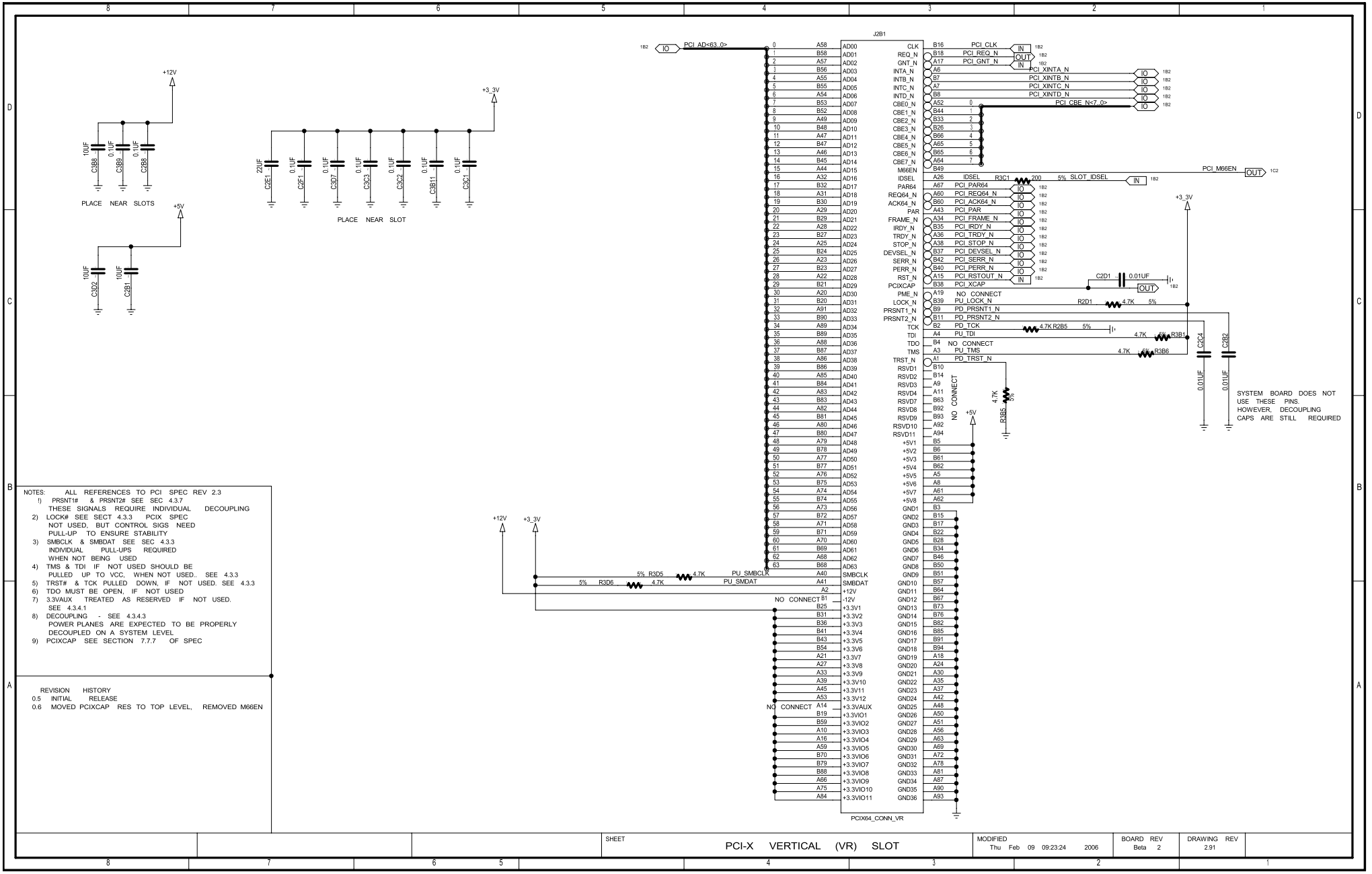
LAYOUT NOTE:
PLACE AC COUPLING CAPS NEAR EITHER SOURCE OR DESTINATION

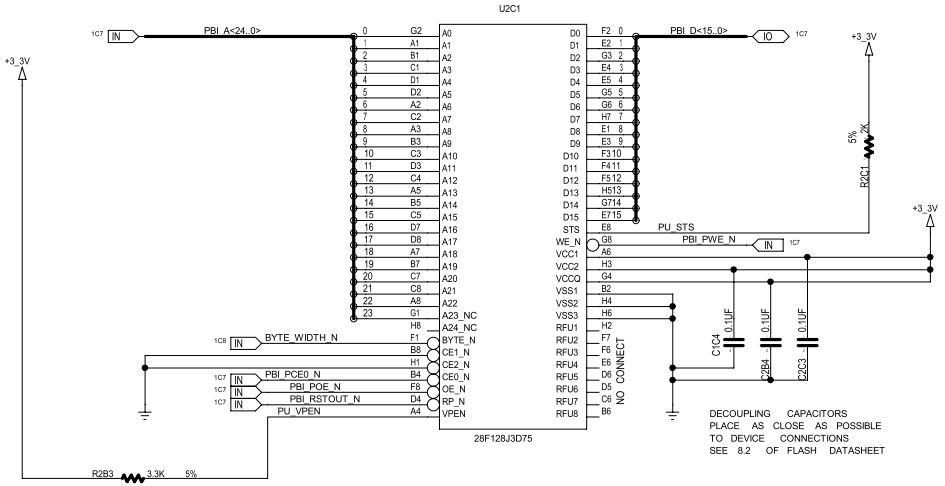
SAS SIGNALS FROM 8134x IO PROCESSOR TO X4 INTERNAL SAS CONNECTOR SWAPPED TO MINIMIZE VIAS. 8134x B0 WILL ENABLE REORDERING SGPIO TRANSMIT ORDER TO MATCH LANE SWAPS ON BOARD.

SAS LANE CONNECTIONS

8134x	X4 INTERNAL SAS CONNECTOR
LANE 0	LANE 2
LANE 1	LANE 1
LANE 2	LANE 3
LANE 3	LANE 0

SHEET: SAS CONNECTOR X4 INTERNAL - VERTICAL - NO CAPS
MODIFIED: Fri Sep 30 12:15:13 2005
BOARD REV: Beta 2
DRAWING REV: 2.91

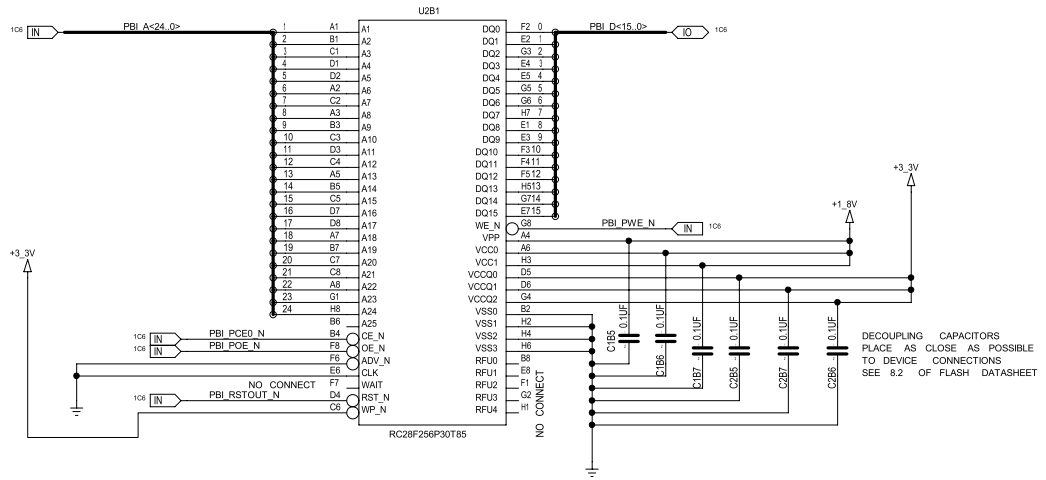

PCI_AD<63..0>
PCI_CLK
PCI_REQ_N
PCI_GNT_N
PCI_XINTA_N
PCI_XINTB_N
PCI_XINTC_N
PCI_XINTD_N
PCI_CBE_N<7..0>
PCI_M66EN
SLOT_IDSEL
PCI_PAR64
PCI_REQ64_N
PCI_ACK64_N
PCI_PAR
PCI_FRAME_N
PCI_IRDY_N
PCI_TRDY_N
PCI_STOP_N
PCI_DEVSEL_N
PCI_SERR_N
PCI_PERR_N
PCI_RSTOUT_N
PCI_XCAP
NO_CONNECT
PU_LOCK_N
PD_PRSNT1_N
PD_PRSNT2_N
PD_TCK
PU_TDI
PD_TRST_N
PU_SMBCLK
PU_SMDAT
PLACE NEAR SLOTS
PLACE NEAR SLOT
SYSTEM BOARD DOES NOT USE THESE PINS. HOWEVER, DECOUPLING CAPS ARE STILL REQUIRED
PCIX64_CONN_VR
NOTES:
1) PRSNT1# & PRSNT2# SEE SEC 4.3.7 THESE SIGNALS REQUIRE INDIVIDUAL DECOUPLING
2) LOCK# SEE SECT 4.3.3 PCIX SPEC NOT USED, BUT CONTROL SIGS NEED PULL-UP TO ENSURE STABILITY
3) SMBCLK & SMBDAT SEE SEC 4.3.3 INDIVIDUAL PULL-UPS REQUIRED WHEN NOT BEING USED
4) TMS & TDI IF NOT USED SHOULD BE PULLED UP TO VCC, WHEN NOT USED.. SEE 4.3.3
5) TRST# & TCK PULLED DOWN, IF NOT USED. SEE 4.3.3
6) TDO MUST BE OPEN, IF NOT USED
7) 3.3VAUX TREATED AS RESERVED IF NOT USED. SEE 4.3.4.1
8) DECOUPLING - SEE 4.3.4.3 POWER PLANES ARE EXPECTED TO BE PROPERLY DECOUPLED ON A SYSTEM LEVEL
9) PCIXCAP SEE SECTION 7.7.7 OF SPEC
REVISION HISTORY
0.5 INITIAL RELEASE
0.6 MOVED PCIXCAP RES TO TOP LEVEL, REMOVED M66EN
SHEET
PCI-X VERTICAL (VR) SLOT
MODIFIED
Thu Feb 09 09:23:24 2006
BOARD REV
Beta 2
DRAWING REV
2.91



NOTES
1) ADDRESS 24 IS NOT VALID FOR THIS DENSITY
2) 3.3K PULL-UP REQUESTED BY FPG ON VPEN

REVISION LIST
0.5 INITAL RELEASE 1/31/06
0.6 ADDED ADDITIONAL DECOUPLING CAP

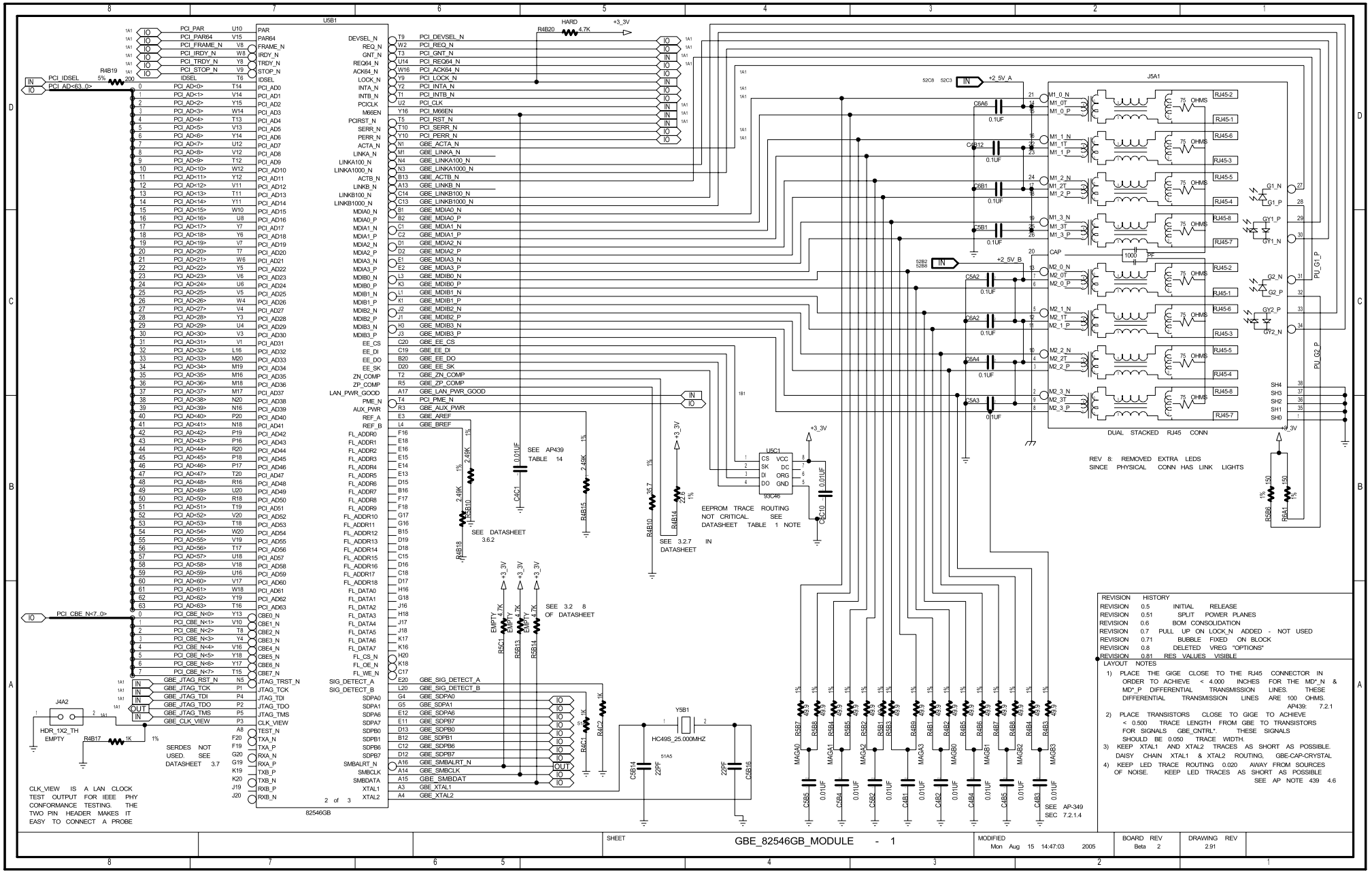
SHEET	MODIFIED	BOARD REV	DRAWING REV
J3D STRATAFLASH - 16M	Wed Feb 01 15:50:12 2006	Beta 2	2.91

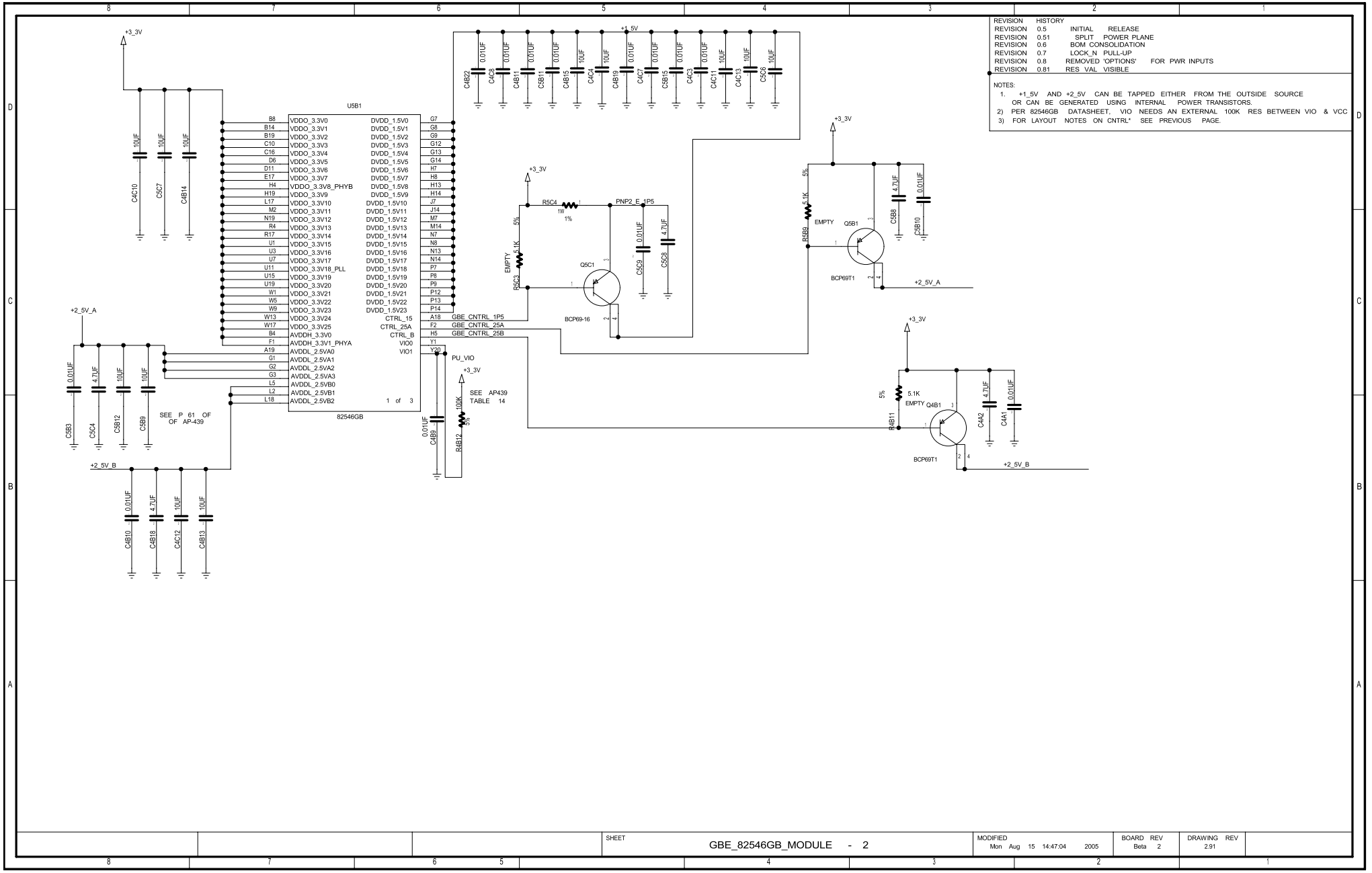


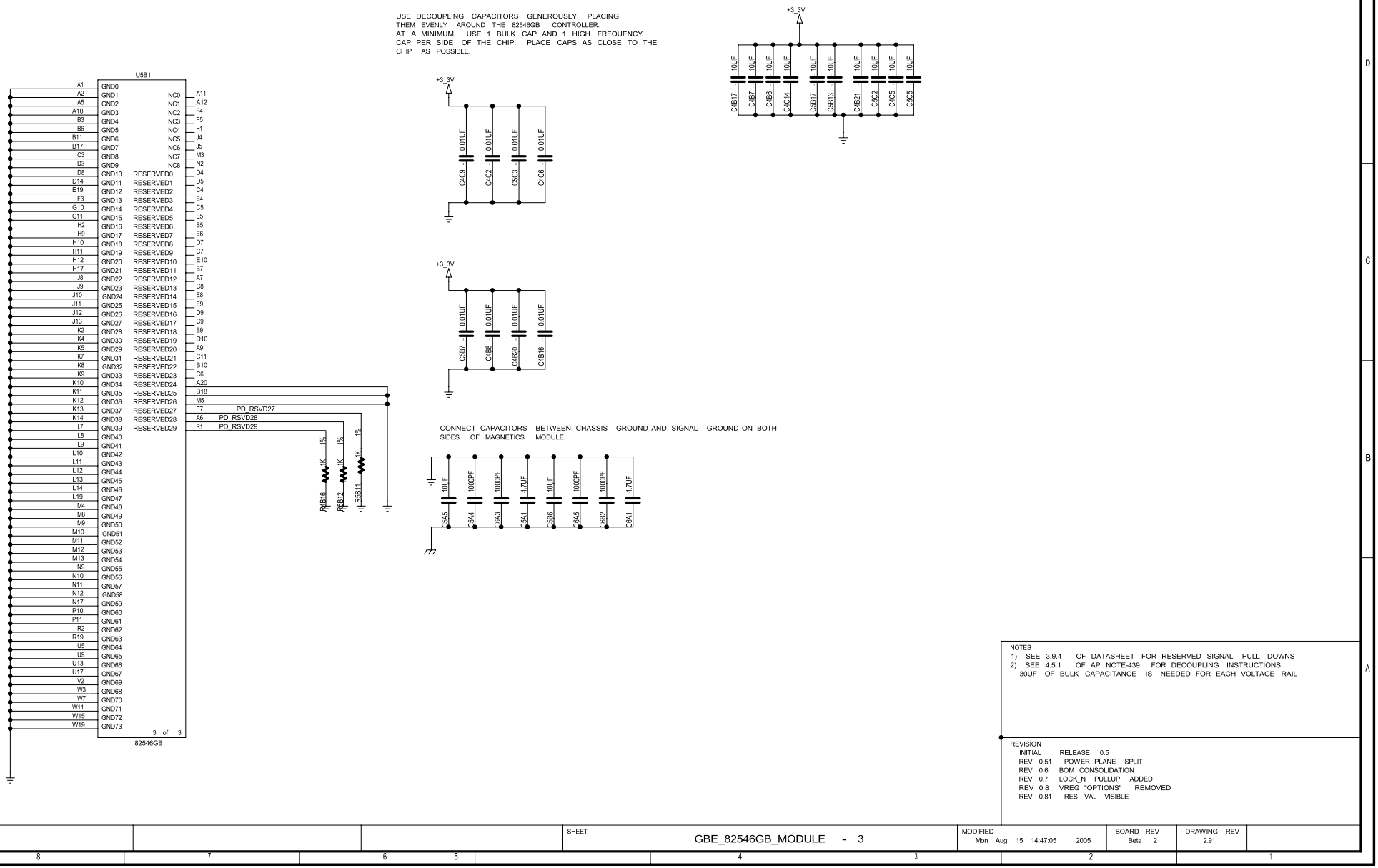
NOTES
1) VPP & VCC CAN BE TIED TOGETHER TO 1.8V PER CH 2.0 IN THE P30 DATASHEET
2) OUR PBI BUS IS ASYNCHRONOUS, THEREFORE ADV# IS TIED TO GROUNDTO ALLOW ADDRESES TO FLOW THROUGH. CLK IS ALSO TIED TO VSS.
3) BECAUSE THIS IS A 16-BIT DEVICE, A0 SHOULD BE SKIPPED FROM THE IOP'S PROSPECTIVE
4) WP# I STIED TO 3.3V TO ALLOW CHANGE OF FLASH CONTENT
5) IF WAIT IS UNUSED, IT CAN BE LEFT OPEN
6) PBI A0 SHOULD NOT BE CONNECTED TO FLASH A25 OF FLASH IS NOT VALID IN THIS DENSITY

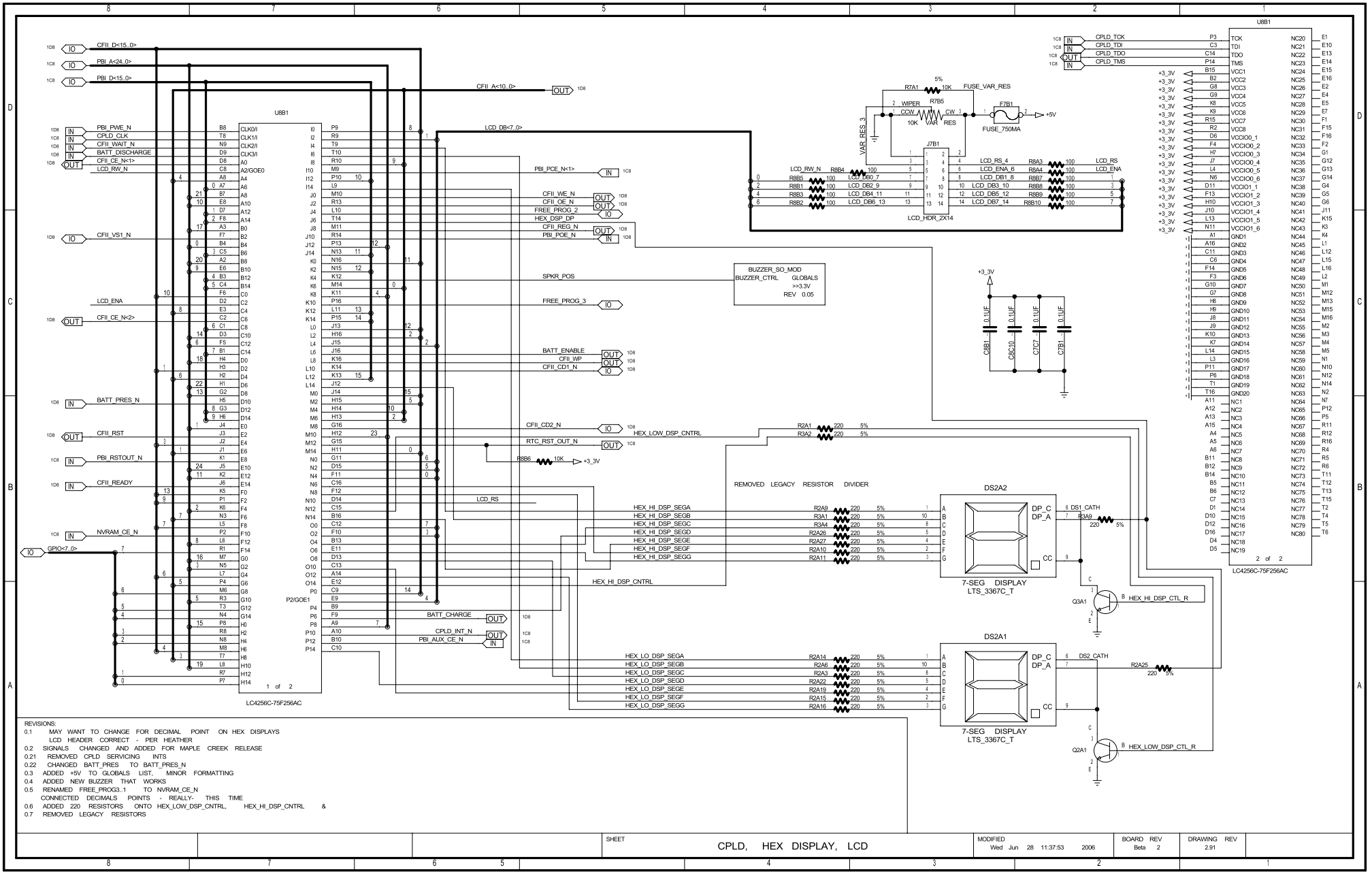
REVISION LIST
0.5 INITAL RELEASE 9/27/05
0.6 SENT DESIGN FOR REVIEW TO FPG - FIXED ISSUES
0.7 A1-A24 CORRECTED

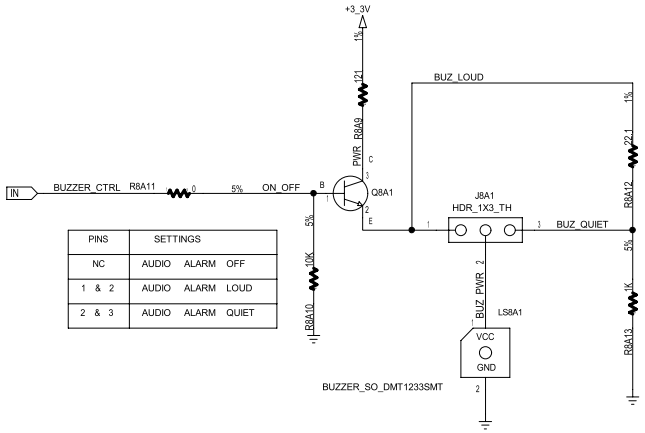
			SHEET	MODIFIED	BOARD REV	DRAWING REV	
			P30 FLASH - 256M	Tue Oct 04 16:53:06 2005	Beta 2	2.91	


U5B1
82546GB
2 of 3
PCI_PAR
PCI_PAR64
PCI_FRAME_N
PCI_IRDY_N
PCI_TRDY_N
PCI_STOP_N
PCI_IDSEL
PCI_AD<63..0>
PCI_CBE_N<7..0>
GBE_JTAG_RST_N
GBE_JTAG_TCK
GBE_JTAG_TDI
GBE_JTAG_TDO
GBE_JTAG_TMS
GBE_CLK_VIEW
R4B19
R4B20
HARD
+3_3V
+2_5V_A
+2_5V_B
J5A1
DUAL STACKED RJ45 CONN
RJ45-1
RJ45-2
RJ45-3
RJ45-4
RJ45-5
RJ45-6
RJ45-7
RJ45-8
75 OHMS
G1_N
G1_P
GY1_P
GY1_N
G2_N
G2_P
GY2_P
GY2_N
PU_G1_P
PU_G2_P
SH4
SH3
SH2
SH1
SH0
U5C1
93C46
EEPROM TRACE ROUTING NOT CRITICAL. SEE DATASHEET TABLE 1 NOTE
SEE 3.2.7 IN DATASHEET
SEE AP439 TABLE 14
SEE DATASHEET 3.6.2
SEE 3.2 8 OF DATASHEET
SERDES NOT USED. SEE DATASHEET 3.7
CLK_VIEW IS A LAN CLOCK TEST OUTPUT FOR IEEE PHY CONFORMANCE TESTING. THE TWO PIN HEADER MAKES IT EASY TO CONNECT A PROBE
HDR_1X2_TH
EMPTY
J4A2
Y5B1
HC49S_25.000MHZ
SEE AP-349 SEC 7.2.1.4
REV 8: REMOVED EXTRA LEDS SINCE PHYSICAL CONN HAS LINK LIGHTS
REVISION HISTORY
REVISION 0.5 INITIAL RELEASE
REVISION 0.51 SPLIT POWER PLANES
REVISION 0.6 BOM CONSOLIDATION
REVISION 0.7 PULL UP ON LOCK_N ADDED - NOT USED
REVISION 0.71 BUBBLE FIXED ON BLOCK
REVISION 0.8 DELETED VREG "OPTIONS"
REVISION 0.81 RES VALUES VISIBLE
LAYOUT NOTES
1) PLACE THE GIGE CLOSE TO THE RJ45 CONNECTOR IN ORDER TO ACHIEVE < 4.000 INCHES FOR THE MD*_N & MD*_P DIFFERENTIAL TRANSMISSION LINES. THESE DIFFERENTIAL TRANSMISSION LINES ARE 100 OHMS. AP439: 7.2.1
2) PLACE TRANSISTORS CLOSE TO GIGE TO ACHIEVE < 0.500 TRACE LENGTH FROM GBE TO TRANSISTORS FOR SIGNALS GBE_CNTRL*. THESE SIGNALS SHOULD BE 0.050 TRACE WIDTH.
3) KEEP XTAL1 AND XTAL2 TRACES AS SHORT AS POSSIBLE. DAISY CHAIN XTAL1 & XTAL2 ROUTING. GBE-CAP-CRYSTAL
4) KEEP LED TRACE ROUTING 0.020 AWAY FROM SOURCES OF NOISE. KEEP LED TRACES AS SHORT AS POSSIBLE SEE AP NOTE 439 4.6
SHEET
GBE_82546GB_MODULE - 1
MODIFIED Mon Aug 15 14:47:03 2005
BOARD REV Beta 2
DRAWING REV 2.91


REVISION HISTORY
REVISION 0.5 INITIAL RELEASE
REVISION 0.51 SPLIT POWER PLANE
REVISION 0.6 BOM CONSOLIDATION
REVISION 0.7 LOCK_N PULL-UP
REVISION 0.8 REMOVED 'OPTIONS' FOR PWR INPUTS
REVISION 0.81 RES VAL VISIBLE
NOTES:
1. +1_5V AND +2_5V CAN BE TAPPED EITHER FROM THE OUTSIDE SOURCE OR CAN BE GENERATED USING INTERNAL POWER TRANSISTORS.
2) PER 82546GB DATASHEET, VIO NEEDS AN EXTERNAL 100K RES BETWEEN VIO & VCC
3) FOR LAYOUT NOTES ON CNTRL* SEE PREVIOUS PAGE.
U5B1
82546GB
SEE P 61 OF OF AP-439
SEE AP439 TABLE 14
PU_VIO
GBE_CNTRL_1P5
GBE_CNTRL_25A
GBE_CNTRL_25B
PNP2_E_1P5
BCP69-16
BCP69T1
EMPTY
SHEET
GBE_82546GB_MODULE - 2
MODIFIED
Mon Aug 15 14:47:04 2005
BOARD REV
Beta 2
DRAWING REV
2.91


USE DECOUPLING CAPACITORS GENEROUSLY, PLACING THEM EVENLY AROUND THE 82546GB CONTROLLER.
AT A MINIMUM, USE 1 BULK CAP AND 1 HIGH FREQUENCY CAP PER SIDE OF THE CHIP. PLACE CAPS AS CLOSE TO THE CHIP AS POSSIBLE.
U5B1
82546GB
3 of 3
+3_3V
0.01UF
10UF
1000PF
4.7UF
1K
1%
PD_RSVD27
PD_RSVD28
PD_RSVD29
CONNECT CAPACITORS BETWEEN CHASSIS GROUND AND SIGNAL GROUND ON BOTH SIDES OF MAGNETICS MODULE.
NOTES
1) SEE 3.9.4 OF DATASHEET FOR RESERVED SIGNAL PULL DOWNS
2) SEE 4.5.1 OF AP NOTE-439 FOR DECOUPLING INSTRUCTIONS
30UF OF BULK CAPACITANCE IS NEEDED FOR EACH VOLTAGE RAIL
REVISION
INITIAL RELEASE 0.5
REV 0.51 POWER PLANE SPLIT
REV 0.6 BOM CONSOLIDATION
REV 0.7 LOCK_N PULLUP ADDED
REV 0.8 VREG "OPTIONS" REMOVED
REV 0.81 RES VAL VISIBLE
SHEET
GBE_82546GB_MODULE - 3
MODIFIED
Mon Aug 15 14:47:05 2005
BOARD REV
Beta 2
DRAWING REV
2.91


CFII_D<15..0>
PBI_A<24..0>
PBI_D<15..0>
CFII_A<10..0>
PBI_PWE_N
CPLD_CLK
CFII_WAIT_N
BATT_DISCHARGE
CFII_CE_N<1>
LCD_RW_N
CFII_VS1_N
LCD_ENA
CFII_CE_N<2>
BATT_PRES_N
CFII_RST
PBI_RSTOUT_N
CFII_READY
NVRAM_CE_N
GPIO<7..0>
U8B1
LC4256C-75F256AC
1 of 2
LCD_DB<7..0>
PBI_PCE_N<1>
CFII_WE_N
CFII_OE_N
FREE_PROG_2
HEX_DSP_DP
CFII_REG_N
PBI_POE_N
SPKR_POS
FREE_PROG_3
BATT_ENABLE
CFII_WP
CFII_CD1_N
CFII_CD2_N
RTC_RST_OUT_N
R8B6 10K
+3_3V
LCD_RS
HEX_HI_DSP_CNTRL
BATT_CHARGE
CPLD_INT_N
PBI_AUX_CE_N
R7A1 10K FUSE_VAR_RES
R7B5
WIPER
CCW
CW
10K VAR RES
VAR_RES_3
F7B1
FUSE_750MA
+5V
J7B1
LCD_HDR_2X14
LCD_RW_N R8B4 100
LCD_DB0_7
LCD_DB2_9
LCD_DB4_11
LCD_DB6_13
LCD_RS_4 R8A3 100 LCD_RS
LCD_ENA_6 R8A4 100 LCD_ENA
LCD_DB1_8 R8B7 100
LCD_DB3_10 R8B8 100
LCD_DB5_12 R8B9 100
LCD_DB7_14 R8B10 100
BUZZER_SQ_MOD
BUZZER_CTRL GLOBALS
>>3.3V
REV 0.05
C9B1 0.1UF
C8C10 0.1UF
C7C7 0.1UF
C7B1 0.1UF
CPLD_TCK
CPLD_TDI
CPLD_TDO
CPLD_TMS
REMOVED LEGACY RESISTOR DIVIDER
HEX_HI_DSP_SEGA
HEX_HI_DSP_SEGB
HEX_HI_DSP_SEGC
HEX_HI_DSP_SEGD
HEX_HI_DSP_SEGE
HEX_HI_DSP_SEGF
HEX_HI_DSP_SEGG
R2A9 220 5%
R3A1 220 5%
R3A4 220 5%
R2A26 220 5%
R2A27 220 5%
R2A10 220 5%
R2A11 220 5%
DS2A2
DP_C
DP_A
CC
7-SEG DISPLAY
LTS_3367C_T
DS1_CATH
R3A9 220 5%
Q3A1
HEX_HI_DSP_CTL_R
HEX_LO_DSP_SEGA
HEX_LO_DSP_SEGB
HEX_LO_DSP_SEGC
HEX_LO_DSP_SEGD
HEX_LO_DSP_SEGE
HEX_LO_DSP_SEGF
HEX_LO_DSP_SEGG
R2A14 220 5%
R2A6 220 5%
R2A3 220 5%
R2A22 220 5%
R2A19 220 5%
R2A15 220 5%
R2A16 220 5%
DS2A1
DS2_CATH
R2A25 220 5%
Q2A1
HEX_LOW_DSP_CTL_R
HEX_LOW_DSP_CNTRL
R2A1 220 5%
R3A2 220 5%
REVISIONS:
0.1 MAY WANT TO CHANGE FOR DECIMAL POINT ON HEX DISPLAYS
LCD HEADER CORRECT - PER HEATHER
0.2 SIGNALS CHANGED AND ADDED FOR MAPLE CREEK RELEASE
0.21 REMOVED CPLD SERVICING INTS
0.22 CHANGED BATT_PRES TO BATT_PRES_N
0.3 ADDED +5V TO GLOBALS LIST, MINOR FORMATTING
0.4 ADDED NEW BUZZER THAT WORKS
0.5 RENAMED FREE_PROG3..1 TO NVRAM_CE_N
CONNECTED DECIMALS POINTS - REALLY- THIS TIME
0.6 ADDED 220 RESISTORS ONTO HEX_LOW_DSP_CNTRL, HEX_HI_DSP_CNTRL &
0.7 REMOVED LEGACY RESISTORS
SHEET
CPLD, HEX DISPLAY, LCD
MODIFIED
Wed Jun 28 11:37:53 2006
BOARD REV
Beta 2
DRAWING REV
2.91

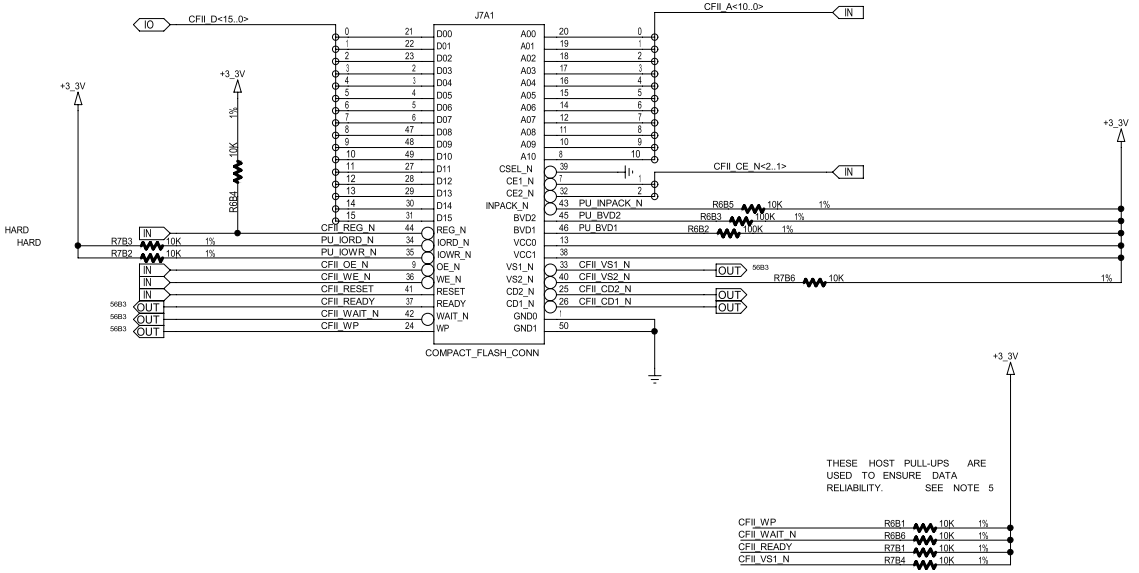


PINS	SETTINGS
NC	AUDIO ALARM OFF
1 & 2	AUDIO ALARM LOUD
2 & 3	AUDIO ALARM QUIET

REVISION LIST

0.01 INITIAL DRAFT 10/11/04

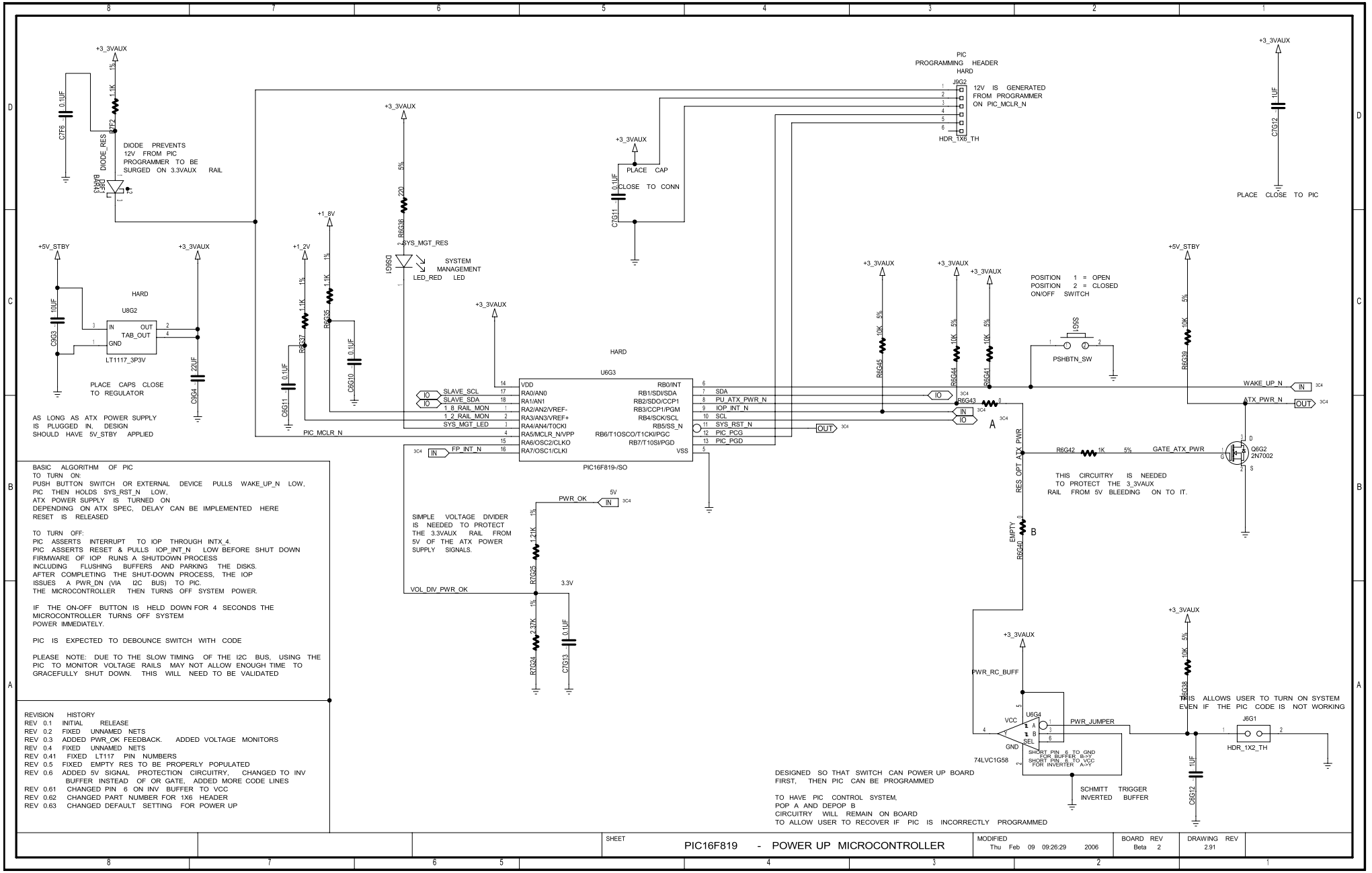
			SHEET		MODIFIED	BOARD REV	DRAWING REV	
			BUZZER		Mon Mar 20 09:38:25 2006	Beta 2	2.91	



NOTES
1) DESIGN SUPPORTS PC MEMORY MODE ONLY CARD. IN THIS MODE CSEL_N SHOULD BE TIED TO GROUND SINCE IT IS IGNORED. SEE TABLE 4, NOTE 5 IN CF & CF+ SPEC REV 3.0
NO SUPPORT FOR HOT PLUG
NO TRUE IDE MODE SUPPORT
2) BVD1 AND BVD2 ARE ASSERTED HIGH SINCE THEY ARE NOT SUPPORTED IN THIS MODE. SEE TABLE 5 IN SPEC
3) CSEL_N IS NOT USED IN THIS MODE & IS GROUNDED BY HOST.
4) INPACK_N, IORD_N, & IOWR_N ARE NOT USED IN THIS MODE. DE'S DECISION TO TIE HIGH BASED OFF OLDER DESIGNS (WC).
5) ADDITIONAL PULLUPS NEEDED TO ENSURE DATA REALIABILITY. SEE 4.3.6 IN CF & CF+ SPEC REV 3.0

REVISION HISTORY
REV 0.1 INITIAL RELEASE 4/05
REV 0.3 MODIFIED PORT NAMES 8/19
REV 0.4 COMBINED CE_N INTO A BUS 1/30/06

SHEET: COMPACT FLASH II CONNECTOR
MODIFIED: Wed Feb 01 10:32:17 2006
BOARD REV: Beta 2
DRAWING REV: 2.91

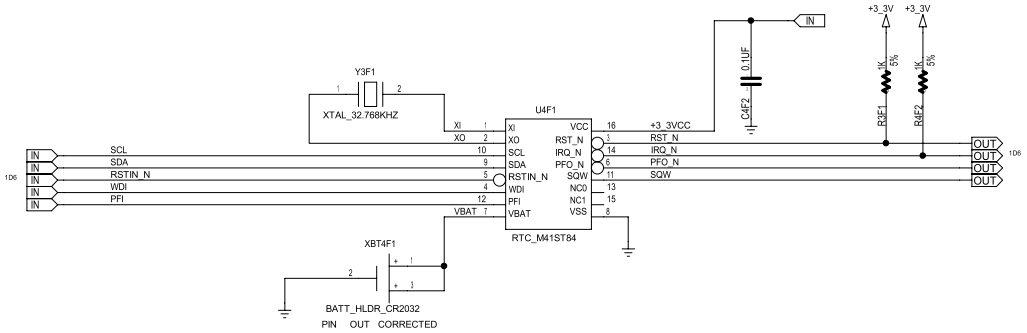

PIC16F819 - POWER UP MICROCONTROLLER
PIC16F819-/SO
U6G3
U8G2
LT1117_3P3V
U6G4
74LVC1G58
J9G2
HDR_1X6_TH
J6G1
HDR_1X2_TH
Q6G2
2N7002
DIODE PREVENTS 12V FROM PIC PROGRAMMER TO BE SURGED ON 3.3VAUX RAIL
PLACE CAP CLOSE TO CONN
PLACE CLOSE TO PIC
PLACE CAPS CLOSE TO REGULATOR
AS LONG AS ATX POWER SUPPLY IS PLUGGED IN, DESIGN SHOULD HAVE 5V_STBY APPLIED
SYSTEM MANAGEMENT LED_RED LED
SYS_MGT_RES
PIC_MCLR_N
SLAVE_SCL
SLAVE_SDA
1_8_RAIL_MON
1_2_RAIL_MON
SYS_MGT_LED
FP_INT_N
SDA
PU_ATX_PWR_N
IOP_INT_N
SCL
SYS_RST_N
PIC_PCG
PIC_PGD
POSITION 1 = OPEN
POSITION 2 = CLOSED
ON/OFF SWITCH
PSHBTN_SW
WAKE_UP_N
ATX_PWR_N
GATE_ATX_PWR
THIS CIRCUITRY IS NEEDED TO PROTECT THE 3_3VAUX RAIL FROM 5V BLEEDING ON TO IT.
SIMPLE VOLTAGE DIVIDER IS NEEDED TO PROTECT THE 3.3VAUX RAIL FROM 5V OF THE ATX POWER SUPPLY SIGNALS.
PWR_OK
VOL_DIV_PWR_OK
PWR_RC_BUFF
PWR_JUMPER
SCHMITT TRIGGER INVERTED BUFFER
THIS ALLOWS USER TO TURN ON SYSTEM EVEN IF THE PIC CODE IS NOT WORKING
DESIGNED SO THAT SWITCH CAN POWER UP BOARD FIRST, THEN PIC CAN BE PROGRAMMED
TO HAVE PIC CONTROL SYSTEM, POP A AND DEPOP B
CIRCUITRY WILL REMAIN ON BOARD
TO ALLOW USER TO RECOVER IF PIC IS INCORRECTLY PROGRAMMED
BASIC ALGORITHM OF PIC
TO TURN ON:
PUSH BUTTON SWITCH OR EXTERNAL DEVICE PULLS WAKE_UP_N LOW,
PIC THEN HOLDS SYS_RST_N LOW,
ATX POWER SUPPLY IS TURNED ON
DEPENDING ON ATX SPEC, DELAY CAN BE IMPLEMENTED HERE
RESET IS RELEASED
TO TURN OFF:
PIC ASSERTS INTERRUPT TO IOP THROUGH INTX_4.
PIC ASSERTS RESET & PULLS IOP_INT_N LOW BEFORE SHUT DOWN
FIRMWARE OF IOP RUNS A SHUTDOWN PROCESS
INCLUDING FLUSHING BUFFERS AND PARKING THE DISKS.
AFTER COMPLETING THE SHUT-DOWN PROCESS, THE IOP
ISSUES A PWR_DN (VIA I2C BUS) TO PIC.
THE MICROCONTROLLER THEN TURNS OFF SYSTEM POWER.
IF THE ON-OFF BUTTON IS HELD DOWN FOR 4 SECONDS THE
MICROCONTROLLER TURNS OFF SYSTEM
POWER IMMEDIATELY.
PIC IS EXPECTED TO DEBOUNCE SWITCH WITH CODE
PLEASE NOTE: DUE TO THE SLOW TIMING OF THE I2C BUS, USING THE
PIC TO MONITOR VOLTAGE RAILS MAY NOT ALLOW ENOUGH TIME TO
GRACEFULLY SHUT DOWN. THIS WILL NEED TO BE VALIDATED
REVISION HISTORY
REV 0.1 INITIAL RELEASE
REV 0.2 FIXED UNNAMED NETS
REV 0.3 ADDED PWR_OK FEEDBACK. ADDED VOLTAGE MONITORS
REV 0.4 FIXED UNNAMED NETS
REV 0.41 FIXED LT117 PIN NUMBERS
REV 0.5 FIXED EMPTY RES TO BE PROPERLY POPULATED
REV 0.6 ADDED 5V SIGNAL PROTECTION CIRCUITRY, CHANGED TO INV BUFFER INSTEAD OF OR GATE, ADDED MORE CODE LINES
REV 0.61 CHANGED PIN 6 ON INV BUFFER TO VCC
REV 0.62 CHANGED PART NUMBER FOR 1X6 HEADER
REV 0.63 CHANGED DEFAULT SETTING FOR POWER UP
SHEET
MODIFIED Thu Feb 09 09:26:29 2006
BOARD REV Beta 2
DRAWING REV 2.91

REVISIONS

0.5	INITIAL	RELEASE
0.6	HOLDER	DELETED PER MARK
0.61	HOLDER	ADDED BACK IN PER MANUFACTURING
0.7	PIN	OUT ON HOLDER CORRECTED

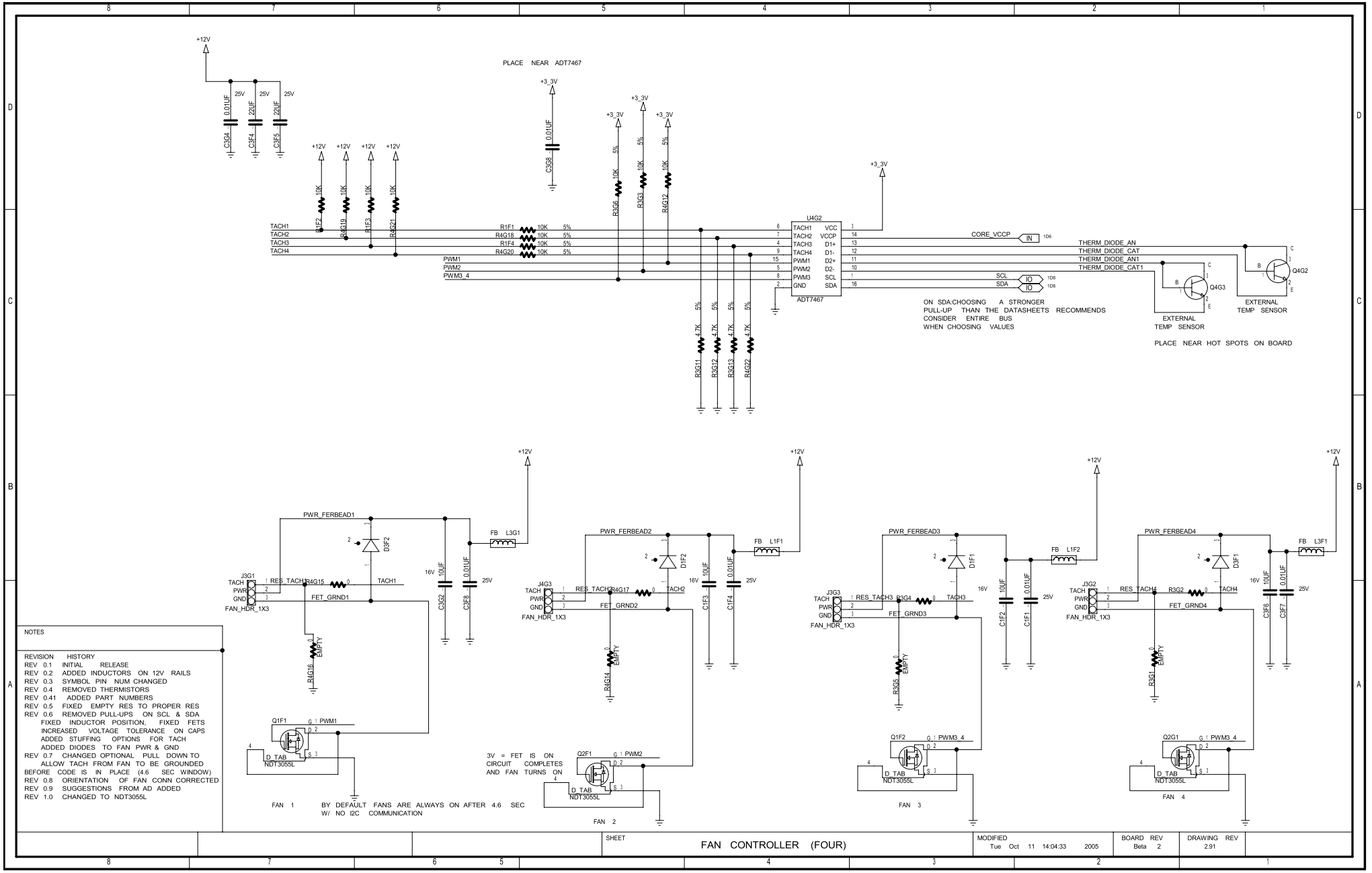
RM9L1

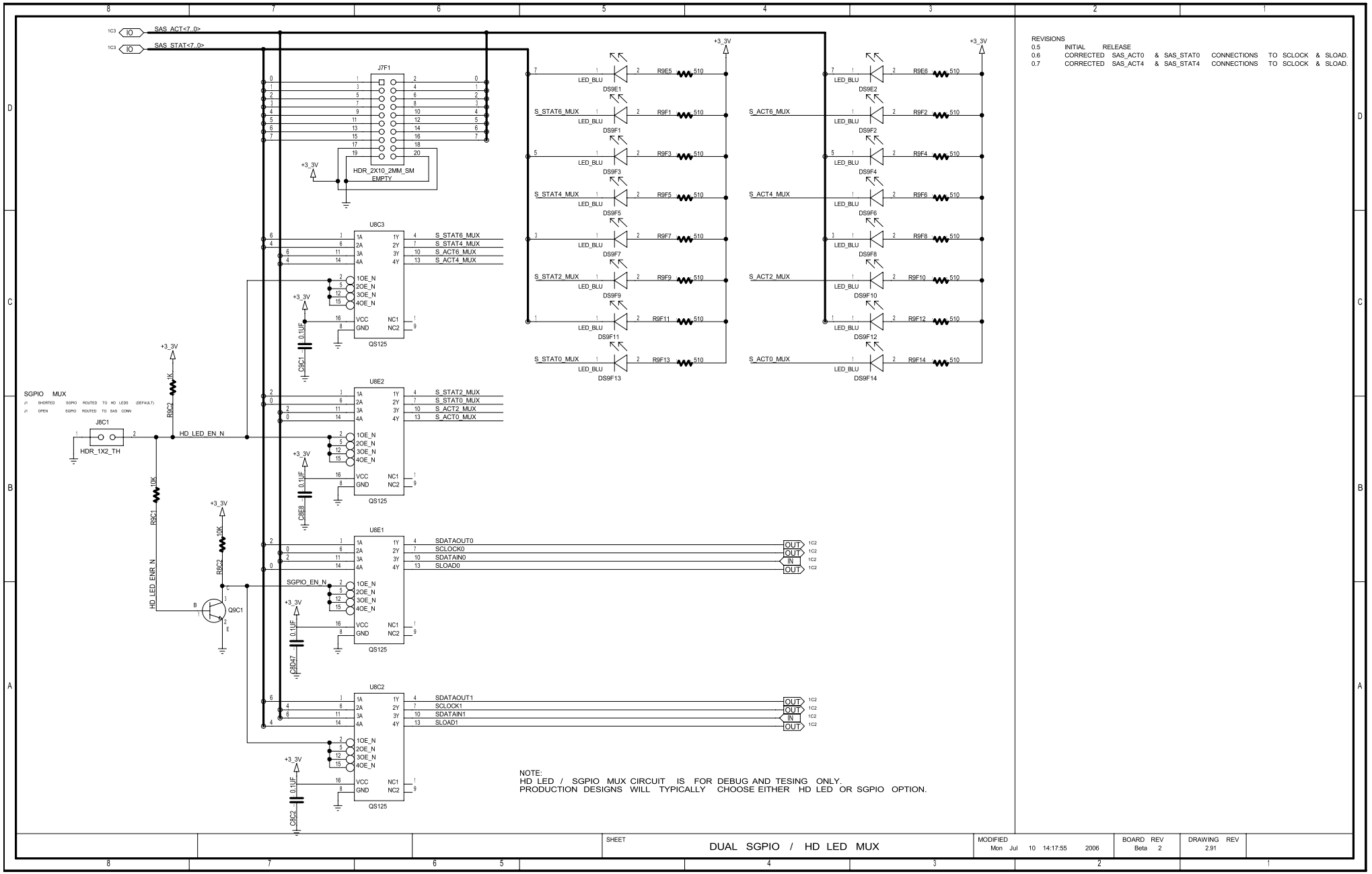
HOR_XTAL_HLDR
THIS REATINER IS NEEDED FOR CRYSTAL

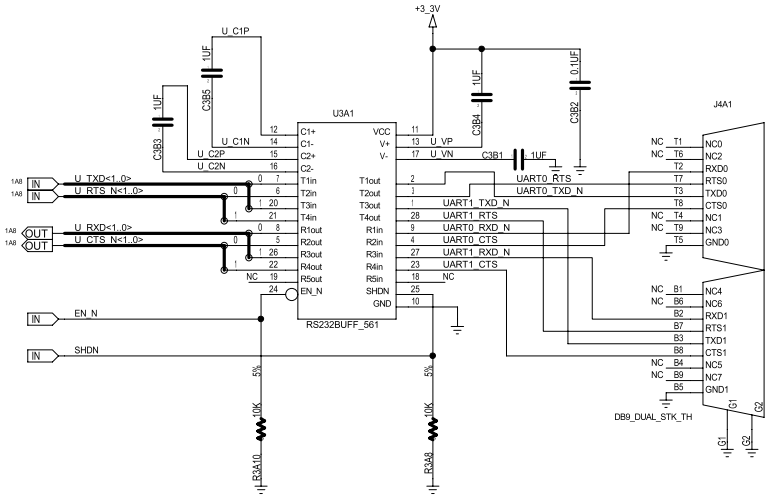


NOTES:
RST_N IS ASSERTED WHEN RSTIN_N IS ASSERTED OR WHEN +3_3VCC IS LESS THAN 2.65V.
PFO IS ASSERTED WHEN PFI IS LESS THAN 1.25V.
MINIMIZE CRYSTAL TRACE LENGTHS XI AND XO AND KEEP AWAY FROM RF GENERATING SIGNALS.

			SHEET: REAL TIME CLOCK	MODIFIED: Tue Jan 10 14:44:36 2006	BOARD REV: Beta 2	DRAWING REV: 2.91

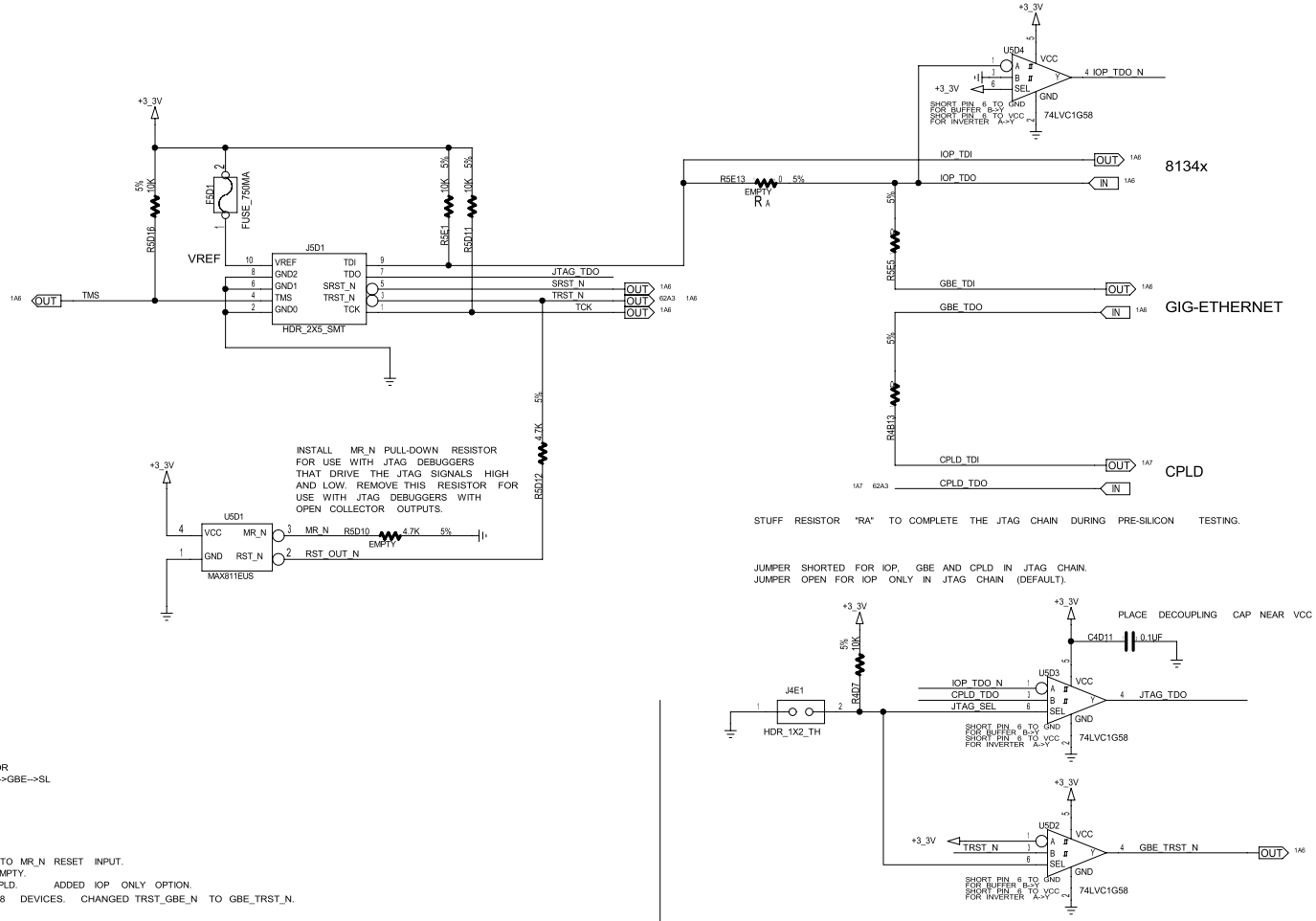

PLACE NEAR ADT7467
ADT7467
ON SDA:CHOOSING A STRONGER PULL-UP THAN THE DATASHEETS RECOMMENDS CONSIDER ENTIRE BUS WHEN CHOOSING VALUES
EXTERNAL TEMP SENSOR
EXTERNAL TEMP SENSOR
PLACE NEAR HOT SPOTS ON BOARD
NOTES
REVISION HISTORY
REV 0.1 INITIAL RELEASE
REV 0.2 ADDED INDUCTORS ON 12V RAILS
REV 0.3 SYMBOL PIN NUM CHANGED
REV 0.4 REMOVED THERMISTORS
REV 0.41 ADDED PART NUMBERS
REV 0.5 FIXED EMPTY RES TO PROPER RES
REV 0.6 REMOVED PULL-UPS ON SCL & SDA
FIXED INDUCTOR POSITION, FIXED FETS
INCREASED VOLTAGE TOLERANCE ON CAPS
ADDED STUFFING OPTIONS FOR TACH
ADDED DIODES TO FAN PWR & GND
REV 0.7 CHANGED OPTIONAL PULL DOWN TO ALLOW TACH FROM FAN TO BE GROUNDED
BEFORE CODE IS IN PLACE (4.6 SEC WINDOW)
REV 0.8 ORIENTATION OF FAN CONN CORRECTED
REV 0.9 SUGGESTIONS FROM AD ADDED
REV 1.0 CHANGED TO NDT3055L
FAN 1
BY DEFAULT FANS ARE ALWAYS ON AFTER 4.6 SEC W/ NO I2C COMMUNICATION
3V = FET IS ON CIRCUIT COMPLETES AND FAN TURNS ON
FAN 2
FAN 3
FAN 4
SHEET
FAN CONTROLLER (FOUR)
MODIFIED
Tue Oct 11 14:04:33 2005
BOARD REV
Beta 2
DRAWING REV
2.91


SAS_ACT<7..0>
SAS_STAT<7..0>
J7F1
HDR_2X10_2MM_SM
EMPTY
U8C3
U8E2
U8E1
U8C2
QS125
S_STAT6_MUX
S_STAT4_MUX
S_ACT6_MUX
S_ACT4_MUX
S_STAT2_MUX
S_STAT0_MUX
S_ACT2_MUX
S_ACT0_MUX
SDATAOUT0
SCLOCK0
SDATAIN0
SLOAD0
SDATAOUT1
SCLOCK1
SDATAIN1
SLOAD1
SGPIO MUX
J1 SHORTED SGPIO ROUTED TO HD LEDS (DEFAULT)
J1 OPEN SGPIO ROUTED TO SAS CONN
J8C1
HDR_1X2_TH
HD_LED_EN_N
SGPIO_EN_N
HD_LED_ENR_N
Q9C1
LED_BLU
NOTE:
HD LED / SGPIO MUX CIRCUIT IS FOR DEBUG AND TESING ONLY.
PRODUCTION DESIGNS WILL TYPICALLY CHOOSE EITHER HD LED OR SGPIO OPTION.
REVISIONS
0.5 INITIAL RELEASE
0.6 CORRECTED SAS_ACT0 & SAS_STAT0 CONNECTIONS TO SCLOCK & SLOAD.
0.7 CORRECTED SAS_ACT4 & SAS_STAT4 CONNECTIONS TO SCLOCK & SLOAD.
SHEET
DUAL SGPIO / HD LED MUX
MODIFIED
Mon Jul 10 14:17:55 2006
BOARD REV
Beta 2
DRAWING REV
2.91



REVISION LIST
0.1 INITAL DRAFT 4/28/05
0.5 CORRECTED NET NAMES 7/13/05

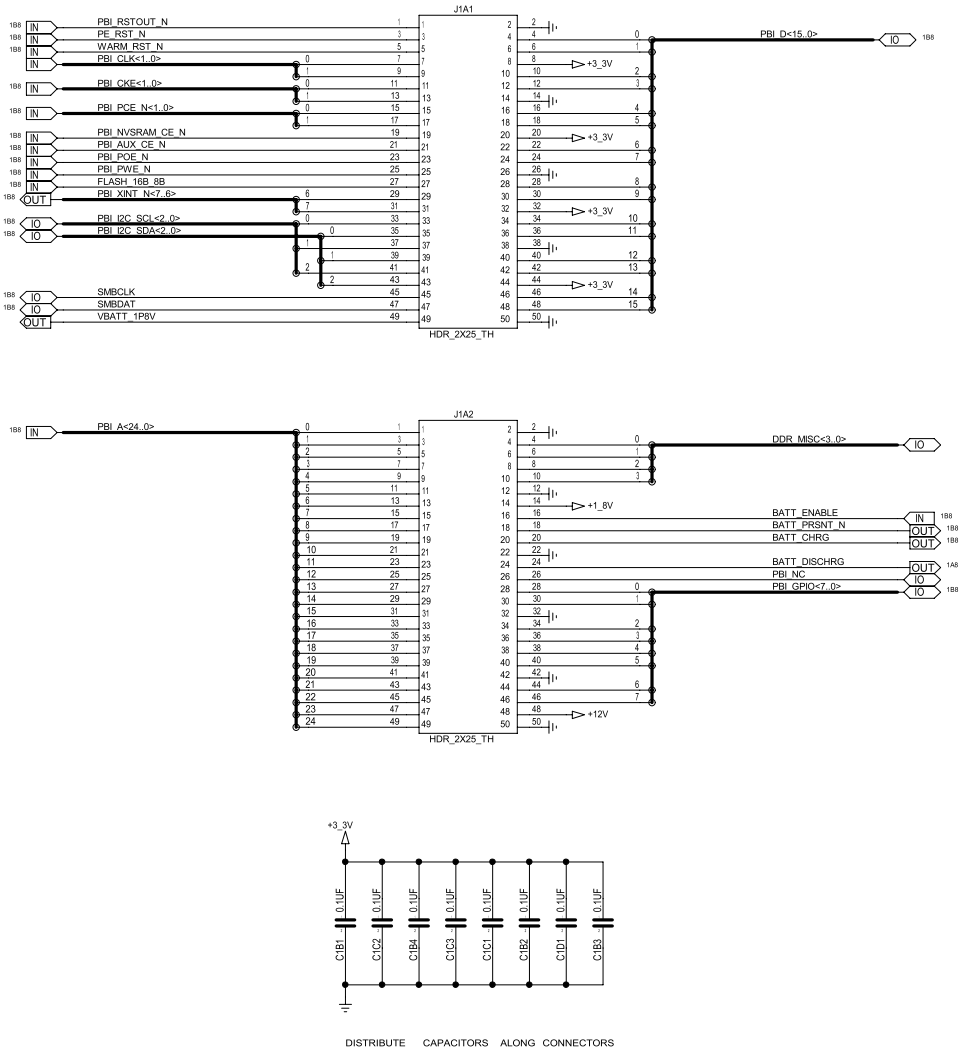
			SHEET	MODIFIED	BOARD REV	DRAWING REV	
			RS232_DB9_MOD	Thu Jan 26 10:30:15 2006	Beta 2	2.91	



REVISION HISTORY

0.50: FIRST RELEASE
0.51: COVERTED TO SINGLE JTAG CONNECTOR
CHAIN ORDER CHANGED TO CPLD-->GBE-->SL
0.52: HARD REFDES. FUSE_SMT UPDATED.
0.53: CHANGED 0 OHM RESISTORS TO 0402.
0.54: JTAG_CONN UPDATED
0.55: MORE RESISTORS CHANGED TO 0402
0.56: MORE RESISTORS CHANGED TO 0402
0.60: ADDED PULL-DOWN OPTION TO TRST_N.
0.61: MOVED TRST_N PULL-DOWN RESISTOR TO MR_N RESET INPUT.
0.62: CHANGED MR_N RESET RESISTOR TO EMPTY.
0.70: CHANGED CHAIN ORDER TO SL-->GBE-->CPLD. ADDED IOP ONLY OPTION.
0.80: ADDED DECOUPLING CAP FOR 74LVC1G58 DEVICES. CHANGED TRST_GBE_N TO GBE_TRST_N.
0.81: MINOR TEXT UPDATES.

SHEET	MODIFIED	BOARD REV	DRAWING REV
JTAG_CONN_MODULE	Thu Sep 01 10:34:33 2005	Beta 2	2.91



REVISIONS

0.1: RELEASE FOR DESIGN REVIEW

0.2: ADDED BATTERY CONTROL SIGNALS
RENAMED VBATT, PBI_SMBCLK & PBI_SMBDAT SIGNALS

0.3: RENUMBERED 2X25 HEADER PINS
CHANGED POLARITY OF PBI_AUX_CE AND PBI_NVSRAM_CE

1.0: ADDED BBU BUS

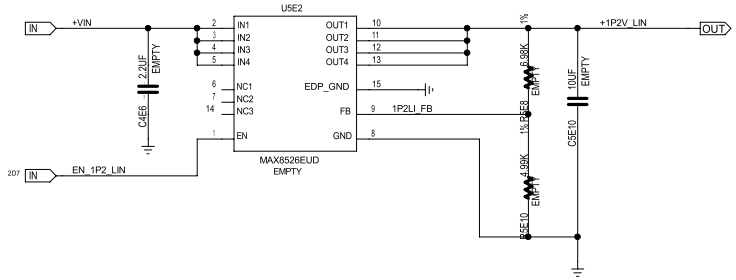
1.1: ECO5: RENAMED PBI_XINT<7..6> TO PBI_XINT_N<7..6>

1.2: CHANGED POLARITY OF BATT_PRSNT TO LOW ACTIVE BATT_PRSNT_N.

SHEET	MODIFIED	BOARD REV	DRAWING REV
PBI AUXILARY CONNECTOR	Fri Aug 05 14:05:34 2005	Beta 2	2.91

+VIN	MAX OUTPUT CURRENT
3.3V	0.81A
2.5V	1.31A
1.5V	2.0A (GUARANTEED LIMIT)

VIN RANGE (1.425V TO 3.6V)



REVISION

1 REVISION 0.5

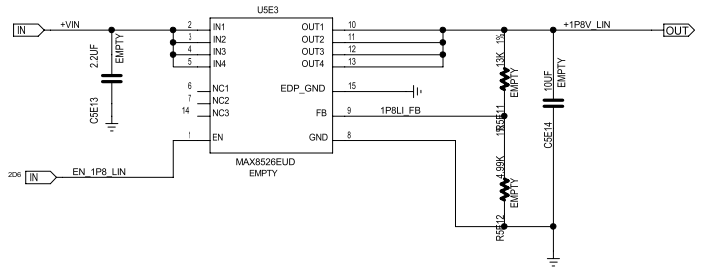
LAYOUT GUIDE

1 THE PACKAGE FEATURES AN EXPOSED THERMAL PAD ON ITS UNDERSIDE. THIS PAD LOWERS THE THERMAL RESISTANCE OF THE PACKAGE BY PROVIDING A DIRECT HEAT CONDUCTION PATH FROM THE DIE TO THE PC BOARD. ADDITIONALLY, THE GROUND PIN (GND) PERFORM THE DUAL FUNCTION OF PROVIDING AN ELECTRICAL CONNECTION TO SYSTEM GROUND AND CHANNELING HEAT AWAY. CONNECT THE EXPOSED BACKSIDE PAD AND GND TO THE SYSTEM GROUND USING A LARGE PAD OR GROUND PLANE, OR MULTIPLE VIAS TO THE GROUND-PLANE LAYER.

SHEET	MODIFIED	BOARD REV	DRAWING REV
VREG +1P2V_LINEAR (NOT POPULATED)	Fri Dec 23 18:13:58 2005	Beta 2	2.91

+VIN	MAX OUTPUT CURRENT
3.3V	1.13A
2.5V	2.0A (GUARANTEED LIMIT)

VIN RANGE 2V TO 3.6V)



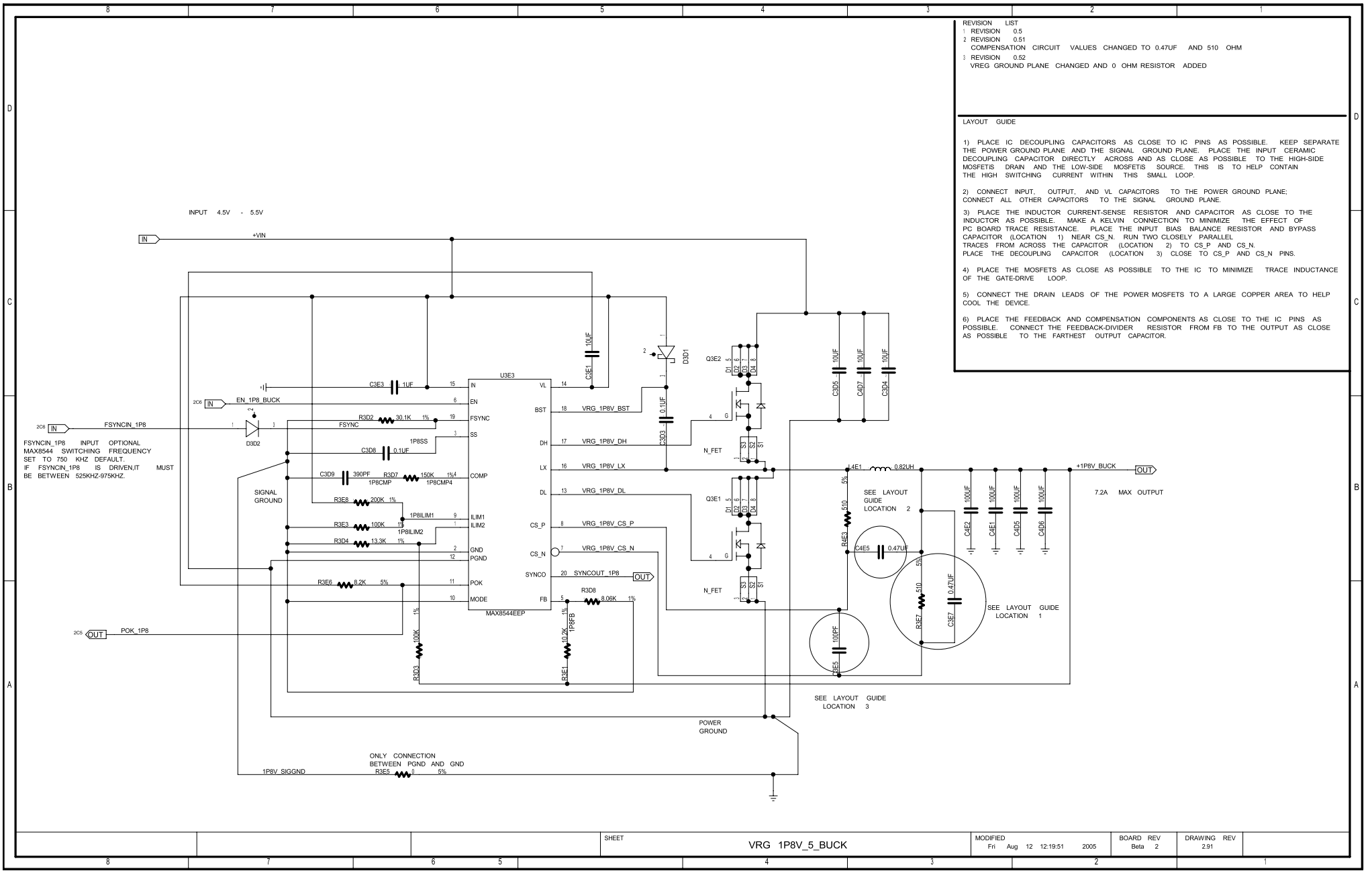
REVISION HISTORY

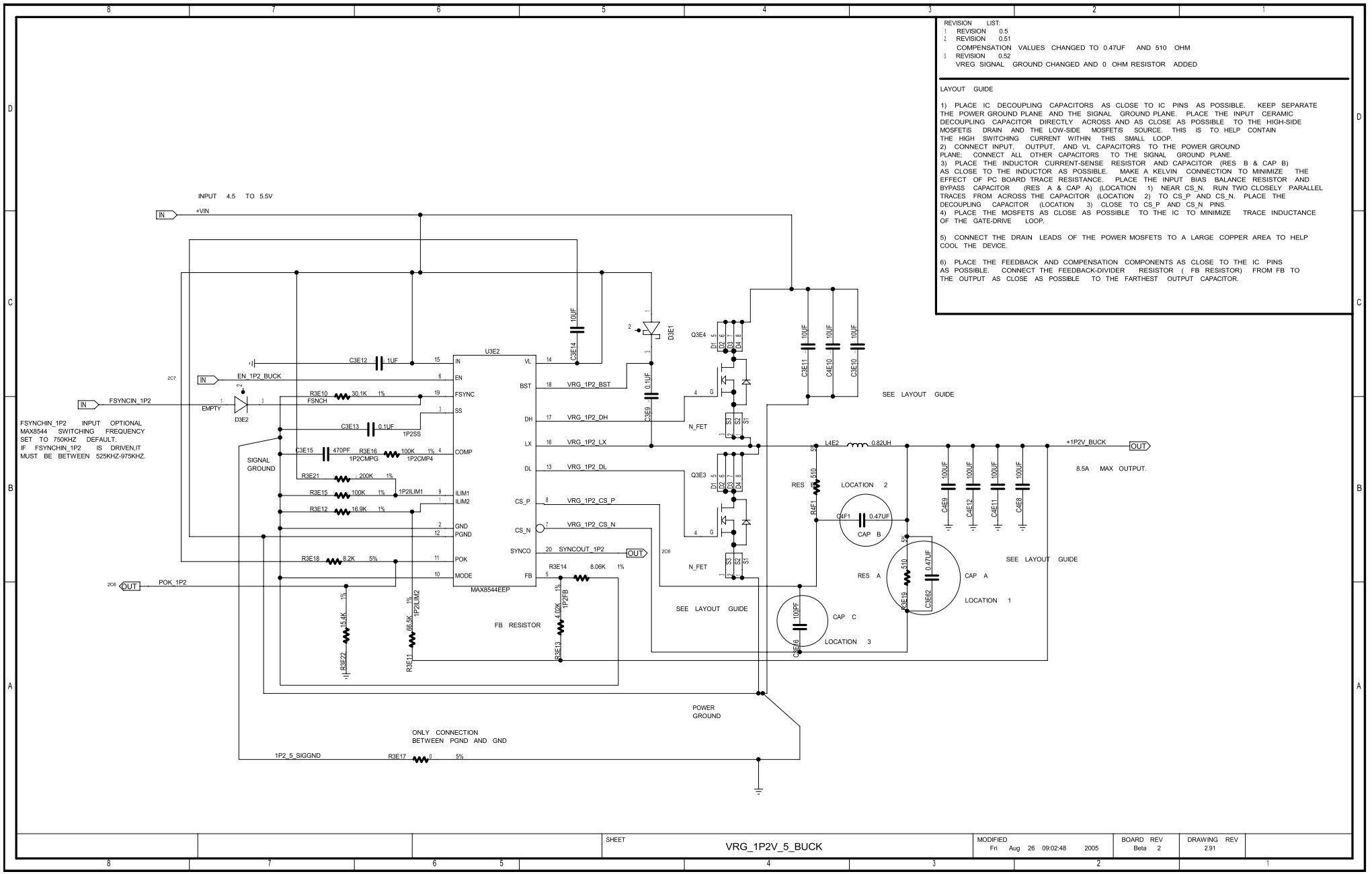
REVISION 0.5 INITIAL RELEASE.
REVISION 0.51 ADDED NO_BACKANNOTATE ATTRIBUTE.

LAYOUT GUIDE

1. THE PACKAGE FEATURES AN EXPOSED THERMAL PAD ON ITS UNDERSIDE. THIS PAD LOWERS THE THERMAL RESISTANCE OF THE PACKAGE BY PROVIDING A DIRECT HEAT CONDUCTION PATH FROM THE DIE TO THE PC BOARD. ADDITIONALLY, THE GROUND PIN (GND) PERFORM THE DUAL FUNCTION OF PROVIDING AN ELECTRICAL CONNECTION TO SYSTEM GROUND AND CHANNELING HEAT AWAY. CONNECT THE EXPOSED BACKSIDE PAD AND GND TO THE SYSTEM GROUND USING A LARGE PAD OR GROUND PLANE, OR MULTIPLE VIAS TO THE GROUND-PLANE LAYER.

SHEET	MODIFIED	BOARD REV	DRAWING REV
VREG 1P8V LINEAR (NOT POPULATED)	Fri Dec 23 18:31:11 2005	Beta 2	2.91


REVISION LIST
1 REVISION 0.5
2 REVISION 0.51
COMPENSATION CIRCUIT VALUES CHANGED TO 0.47UF AND 510 OHM
3 REVISION 0.52
VREG GROUND PLANE CHANGED AND 0 OHM RESISTOR ADDED
LAYOUT GUIDE
1) PLACE IC DECOUPLING CAPACITORS AS CLOSE TO IC PINS AS POSSIBLE. KEEP SEPARATE THE POWER GROUND PLANE AND THE SIGNAL GROUND PLANE. PLACE THE INPUT CERAMIC DECOUPLING CAPACITOR DIRECTLY ACROSS AND AS CLOSE AS POSSIBLE TO THE HIGH-SIDE MOSFETS DRAIN AND THE LOW-SIDE MOSFETS SOURCE. THIS IS TO HELP CONTAIN THE HIGH SWITCHING CURRENT WITHIN THIS SMALL LOOP.
2) CONNECT INPUT, OUTPUT, AND VL CAPACITORS TO THE POWER GROUND PLANE; CONNECT ALL OTHER CAPACITORS TO THE SIGNAL GROUND PLANE.
3) PLACE THE INDUCTOR CURRENT-SENSE RESISTOR AND CAPACITOR AS CLOSE TO THE INDUCTOR AS POSSIBLE. MAKE A KELVIN CONNECTION TO MINIMIZE THE EFFECT OF PC BOARD TRACE RESISTANCE. PLACE THE INPUT BIAS BALANCE RESISTOR AND BYPASS CAPACITOR (LOCATION 1) NEAR CS_N. RUN TWO CLOSELY PARALLEL TRACES FROM ACROSS THE CAPACITOR (LOCATION 2) TO CS_P AND CS_N. PLACE THE DECOUPLING CAPACITOR (LOCATION 3) CLOSE TO CS_P AND CS_N PINS.
4) PLACE THE MOSFETS AS CLOSE AS POSSIBLE TO THE IC TO MINIMIZE TRACE INDUCTANCE OF THE GATE-DRIVE LOOP.
5) CONNECT THE DRAIN LEADS OF THE POWER MOSFETS TO A LARGE COPPER AREA TO HELP COOL THE DEVICE.
6) PLACE THE FEEDBACK AND COMPENSATION COMPONENTS AS CLOSE TO THE IC PINS AS POSSIBLE. CONNECT THE FEEDBACK-DIVIDER RESISTOR FROM FB TO THE OUTPUT AS CLOSE AS POSSIBLE TO THE FARTHEST OUTPUT CAPACITOR.
INPUT 4.5V - 5.5V
+VIN
FSYNCIN_1P8 INPUT OPTIONAL
MAX8544 SWITCHING FREQUENCY
SET TO 750 KHZ DEFAULT.
IF FSYNCIN_1P8 IS DRIVEN,IT MUST
BE BETWEEN 525KHZ-975KHZ.
SIGNAL GROUND
POWER GROUND
ONLY CONNECTION
BETWEEN PGND AND GND
R3E5 0 5%
1P8V_SIGGND
U3E3
MAX8544EEP
IN
EN
FSYNC
SS
COMP
ILIM1
ILIM2
GND
PGND
POK
MODE
VL
BST
DH
LX
DL
CS_P
CS_N
SYNCO
FB
EN_1P8_BUCK
FSYNCIN_1P8
POK_1P8
VRG_1P8V_BST
VRG_1P8V_DH
VRG_1P8V_LX
VRG_1P8V_DL
VRG_1P8V_CS_P
VRG_1P8V_CS_N
SYNCOUT_1P8
C3E3 1UF
C3E1 10UF
C3D3 0.1UF
C3D8 0.1UF
C3D9 390PF
R3D2 30.1K 1%
R3D7 150K 1%
1P8CMP
1P8CMP4
R3E8 200K 1%
R3E3 100K 1%
R3D4 13.3K 1%
R3E6 8.2K 5%
R3D3 100K 1%
R3E1 10.2K 1%
1P8FB
R3D8 8.06K 1%
D3D2
D3D1
Q3E2
Q3E1
N_FET
C3D5 10UF
C4D7 10UF
C3D4 10UF
L4E1 0.82UH
+1P8V_BUCK
7.2A MAX OUTPUT
R4E3 510 5%
C4E5 0.47UF
C4E2 100UF
C4E1 100UF
C4D5 100UF
C4D6 100UF
R3E7 510 5%
C3E7 0.47UF
C2E5 100PF
SEE LAYOUT GUIDE LOCATION 1
SEE LAYOUT GUIDE LOCATION 2
SEE LAYOUT GUIDE LOCATION 3
SHEET
VRG 1P8V_5_BUCK
MODIFIED
Fri Aug 12 12:19:51 2005
BOARD REV
Beta 2
DRAWING REV
2.91


REVISION LIST:
1. REVISION 0.5
2. REVISION 0.51
COMPENSATION VALUES CHANGED TO 0.47UF AND 510 OHM
3. REVISION 0.52
VREG SIGNAL GROUND CHANGED AND 0 OHM RESISTOR ADDED
LAYOUT GUIDE
1) PLACE IC DECOUPLING CAPACITORS AS CLOSE TO IC PINS AS POSSIBLE. KEEP SEPARATE THE POWER GROUND PLANE AND THE SIGNAL GROUND PLANE. PLACE THE INPUT CERAMIC DECOUPLING CAPACITOR DIRECTLY ACROSS AND AS CLOSE AS POSSIBLE TO THE HIGH-SIDE MOSFETIS DRAIN AND THE LOW-SIDE MOSFETIS SOURCE. THIS IS TO HELP CONTAIN THE HIGH SWITCHING CURRENT WITHIN THIS SMALL LOOP.
2) CONNECT INPUT, OUTPUT, AND VL CAPACITORS TO THE POWER GROUND PLANE; CONNECT ALL OTHER CAPACITORS TO THE SIGNAL GROUND PLANE.
3) PLACE THE INDUCTOR CURRENT-SENSE RESISTOR AND CAPACITOR (RES B & CAP B) AS CLOSE TO THE INDUCTOR AS POSSIBLE. MAKE A KELVIN CONNECTION TO MINIMIZE THE EFFECT OF PC BOARD TRACE RESISTANCE. PLACE THE INPUT BIAS BALANCE RESISTOR AND BYPASS CAPACITOR (RES A & CAP A) (LOCATION 1) NEAR CS_N. RUN TWO CLOSELY PARALLEL TRACES FROM ACROSS THE CAPACITOR (LOCATION 2) TO CS_P AND CS_N. PLACE THE DECOUPLING CAPACITOR (LOCATION 3) CLOSE TO CS_P AND CS_N PINS.
4) PLACE THE MOSFETS AS CLOSE AS POSSIBLE TO THE IC TO MINIMIZE TRACE INDUCTANCE OF THE GATE-DRIVE LOOP.
5) CONNECT THE DRAIN LEADS OF THE POWER MOSFETS TO A LARGE COPPER AREA TO HELP COOL THE DEVICE.
6) PLACE THE FEEDBACK AND COMPENSATION COMPONENTS AS CLOSE TO THE IC PINS AS POSSIBLE. CONNECT THE FEEDBACK-DIVIDER RESISTOR (FB RESISTOR) FROM FB TO THE OUTPUT AS CLOSE AS POSSIBLE TO THE FARTHEST OUTPUT CAPACITOR.
INPUT 4.5 TO 5.5V
+VIN
IN
U3E2
MAX8544EEP
EN_1P2_BUCK
FSYNCIN_1P2
EMPTY
D3E2
FSYNCHIN_1P2 INPUT OPTIONAL
MAX8544 SWITCHING FREQUENCY
SET TO 750KHZ DEFAULT.
IF FSYNCHIN_1P2 IS DRIVEN,IT
MUST BE BETWEEN 525KHZ-975KHZ.
SIGNAL GROUND
C3E12 1UF
C3E13 0.1UF 1P2SS
C3E15 470PF
R3E16 100K 1% 1P2CMP4
1P2CMPG
R3E10 30.1K 1% FSNCH
R3E21 200K 1%
R3E15 100K 1% 1P2ILIM1
R3E12 16.9K 1%
R3E18 8.2K 5%
POK_1P2
R3E22 15.4K 1%
R3E11 66.5K 1% 1P2ILIM2
R3E14 8.06K 1%
R3E13 4.02K 1% 1P2FB
FB RESISTOR
C3E14 10UF
D3E1
0.1UF C3E9
Q3E4
Q3E3
N_FET
SEE LAYOUT GUIDE
C3E11 10UF
C4E10 10UF
C3E10 10UF
L4E2 0.82UH
+1P2V_BUCK
8.5A MAX OUTPUT.
RES B 510
R4F1
LOCATION 2
C4F1 0.47UF
CAP B
C4E9 100UF
C4E12 100UF
C4E11 100UF
C4E8 100UF
RES A 510
R3E19
C3E62 0.47UF
CAP A
LOCATION 1
C3E16 100PF
CAP C
LOCATION 3
VRG_1P2_BST
VRG_1P2_DH
VRG_1P2_LX
VRG_1P2_DL
VRG_1P2_CS_P
VRG_1P2_CS_N
SYNCOUT_1P2
POWER GROUND
ONLY CONNECTION
BETWEEN PGND AND GND
1P2_5_SIGGND
R3E17 0 5%
SHEET
VRG_1P2V_5_BUCK
MODIFIED
Fri Aug 26 09:02:48 2005
BOARD REV
Beta 2
DRAWING REV
2.91