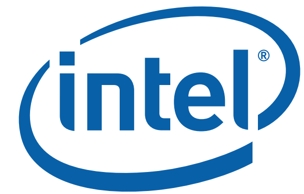
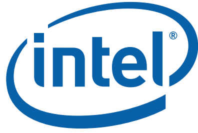


Host Bus Adapter Schematics for Intel(R) 8134x I/O Processors

February 2007

Order Number: 315367-002US



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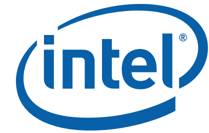

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15.0 DDR2 DIMM Socket 22

16.0 VTT Generation and DIMM Power 23

17.0 SAS Connector 4X1 Internal (Dual Stacked) 24

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19.0 SGPIO/ HD LED MUX 26

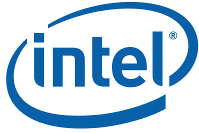
20.0 PCI-X Straddle Mount (SM) Slot 27

21.0 VREG 3P3V_BUCK 28

22.0 GBE_82545GM_Module - 1 29

23.0 GBE_82545GM_Module - 2 30

24.0 GBE_82545GM_Module - 3 31



25.0 Flash - 8M 32

26.0 NVSRAM...33

27.0 PBI Auxiliary Connector 34

28.0 CPLD Version A Module 35

29.0 Buzzer 36

30.0 RS232_Dual_MOD...37

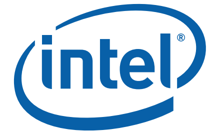
31.0 JTAG_CONN_Module 38

32.0 VREG +1P2V Linear (Not Populated)...39

33.0 VREG 1P8V Linear (Not Populated) 40

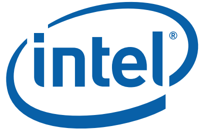
34.0 VREG 1P8V_5_BUCK 41

35.0 VREG 1P2V_BUCK 42



Revision History

Date	Revision	Description
February 2007	002	Added Differential Oscillator 125 MHz page.
September 2006	001	Initial release.



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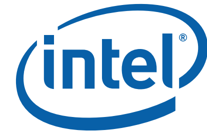


1.0 Schematics Overview

This manual provides the Host Bus Adapter schematics for Intel(R) 8134x I/O Processors.

1.1 Product Descriptions

The products available from Intel in the 8134x family include:

- Intel® 81348 I/O Processor-based host bus adapter with 8-port SAS/SATA controller.
- Intel® 81341 I/O Processor-based host bus adapter with one processing core.
- Intel® 81342 I/O Processor-based host bus adapter with two processing cores.
- Intel® 413808 I/O Controller-based host bus adapter with 8-port SAS/SATA controller and 800 MHz SAS engine
- Intel® 413812 I/O Controller-based host bus adapter with 8-port SAS/SATA controller and 1200 MHz SAS engine

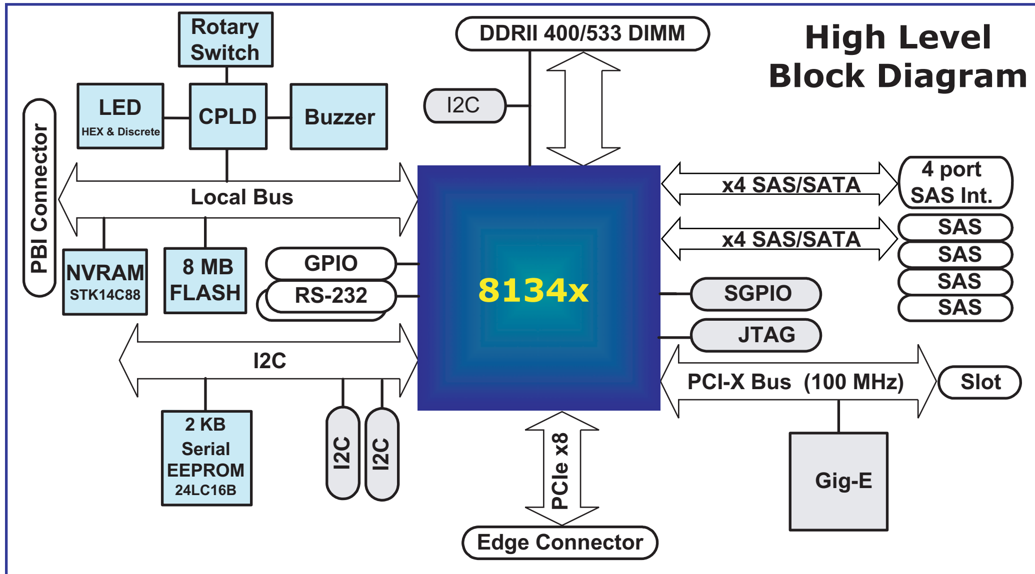
Note: The Intel® 81348 and Intel® 81341 and Intel® 81342 products are I/O Processors (8134x). The Intel® 413808 and Intel® 413812 products are I/O Controllers (4138xx). In this manual for simplicity, we refer to all products as "processors".

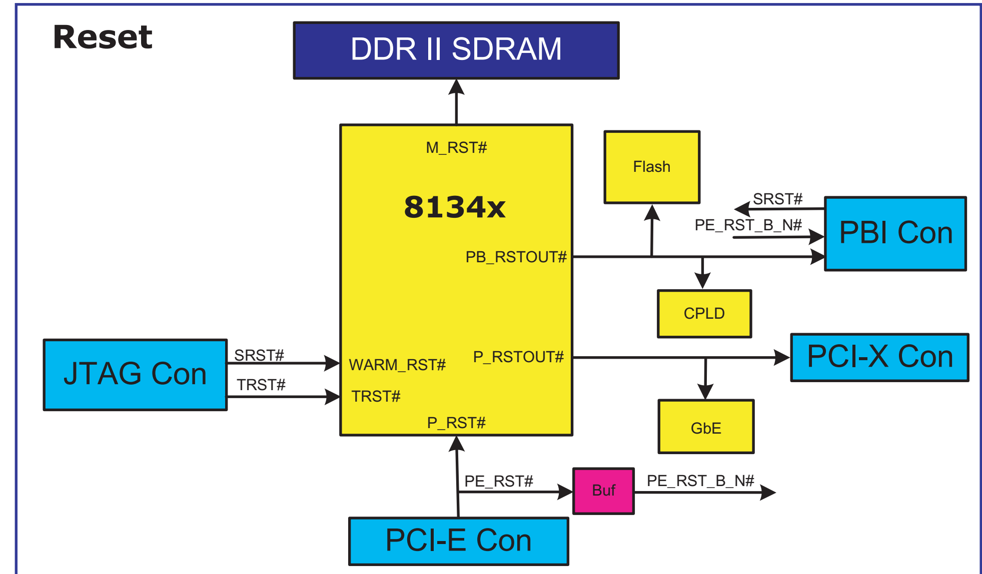
Contact your Intel Representative for more product information.

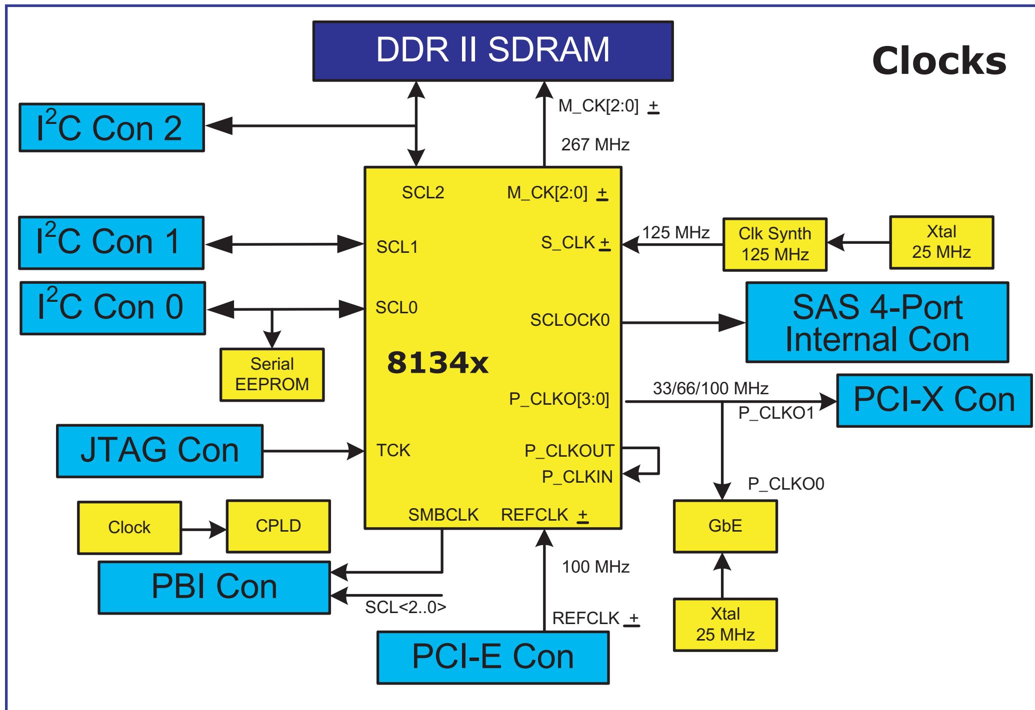
1.2 CRB Block Diagrams

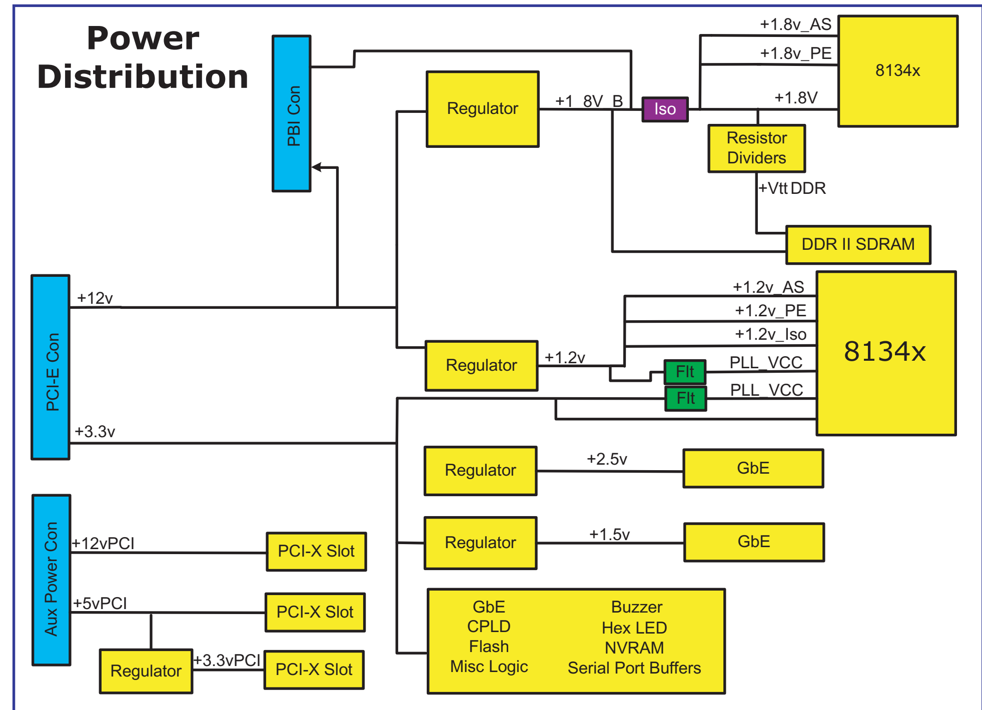
Figure 1 shows the product block diagrams.

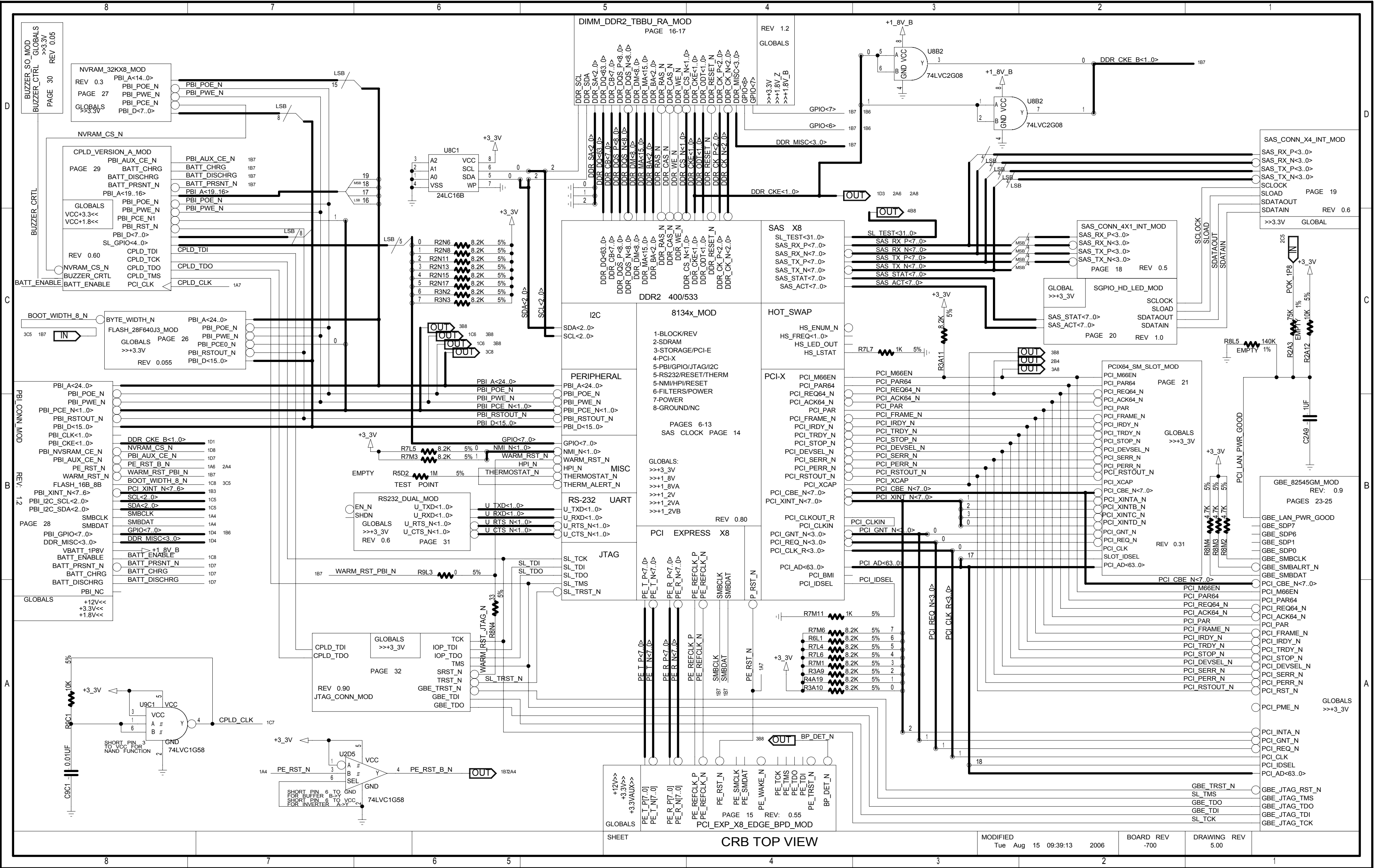
CRB Block Diagrams










DIMM_DDR2_TBBU_RA_MOD
PAGE 16-17
REV 1.2
GLOBALS
NVRAM_32KX8_MOD
CPLD_VERSION_A_MOD
FLASH_28F640J3_MOD
PBI_CONN_MOD
RS232_DUAL_MOD
JTAG_CONN_MOD
24LC16B
74LVC2G08
74LVC1G58
DDR2 400/533
8134x_MOD
1-BLOCK/REV
2-SDRAM
3-STORAGE/PCI-E
4-PCI-X
5-PBI/GPIO/JTAG/I2C
5-RS232/RESET/THERM
5-NMI/HPI/RESET
6-FILTERS/POWER
7-POWER
8-GROUND/NC
PAGES 6-13
SAS CLOCK PAGE 14
I2C
PERIPHERAL
MISC
RS-232 UART
JTAG
SAS X8
HOT_SWAP
PCI-X
PCI EXPRESS X8
SAS_CONN_X4_INT_MOD
SAS_CONN_4X1_INT_MOD
SGPIO_HD_LED_MOD
PCIX64_SM_SLOT_MOD
GBE_82545GM_MOD
PCI_EXP_X8_EDGE_BPD_MOD
CRB TOP VIEW
MODIFIED
Tue Aug 15 09:39:13 2006
BOARD REV
-700
DRAWING REV
5.00

SEQUENCING REQUIREMENT:
1.2V RAILS MUST TURN ON BEFORE OR EVEN WITH 1.8V RAILS
1.2V RAILS MUST TURN OFF AFTER OR EVEN WITH 1.8V RAILS

THIS CIRCUIT OPENS THE FET SLOWLY ON THE RISING EDGE OF POK_1P8 TO MINIMIZE INRUSH CURRENT.
IT CLOSES THE FET QUICKLY WHEN POK_1P8 IS GONE, TO MINIMIZE CURRENT DRAIN FROM THE BACKUP BATTERY.

THIS IS THE BATTERY BACKED +1_8V RAIL FOR THE DIMM

BULK DECOUPLING PLACEMENT NOT CRITICAL

THIS FET ISOLATES THE BATTERY BACKED RAIL FROM THE NON-BATTERY BACKED RAIL

THIS IS THE +1_8V RAIL FOR 8431x AND THE DDR2 TERMINATORS

1% VALUE USED FOR BOM CONSOLIDATION

THIS VOLTAGE SUPERVISOR PULLS POK_1P2 LOW WHEN +3_3V IS BELOW 2.7V.

THESE TWO FETS CREATE AN INVERTED AND NON-INVERTED COPY OF POK_1P8 AT A 12V LEVEL TO DRIVE THE FET GATE

THIS VOLTAGE SUPERVISOR PULLS POK_1P2 LOW WHEN +12V IS BELOW 10.1V.

THIS NFET DRAINS +1_8V WHEN THE 1.8V ENABLE SIGNAL IS NOT ASSERTED

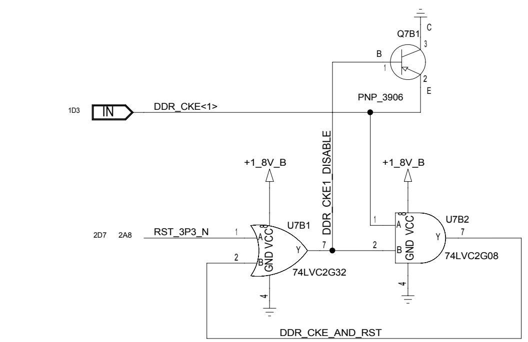
DRIVING THE 1P8V ENABLE INPUTS WITH THE 1.2V POK SIGNALS FORCES 1.8V RAILS TO POWER-UP AFTER THE 1.2V RAILS.

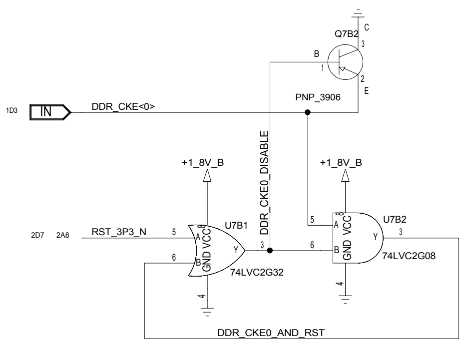
THIS CIRCUIT WILL ENABLE THE +1_8V DRAIN SLOWLY, BUT DISABLE IT QUICKLY WHEN THE 1.8V ENABLE SIGNAL IS ASSERTED

SPC CAPS, CAN BE RUN AT 90% RATING

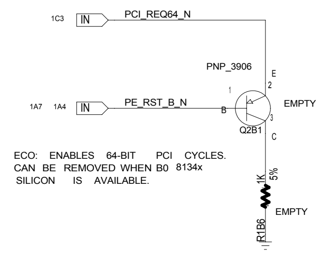
THESE RESISTORS ARE POPULATED BECAUSE THE LINEAR REGULATORS HAVE BEEN DEPOPULATED.

+1.8V FOR 8431x
+1.8V_B IS FOR DIMM
+1.8V_Z IS FOR TERMINATIONS
8431x AND TERMINATIONS CAN BE THE SAME RAIL

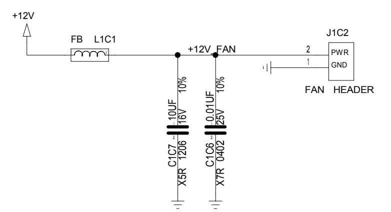




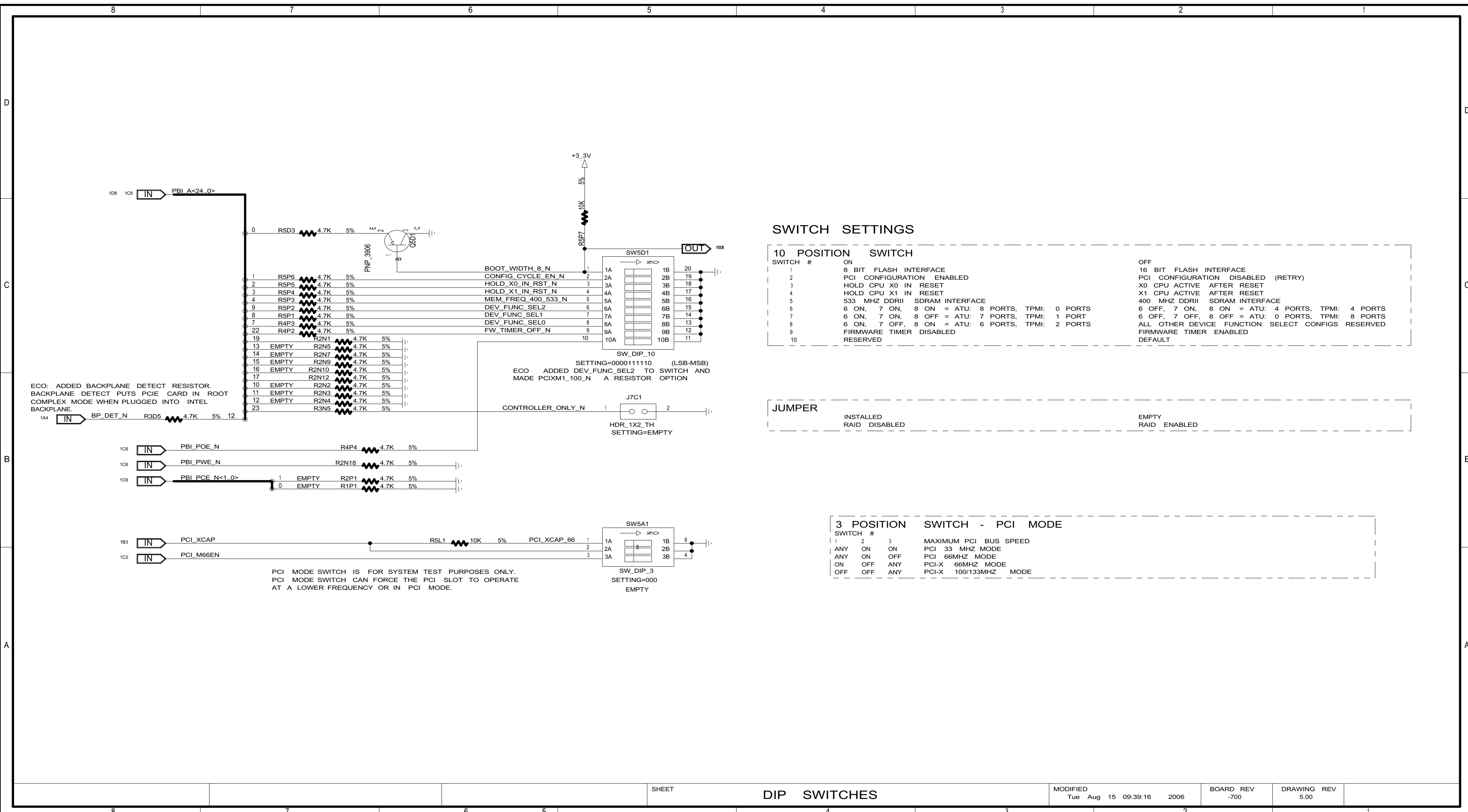
CKE LATCH CIRCUIT ONLY REQUIRED FOR BATTERY BACKED MEMORY IMPLEMENTATIONS.



ECO: ENABLES 64-BIT PCI CYCLES. CAN BE REMOVED WHEN B0 8134x SILICON IS AVAILABLE.



SHEET	POWER REGULATORS TOP VIEW	MODIFIED Tue Aug 15 09:39:15 2006	BOARD REV -700	DRAWING REV 5.00



PBI_A<24..0>
+3_3V
R5P7 10K 5%
PNP_3906
Q5D1
OUT
SW5D1
BOOT_WIDTH_8_N
CONFIG_CYCLE_EN_N
HOLD_X0_IN_RST_N
HOLD_X1_IN_RST_N
MEM_FREQ_400_533_N
DEV_FUNC_SEL2
DEV_FUNC_SEL1
DEV_FUNC_SEL0
FW_TIMER_OFF_N
SW_DIP_10
SETTING=0000111110 (LSB-MSB)
ECO ADDED DEV_FUNC_SEL2 TO SWITCH AND MADE PCIXM1_100_N A RESISTOR OPTION
ECO: ADDED BACKPLANE DETECT RESISTOR. BACKPLANE DETECT PUTS PCIE CARD IN ROOT COMPLEX MODE WHEN PLUGGED INTO INTEL BACKPLANE.
BP_DET_N
CONTROLLER_ONLY_N
J7C1
HDR_1X2_TH
SETTING=EMPTY
PBI_POE_N
PBI_PWE_N
PBI_PCE_N<1..0>
PCI_XCAP
PCI_M66EN
PCI_XCAP_66
SW5A1
SW_DIP_3
SETTING=000
EMPTY
PCI MODE SWITCH IS FOR SYSTEM TEST PURPOSES ONLY. PCI MODE SWITCH CAN FORCE THE PCI SLOT TO OPERATE AT A LOWER FREQUENCY OR IN PCI MODE.
SWITCH SETTINGS
10 POSITION SWITCH
SWITCH # | ON | OFF
1 | 8 BIT FLASH INTERFACE | 16 BIT FLASH INTERFACE
2 | PCI CONFIGURATION ENABLED | PCI CONFIGURATION DISABLED (RETRY)
3 | HOLD CPU X0 IN RESET | X0 CPU ACTIVE AFTER RESET
4 | HOLD CPU X1 IN RESET | X1 CPU ACTIVE AFTER RESET
5 | 533 MHZ DDRII SDRAM INTERFACE | 400 MHZ DDRII SDRAM INTERFACE
6 | 6 ON, 7 ON, 8 ON = ATU: 8 PORTS, TPMI: 0 PORTS | 6 OFF, 7 ON, 8 ON = ATU: 4 PORTS, TPMI: 4 PORTS
7 | 6 ON, 7 ON, 8 OFF = ATU: 7 PORTS, TPMI: 1 PORT | 6 OFF, 7 OFF, 8 OFF = ATU: 0 PORTS, TPMI: 8 PORTS
8 | 6 ON, 7 OFF, 8 ON = ATU: 6 PORTS, TPMI: 2 PORTS | ALL OTHER DEVICE FUNCTION SELECT CONFIGS RESERVED
9 | FIRMWARE TIMER DISABLED | FIRMWARE TIMER ENABLED
10 | RESERVED | DEFAULT
JUMPER
INSTALLED | EMPTY
RAID DISABLED | RAID ENABLED
3 POSITION SWITCH - PCI MODE
SWITCH # 1 2 3 | MAXIMUM PCI BUS SPEED
ANY ON ON | PCI 33 MHZ MODE
ANY ON OFF | PCI 66MHZ MODE
ON OFF ANY | PCI-X 66MHZ MODE
OFF OFF ANY | PCI-X 100/133MHZ MODE
SHEET
DIP SWITCHES
MODIFIED Tue Aug 15 09:39:16 2006
BOARD REV -700
DRAWING REV 5.00

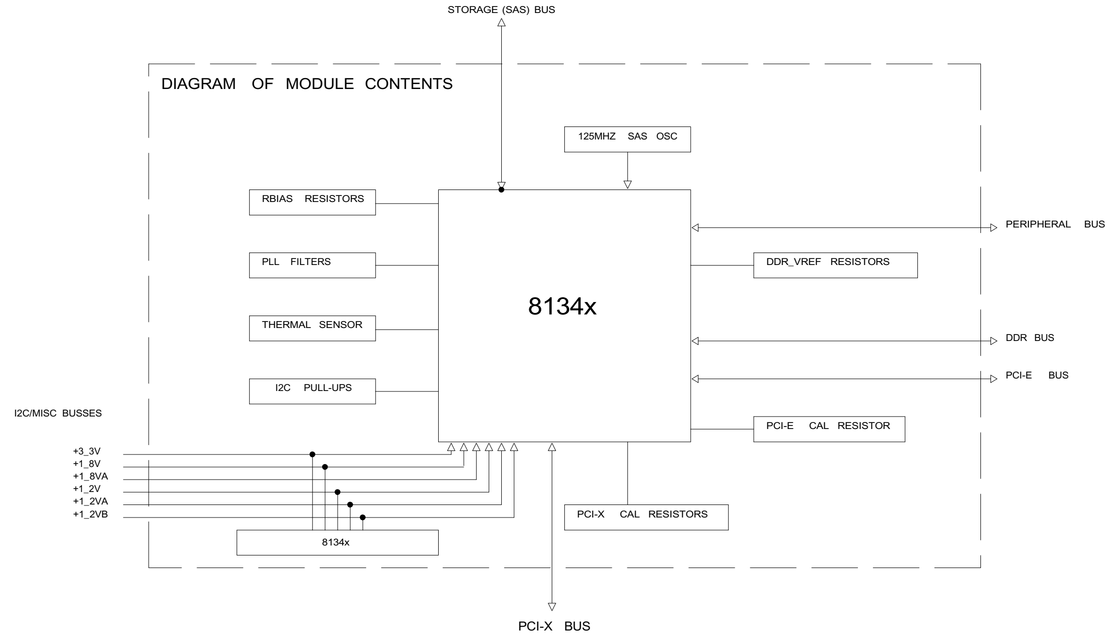
8 7 6 5 4 3 2 1

8134x MODULE

2 - SDRAM
3 - STORAGE/PCI-EXPRESS
4 - PCI-X BUS
5 - PERIPHERAL BUS/MISC
6 - POWER/FILTERS
7 - POWER
8 - GROUND/NO CONNECTS

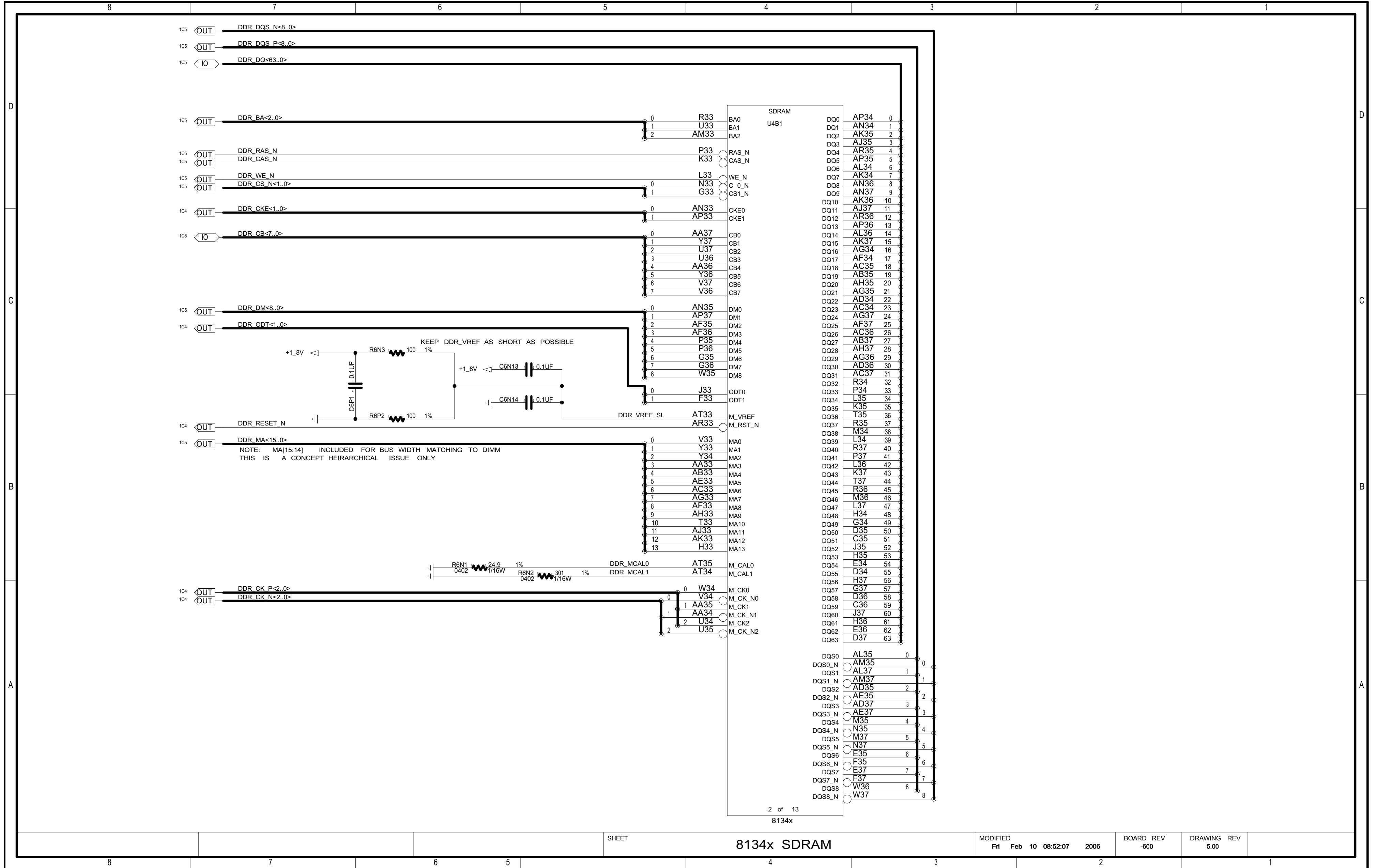
REVISIONS

0.3 - SEP 18: PINOUT CHANGES INCORPORATED
0.4 - SEP 29: PORT NAME CHANGES, CORRECT DDR CLOCK SWAPPING
0.5 - SEP 29: RELEASE FOR CHECK
0.51- OCT 01: PCI_REQ64 -> PCI_REQ64_N
0.52- OCT 05: MOST OF THE BLOCK REVIEW FEEDBACK INC.
0.53- OCT 12: FIX REQ0 AND GNT0 DIRECTIONS
0.54 OCT 12: RESIZED MODULE SYMBOL
0.55 OCT 19: REMOVED SOME DECOUPLING, CHANGED SOME TO 0603
0.56 OCT 28: CHANGED DDR_MCAL1 SIZE TO 0402
0.57 OCT 29: ADDED PULLUPS ON SMB SIGNALS AND WARM_RST_N
0.58 NOV 1: ADJUSTED DECOUPLING TO NEW RECOMMENDATIONS
0.59 NOV 10: ADDED SL_TEST <31..0>
0.60 DEC 9: CHANGED 4.7NH IND TO -024
0.70 DEC 14: ADDED PCI_CLKOUT_R AND PCI_CLKIN
MOVED P_RST_N PIN, FIXED TABLE OF CONTENTS
0.71 JAN 7: ADDED 5PF CAP TO PCI_CLKIN
GROUNDED VSSPLLS0 AND VSSPLLS1
CHANGED PIN AN8 TO PUR1
CHANGED I2C PULLUPS TO 3.3K
0.72 FEB 28: ECO8: RENAMED VECTORED NETS TO HAVE VECTOR LAST
0.73 MAR 08: RENAMED PLL_VCC13P3_L_X NET TO PLL_VCC3P3_L_X
CHANGED 14 DECOUPLING CAPS TO EMPTY (NOT POPULATED)
0.74 APR 11: RENAMED S_CLK_N/P TO S_CLK0_N/P, SWAPPED ASSIGNMENTS OF PINS
H15 WITH H20 (S_CLK0_N WITH VSS) AND H16 WITH H21 (S_CLK0_P WITH VSS)
0.75 OCT 14: UPGRADED IOP TO A1 IPN
0.76 DEC 23: DEPOPULATED P_CLKIN CAP
ADDED PULL-DOWN RESISTOR OPTION TO PUR1 PIN
0.80 FEB 10: MODIFIED SL PART FOR 800MHZ B0 VERSION

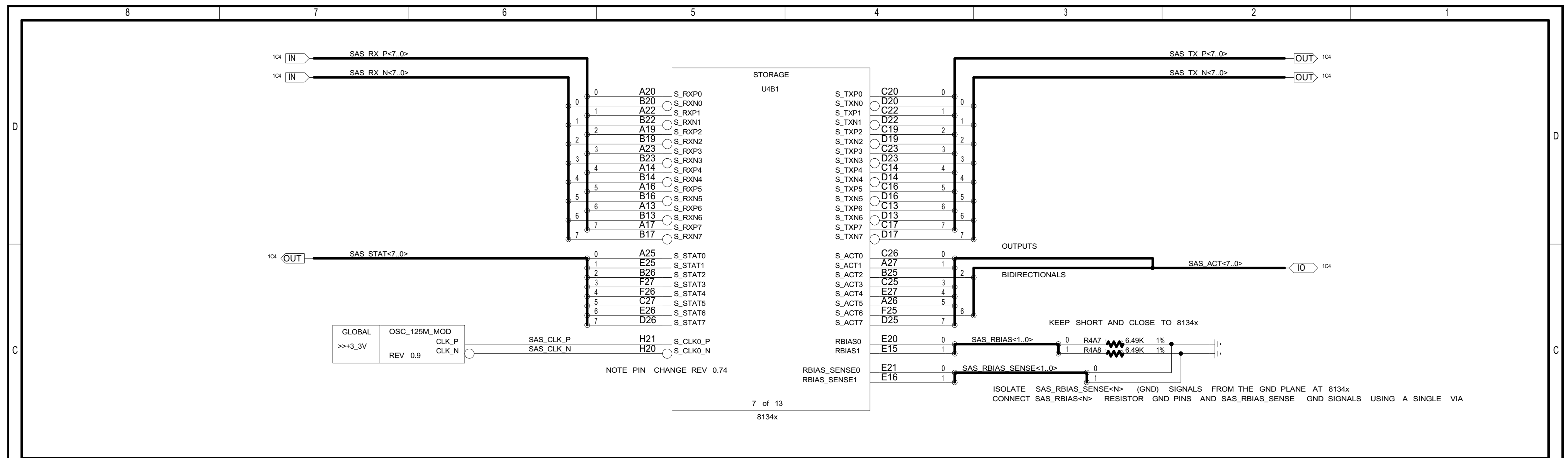


SHEET	8134x MODULE CONTENTS	MODIFIED Fri Feb 10 08:54:38 2006	BOARD REV -600	DRAWING REV 5.00

8 7 6 5 4 3 2 1



DDR_DQS_N<8..0>
DDR_DQS_P<8..0>
DDR_DQ<63..0>
DDR_BA<2..0>
DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_CS_N<1..0>
DDR_CKE<1..0>
DDR_CB<7..0>
DDR_DM<8..0>
DDR_ODT<1..0>
KEEP DDR_VREF AS SHORT AS POSSIBLE
DDR_RESET_N
DDR_MA<15..0>
NOTE: MA[15:14] INCLUDED FOR BUS WIDTH MATCHING TO DIMM
THIS IS A CONCEPT HEIRARCHICAL ISSUE ONLY
DDR_VREF_SL
DDR_MCAL0
DDR_MCAL1
DDR_CK_P<2..0>
DDR_CK_N<2..0>
SDRAM
U4B1
2 of 13
8134x
SHEET
8134x SDRAM
MODIFIED
Fri Feb 10 08:52:07 2006
BOARD REV
-600
DRAWING REV
5.00



PCI-EXPRESS
U4B1

PE_REFCLK_P AK20 REFCLKP
PE_REFCLK_N AK19 REFCLKN
R4D1 1.4K 1% PE_CAL_P AN20 PE_CALP
PE_CAL_N AN19 PE_CALN
PE_R_P<7..0>
PE_R_N<7..0>

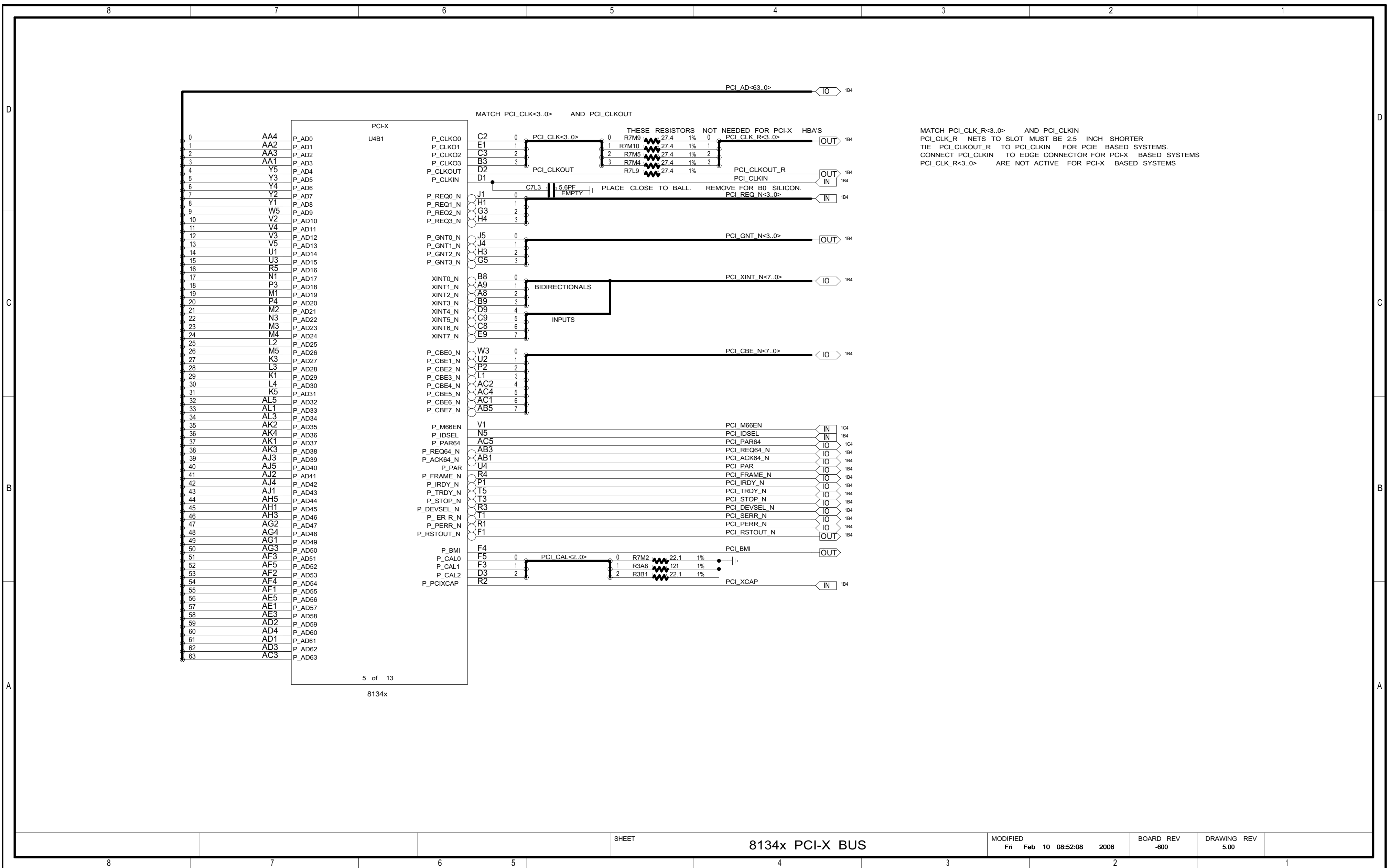
PERP0 PERN0 PERP1 PERN1 PERP2 PERN2 PERP3 PERN3 PERP4 PERN4 PERP5 PERN5 PERP6 PERN6 PERP7 PERN7
AU14 AT14 AU15 AT15 AU17 AT17 AU18 AT18 AU20 AT20 AU21 AT21 AU23 AT23 AU24 AT24

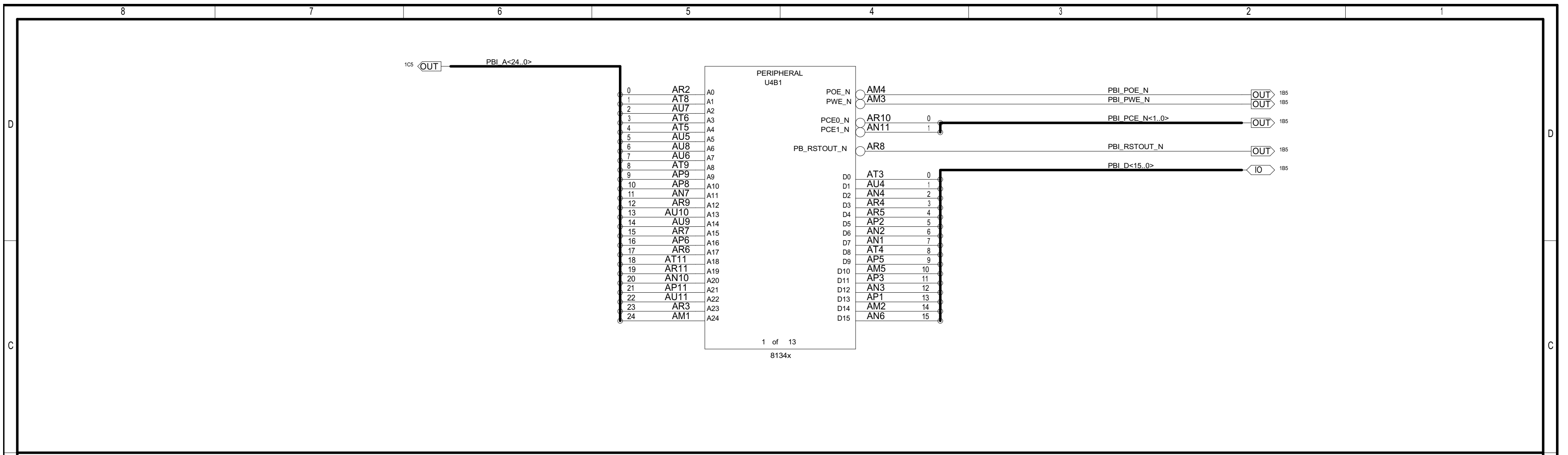
PETP0 PETN0 PETP1 PETN1 PETP2 PETN2 PETP3 PETN3 PETP4 PETN4 PETP5 PETN5 PETP6 PETN6 PETP7 PETN7
AR14 AP14 AR15 AP15 AR17 AP17 AR18 AP18 AR20 AP20 AR21 AP21 AR23 AP23 AR24 AP24

PE_T_P<7..0>
PE_T_N<7..0>

6 of 13
8134x

SHEET	8134x STORAGE / PCI-EXPRESS	MODIFIED Fri Feb 10 08:52:08 2006	BOARD REV -700	DRAWING REV 5.00


PCI_AD<63..0>
MATCH PCI_CLK<3..0> AND PCI_CLKOUT
THESE RESISTORS NOT NEEDED FOR PCI-X HBA'S
MATCH PCI_CLK_R<3..0> AND PCI_CLKIN
PCI_CLK_R NETS TO SLOT MUST BE 2.5 INCH SHORTER
TIE PCI_CLKOUT_R TO PCI_CLKIN FOR PCIE BASED SYSTEMS.
CONNECT PCI_CLKIN TO EDGE CONNECTOR FOR PCI-X BASED SYSTEMS
PCI_CLK_R<3..0> ARE NOT ACTIVE FOR PCI-X BASED SYSTEMS
PLACE CLOSE TO BALL. REMOVE FOR B0 SILICON.
BIDIRECTIONALS
INPUTS
PCI-X
U4B1
5 of 13
8134x
SHEET
8134x PCI-X BUS
MODIFIED
Fri Feb 10 08:52:08 2006
BOARD REV
-600
DRAWING REV
5.00



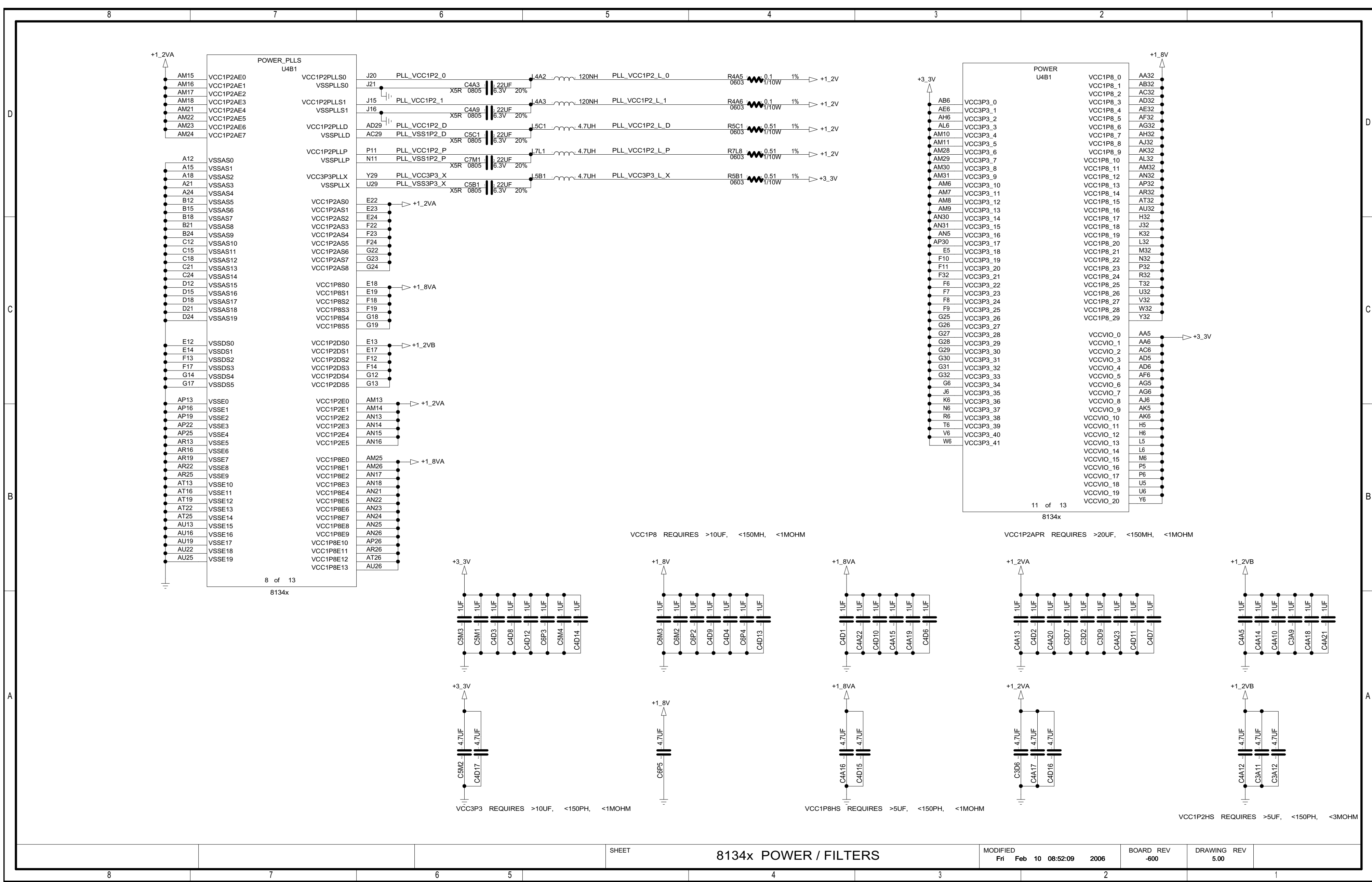
THERM_ALERT CAN BE USED TO GENERATE AN INTERRUPT

THERMOSTAT_N CAN BE USED TO CONTROL A FAN OR THROTTLE A CPU CLOCK

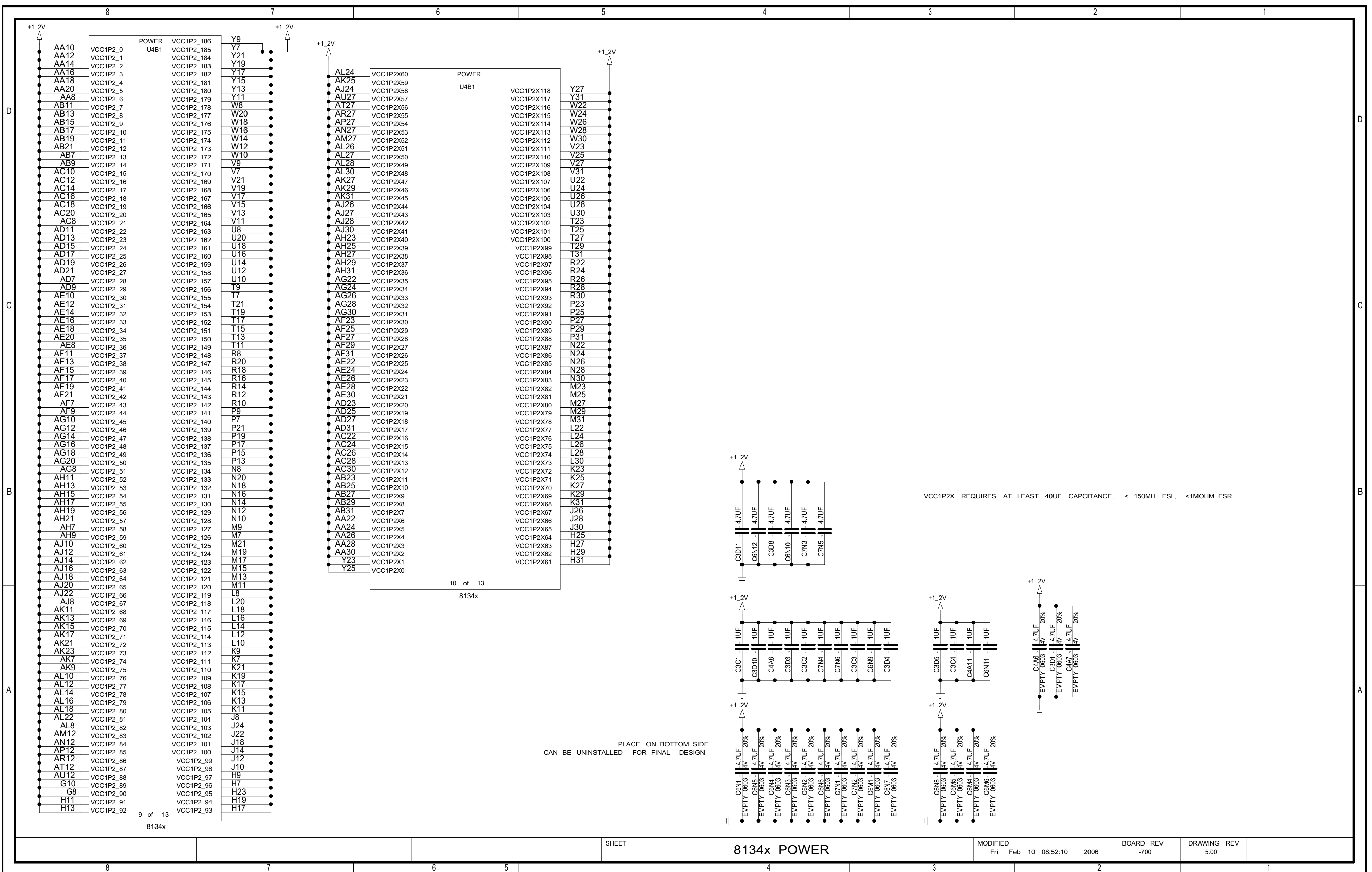
THERM_ADM1032ARM HAS INTERNAL THERMOMETER
AS WELL AS THERMAL DIODE ATTACHEMENT.
PLACE FOR MONITORING AMBIANT BOARD AIR

KEEP THERMDA AND THERMDC < 6 INCHES
ROUTE THERMDA AND THERMDC TOGETHER WITH GROUND GUARD TRACES ON EACH SIDE
KEEP SWITCHING SIGNALS AWAY FROM THERMDA AND THERMDC

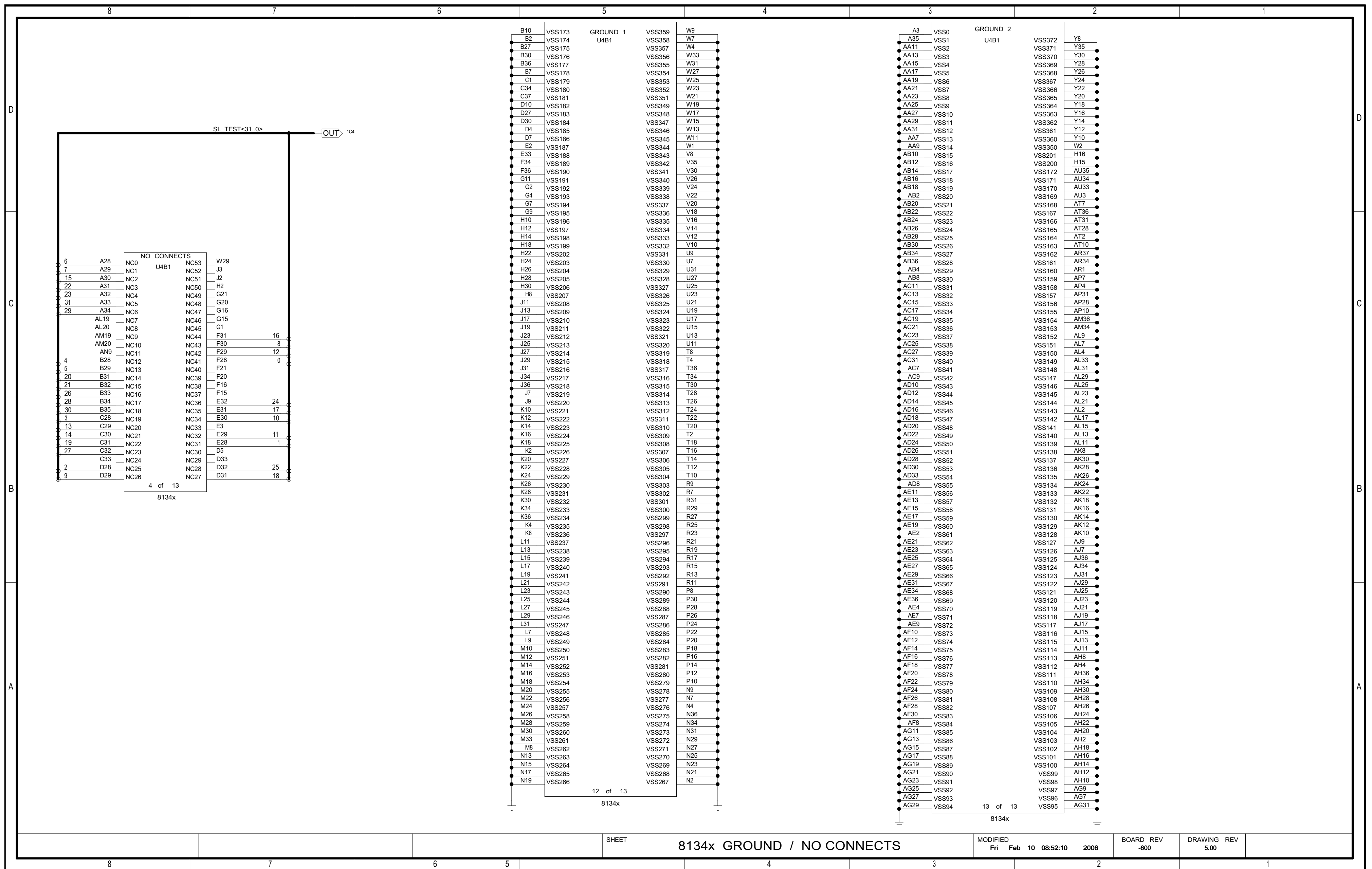
SHEET	MODIFIED	BOARD REV	DRAWING REV
8134x PERIPHERAL BUS / MISC	Fri Feb 10 08:52:09 2006	-700	5.00

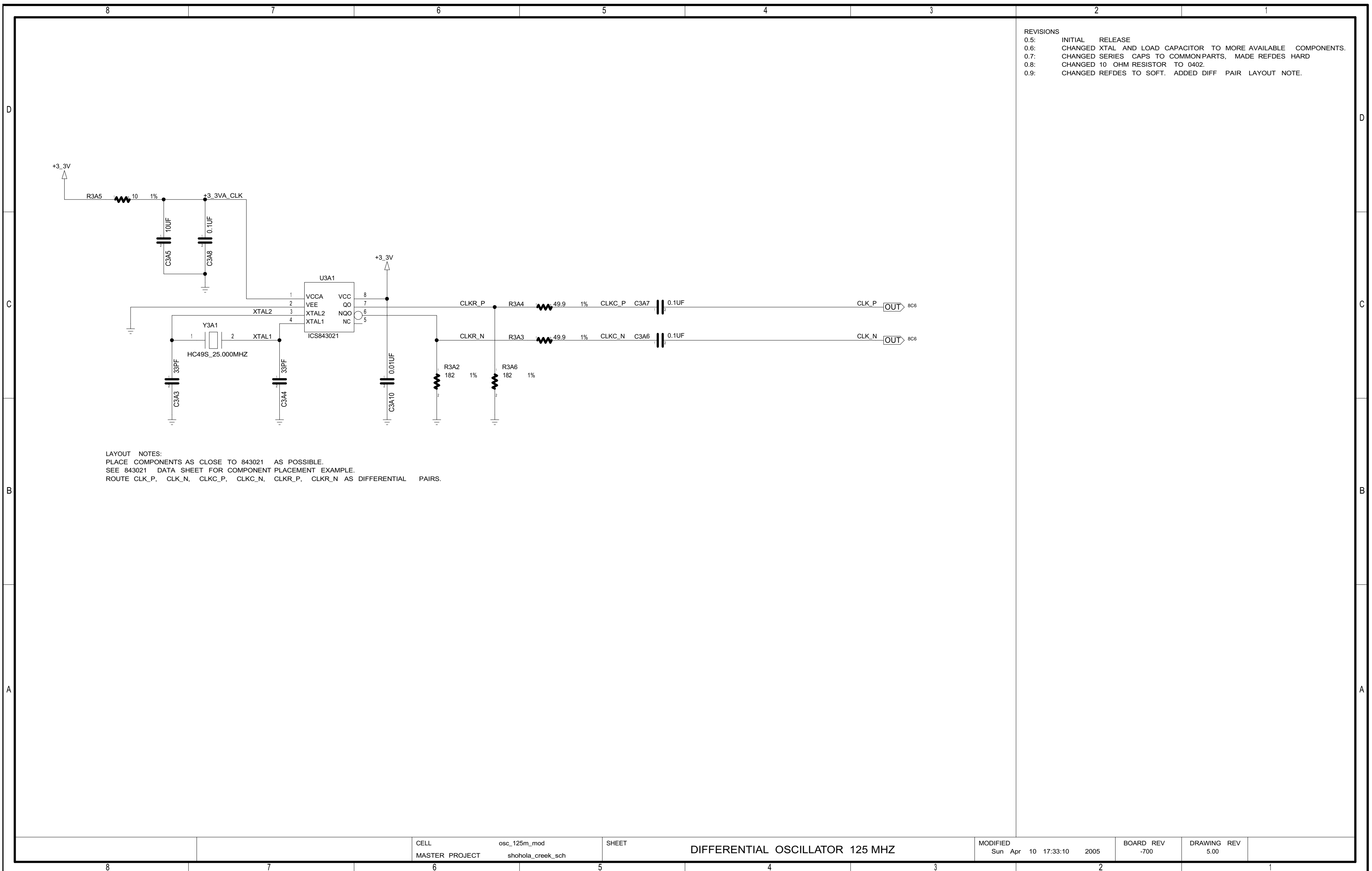


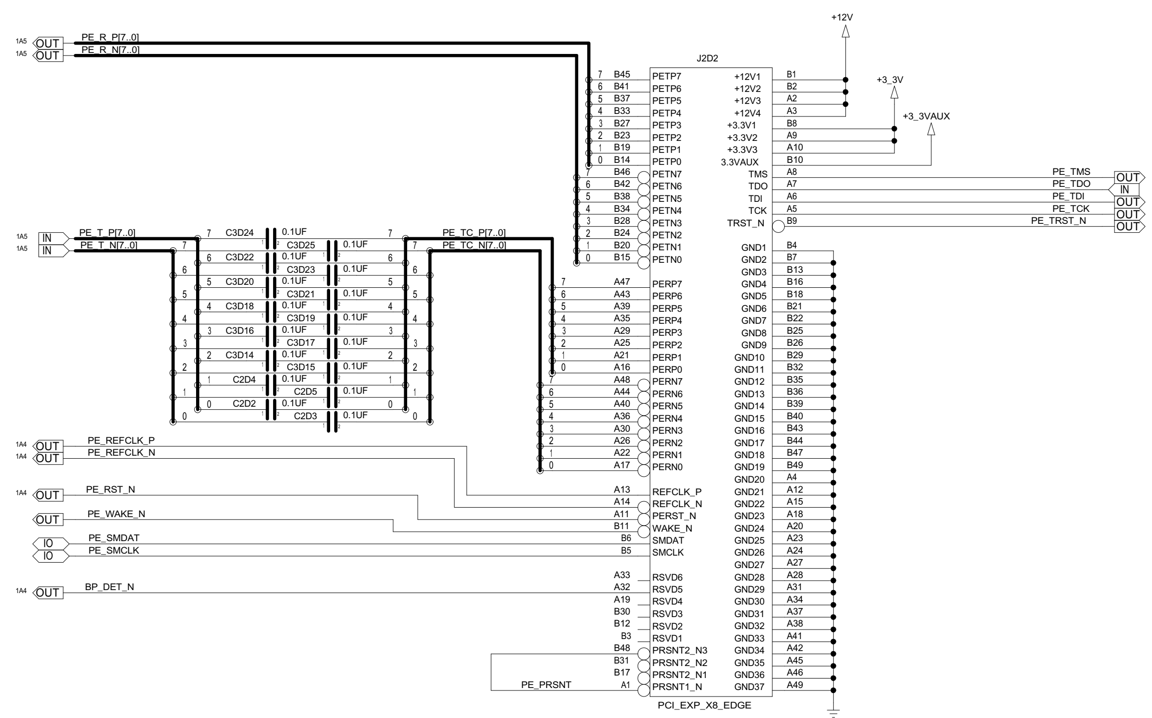
8134x POWER / FILTERS
POWER_PLLS
U4B1
POWER
VCC1P8 REQUIRES >10UF, <150MH, <1MOHM
VCC1P2APR REQUIRES >20UF, <150MH, <1MOHM
VCC3P3 REQUIRES >10UF, <150PH, <1MOHM
VCC1P8HS REQUIRES >5UF, <150PH, <1MOHM
VCC1P2HS REQUIRES >5UF, <150PH, <3MOHM
MODIFIED
Fri Feb 10 08:52:09 2006
BOARD REV
-600
DRAWING REV
5.00



VCC1P2X REQUIRES AT LEAST 40UF CAPCITANCE, < 150MH ESL, <1MOHM ESR.
PLACE ON BOTTOM SIDE
CAN BE UNINSTALLED FOR FINAL DESIGN
8134x POWER
MODIFIED
Fri Feb 10 08:52:10 2006
BOARD REV
-700
DRAWING REV
5.00


SL_TEST<31..0>
OUT
NO CONNECTS
U4B1
4 of 13
8134x
GROUND 1
U4B1
12 of 13
8134x
GROUND 2
U4B1
13 of 13
8134x
SHEET
8134x GROUND / NO CONNECTS
MODIFIED
Fri Feb 10 08:52:10 2006
BOARD REV
-600
DRAWING REV
5.00

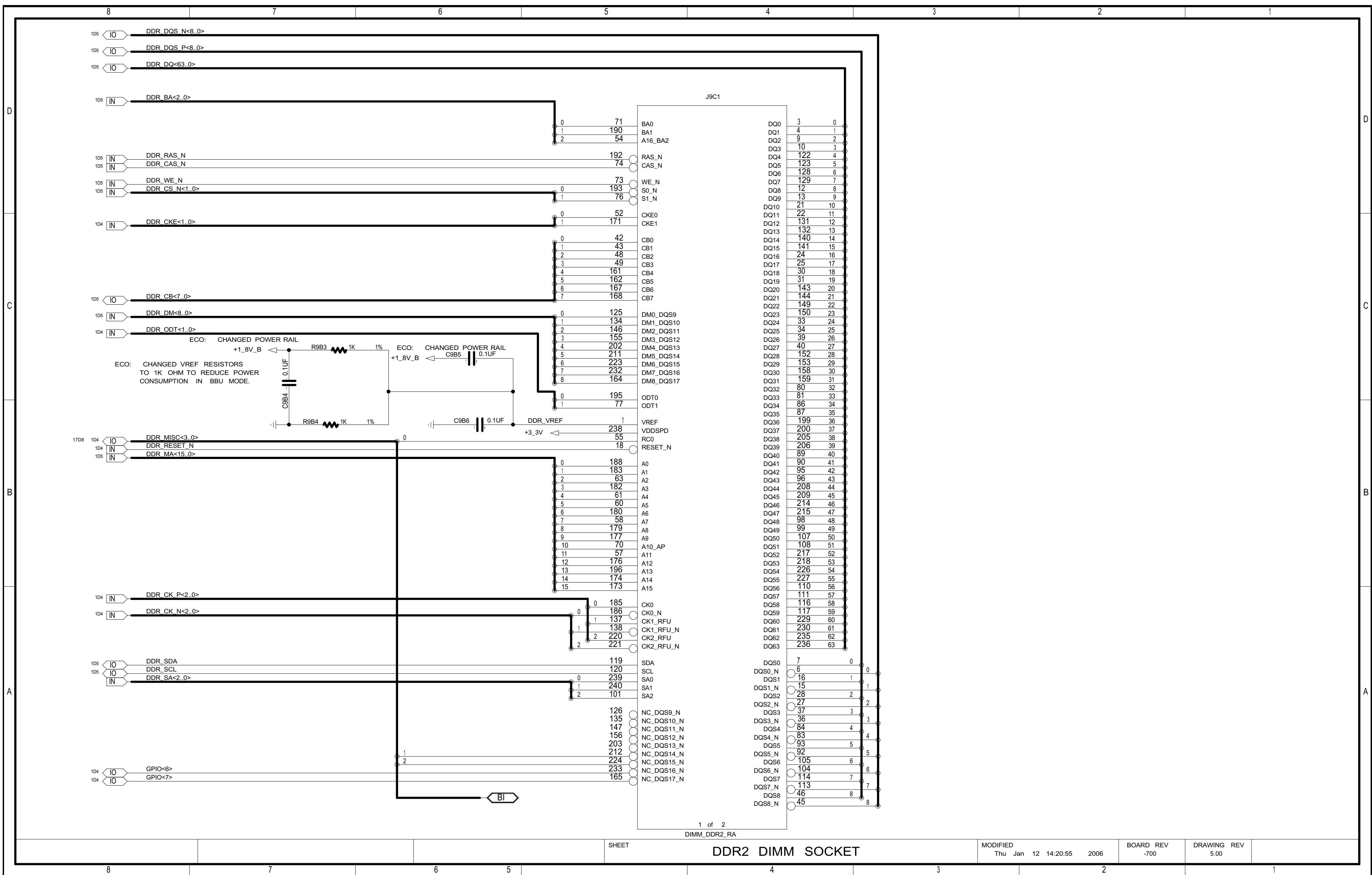

REVISIONS
0.5: INITIAL RELEASE
0.6: CHANGED XTAL AND LOAD CAPACITOR TO MORE AVAILABLE COMPONENTS.
0.7: CHANGED SERIES CAPS TO COMMON PARTS, MADE REFDES HARD
0.8: CHANGED 10 OHM RESISTOR TO 0402.
0.9: CHANGED REFDES TO SOFT. ADDED DIFF PAIR LAYOUT NOTE.
+3_3V
R3A5 10 1%
+3_3VA_CLK
10UF C3A5
0.1UF C3A8
U3A1
VCCA VEE XTAL2 XTAL1 VCC QO NQO NC
ICS843021
XTAL2
XTAL1
Y3A1
HC49S_25.000MHZ
33PF C3A3
33PF C3A4
0.01UF C3A10
CLKR_P R3A4 49.9 1% CLKC_P C3A7 0.1UF CLK_P OUT 8C6
CLKR_N R3A3 49.9 1% CLKC_N C3A6 0.1UF CLK_N OUT 8C6
R3A2 182 1%
R3A6 182 1%
LAYOUT NOTES:
PLACE COMPONENTS AS CLOSE TO 843021 AS POSSIBLE.
SEE 843021 DATA SHEET FOR COMPONENT PLACEMENT EXAMPLE.
ROUTE CLK_P, CLK_N, CLKC_P, CLKC_N, CLKR_P, CLKR_N AS DIFFERENTIAL PAIRS.
CELL osc_125m_mod
MASTER PROJECT shohola_creek_sch
SHEET
DIFFERENTIAL OSCILLATOR 125 MHZ
MODIFIED Sun Apr 10 17:33:10 2005
BOARD REV -700
DRAWING REV 5.00



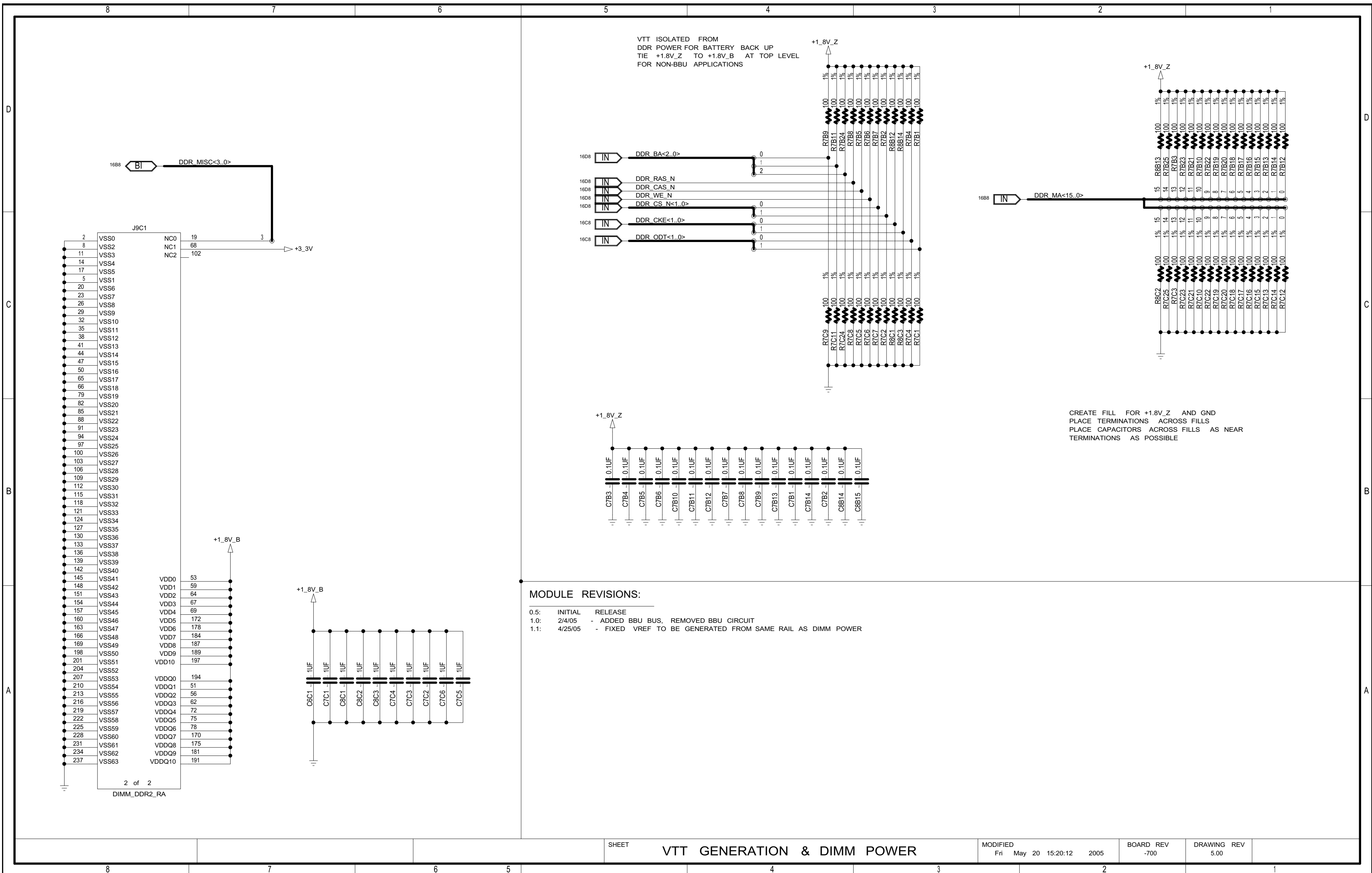
MODULE REVISIONS:

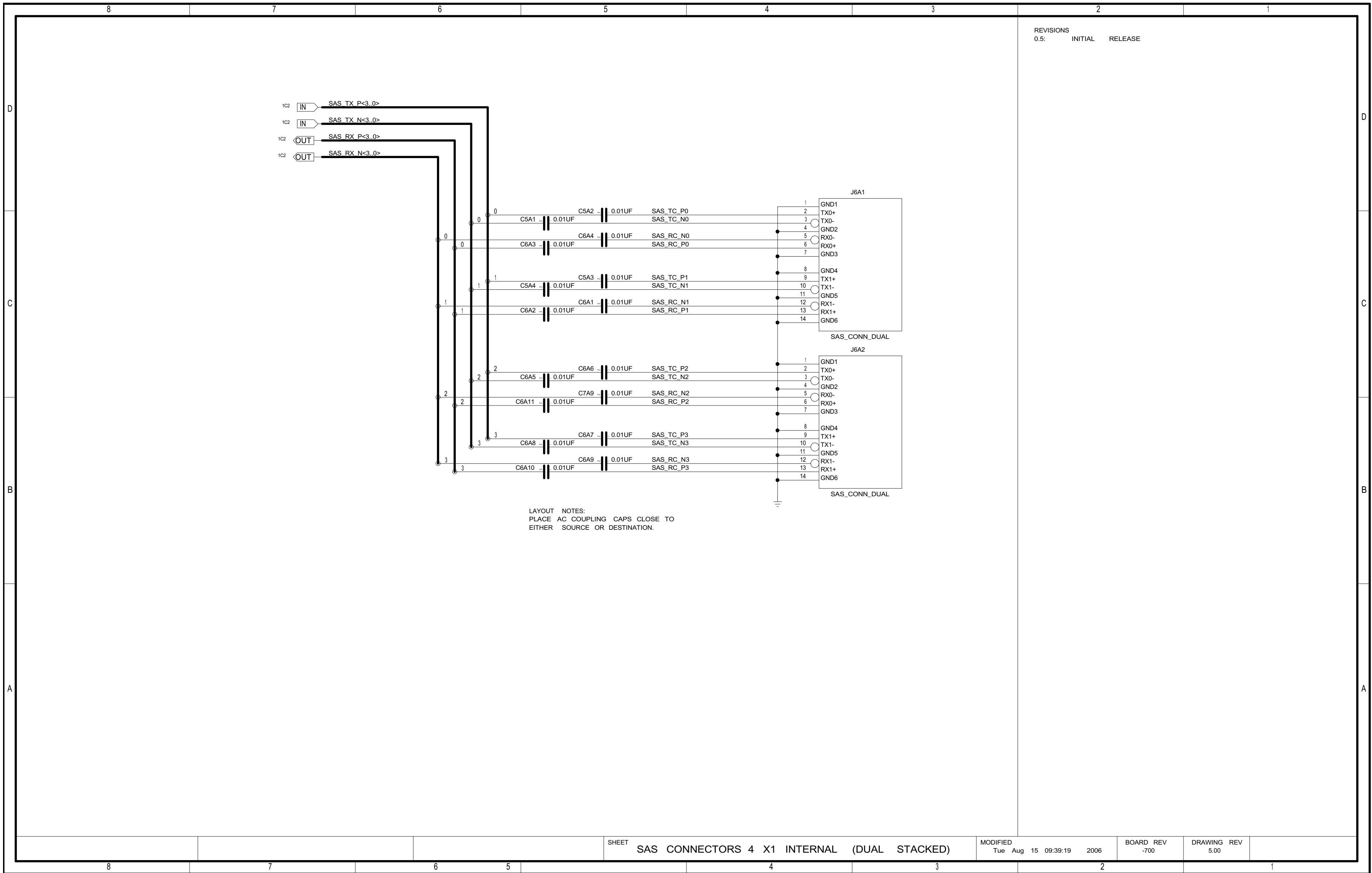
0.1: DESIGN REVIEW
0.51: SWAPPED PE_T AND PE_R CONNECTIONS
ALL SIGNALS HAVE PE PREFIX
ADDED BUBBLES FOR ACTIVE LOW SIGNALS
0.52: CHANGE SIGNAL NAMES FOR VECTORS, ADD CONSTRAINTS
0.53: MOVED TEXT ON MOD SYMBOL, MOVED C NET LABELS TO CONNECTOR SIDE
0.54: CHANGED PE_TDO TO IN, PE_TDI TO OUT
0.55: ADDED BACKPLANE DETECT SIGNAL ON PIN A32.

SHEET	PCI-EXPRESS EDGE CONNECTOR	MODIFIED Fri Dec 23 15:07:25 2005	BOARD REV -700	DRAWING REV 5.00

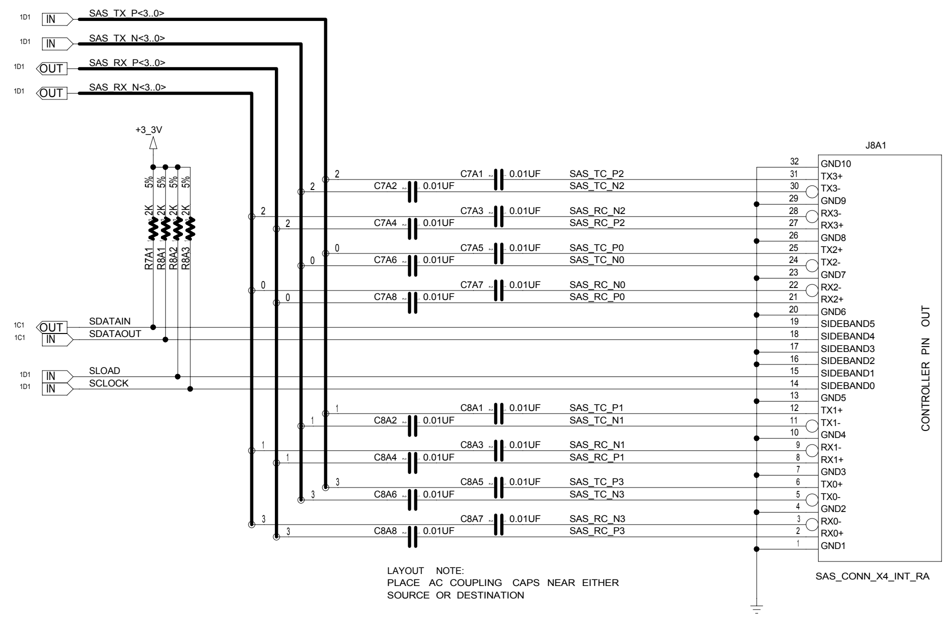


DDR_DQS_N<8..0>
DDR_DQS_P<8..0>
DDR_DQ<63..0>
DDR_BA<2..0>
J9C1
DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_CS_N<1..0>
DDR_CKE<1..0>
DDR_CB<7..0>
DDR_DM<8..0>
DDR_ODT<1..0>
ECO: CHANGED POWER RAIL
+1_8V_B
R9B3 1K 1%
ECO: CHANGED POWER RAIL
+1_8V_B C9B5 0.1UF
ECO: CHANGED VREF RESISTORS TO 1K OHM TO REDUCE POWER CONSUMPTION IN BBU MODE.
C9B4 0.1UF
R9B4 1K 1%
C9B6 0.1UF DDR_VREF
+3_3V
DDR_MISC<3..0>
DDR_RESET_N
DDR_MA<15..0>
DDR_CK_P<2..0>
DDR_CK_N<2..0>
DDR_SDA
DDR_SCL
DDR_SA<2..0>
GPIO<6>
GPIO<7>
BI
BA0 BA1 A16_BA2 RAS_N CAS_N WE_N S0_N S1_N CKE0 CKE1
CB0 CB1 CB2 CB3 CB4 CB5 CB6 CB7
DM0_DQS9 DM1_DQS10 DM2_DQS11 DM3_DQS12 DM4_DQS13 DM5_DQS14 DM6_DQS15 DM7_DQS16 DM8_DQS17
ODT0 ODT1 VREF VDDSPD RC0 RESET_N
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10_AP A11 A12 A13 A14 A15
CK0 CK0_N CK1_RFU CK1_RFU_N CK2_RFU CK2_RFU_N
SDA SCL SA0 SA1 SA2
NC_DQS9_N NC_DQS10_N NC_DQS11_N NC_DQS12_N NC_DQS13_N NC_DQS14_N NC_DQS15_N NC_DQS16_N NC_DQS17_N
DQ0–DQ63
DQS0 DQS0_N DQS1 DQS1_N DQS2 DQS2_N DQS3 DQS3_N DQS4 DQS4_N DQS5 DQS5_N DQS6 DQS6_N DQS7 DQS7_N DQS8 DQS8_N
1 of 2
DIMM_DDR2_RA
SHEET
DDR2 DIMM SOCKET
MODIFIED Thu Jan 12 14:20:55 2006
BOARD REV -700
DRAWING REV 5.00


VTT ISOLATED FROM
DDR POWER FOR BATTERY BACK UP
TIE +1.8V_Z TO +1.8V_B AT TOP LEVEL
FOR NON-BBU APPLICATIONS
CREATE FILL FOR +1.8V_Z AND GND
PLACE TERMINATIONS ACROSS FILLS
PLACE CAPACITORS ACROSS FILLS AS NEAR
TERMINATIONS AS POSSIBLE
MODULE REVISIONS:
0.5: INITIAL RELEASE
1.0: 2/4/05 - ADDED BBU BUS, REMOVED BBU CIRCUIT
1.1: 4/25/05 - FIXED VREF TO BE GENERATED FROM SAME RAIL AS DIMM POWER
J9C1
DIMM_DDR2_RA
2 of 2
DDR_MISC<3..0>
DDR_BA<2..0>
DDR_RAS_N
DDR_CAS_N
DDR_WE_N
DDR_CS_N<1..0>
DDR_CKE<1..0>
DDR_ODT<1..0>
DDR_MA<15..0>
+1_8V_Z
+1_8V_B
+3_3V
SHEET
VTT GENERATION & DIMM POWER
MODIFIED
Fri May 20 15:20:12 2005
BOARD REV
-700
DRAWING REV
5.00


REVISIONS
0.5: INITIAL RELEASE
SAS_TX_P<3..0>
SAS_TX_N<3..0>
SAS_RX_P<3..0>
SAS_RX_N<3..0>
IN
IN
OUT
OUT
J6A1
J6A2
SAS_CONN_DUAL
SAS_CONN_DUAL
LAYOUT NOTES:
PLACE AC COUPLING CAPS CLOSE TO
EITHER SOURCE OR DESTINATION.
SHEET
SAS CONNECTORS 4 X1 INTERNAL (DUAL STACKED)
MODIFIED
Tue Aug 15 09:39:19 2006
BOARD REV
-700
DRAWING REV
5.00

REVISIONS
0.5: INITIAL RELEASE
0.6: SWAPPED SAS LANES TO IMPROVE ROUTING.



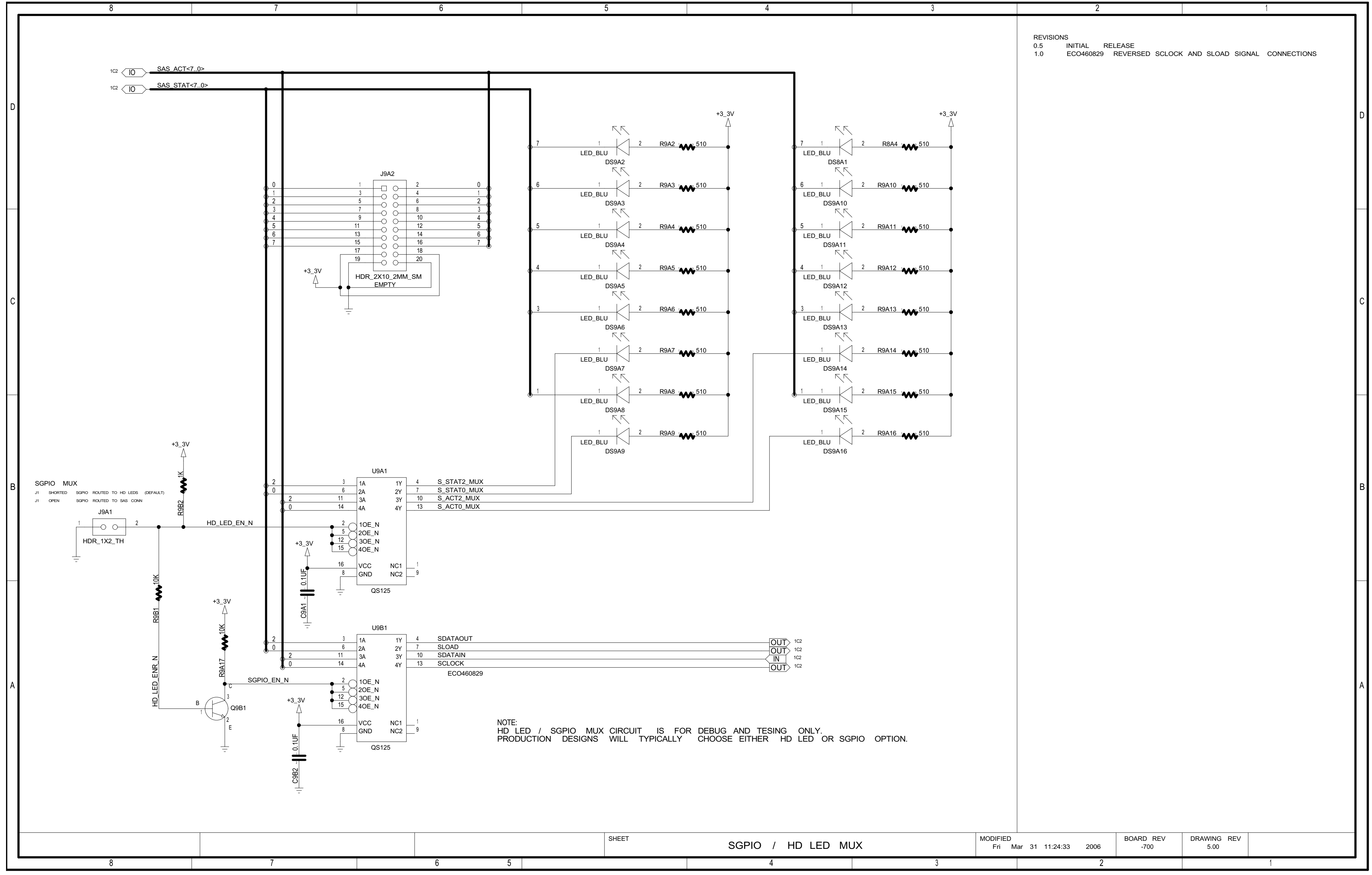
LAYOUT NOTE:
PLACE AC COUPLING CAPS NEAR EITHER SOURCE OR DESTINATION

SAS SIGNALS FROM 8134x IO PROCESSOR TO X4 INTERNAL SAS CONNECTOR SWAPPED TO MINIMIZE VIAS. 8134x B0 WILL ENABLE REORDERING SGPIO TRANSMIT ORDER TO MATCH LANE SWAPS ON BOARD.

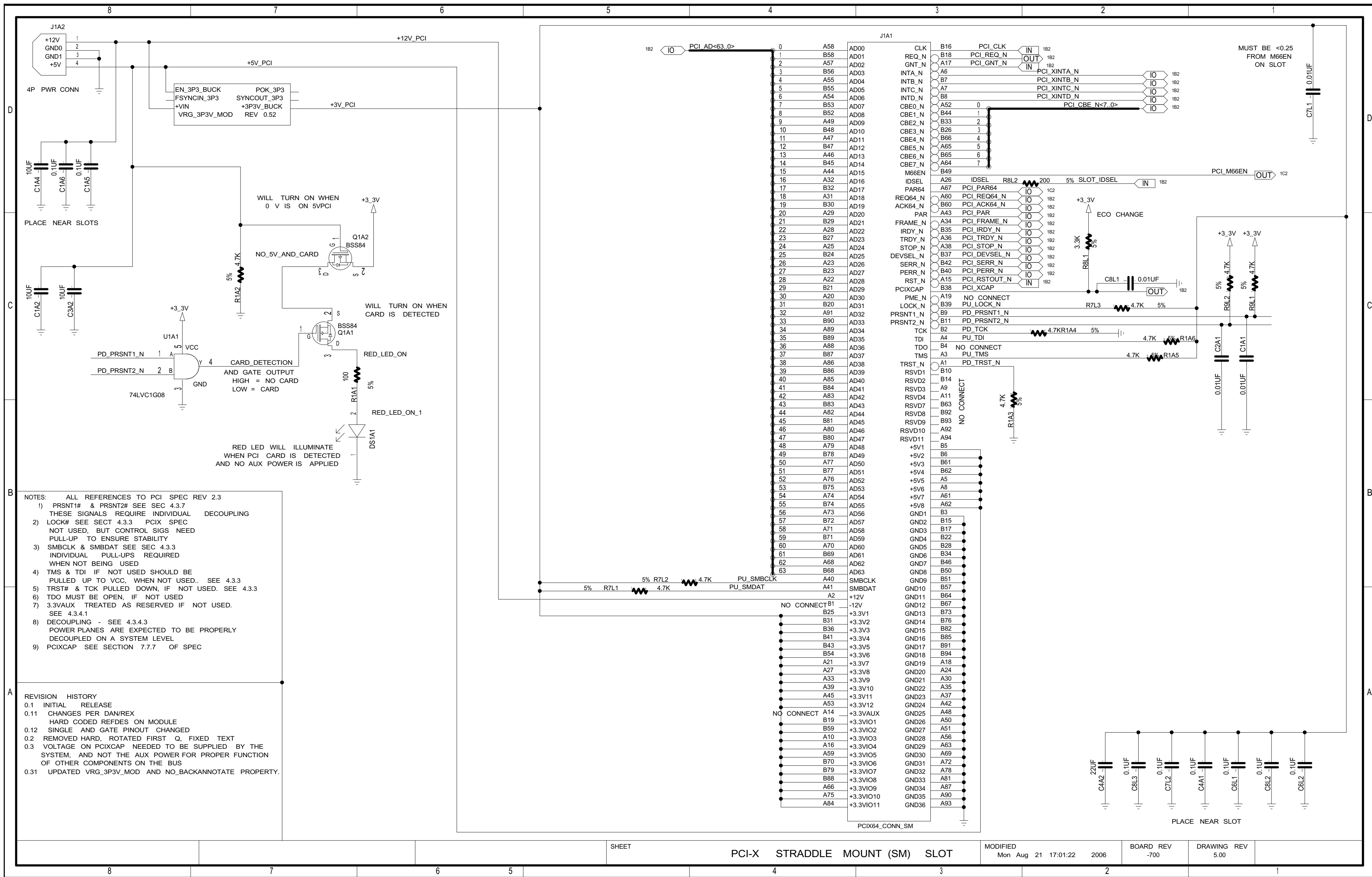
SAS LANE CONNECTIONS

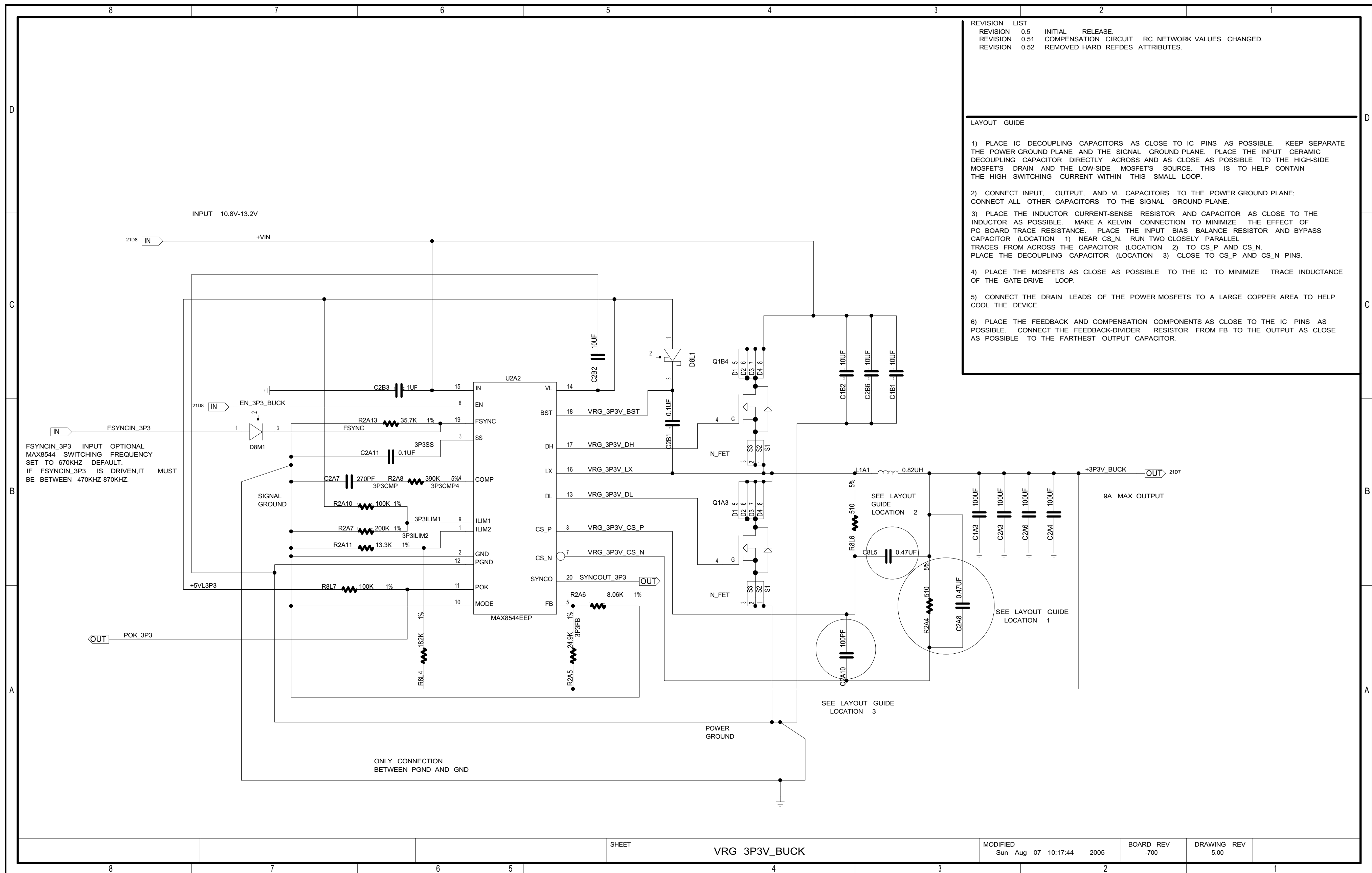
8134x	X4 INTERNAL SAS CONNECTOR
LANE 0	LANE 2
LANE 1	LANE 1
LANE 2	LANE 3
LANE 3	LANE 0

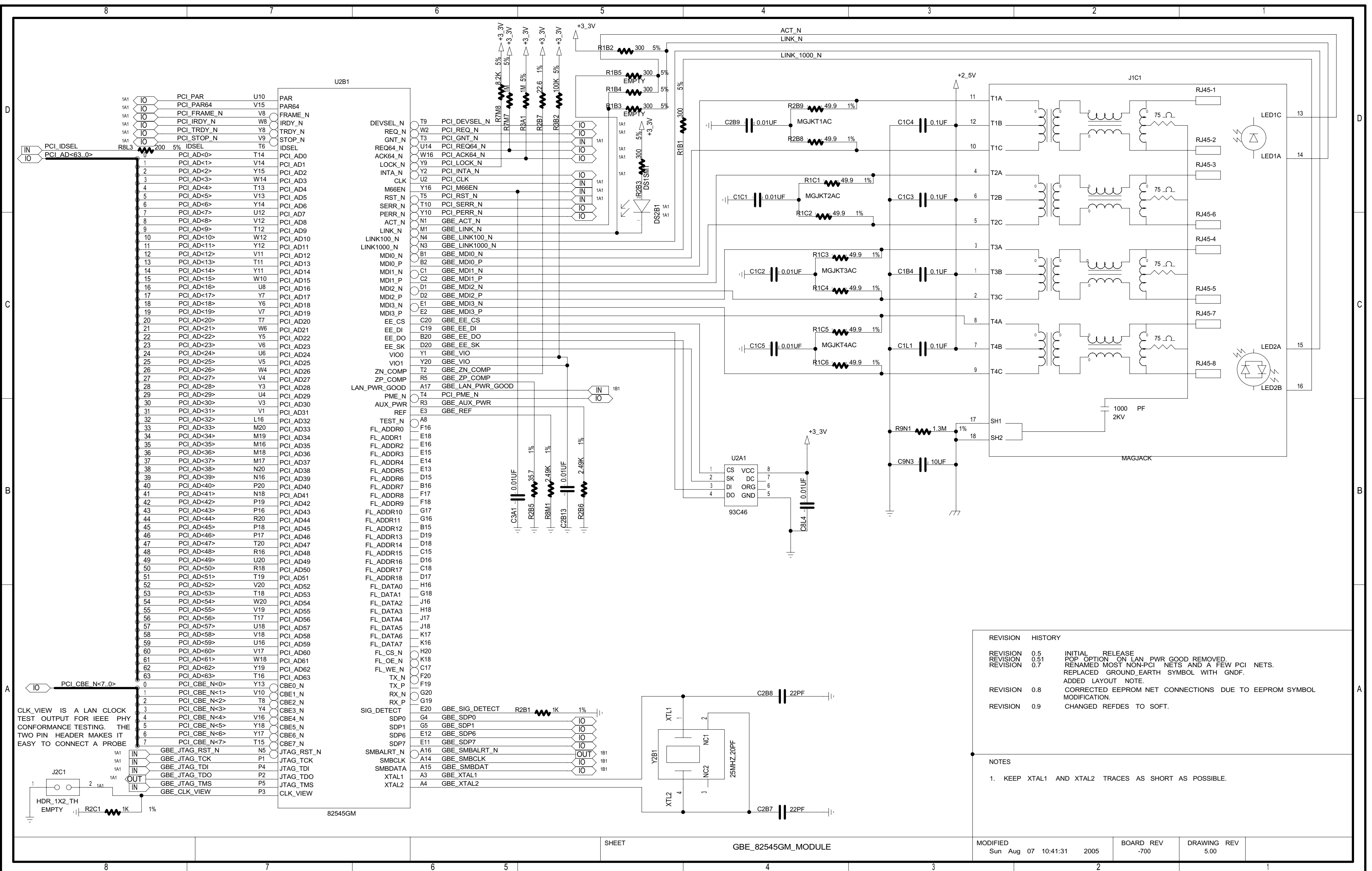
SHEET	SAS CONNECTOR X4 INTERNAL	MODIFIED Tue Jan 31 16:56:12 2006	BOARD REV -700	DRAWING REV 5.00

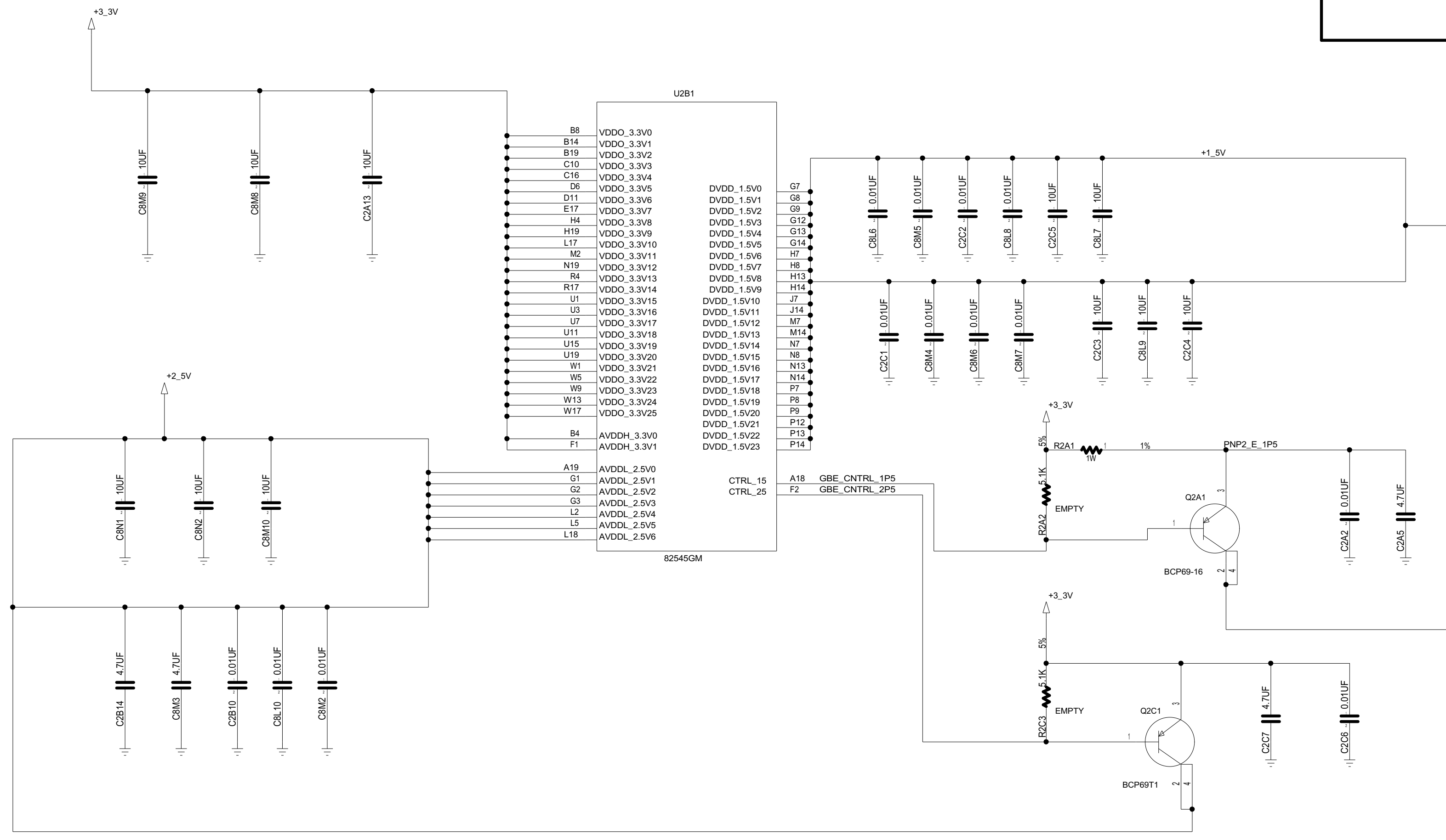


REVISIONS
0.5 INITIAL RELEASE
1.0 ECO460829 REVERSED SCLOCK AND SLOAD SIGNAL CONNECTIONS
SAS_ACT<7..0>
SAS_STAT<7..0>
J9A2
HDR_2X10_2MM_SM
EMPTY
+3_3V
LED_BLU
SGPIO MUX
J1 SHORTED SGPIO ROUTED TO HD LEDS (DEFAULT)
J1 OPEN SGPIO ROUTED TO SAS CONN
J9A1
HDR_1X2_TH
HD_LED_EN_N
HD_LED_ENR_N
SGPIO_EN_N
U9A1
U9B1
QS125
S_STAT2_MUX
S_STAT0_MUX
S_ACT2_MUX
S_ACT0_MUX
SDATAOUT
SLOAD
SDATAIN
SCLOCK
ECO460829
Q9B1
NOTE:
HD LED / SGPIO MUX CIRCUIT IS FOR DEBUG AND TESING ONLY.
PRODUCTION DESIGNS WILL TYPICALLY CHOOSE EITHER HD LED OR SGPIO OPTION.
SHEET
SGPIO / HD LED MUX
MODIFIED
Fri Mar 31 11:24:33 2006
BOARD REV
-700
DRAWING REV
5.00


PCI-X STRADDLE MOUNT (SM) SLOT
J1A2
4P PWR CONN
PLACE NEAR SLOTS
VRG_3P3V_MOD REV 0.52
WILL TURN ON WHEN 0 V IS ON 5VPCI
NO_5V_AND_CARD
WILL TURN ON WHEN CARD IS DETECTED
CARD_DETECTION
AND GATE OUTPUT
HIGH = NO CARD
LOW = CARD
74LVC1G08
RED LED WILL ILLUMINATE WHEN PCI CARD IS DETECTED AND NO AUX POWER IS APPLIED
NOTES: ALL REFERENCES TO PCI SPEC REV 2.3
1) PRSNT1# & PRSNT2# SEE SEC 4.3.7 THESE SIGNALS REQUIRE INDIVIDUAL DECOUPLING
2) LOCK# SEE SECT 4.3.3 PCIX SPEC NOT USED, BUT CONTROL SIGS NEED PULL-UP TO ENSURE STABILITY
3) SMBCLK & SMBDAT SEE SEC 4.3.3 INDIVIDUAL PULL-UPS REQUIRED WHEN NOT BEING USED
4) TMS & TDI IF NOT USED SHOULD BE PULLED UP TO VCC, WHEN NOT USED.. SEE 4.3.3
5) TRST# & TCK PULLED DOWN, IF NOT USED. SEE 4.3.3
6) TDO MUST BE OPEN, IF NOT USED
7) 3.3VAUX TREATED AS RESERVED IF NOT USED. SEE 4.3.4.1
8) DECOUPLING - SEE 4.3.4.3 POWER PLANES ARE EXPECTED TO BE PROPERLY DECOUPLED ON A SYSTEM LEVEL
9) PCIXCAP SEE SECTION 7.7.7 OF SPEC
REVISION HISTORY
0.1 INITIAL RELEASE
0.11 CHANGES PER DAN/REX HARD CODED REFDES ON MODULE
0.12 SINGLE AND GATE PINOUT CHANGED
0.2 REMOVED HARD, ROTATED FIRST Q, FIXED TEXT
0.3 VOLTAGE ON PCIXCAP NEEDED TO BE SUPPLIED BY THE SYSTEM, AND NOT THE AUX POWER FOR PROPER FUNCTION OF OTHER COMPONENTS ON THE BUS
0.31 UPDATED VRG_3P3V_MOD AND NO_BACKANNOTATE PROPERTY.
J1A1
PCIX64_CONN_SM
MUST BE <0.25 FROM M66EN ON SLOT
ECO CHANGE
PLACE NEAR SLOT
MODIFIED Mon Aug 21 17:01:22 2006
BOARD REV -700
DRAWING REV 5.00


REVISION LIST
REVISION 0.5 INITIAL RELEASE.
REVISION 0.51 COMPENSATION CIRCUIT RC NETWORK VALUES CHANGED.
REVISION 0.52 REMOVED HARD REFDES ATTRIBUTES.
LAYOUT GUIDE
1) PLACE IC DECOUPLING CAPACITORS AS CLOSE TO IC PINS AS POSSIBLE. KEEP SEPARATE THE POWER GROUND PLANE AND THE SIGNAL GROUND PLANE. PLACE THE INPUT CERAMIC DECOUPLING CAPACITOR DIRECTLY ACROSS AND AS CLOSE AS POSSIBLE TO THE HIGH-SIDE MOSFET'S DRAIN AND THE LOW-SIDE MOSFET'S SOURCE. THIS IS TO HELP CONTAIN THE HIGH SWITCHING CURRENT WITHIN THIS SMALL LOOP.
2) CONNECT INPUT, OUTPUT, AND VL CAPACITORS TO THE POWER GROUND PLANE; CONNECT ALL OTHER CAPACITORS TO THE SIGNAL GROUND PLANE.
3) PLACE THE INDUCTOR CURRENT-SENSE RESISTOR AND CAPACITOR AS CLOSE TO THE INDUCTOR AS POSSIBLE. MAKE A KELVIN CONNECTION TO MINIMIZE THE EFFECT OF PC BOARD TRACE RESISTANCE. PLACE THE INPUT BIAS BALANCE RESISTOR AND BYPASS CAPACITOR (LOCATION 1) NEAR CS_N. RUN TWO CLOSELY PARALLEL TRACES FROM ACROSS THE CAPACITOR (LOCATION 2) TO CS_P AND CS_N. PLACE THE DECOUPLING CAPACITOR (LOCATION 3) CLOSE TO CS_P AND CS_N PINS.
4) PLACE THE MOSFETS AS CLOSE AS POSSIBLE TO THE IC TO MINIMIZE TRACE INDUCTANCE OF THE GATE-DRIVE LOOP.
5) CONNECT THE DRAIN LEADS OF THE POWER MOSFETS TO A LARGE COPPER AREA TO HELP COOL THE DEVICE.
6) PLACE THE FEEDBACK AND COMPENSATION COMPONENTS AS CLOSE TO THE IC PINS AS POSSIBLE. CONNECT THE FEEDBACK-DIVIDER RESISTOR FROM FB TO THE OUTPUT AS CLOSE AS POSSIBLE TO THE FARTHEST OUTPUT CAPACITOR.
INPUT 10.8V-13.2V
21D8 IN +VIN
21D8 IN EN_3P3_BUCK
IN FSYNCIN_3P3
FSYNCIN_3P3 INPUT OPTIONAL MAX8544 SWITCHING FREQUENCY SET TO 670KHZ DEFAULT.
IF FSYNCIN_3P3 IS DRIVEN,IT MUST BE BETWEEN 470KHZ-870KHZ.
D8M1
C2B3 1UF
R2A13 35.7K 1% FSYNC
C2A11 0.1UF 3P3SS
C2A7 270PF 3P3CMP R2A8 390K 5% 3P3CMP4
R2A10 100K 1% 3P3ILIM1
R2A7 200K 1% 3P3ILIM2
R2A11 13.3K 1%
SIGNAL GROUND
+5VL3P3 R8L7 100K 1%
OUT POK_3P3
U2A2 MAX8544EEP
IN EN FSYNC SS COMP ILIM1 ILIM2 GND PGND POK MODE
VL BST DH LX DL CS_P CS_N SYNCO FB
VRG_3P3V_BST
VRG_3P3V_DH
VRG_3P3V_LX
VRG_3P3V_DL
VRG_3P3V_CS_P
VRG_3P3V_CS_N
SYNCOUT_3P3 OUT
R2A6 8.06K 1%
3P3FB
R8L4 182K 1%
R2A5 24.9K 1%
C2B2 10UF
D8L1
C2B1 0.1UF
Q1B4 N_FET
Q1A3 N_FET
C1B2 10UF C2B6 10UF C1B1 10UF
L1A1 0.82UH
+3P3V_BUCK OUT 21D7
9A MAX OUTPUT
C1A3 100UF C2A3 100UF C2A6 100UF C2A4 100UF
SEE LAYOUT GUIDE LOCATION 2
R8L6 510 5%
C8L5 0.47UF
SEE LAYOUT GUIDE LOCATION 1
R2A4 510 5%
C2A8 0.47UF
C2A10 100PF
SEE LAYOUT GUIDE LOCATION 3
POWER GROUND
ONLY CONNECTION BETWEEN PGND AND GND
SHEET VRG 3P3V_BUCK
MODIFIED Sun Aug 07 10:17:44 2005
BOARD REV -700
DRAWING REV 5.00


U2B1
82545GM
J1C1
MAGJACK
U2A1
93C46
CLK_VIEW IS A LAN CLOCK TEST OUTPUT FOR IEEE PHY CONFORMANCE TESTING. THE TWO PIN HEADER MAKES IT EASY TO CONNECT A PROBE
J2C1
HDR_1X2_TH
EMPTY
REVISION HISTORY
REVISION 0.5 INITIAL RELEASE
REVISION 0.51 POP OPTION ON LAN_PWR_GOOD REMOVED.
REVISION 0.7 RENAMED MOST NON-PCI NETS AND A FEW PCI NETS. REPLACED GROUND_EARTH SYMBOL WITH GNDF. ADDED LAYOUT NOTE.
REVISION 0.8 CORRECTED EEPROM NET CONNECTIONS DUE TO EEPROM SYMBOL MODIFICATION.
REVISION 0.9 CHANGED REFDES TO SOFT.
NOTES
1. KEEP XTAL1 AND XTAL2 TRACES AS SHORT AS POSSIBLE.
SHEET
GBE_82545GM_MODULE
MODIFIED
Sun Aug 07 10:41:31 2005
BOARD REV
-700
DRAWING REV
5.00



REVISION HISTORY

REVISION 0.5 INITIAL RELEASE
REVISION 0.7 REPLACED 1.5 POWER TRANSISTOR WITH BCP69-16.
RENAMED POWER PLANE NETS.
REVISION 0.9 REMOVED EXTERNAL +2.5V AND +1.5V INPUT OPTION.
CHANGED REFDES TO SOFT.

NOTES:

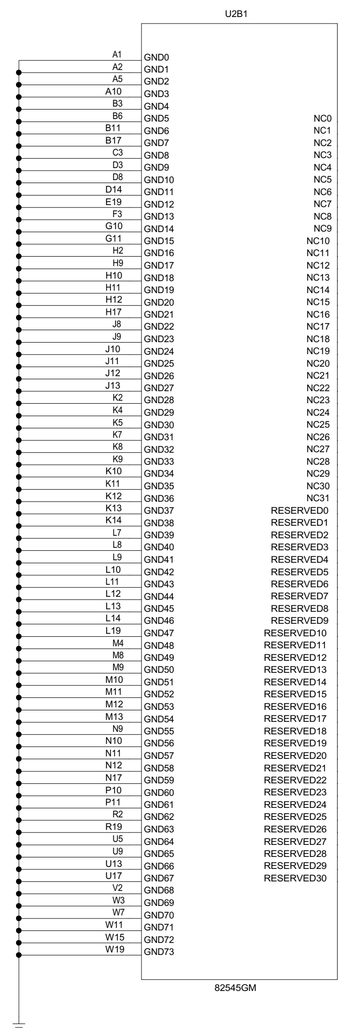
SHEET	MODIFIED	BOARD REV	DRAWING REV
GBE_82545GM_MODULE	Sun Aug 07 10:41:32 2005	-700	5.00

8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

REVISION HISTORY
REVISION 0.5 INITIAL RELEASE.
REVISION 0.9 CHANGED REFDES TO SOFT.

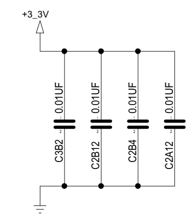
USE DECOUPLING CAPACITORS GENEROUSLY, PLACING THEM EVENLY AROUND THE 82545 GM CONTROLLER. AT A MINIMUM, USE 1 BULK CAP AND 1 HIGH FREQUENCY CAP PER SIDE OF THE CHIP. PLACE CAPS AS CLOSE TO THE CHIP AS POSSIBLE.

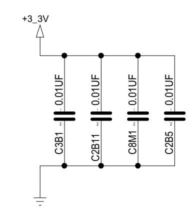
U2B1



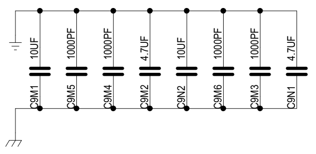
NC0 A13
NC1 B12
NC2 B13
NC3 C12
NC4 A11
NC5 A12
NC6 C13
NC7 C14
NC8 D12
NC9 D13
NC10 F4
NC11 F5
NC12 H1
NC13 H3
NC14 H5
NC15 J1
NC16 J2
NC17 J3
NC18 J4
NC19 J5
NC20 J19
NC21 J20
NC22 K1
NC23 K3
NC24 K19
NC25 K20
NC26 L1
NC27 L3
NC28 L4
NC29 M3
NC30 N2
NC31 T1
RESERVED0 D4
RESERVED1 D5
RESERVED2 C4
RESERVED3 E4
RESERVED4 C5
RESERVED5 E5
RESERVED6 B5
RESERVED7 E6
RESERVED8 D7
RESERVED9 C7
RESERVED10 E10
RESERVED11 B7
RESERVED12 A7
RESERVED13 C8
RESERVED14 E8
RESERVED15 E9
RESERVED16 D9
RESERVED17 C9
RESERVED18 B9
RESERVED19 D10
RESERVED20 A9
RESERVED21 C11
RESERVED22 B10
RESERVED23 C6
RESERVED24 A20
RESERVED25 B18
RESERVED26 M5
RESERVED27 E7 RESRVD_2728
RESERVED28 A6 RESRVD_2728
RESERVED29 R1 RESRVD_2930
RESERVED30 L20 RESRVD_2930

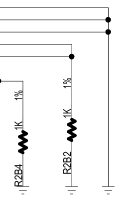
82545GM





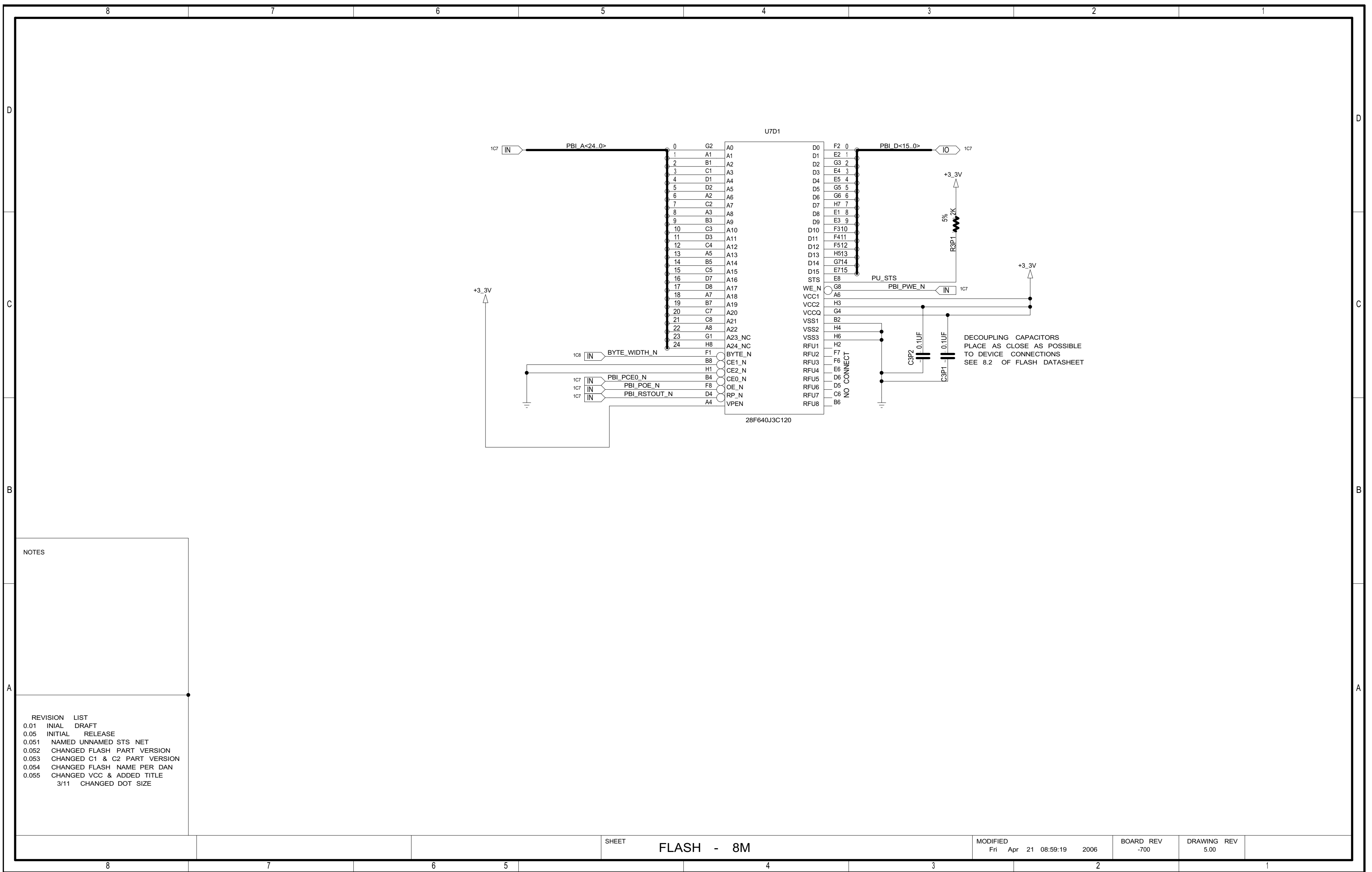
CONNECT CAPACITORS BETWEEN CHASSIS GROUND AND SIGNAL GROUND ON BOTH SIDES OF MAGNETICS MODULE.

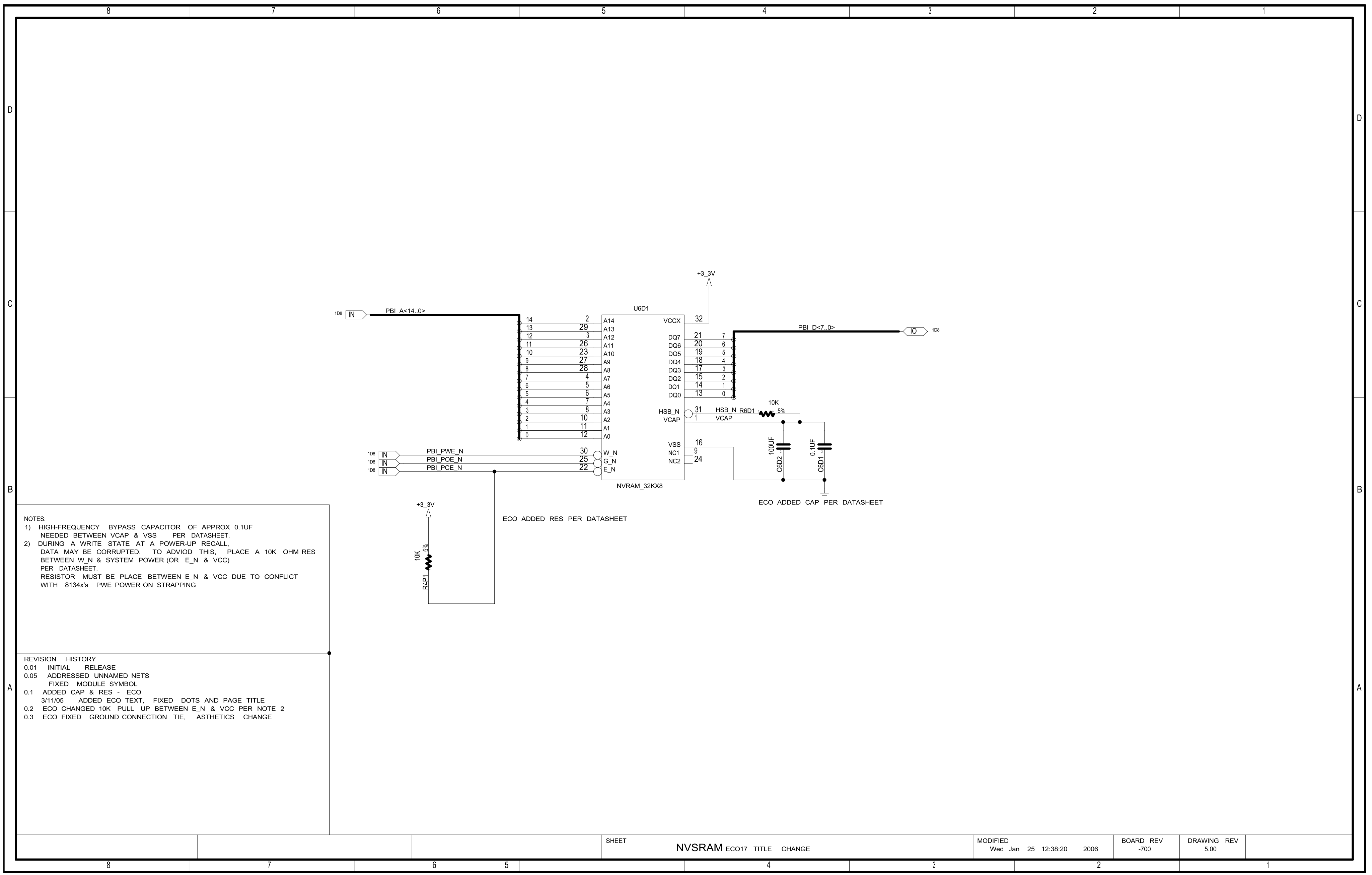




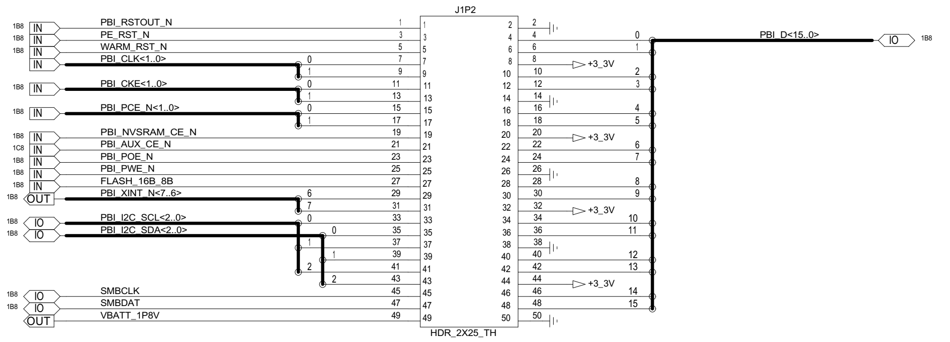
			SHEET	MODIFIED	BOARD REV	DRAWING REV
			GBE_82545GM_MODULE	Sun Aug 07 10:41:33 2005	-700	5.00

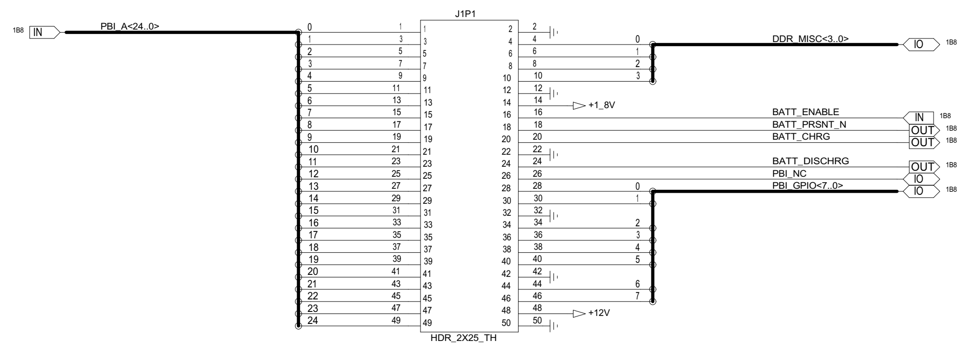
8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

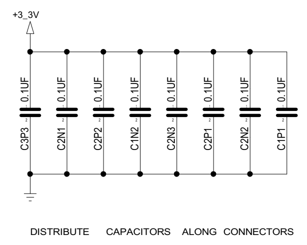

U7D1
PBI_A<24..0>
PBI_D<15..0>
28F640J3C120
PU_STS
PBI_PWE_N
BYTE_WIDTH_N
PBI_PCE0_N
PBI_POE_N
PBI_RSTOUT_N
+3_3V
NO CONNECT
DECOUPLING CAPACITORS
PLACE AS CLOSE AS POSSIBLE
TO DEVICE CONNECTIONS
SEE 8.2 OF FLASH DATASHEET
C3P2 0.1UF
C3P1 0.1UF
R3P1 2K 5%
NOTES
REVISION LIST
0.01 INIAL DRAFT
0.05 INITIAL RELEASE
0.051 NAMED UNNAMED STS NET
0.052 CHANGED FLASH PART VERSION
0.053 CHANGED C1 & C2 PART VERSION
0.054 CHANGED FLASH NAME PER DAN
0.055 CHANGED VCC & ADDED TITLE
3/11 CHANGED DOT SIZE
SHEET
FLASH - 8M
MODIFIED
Fri Apr 21 08:59:19 2006
BOARD REV
-700
DRAWING REV
5.00



PBI_A<14..0>
U6D1
+3_3V
VCCX
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
DQ7
DQ6
DQ5
DQ4
DQ3
DQ2
DQ1
DQ0
PBI_D<7..0>
IO
HSB_N
VCAP
R6D1
10K
5%
VSS
NC1
NC2
W_N
G_N
E_N
PBI_PWE_N
PBI_POE_N
PBI_PCE_N
IN
NVRAM_32KX8
100UF
C6D2
0.1UF
C6D1
ECO ADDED CAP PER DATASHEET
ECO ADDED RES PER DATASHEET
R4P1
NOTES:
1) HIGH-FREQUENCY BYPASS CAPACITOR OF APPROX 0.1UF
NEEDED BETWEEN VCAP & VSS PER DATASHEET.
2) DURING A WRITE STATE AT A POWER-UP RECALL,
DATA MAY BE CORRUPTED. TO ADVIOD THIS, PLACE A 10K OHM RES
BETWEEN W_N & SYSTEM POWER (OR E_N & VCC)
PER DATASHEET.
RESISTOR MUST BE PLACE BETWEEN E_N & VCC DUE TO CONFLICT
WITH 8134x's PWE POWER ON STRAPPING
REVISION HISTORY
0.01 INITIAL RELEASE
0.05 ADDRESSED UNNAMED NETS
FIXED MODULE SYMBOL
0.1 ADDED CAP & RES - ECO
3/11/05 ADDED ECO TEXT, FIXED DOTS AND PAGE TITLE
0.2 ECO CHANGED 10K PULL UP BETWEEN E_N & VCC PER NOTE 2
0.3 ECO FIXED GROUND CONNECTION TIE, ASTHETICS CHANGE
SHEET
NVSRAM ECO17 TITLE CHANGE
MODIFIED
Wed Jan 25 12:38:20 2006
BOARD REV
-700
DRAWING REV
5.00



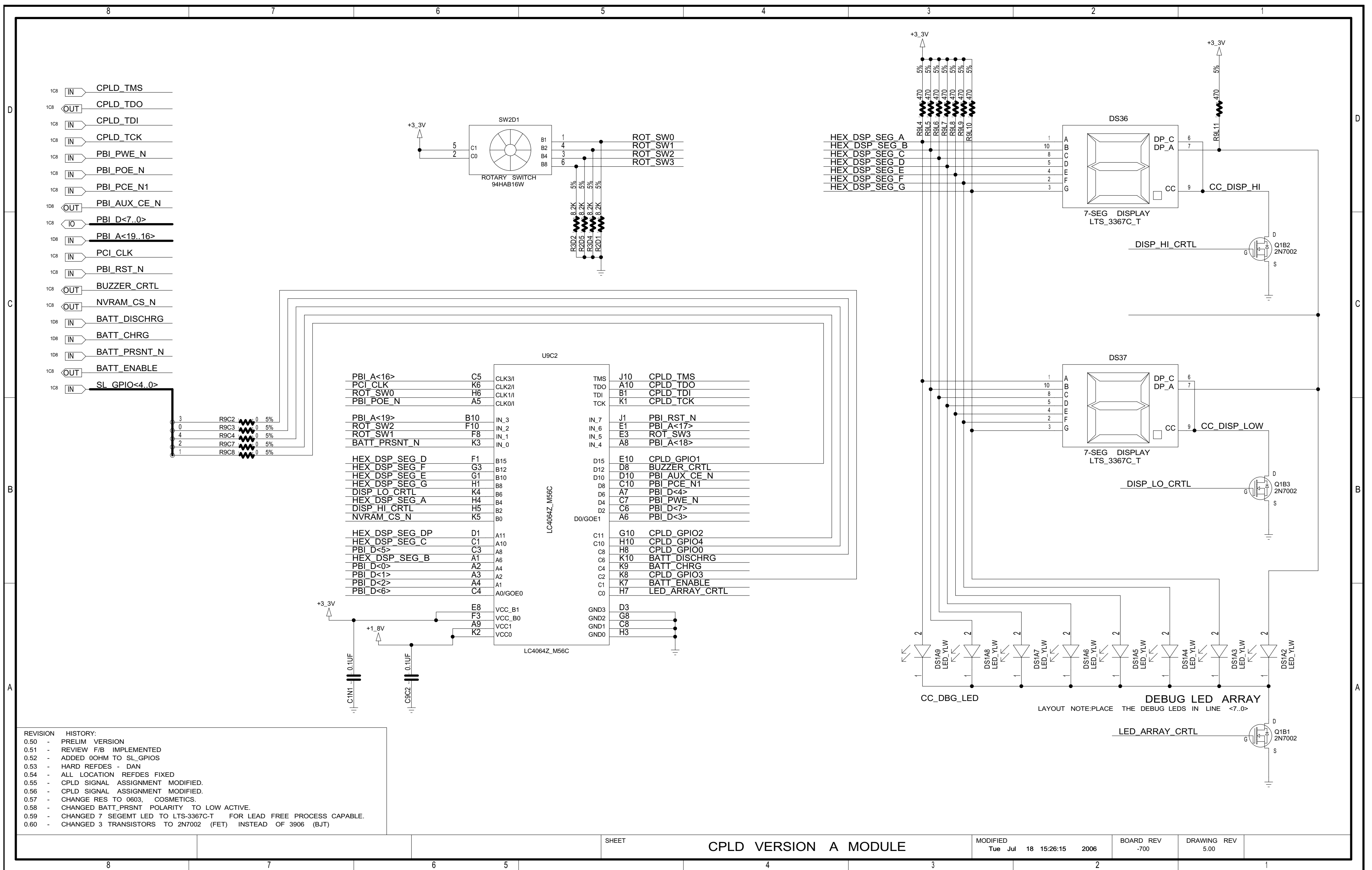


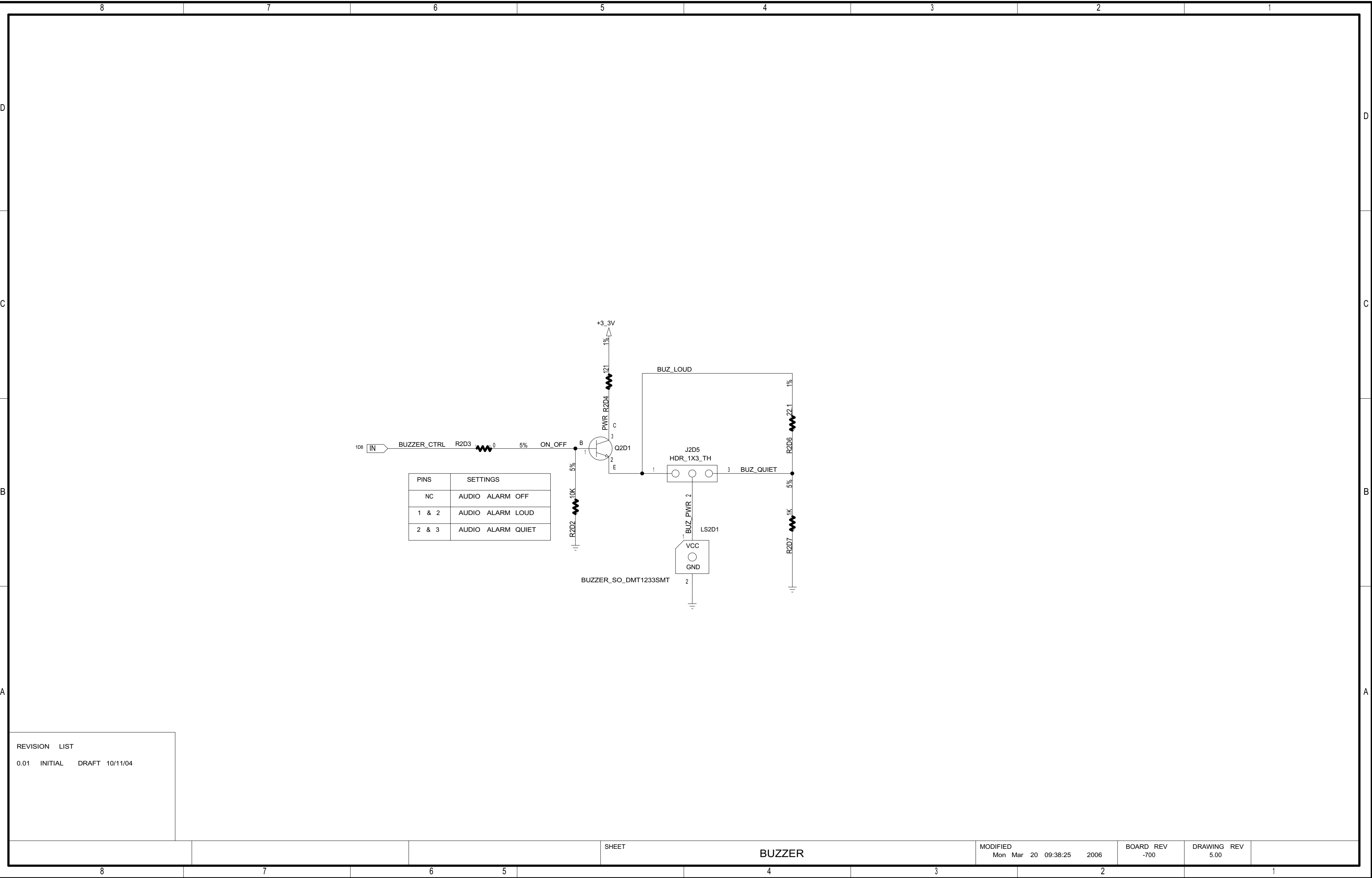


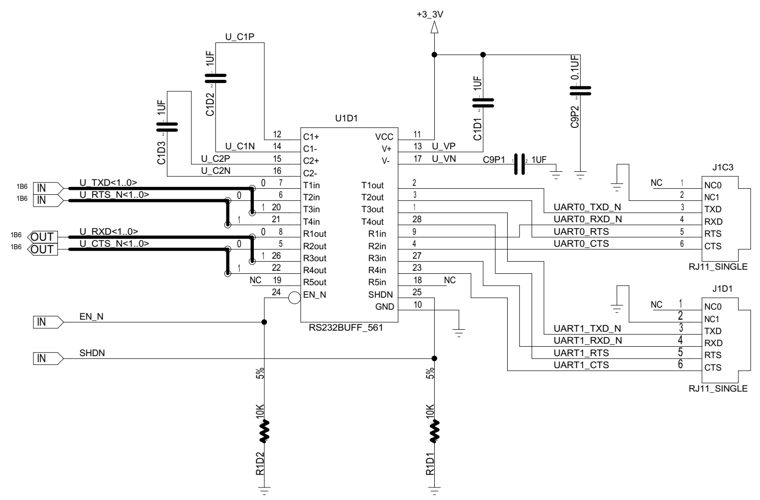
DISTRIBUTE CAPACITORS ALONG CONNECTORS

REVISIONS
0.1: RELEASE FOR DESIGN REVIEW
0.2: ADDED BATTERY CONTROL SIGNALS
RENAMED VBATT, PBI_SMBCLK & PBI_SMBDAT SIGNALS
0.3: RENUMBERED 2X25 HEADER PINS
CHANGED POLARITY OF PBI_AUX_CE AND PBI_NVSRAM_CE
1.0: ADDED BBU BUS
1.1: ECO5: RENAMED PBI_XINT<7..6> TO PBI_XINT_N<7..6>
1.2: CHANGED POLARITY OF BATT_PRSNT TO LOW ACTIVE BATT_PRSNT_N.

SHEET	MODIFIED	BOARD REV	DRAWING REV
PBI AUXILARY CONNECTOR	Fri Aug 05 14:05:34 2005	-700	5.00

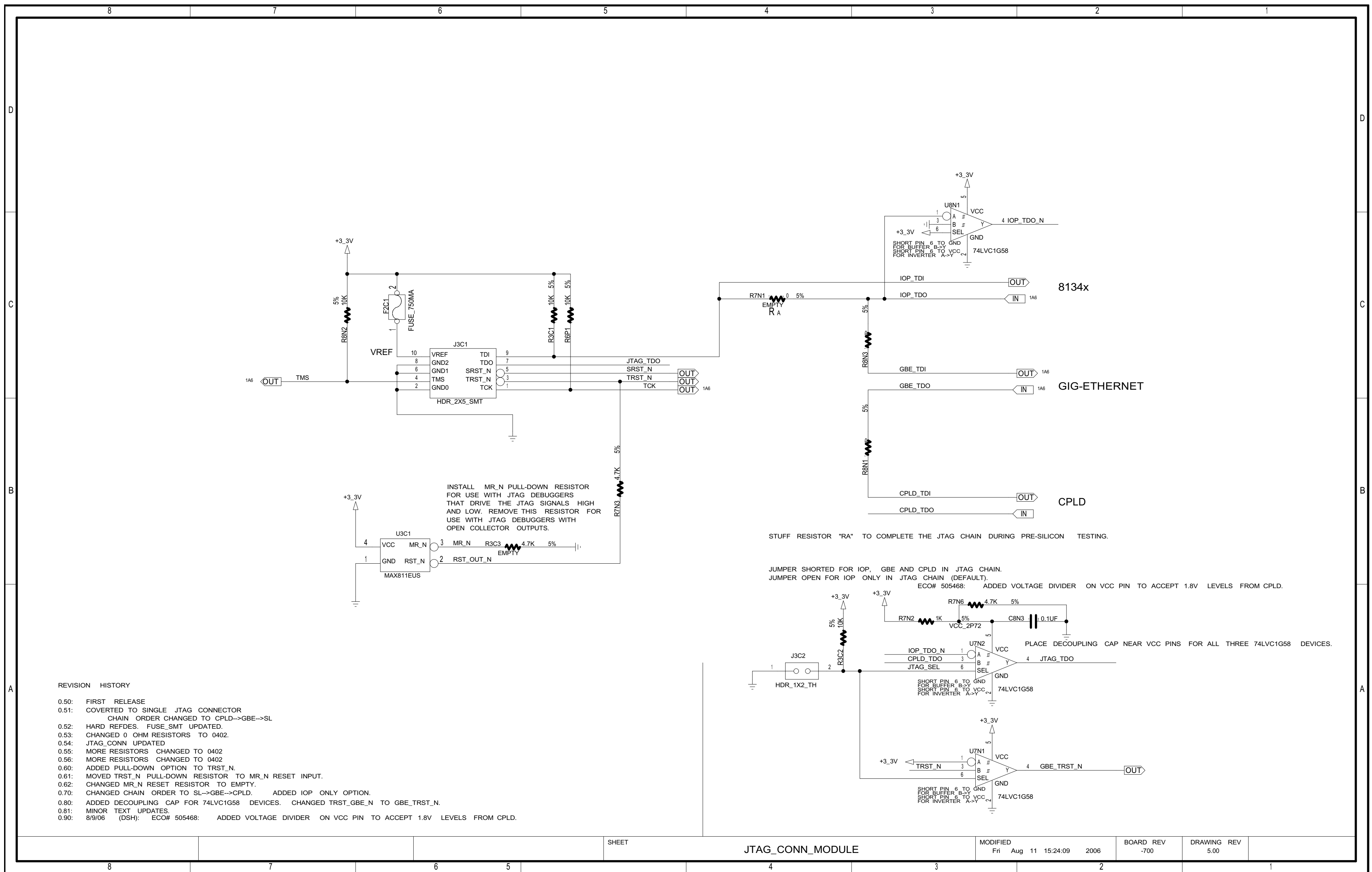

CPLD_TMS
CPLD_TDO
CPLD_TDI
CPLD_TCK
PBI_PWE_N
PBI_POE_N
PBI_PCE_N1
PBI_AUX_CE_N
PBI_D<7..0>
PBI_A<19..16>
PCI_CLK
PBI_RST_N
BUZZER_CRTL
NVRAM_CS_N
BATT_DISCHRG
BATT_CHRG
BATT_PRSNT_N
BATT_ENABLE
SL_GPIO<4..0>
SW2D1
ROTARY SWITCH
94HAB16W
ROT_SW0
ROT_SW1
ROT_SW2
ROT_SW3
U9C2
LC4064Z_M56C
HEX_DSP_SEG_A
HEX_DSP_SEG_B
HEX_DSP_SEG_C
HEX_DSP_SEG_D
HEX_DSP_SEG_E
HEX_DSP_SEG_F
HEX_DSP_SEG_G
HEX_DSP_SEG_DP
DS36
DS37
7-SEG DISPLAY
LTS_3367C_T
CC_DISP_HI
CC_DISP_LOW
DISP_HI_CRTL
DISP_LO_CRTL
Q1B2 2N7002
Q1B3 2N7002
Q1B1 2N7002
CPLD_GPIO0
CPLD_GPIO1
CPLD_GPIO2
CPLD_GPIO3
CPLD_GPIO4
LED_ARRAY_CRTL
CC_DBG_LED
DEBUG LED ARRAY
LAYOUT NOTE:PLACE THE DEBUG LEDS IN LINE <7..0>
REVISION HISTORY:
0.50 - PRELIM VERSION
0.51 - REVIEW F/B IMPLEMENTED
0.52 - ADDED 0OHM TO SL_GPIOS
0.53 - HARD REFDES - DAN
0.54 - ALL LOCATION REFDES FIXED
0.55 - CPLD SIGNAL ASSIGNMENT MODIFIED.
0.56 - CPLD SIGNAL ASSIGNMENT MODIFIED.
0.57 - CHANGE RES TO 0603, COSMETICS.
0.58 - CHANGED BATT_PRSNT POLARITY TO LOW ACTIVE.
0.59 - CHANGED 7 SEGEMT LED TO LTS-3367C-T FOR LEAD FREE PROCESS CAPABLE.
0.60 - CHANGED 3 TRANSISTORS TO 2N7002 (FET) INSTEAD OF 3906 (BJT)
SHEET
CPLD VERSION A MODULE
MODIFIED
Tue Jul 18 15:26:15 2006
BOARD REV
-700
DRAWING REV
5.00


+3_3V
1%
121
PWR R2D4
BUZ_LOUD
1D8 IN
BUZZER_CTRL
R2D3
0
5%
ON_OFF
B
C
E
Q2D1
J2D5
HDR_1X3_TH
BUZ_QUIET
22.1
R2D6
5%
10K
R2D2
1K
R2D7
BUZ_PWR
LS2D1
VCC
GND
BUZZER_SO_DMT1233SMT
PINS
SETTINGS
NC
AUDIO ALARM OFF
1 & 2
AUDIO ALARM LOUD
2 & 3
AUDIO ALARM QUIET
REVISION LIST
0.01 INITIAL DRAFT 10/11/04
SHEET
BUZZER
MODIFIED
Mon Mar 20 09:38:25 2006
BOARD REV
-700
DRAWING REV
5.00



REVISION LIST
0.01 INITAL DRAFT 10/7/04
0.2 GROUNDED PIN 2 3/2/05
0.5 MADE ALL REFDES SOFT 3/21/05
0.6 CHANGED NET NAMES 8/04/05

SHEET	MODIFIED	BOARD REV	DRAWING REV
RS232_DUAL_MOD	Sat Dec 24 14:42:48 2005	-700	5.00


8134x
GIG-ETHERNET
CPLD
INSTALL MR_N PULL-DOWN RESISTOR FOR USE WITH JTAG DEBUGGERS THAT DRIVE THE JTAG SIGNALS HIGH AND LOW. REMOVE THIS RESISTOR FOR USE WITH JTAG DEBUGGERS WITH OPEN COLLECTOR OUTPUTS.
STUFF RESISTOR "RA" TO COMPLETE THE JTAG CHAIN DURING PRE-SILICON TESTING.
JUMPER SHORTED FOR IOP, GBE AND CPLD IN JTAG CHAIN.
JUMPER OPEN FOR IOP ONLY IN JTAG CHAIN (DEFAULT).
ECO# 505468: ADDED VOLTAGE DIVIDER ON VCC PIN TO ACCEPT 1.8V LEVELS FROM CPLD.
PLACE DECOUPLING CAP NEAR VCC PINS FOR ALL THREE 74LVC1G58 DEVICES.
REVISION HISTORY
0.50: FIRST RELEASE
0.51: COVERTED TO SINGLE JTAG CONNECTOR
CHAIN ORDER CHANGED TO CPLD-->GBE-->SL
0.52: HARD REFDES. FUSE_SMT UPDATED.
0.53: CHANGED 0 OHM RESISTORS TO 0402.
0.54: JTAG_CONN UPDATED
0.55: MORE RESISTORS CHANGED TO 0402
0.56: MORE RESISTORS CHANGED TO 0402
0.60: ADDED PULL-DOWN OPTION TO TRST_N.
0.61: MOVED TRST_N PULL-DOWN RESISTOR TO MR_N RESET INPUT.
0.62: CHANGED MR_N RESET RESISTOR TO EMPTY.
0.70: CHANGED CHAIN ORDER TO SL-->GBE-->CPLD. ADDED IOP ONLY OPTION.
0.80: ADDED DECOUPLING CAP FOR 74LVC1G58 DEVICES. CHANGED TRST_GBE_N TO GBE_TRST_N.
0.81: MINOR TEXT UPDATES.
0.90: 8/9/06 (DSH): ECO# 505468: ADDED VOLTAGE DIVIDER ON VCC PIN TO ACCEPT 1.8V LEVELS FROM CPLD.
SHEET
JTAG_CONN_MODULE
MODIFIED
Fri Aug 11 15:24:09 2006
BOARD REV
-700
DRAWING REV
5.00

+VIN	MAX OUTPUT CURRENT
3.3V	0.81A
2.5V	1.31A
1.5V	2.0A (GUARANTEED LIMIT)

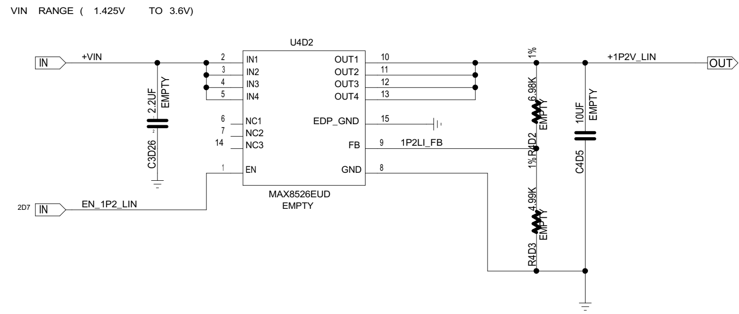
REVISION

1. REVISION 0.5

LAYOUT GUIDE

1. THE PACKAGE FEATURES AN EXPOSED THERMAL PAD ON ITS UNDERSIDE. THIS PAD LOWERS THE THERMAL RESISTANCE OF THE PACKAGE BY PROVIDING A DIRECT HEAT CONDUCTION PATH FROM THE DIE TO THE PC BOARD. ADDITIONALLY, THE GROUND PIN (GND) PERFORM THE DUAL FUNCTION OF PROVIDING AN ELECTRICAL CONNECTION TO SYSTEM GROUND AND CHANNELING HEAT AWAY. CONNECT THE EXPOSED BACKSIDE PAD AND GND TO THE SYSTEM GROUND USING A LARGE PAD OR GROUND PLANE, OR MULTIPLE VIAS TO THE GROUND-PLANE LAYER.

VIN RANGE (1.425V TO 3.6V)



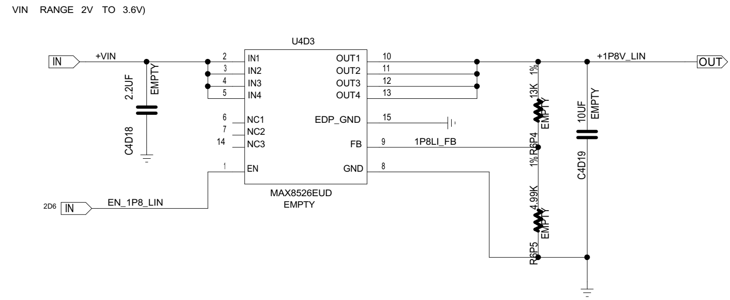
SHEET	VREG +1P2V_LINEAR (NOT POPULATED)	MODIFIED Fri Dec 23 18:13:58 2005	BOARD REV -700	DRAWING REV 5.00

REVISION HISTORY

REVISION 0.5 INITIAL RELEASE.
REVISION 0.51 ADDED NO_BACKANNOTATE ATTRIBUTE.

+VIN	MAX OUTPUT CURRENT
3.3V	1.13A
2.5V	2.0A (GUARANTEED LIMIT)

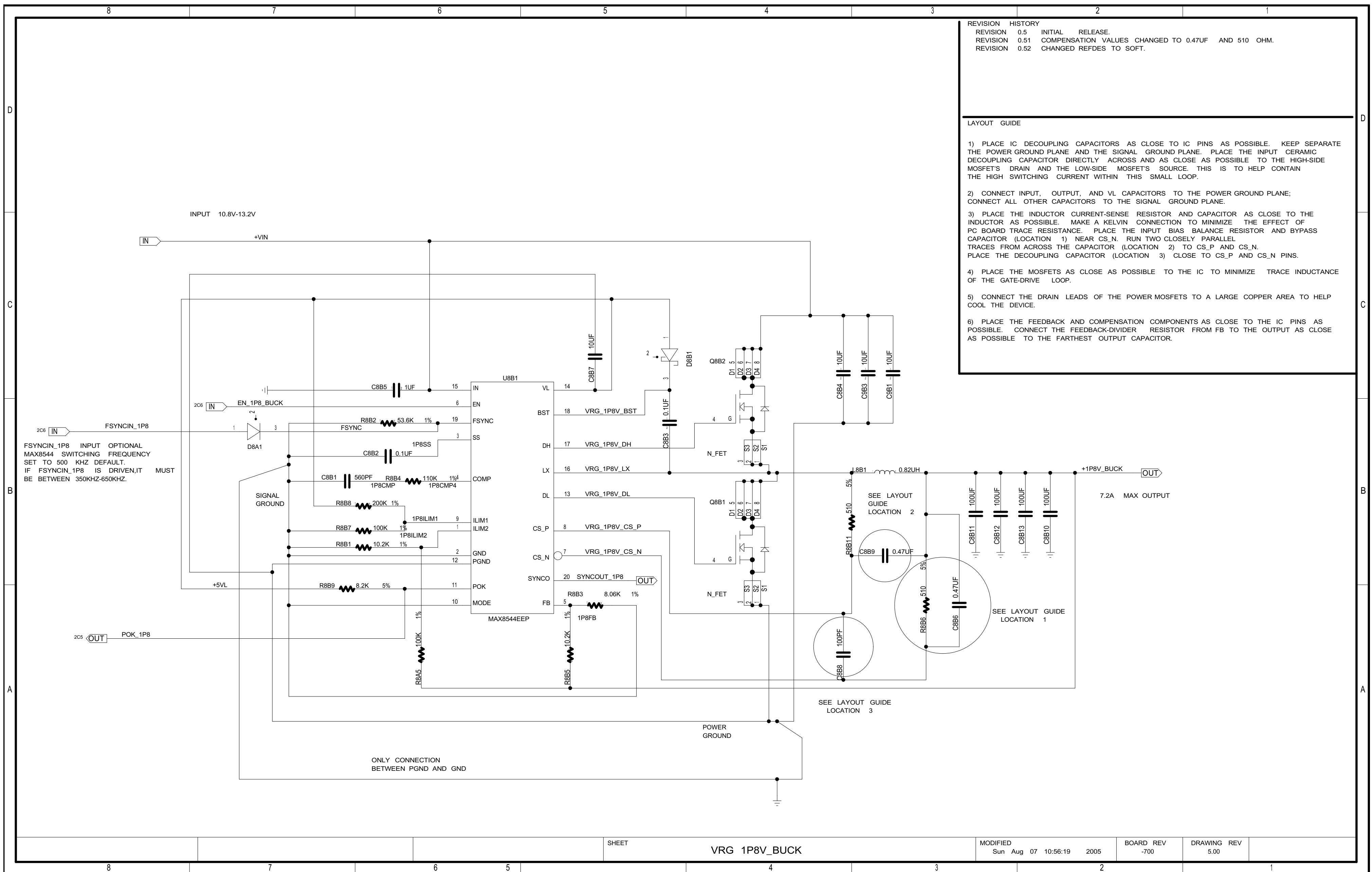
VIN RANGE 2V TO 3.6V)

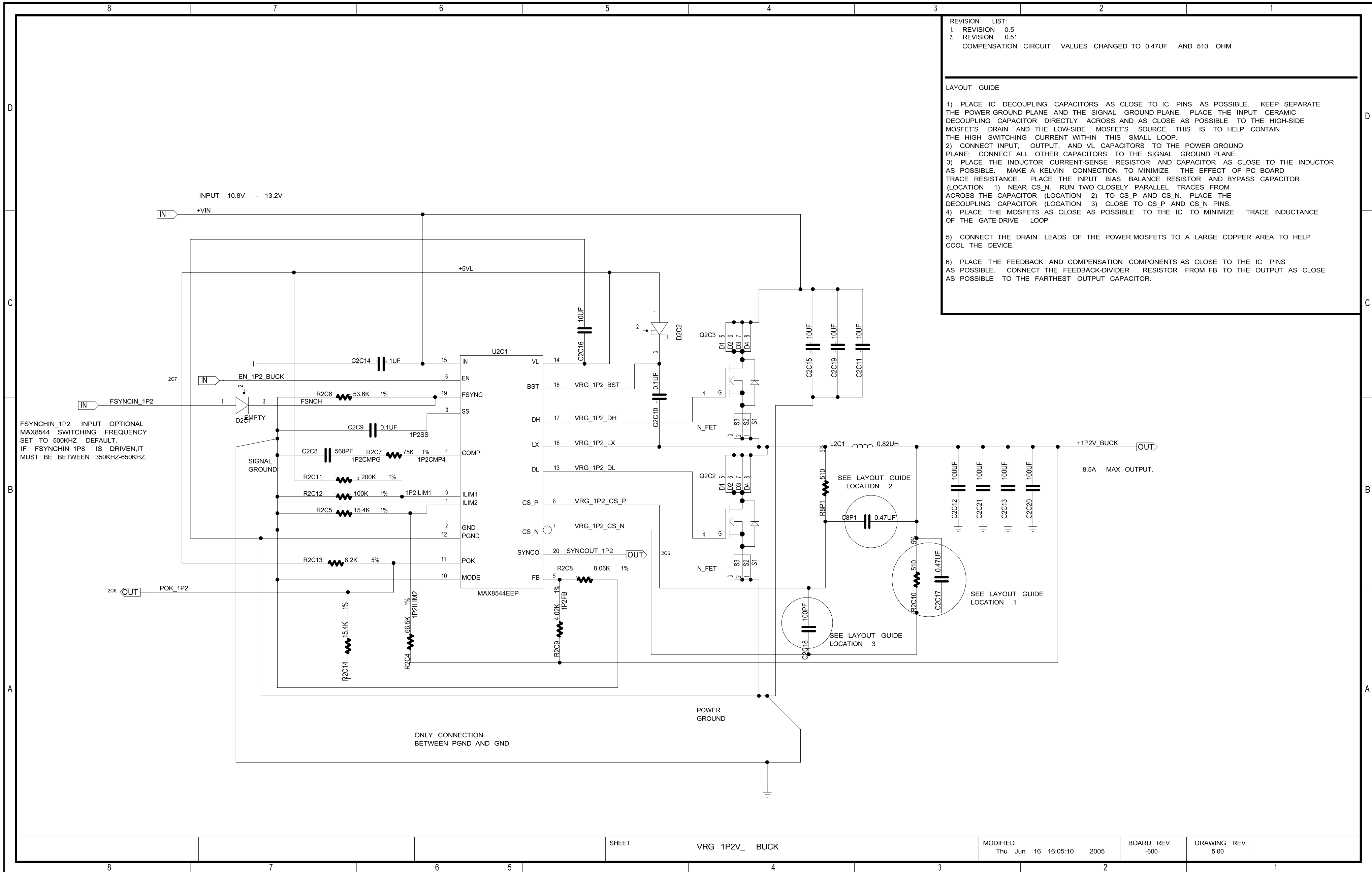


LAYOUT GUIDE

1. THE PACKAGE FEATURES AN EXPOSED THERMAL PAD ON ITS UNDERSIDE. THIS PAD LOWERS THE THERMAL RESISTANCE OF THE PACKAGE BY PROVIDING A DIRECT HEAT CONDUCTION PATH FROM THE DIE TO THE PC BOARD. ADDITIONALLY, THE GROUND PIN (GND) PERFORM THE DUAL FUNCTION OF PROVIDING AN ELECTRICAL CONNECTION TO SYSTEM GROUND AND CHANNELING HEAT AWAY. CONNECT THE EXPOSED BACKSIDE PAD AND GND TO THE SYSTEM GROUND USING A LARGE PAD OR GROUND PLANE, OR MULTIPLE VIAS TO THE GROUND-PLANE LAYER.

SHEET		MODIFIED	BOARD REV	DRAWING REV
	VREG 1P8V LINEAR (NOT POPULATED)	Fri Dec 23 18:31:11 2005	-700	5.00


REVISION HISTORY
REVISION 0.5 INITIAL RELEASE.
REVISION 0.51 COMPENSATION VALUES CHANGED TO 0.47UF AND 510 OHM.
REVISION 0.52 CHANGED REFDES TO SOFT.
LAYOUT GUIDE
1) PLACE IC DECOUPLING CAPACITORS AS CLOSE TO IC PINS AS POSSIBLE. KEEP SEPARATE THE POWER GROUND PLANE AND THE SIGNAL GROUND PLANE. PLACE THE INPUT CERAMIC DECOUPLING CAPACITOR DIRECTLY ACROSS AND AS CLOSE AS POSSIBLE TO THE HIGH-SIDE MOSFET'S DRAIN AND THE LOW-SIDE MOSFET'S SOURCE. THIS IS TO HELP CONTAIN THE HIGH SWITCHING CURRENT WITHIN THIS SMALL LOOP.
2) CONNECT INPUT, OUTPUT, AND VL CAPACITORS TO THE POWER GROUND PLANE; CONNECT ALL OTHER CAPACITORS TO THE SIGNAL GROUND PLANE.
3) PLACE THE INDUCTOR CURRENT-SENSE RESISTOR AND CAPACITOR AS CLOSE TO THE INDUCTOR AS POSSIBLE. MAKE A KELVIN CONNECTION TO MINIMIZE THE EFFECT OF PC BOARD TRACE RESISTANCE. PLACE THE INPUT BIAS BALANCE RESISTOR AND BYPASS CAPACITOR (LOCATION 1) NEAR CS_N. RUN TWO CLOSELY PARALLEL TRACES FROM ACROSS THE CAPACITOR (LOCATION 2) TO CS_P AND CS_N. PLACE THE DECOUPLING CAPACITOR (LOCATION 3) CLOSE TO CS_P AND CS_N PINS.
4) PLACE THE MOSFETS AS CLOSE AS POSSIBLE TO THE IC TO MINIMIZE TRACE INDUCTANCE OF THE GATE-DRIVE LOOP.
5) CONNECT THE DRAIN LEADS OF THE POWER MOSFETS TO A LARGE COPPER AREA TO HELP COOL THE DEVICE.
6) PLACE THE FEEDBACK AND COMPENSATION COMPONENTS AS CLOSE TO THE IC PINS AS POSSIBLE. CONNECT THE FEEDBACK-DIVIDER RESISTOR FROM FB TO THE OUTPUT AS CLOSE AS POSSIBLE TO THE FARTHEST OUTPUT CAPACITOR.
INPUT 10.8V-13.2V
IN
+VIN
EN_1P8_BUCK
FSYNCIN_1P8
FSYNC
FSYNCIN_1P8 INPUT OPTIONAL
MAX8544 SWITCHING FREQUENCY
SET TO 500 KHZ DEFAULT.
IF FSYNCIN_1P8 IS DRIVEN,IT MUST
BE BETWEEN 350KHZ-650KHZ.
D8A1
SIGNAL
GROUND
C8B5 1UF
R8B2 53.6K 1%
C8B2 0.1UF
1P8SS
C8B1 560PF
1P8CMP
R8B4 110K 1%
1P8CMP4
R8B8 200K 1%
1P8ILIM1
R8B7 100K 1%
1P8ILIM2
R8B1 10.2K 1%
+5VL
R8B9 8.2K 5%
POK_1P8
OUT
U8B1
IN EN FSYNC SS COMP ILIM1 ILIM2 GND PGND POK MODE
VL BST DH LX DL CS_P CS_N SYNCO FB
MAX8544EEP
VRG_1P8V_BST
VRG_1P8V_DH
VRG_1P8V_LX
VRG_1P8V_DL
VRG_1P8V_CS_P
VRG_1P8V_CS_N
SYNCOUT_1P8
R8B3 8.06K 1%
1P8FB
R8A5 100K 1%
R8B5 10.2K 1%
C8B7 10UF
D8B1
C8B3 0.1UF
Q8B2
Q8B1
N_FET
C8B4 10UF
C9B3 10UF
C9B1 10UF
L8B1 0.82UH
R8B11 510 5%
SEE LAYOUT GUIDE LOCATION 2
C8B9 0.47UF
R8B6 510 5%
C8B6 0.47UF
SEE LAYOUT GUIDE LOCATION 1
C8B8 100PF
SEE LAYOUT GUIDE LOCATION 3
C8B11 100UF
C8B12 100UF
C8B13 100UF
C8B10 100UF
+1P8V_BUCK
7.2A MAX OUTPUT
POWER
GROUND
ONLY CONNECTION
BETWEEN PGND AND GND
SHEET
VRG 1P8V_BUCK
MODIFIED
Sun Aug 07 10:56:19 2005
BOARD REV
-700
DRAWING REV
5.00


REVISION LIST:
1. REVISION 0.5
2. REVISION 0.51
COMPENSATION CIRCUIT VALUES CHANGED TO 0.47UF AND 510 OHM
LAYOUT GUIDE
1) PLACE IC DECOUPLING CAPACITORS AS CLOSE TO IC PINS AS POSSIBLE. KEEP SEPARATE THE POWER GROUND PLANE AND THE SIGNAL GROUND PLANE. PLACE THE INPUT CERAMIC DECOUPLING CAPACITOR DIRECTLY ACROSS AND AS CLOSE AS POSSIBLE TO THE HIGH-SIDE MOSFET'S DRAIN AND THE LOW-SIDE MOSFET'S SOURCE. THIS IS TO HELP CONTAIN THE HIGH SWITCHING CURRENT WITHIN THIS SMALL LOOP.
2) CONNECT INPUT, OUTPUT, AND VL CAPACITORS TO THE POWER GROUND PLANE; CONNECT ALL OTHER CAPACITORS TO THE SIGNAL GROUND PLANE.
3) PLACE THE INDUCTOR CURRENT-SENSE RESISTOR AND CAPACITOR AS CLOSE TO THE INDUCTOR AS POSSIBLE. MAKE A KELVIN CONNECTION TO MINIMIZE THE EFFECT OF PC BOARD TRACE RESISTANCE. PLACE THE INPUT BIAS BALANCE RESISTOR AND BYPASS CAPACITOR (LOCATION 1) NEAR CS_N. RUN TWO CLOSELY PARALLEL TRACES FROM ACROSS THE CAPACITOR (LOCATION 2) TO CS_P AND CS_N. PLACE THE DECOUPLING CAPACITOR (LOCATION 3) CLOSE TO CS_P AND CS_N PINS.
4) PLACE THE MOSFETS AS CLOSE AS POSSIBLE TO THE IC TO MINIMIZE TRACE INDUCTANCE OF THE GATE-DRIVE LOOP.
5) CONNECT THE DRAIN LEADS OF THE POWER MOSFETS TO A LARGE COPPER AREA TO HELP COOL THE DEVICE.
6) PLACE THE FEEDBACK AND COMPENSATION COMPONENTS AS CLOSE TO THE IC PINS AS POSSIBLE. CONNECT THE FEEDBACK-DIVIDER RESISTOR FROM FB TO THE OUTPUT AS CLOSE AS POSSIBLE TO THE FARTHEST OUTPUT CAPACITOR.
INPUT 10.8V - 13.2V
+VIN
+5VL
U2C1
MAX8544EEP
IN
EN
FSYNC
SS
COMP
ILIM1
ILIM2
GND
PGND
POK
MODE
VL
BST
DH
LX
DL
CS_P
CS_N
SYNCO
FB
C2C14 1UF
EN_1P2_BUCK
FSYNCIN_1P2
FSNCH
EMPTY
D2C1
R2C6 53.6K 1%
C2C9 0.1UF
1P2SS
C2C8 560PF
R2C7 75K 1%
1P2CMPG
1P2CMP4
R2C11 200K 1%
R2C12 100K 1%
1P2ILIM1
R2C5 15.4K 1%
R2C13 8.2K 5%
POK_1P2
R2C14 15.4K 1%
R2C4 66.5K 1%
1P2ILIM2
R2C9 4.02K 1%
1P2FB
R2C8 8.06K 1%
FSYNCHIN_1P2 INPUT OPTIONAL MAX8544 SWITCHING FREQUENCY SET TO 500KHZ DEFAULT. IF FSYNCHIN_1P8 IS DRIVEN,IT MUST BE BETWEEN 350KHZ-650KHZ.
SIGNAL GROUND
C2C16 10UF
D2C2
C2C10 0.1UF
VRG_1P2_BST
VRG_1P2_DH
VRG_1P2_LX
VRG_1P2_DL
VRG_1P2_CS_P
VRG_1P2_CS_N
SYNCOUT_1P2
Q2C3
Q2C2
N_FET
C2C15 10UF
C2C19 10UF
C2C11 10UF
L2C1 0.82UH
+1P2V_BUCK
8.5A MAX OUTPUT.
C2C12 100UF
C2C21 100UF
C2C13 100UF
C2C20 100UF
R8P1 510 5%
C8P1 0.47UF
SEE LAYOUT GUIDE LOCATION 2
R2C10 510 5%
C2C17 0.47UF
SEE LAYOUT GUIDE LOCATION 1
C2C18 100PF
SEE LAYOUT GUIDE LOCATION 3
POWER GROUND
ONLY CONNECTION BETWEEN PGND AND GND
SHEET
VRG 1P2V_ BUCK
MODIFIED
Thu Jun 16 16:05:10 2005
BOARD REV
-600
DRAWING REV
5.00