Intel in Communications

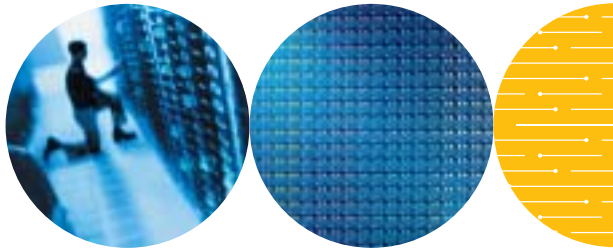
Intel® IOP331 I/O Processor with Intel® XScale™ Microarchitecture

Up to 800 MHz CPU, Integrated PCI-X Bridge and Dual-Ported High-Bandwidth Memory Controller Deliver Superior Performance

Product Highlights

- 32-bit high-performance CPU (500, 667, 800 MHz) based upon Intel® XScale™ microarchitecture
- Integrated 133 MHz/64-bit PCI-X to PCI-X Bridge (PCI 1.0A, PCI 2.3, PCI Bridge 1.1 compliant, scalability/flexibility on both PCI-X buses, four secondary devices supported by integrated clockouts and arbiter, private device and private memory support)
- DDR 333 and DDRII 400 SDRAM with ECC (up to 2 GB of 32- or 64-bit memory, optional single-bit error correction/multi-bit detection support)
- Dual-ported memory controller with pipelined access from Intel XScale core and internal peripherals (programmable control for preemption by Intel XScale core and multi-transaction counter for performance tuning)
- RAID5 XOR and iSCSI CRC32C off-load engines
- 8 or 16-bit, 66 MHz Peripheral Bus Interface (programmable bus width and wait states for two memory windows, two chip selects)
- 266 MHz, 64-bit (2.1 GB/sec) internal bus
- 2-channel DMA engine with support for scatter and gather of data blocks, automatic data chaining, and unaligned data transfers between PCI-to-local memory, local memory-to-PCI and memory-to-memory (three 1 Kbyte data buffers per channel)

- Up to 13 external interrupt inputs to Interrupt Controller supports vector generation and 4-level priorities
- (2) 16550-compatible UARTs (4-pin, Master/Slave capable, 64-byte Receive/Transmit FIFOs)
- (8) GPIO pins that can also be used as external interrupt pins
- (2) industry-standards-based I^2C interfaces
- Two programmable 32-bit Timers and Watchdog Timer
- Typical power consumption of 7.5 watts (500 MHz)
- 829-ball FCBGA (37.5 mm^2)



Product Overview

High-performance I/O processor based on Intel® XScale™ Technology

The Intel® IOP331 is a highly integrated I/O system on a chip for I/O-intensive storage, networking, communications, and embedded applications. The IOP331 features an 800 MHz CPU, high-performance internal bus, dual-ported memory controller, a high-bandwidth PCI-X to PCI-X Bridge, and an improved interrupt controller to provide a high-performance, highly integrated processor solution. Target applications include PCI/PCI-X host-based adapters (RAID cards, iSCSI cards, FC cards, Security/SSL NICs, etc), control plane and system controller applications utilizing PCI/PCI-X as a system interconnect and/or backplane Virtual Private Network devices, video servers, Network gateways, Network Attached Storage, External Storage Arrays), PCI/PCI-X-based line cards (VoIP, Routers, etc.), and a host of other applications that require a highly integrated, high-performance system on a chip processor.

As Intel's sixth-generation I/O processor, the IOP331 continues to build on Intel's strength in delivering high-performance, low-power Intel XScale technology processors. It integrates Intel® Super-Pipelined RISC Technology with 7-stage integer/8-stage memory super-pipelined core, 32 Kbyte data and instruction caches and operates up to 800 MHz. The IOP331 is code compatible with the Intel® IOP321 I/O Processor, other Intel XScale core processors, and ARM*-based devices, simplifying code porting from existing designs. It is compliant with the ARM v5TE* instruction set (excluding the floating-point instruction set). The internal bus operates at 266 MHz and offers internal bandwidth of up to 2.1 Gbytes/second.

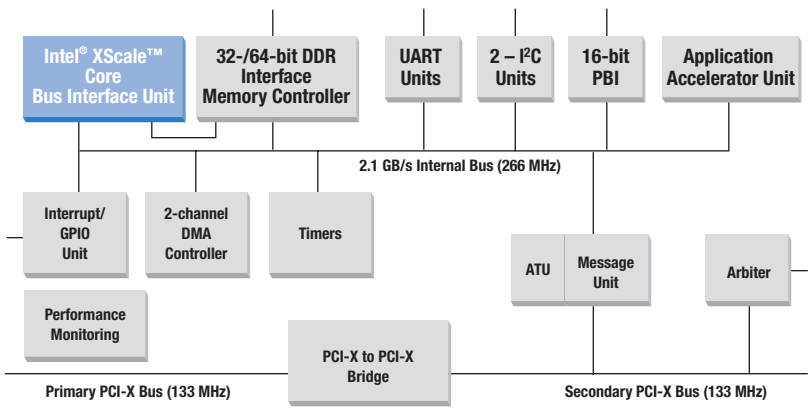
The IOP331 provides ultra-fast memory transactions due to its Double Data Rate (DDR) SDRAM dual-ported memory controller that supports up to 2 GB of DDR 333 MHz memory or 1 GB of DDRII 400 MHz memory. Registered and unbuffered DDR 333 and registered DDRII 400 DIMMs can be used with IOP331. The memory controller supports 32-bit or 64-bit memory subsystems with or without ECC. The IOP331 features a new dual-ported memory controller that provides both a direct port from the CPU to memory (core port) and a port from the ATU/internal bus to memory (internal bus port). This allows both CPU memory accesses and data movement to and from the internal bus to occur providing high overall system performance. Performance optimizations can be made by using the memory controller arbiter that can be programmed to define the number of transactions a given port can transfer at a time, therefore allowing the other port access to memory. It also helps maximize core processor performance by allowing the core to preempt an active transaction from the internal bus port so the core is not starved. To further provide higher core to memory performance, a 32-bit memory region can be defined in bank 0 to eliminate ECC Read-Modify-Write operations on 4-byte writes (matches Intel XScale data size). This 32-bit region is ideal for core-related data structures, like DMA/AAU descriptors or I/O controller descriptors and control blocks.

The Intel IOP331 also has made significant improvements to the interrupt controller in order to reduce interrupt latency. The interrupt controller includes an advanced vector generator for both FIQ and IRQ interrupts, delivering the vector directly to the interrupt service routine, saving software overhead. Also included is an interrupt prioritizer that uses a two-bit field for each interrupt source to provide four levels of interrupt priority.

High integration provides board space and system-level cost savings

The integrated 133 MHz PCI-X to PCI-X bridge reduces system BOM cost and real estate. The integrated bridge includes 8 Kbyte data buffers in each direction and eliminates the need for an external PCI-X to PCI-X bridge providing a great deal of board

Intel® IOP331 I/O block diagram



space savings. The IOP331 is designed with a single ATU interface on the secondary PCI bus. This greatly simplifies code porting from designs using an external bridge as the programming and data-flow model are the same. The IOP331 provides central resource functionality on the secondary PCI-X bus and includes an integrated arbiter, clock outs for up to four devices and the capability to enable internal pull-up resistors on all the secondary PCI-X bus signals by a reset strap. The secondary PCI-X bus also supports public and private devices. A group of ten secondary IDSELs can be made public to the host or private to IOP331 by a reset strap. The bridge supports different PCI/PCI-X bus speeds and bus widths on the primary and secondary busses. For example, the primary bus can operate at PCI-66, while the secondary bus operates at PCI-X100. The IOP331 integrates a 2-channel DMA controller with support for unaligned transfers using both scatter-gather and direct modes. The 2-channel DMA controller facilitates increased PCI-to-memory throughput and memory-to-memory throughput. The IOP331 also integrates two UARTs, and two I²C ports to further reduce system cost/complexity. The 4-pin UARTs are 16550 register compatible with 64-byte transmit and receive FIFOs, and a programmable baud rate generator (up to 115 Kbps). If UART functionality is not needed, the eight pins used by the UARTs can also be used as GPIOs or external interrupts.

The Intel IOP331 provides an 8-bit or 16-bit, 66 MHz Peripheral Bus Interface (PBI) that is excellent for embedded applications requiring a connection to non-PCI peripheral components such as ASICs, flash memory, or DSPs. The PBI provides two chip selects and supports programmable bus width and wait states for two memory windows.

The IOP331 integrates two application acceleration engines targeted at specific applications: RAID5 XOR and iSCSI CRC32C. The Application Accelerator Unit (AAU) contains a hardware-based XOR capability using a 1 Kbyte queue to accelerate RAID-related parity calculations. The AAU speeds the transfer of read and write data to the memory controller and computes data parity across local memory blocks. The two DMA channels provide a hardware assist for iSCSI applications by calculating CRC32C on the data during the block transfer. The CRC engine uses the CRC32C algorithm required by the iSCSI specification. These application acceleration engines provide a significant performance boost, and eliminate the need for external ASICs saving cost and board space for RAID, Storage, and iSCSI networking applications.

Order Information

Please reference the most up-to-date Order Configurations and Regulatory Compliance Specifications along with additional product information at developer.intel.com/design/storage.

Intel® I/O Processor Comparison

	Intel® IOP331	Intel® IOP321	Intel® IOP315
Core Speed	500/667/800 MHz	400/600 MHz	400 MHz, 600 MHz, 733 MHz
Package Size	37.5 mm x 37.5 mm	35 mm x 35 mm	40 mm x 40 mm and 23 mm x 23 mm
Integrated Bridge	133 MHz, 64-bit PCI-X Bridge	133 MHz, 64-bit PCI-X Interface	133 MHz, 64-bit PCI-X Bridge
Memory Controller	Dual-ported DDR 333 MHz/ DDRII 400 MHz	200 MHz DDR	Dual-ported 200 MHz DDR
Internal Frequency	266 MHz (2.1 GB/s) Bus	200 MHz (1.6 GB/s) Bus	133 MHz Switching Fabric
Memory Addressable	DDR 333 (2 GB)/ DDRII 400 (1 GB)	1 GB	12 GB
Local Bus Width	8/16 Bits (66 MHz)	32 Bits (up to 100 MHz)	32 Bits (up to 133 MHz)
DMA Buffer Size	1024 Bytes	1024 Bytes	Packet-based 4 x 256 Bytes
ATU Buffer Size	4096 Bytes	4096 Bytes	4 x 1024 Bytes
Application Accelerator w/ XOR	Yes	Yes	Yes
I²C Bus	2 Serial Units	2 Serial Units	2 Serial Units
Hardware-based CRC32C check	Yes	No	Yes
UART	(2) 4-Pin (16550)	No	2 – 9-Pin (16550)
Arbiter	Yes	No	Yes
External Interrupts	12 + 1 HPI	4 + 1 HPI	16

Features	Benefits
■ 500/667/800 MHz Intel® XScale™ core ■ Integrated, System on a chip design	High performance with low power
Dual PCI/PCI-X Interfaces ■ Integrated PCI-X Bridge ■ Up to 133 MHz operation ■ 2 DMA units with chaining support ■ Support to configure the device from remote PCI host	PCI-X to PCI-X Bridge integration lowers BOM cost and helps reduce board space
Optimized Memory Controller ■ DDR 333 and DDRII 400 with ECC ■ 64-, 72-bit memory, and 32-bit mode also supported	Intel XScale core has direct memory access resulting in much improved performance
Communications ■ I²C ■ UARTs ■ 16-bit local bus with two chip selects ■ 8 GPIO pins	Integration helps reduce board space and lower BOM cost
Application Accelerator Units in DMA ■ RAID5 XOR ■ iSCSI CRC32C	Application-specific integration in hardware improves RAID5 and iSCSI performance and helps reduce CPU overhead

Intel Access

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Other Intel Support:	Intel® Technical Documentation Center www.intel.com/go/techdoc (800) 548-4725 7 a.m. to 7 p.m. CST (U.S. and Canada) International locations please contact your local sales office.
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