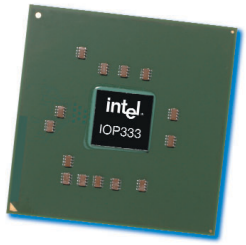
Intel® IOP333 I/O Processor with Intel XScale® Microarchitecture

Up to 800 MHz CPU, integrated PCI Express* to PCI-X* bridge, Application Accelerator for RAID 6, and dual-ported memory controller delivers superior performance

Product Highlights

- 32-bit high-performance CPU (500, 667, 800 MHz) based on Intel XScale® microarchitecture
- Integrated PCI Express* (PCIe) to PCI-X* bridge (PCI Express 1.0A, PCI-X 1.0A, and PCI 2.3 compliant), two PCI-X bus segments: one via transparent bridge for motherboard slots or devices and also supports PCI-X Hot Plug; second segment controlled by Intel XScale core
- Double Data Rate (DDR) 333 and DDR2-400 SDRAM with ECC (up to 2 GB of 32- or 64-bit memory, optional single-bit error correction/multi-bit detection support)
- Dual-ported memory controller with pipe-lined access from the Intel XScale core to internal peripherals (programmable control for preemption by the Intel XScale core and a multi-transaction counter for performance tuning)
- Application accelerator for intelligent RAID 6 processing supports P+Q or 2D XOR methods
- Pin-compatible with the Intel® IOP332 I/O processor
- RAID 5 XOR and iSCSI CRC32C off-load engines
- 8-/16-bit, 66 MHz Peripheral Bus Interface (programmable bus width and wait states for two memory windows, two chip selects)
- 333 MHz, 64-bit (up to 2.7 GB/sec) internal bus
- 2-channel Direct Memory Access (DMA) engine with support for scatter and gather of data blocks, automatic data chaining, and unaligned data transfers between PCI-to-local memory, local memory-to-PCI, and memory-to-memory (three 1 Kbyte data buffers per channel)



- Up to 17 external interrupt inputs to the Interrupt Controller support vector generation and four priority levels
- Two 16550-compatible UARTs (4-pin, master/slave-capable, 64-byte receive/transmit FIFOs)
- Eight GPIO pins that can also be used as external interrupt pins
- Two industry-standard-based I^2C interfaces
- SMBus support
- Two programmable 32-bit Timers and Watchdog Timer
- Typical power consumption is less than 10 Watts (500 MHz)
- 829-ball FCBGA (37.5 mm^2)

Product Overview

High-performance, I/O processor based on Intel XScale® technology

The Intel® IOP333 is a highly integrated I/O system-on-a-chip for RAID on Motherboard and I/O-intensive storage, networking, and communications applications. The IOP333 features an 800 MHz CPU, high-performance internal bus, dual-ported memory controller, high-bandwidth PCI Express to PCI-X bridge, an application accelerator tuned for intelligent RAID 6, and an improved interrupt controller to provide a high-performance, highly integrated processor solution. Target applications include RAID on Motherboard and PCI Express host-

based adapters (RAID cards, iSCSI cards, FC cards, Security SSL NICs, etc.), and a host of other intelligent I/O applications that require a highly integrated, high-performance system-on-a-chip processor with an integrated PCI Express interface.

As Intel's next-generation I/O processor, the Intel® IOP333 continues to build on Intel's strength in delivering high-performance, low-power Intel XScale microarchitecture processors. It integrates Intel's Superpipelined RISC Technology with a 7-stage integer/8-stage memory superpipelined core, 32 Kbyte data and instruction caches, and operates up to 800 MHz. The IOP333 is code-compatible with previous-generation Intel XScale microarchitecture processors such as the Intel® IOP332, Intel® IOP331, and Intel® IOP321 I/O processors and other ARM*-based devices, simplifying code porting from existing designs. It is compliant with the ARM v5TE instruction set (excluding the floating-point instructions). The internal bus operates at 333 MHz and offers internal bandwidth of up to 2.7 GB/sec.

The IOP333 provides ultra-fast memory transactions due to its DDR SDRAM dual-ported memory controller and supports up to 2 GB of DDR 333 MHz memory or 1 GB of DDR2-400 MHz memory. Registered and unbuffered DDR 333 and registered DDR2-400 DIMMs can be used with the IOP333. The memory controller supports 32-bit or 64-bit memory subsystems with or without ECC. The IOP333 features an enhanced memory controller that provides a direct port from the CPU to memory (core port) as well as a port from the ATU/internal bus to memory (internal bus port). This allows CPU memory accesses and data movement to and from the internal bus to occur providing high overall system performance. Performance optimizations can be made by programming the memory controller arbiter to define the number of transactions a given port can transfer at a time, allowing the other port planned access to memory. It also helps maximize processor performance by allowing the core to preempt an active transaction from the internal bus port, so the core is not waiting on a memory access. A 32-bit memory region can be defined in bank 0 to eliminate ECC Read-Modify-Write operations on 4-byte writes (which matches the Intel XScale microarchitecture data size), providing higher core-to-memory performance. This 32-bit region is ideal for core-related data structures, like DMA/AAU descriptors or I/O controller descriptors and control blocks.

The IOP333 also has significant improvements to the interrupt controller to help reduce interrupt latency. The interrupt controller includes an advanced vector generator for both FIQ and IRQ interrupts, delivering the vector directly to the interrupt service routine, which saves software overhead. Also included is an interrupt prioritizer that uses a two-bit field for each interrupt source to provide four levels of interrupt priority.

Features	Benefits
• 500, 667, 800 MHz Intel XScale® core • Integrated, system-on-a-chip design	High performance with low power
PCI Express* to PCI-X* Bridge	
• Dual PCI/PCI-X interfaces • Up to 133 MHz operation	PCI Express to PCI-X bridge integration lowers BOM cost and helps reduce board space
Dual Ported Memory Controller	
• DDR 333 or DDR2-400 with ECC • 64-, 72-bit memory, 32-bit mode also supported	Intel XScale core has direct memory access to external memory resulting in much-improved performance
Other Interfaces	
• Two I^2C • Two UARTs • 16-bit local bus with 2-chip selects • Eight GPIO pins	Integration helps reduce board space and lowers BOM cost
Advanced Interrupt Controller	
• Vector port to interrupts	Software overhead saving and faster interrupt servicing
AAU to DMA	
• RAID 6 P+Q • RAID 5 XOR • iSCSI CRC32C	Application-specific integration in hardware improves RAID and iSCSI performance, and helps reduce CPU overhead

High integration saves board space and system-level costs

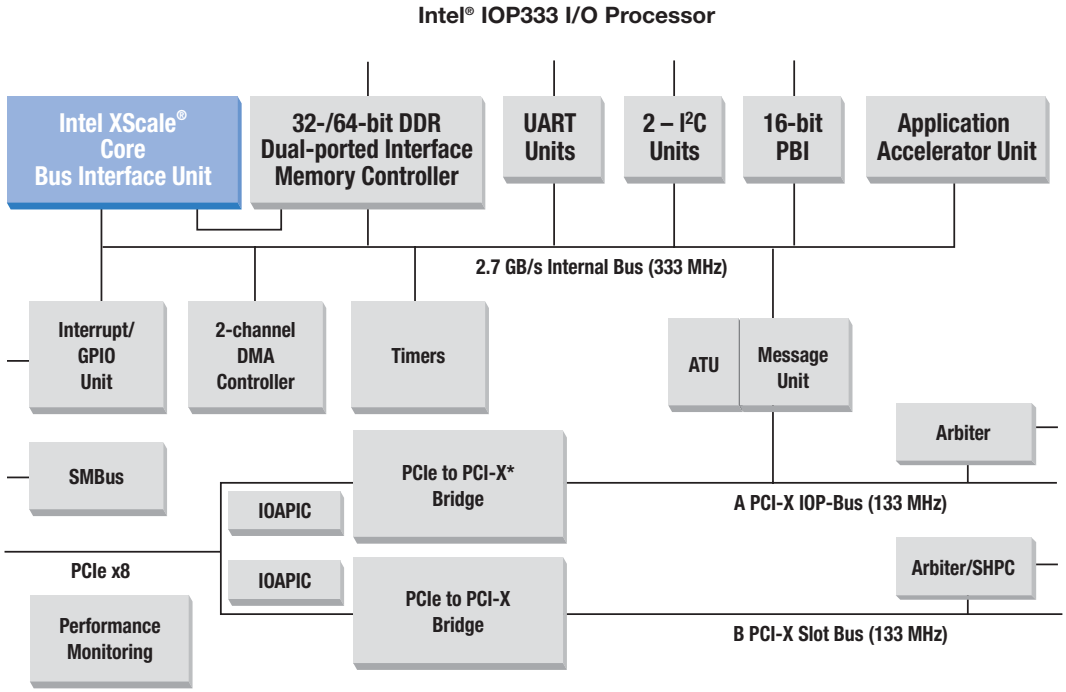
The integrated PCI Express to PCI-X bridge helps reduce system BOM cost and saves board real estate. Both PCI-X buses are highly scalable and flexible with integrated clocks and arbiter to support four secondary devices on the "A-segment" and five secondary devices on the "B-segment." The IOP333 is designed with a single ATU interface to the A-segment PCI-X bus. This greatly simplifies code porting from designs that use an external bridge – the programming and data flow models are very similar. The A-segment PCI-X bus also supports public and private devices. A group of seven secondary IDSELs can be made public to the host or private to the IOP333 by a bridge register setting. The bridge can support different PCI/PCI-X bus speeds and bus widths on the two segments. For example, the A-segment can operate at PCI-66, while the B-segment operates at PCI-X 100.
The IOP333 integrates a 2-channel DMA controller with support for unaligned transfers using both scatter-gather and direct modes. The 2-channel DMA controller facilitates increased PCI-to-memory throughput and memory-to-memory throughput. The IOP333 also integrates two UARTs, SMBus support, and two I^2C ports to further reduce system cost and complexity. The 4-pin UARTs are 16550 register compatible with 64-byte transmit and receive FIFOs, and a programmable baud rate generator (up to 115 Kbps). If UART functionality is not needed, the eight pins used by the UARTs can alternatively be used as GPIOs or external interrupts.

The IOP333 provides an 8-bit or 16-bit, 66 MHz Peripheral Bus Interface (PBI) that is excellent for embedded applications requiring a connection to non-PCI peripheral components such as ASICs, flash memory, or DSPs. The PBI provides two chip selects and supports programmable bus width and wait states for two memory windows.

The IOP333 integrates three application acceleration engines: RAID 6, RAID 5 XOR and iSCSI CRC32C. The newly integrated RAID 6 Application Accelerator provides much faster data reads than previous generations of Intel IOPs. An added advantage, the RAID-6 P+Q AAU offers a hardware foundation that will help simplify software development and upgrades from this IOP generation to the next. The RAID 5 Application Accelerator Unit (AAU) contains a hardware-based XOR using a 1 Kbyte queue to accelerate RAID-related parity calculations. The application accelerator speeds the transfer of Read and Write data to the memory controller and computes data parity across local memory blocks. The two DMA channels provide a hardware assist for iSCSI applications by calculating CRC32C on the data during the block transfer that is required by the iSCSI specification. These application acceleration engines provide a performance boost, and eliminate the need for external ASICs saving cost and board space for RAID, storage, and iSCSI networking applications.

Intel® I/O Processor Comparison

	Intel® IOP333	Intel® IOP332	Intel® IOP331
Core Speed	500/667/800 MHz	500/667/800 MHz	500/667/800 MHz
Package Size	37.5mm x 37.5mm	37.5mm x 37.5mm	37.5mm x 37.5mm
Integrated Bridge	PCI Express* to PCI-X* bridge	PCI Express to PCI-X bridge	133 MHz, 64-bit PCI-X bridge
Memory Controller	Dual-ported DDR 333 MHz/DDR2-400 MHz	DDR 333 MHz/DDR2-400 MHz	Dual-ported DDR 333 MHz/DDR2-400 MHz
Internal Frequency	333 MHz (up to 2.7 GB/s) bus	266 MHz (up to 2.1 GB/s) bus	333 MHz (up to 2.7 GB/s) bus
Memory Addressable	DDR 333 (2 GB)/DDR2-400 (1 GB)	DDR 333 (2 GB)/DDR2-400 (1 GB)	DDR 333 (2 GB)/DDR2-400 (1 GB)
Local Bus Width	8/16 Bits (66 MHz)	8/16 Bits (66 MHz)	8/16 Bits (66 MHz)
DMA Buffer Size	1024 Bytes	1024 Bytes	1024 Bytes
ATU Buffer Size	4096 Bytes	4096 Bytes	4096 Bytes
Application Accelerator with XOR	Yes	Yes	Yes
Application Accelerator for RAID 6	Yes	No	Yes
I^2C Bus	2 Serial Units	2 Serial Units	2 Serial Units
Hardware-based CRC32C check	Yes	Yes	Yes
UART	2 – 4-Pin (16550)	2 – 4-Pin (16550)	2 – 4-Pin (16550)
Arbiter	Yes	Yes	Yes
External Interrupts	16 + 1 HPI	12 + 1 HPI	12 + 1 HPI



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