Intel® 80331 I/O Processor

Schematic Review Checklist

September 2003

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Date	Revision	Description
September 2003	001	Initial Release.

1.0 Introduction

This checklist is for the Intel® 80331 I/O processor[1] (80331) and is a compilation of key signals and strap options. It is not meant to be a complete signal list or a substitute for proper study of available design guides or reference schematics. Designers, use this guide in conjunction with the *Intel® 80331 I/O Processor Design Guide* (#273823) and board schematics.

Routing and layout requirements need to be followed per the *Intel® 80331 I/O Processor Design Guide*, unless board simulations have been performed to validate alternate solutions.

Table 1. Intel® 80331 I/O Processor Checklist (Sheet 1 of 6)

❑	Unit Checklist
Memory Controller Unit	
	1. The 80331 memory controller supports the following: a. DDR: 128/256/512 Mbit, 1 Gbit SDRAM technology, with a maximum memory of 2 Gbytes. b. DDR-II: 256/512 Mbit SDRAM technology, with a maximum memory of 1 Gbytes.
	2. **M_CK[2:0]** and **M_CK[2:0]#** routing and layout requirements must be followed per the *Intel® 80331 I/O Processor Design Guide*. 22 ohm series resistors are recommended for DDR333 unbuffered memory configurations. The 80331 supports only registered (buffered) DDR-II 400 DIMMs, therefore only M_CK[0]/M_CK[0]# are used. Leave unused clocks as 'no connects'.
	3. **M_RST#** is only used by registered (buffered) DIMMs. Can be left as a 'no connect' for unbuffered DIMMs.
	4. When using DDR memory only, the following DDR-II pins are: a. **DQS[8:0]# -** Leave as no connects. b. **ODT[1:0]** - Leave as no connects. c. **DDRRES[2:1]** - 1 K pull-down.
	5. **DDRCRES0** and **DDRIMPCRES** need to be connected together through a 287 ohm resistor for DDR-II and 385 ohm resistor for DDR.
	6. **DDRCRES0** and **DDRSLWCRES** need to be connected together through a 825 ohm resistor for DDR-II and 845 ohm resistor for DDR.
	7. When using DDR-II memory, **DDRRES2** needs to be connected to a 40.2 ohm (.5%) pull-up to 1.8 V. **DDRRES1** needs to be connected to ground via a 40.2 ohm (.5%) resistor. There needs to be a 0.1 µF cap tied to ground for both of these signals.
	8. **MEM_TYPE** is a reset strap, muxed on **AD[2]** (of the peripheral bus), defining the DDR SDRAM interface. 0 = DDR-II 400 (requires a 1.5 K pull down resistor). 1 = DDR333 (default mode, using internal pull-up).
	9. **DQ, DQS, CB** and **DM** signal groups require 22 ohm series resistors and 50 ohm parallel resistors tied to Vtt (0.5 Vcc25/18) for DDR333. Routing and layout requirements need to be followed per the *Intel® 80331 I/O Processor Design Guide*.
	10. Control signal group (**RAS#, CAS#, WE#, BA[1:0], MA[13:0], CS[1:0]#** and **CKE[1:0]**) require 22 ohm series resistors and 50 ohm parallel resistors tied to Vtt (0.5 Vcc25/18) for DDR333. Routing and layout requirements need to be followed per the *Intel® 80331 I/O Processor Design Guide*.

1. ARM* architecture compliant.

Table 1. Intel® 80331 I/O Processor Checklist (Sheet 2 of 6)

❑	Unit Checklist
Peripheral Bus Interface	
	1. **PCE[0]#** needs to be connected to the chip enable on the boot Flash.
	2. **P_BOOT16#** is a reset strap, muxed on **AD[4]** (of the peripheral bus), which sets the default bus width of the PBI memory boot window. 0 = 16 bits wide (requires a 1.5 K pull down resistor). 1 = 8 bits wide (default mode, using internal pull-up).
	3. **AD[15:3]** signals require a latch to demultiplex the address and data. 8-bit devices require a latch on the **AD[7:3]** signals. 16-bit devices require latches on the **AD[15:3]** signals.
	4. The **A[2:0]** signals provide a demultiplexed version of bits 2:0 of the **AD[15:0]** bus, therefore can be connected directly without a latch.

Table 1. Intel® 80331 I/O Processor Checklist (Sheet 3 of 6)

❑	Unit Checklist
Secondary PCI-X Bus	
	1. **PCIODT_EN** is a reset strap, muxed on **A[20]** (of the peripheral bus), which determines when internal pull-ups are enabled on the secondary PCI bus. 0 = ODT disabled (requires a 1.5K pull down resistor). External 8.2 K pull-ups to 3.3 V are required. 1 = ODT enabled (default mode, using internal pull-up). Will enable 8.2 K internal pull-ups to 3.3 V. The following signals are affected by **PCIODT_EN**: S_AD[63:32], S_C/BE[7:4]#, S_PAR64, S_REQ64#, S_REQ[3:0]#, S_ACK64#, S_FRAME#, S_IRDY#, S_DEVSEL#, S_TRDY#, S_STOP#, S_PERR#, S_LOCK#, S_M66EN, S_SERR#, S_INT[D:A]#
	2. 64-bit extensions and control signals need 8.2 K pull-ups, when **PCIODT_EN** is off. When **PCIODT_EN** is on (default mode), then no external pull-ups are required.
	3. **S_REQ[3:0]#** needs 8.2 K pull-ups, when **PCIODT_EN** is off.
	4. **S_PCIXCAP** needs 0.1 µF capacitor and 3.3 K pull-up resistor.
	5. **S_M66EN** needs 0.01 µF capacitor and 4.7 K pull-up resistor (when **PCIODT_EN** is off).
	6. **S_CLKOUT** and **S_CLKIN** are connected together with a 33.2 ohm series termination resistor which must be within 500 mils of **S_CLKOUT**. Routing and trace length recommendations need to be followed per the *Intel® 80331 I/O Processor Design Guide*.
	7. **S_CLKO[3:0]** needs a 33.2 ohm series termination resistor and needs to follow routing and trace length recommendations per the *Intel® 80331 I/O Processor Design Guide*. Do not terminate unused clockouts, they can be turned off in software by the PCI Clock Control register.
	8. **S_RCOMP** needs to be connected to ground via a 100 ohm resistor, 1%.
	9. Add a 200 ohm series resistor to IDSEL signals. The address signal used for IDSEL is dependant on whether it is connected to a private or public device. **S_AD[25:17]** can be used for public or private devices (controlled by reset strap, **PRIVDEV**), and **S_AD[31:26]** are used for public devices only. **S_AD30** is reserved for the ATU and **S_AD16** is reserved for the bridge, and need not be used for IDSEL.
	10. **S_PCIX133EN** is a reset strap, muxed on **AD[3]** (of the peripheral bus), which determines the maximum PCI-X mode operating frequency. 0 = 100 MHz enabled (requires a 1.5 K pull down resistor). 1 = 133 MHz enabled (default mode, using internal pull-up).
	11. **S_LOCK#** needs an 8.2 K pull-up resistor. Do not connect it to any other signal, since the lock feature is not supported on the 80331. This signal is renamed to **PU2** (Pull-Up).

Table 1. Intel® 80331 I/O Processor Checklist (Sheet 4 of 6)

❑	Unit Checklist
Primary PCI-X Bus	
	1. **PCIODT_EN** does not control the internal pull-ups for the primary PCI-X bus. Pull-ups are only needed when not already pulled up on the PCI bus. An add-in card may rely on the motherboard to pull-up these signals.
	2. **P_RCOMP** needs to be connected to ground via a 100 ohm resistor, 1%.
	3. **P_M66EN** needs to be connected to 0.01 µF capacitor.
	4. **P_LOCK#** needs an 8.2 K pull-up resistor. Do not connect it to any other signal, since the lock feature is not supported on 80331. This signal is renamed to **PU1** (Pull-Up).
	5. **P_REQ#** and **P_GNT#** have different ball locations between A-0 and B-0 80331 processors. **P_REQ#** signal is ball T6 on A-0 and ball H11 on B-0. **P_GNT#** signal is ball R4 on A-0 and ball G12 on B-0. The 80331 boards incorporate series resistors that can be populated/de-populated for connection to either the A-0 or B-0 P_REQ#/P_GNT# ball location. Route the P_REQ# net to the two ball locations as separate routes through two 0 ohm series resistor located near the PCI edge connector. Route the P_GNT# net to the two ball locations as separate routes through two 0 ohm series resistor located near the PCI edge connector. Populate the resistor that connects the net to the correct ball according to the silicon revision.
I^2C	
	1. **SCL0/SCD0** and **SCL1/SCD1** need 8.2 K pull-ups on clock and data signals. Pull-up value may need to be adjusted based on I^2C bus loading.
UART/GPIO	
	1. The UART and GPIO signals are muxed. When the UART functionality is used, the GPIO function cannot be used. When the GPIO functionality is used, the UART function cannot be used. Usage models include: — Two UARTs and no GPIOs — One UART and four GPIOs — No UARTs and eight GPIOs (external UART could be placed on PBI bus). These signals default as GPIO inputs, therefore 8.2 K external pull-ups are needed when default is kept. As UART signals, an external driver (i.e., MAX561, MAX3232) is needed.

Table 1. Intel® 80331 I/O Processor Checklist (Sheet 5 of 6)

❑	Unit Checklist
MISC Signals	
	1. **TRST#** and **TCK** must have a 1.5 K pull-down when JTAG port is not used. When JTAG port is needed, use recommended circuit in design guide.
	2. **PWRDELAY** needs to be connected to battery backup circuit per the *Intel® 80331 I/O Processor Design Guide* and reference schematics. When battery backup is not needed, then **PWRDELAY** must have a 1.5 K pull-down.
	3. **RETRY** is a reset strap, muxed on **AD[6]** (of the peripheral bus), which determines when configuration retry is enabled. 0 = Configuration cycles enabled (requires a 1.5 K pull down resistor). 1 = Configuration Retry enabled (default mode, uses internal pull-up).
	4. **CORE_RST#** is a reset strap, muxed on **AD[5]** (of the peripheral bus), which determines when the Intel® Xscale™ core is held in reset. 0 = Hold core in reset (requires a 1.5 K pull-down resistor). 1 = Do not hold core in reset (default mode, uses internal pull-up).
	5. **PRIVMEM** is a reset strap, muxed on **A[1]** (of the peripheral bus), which determines when the 80331 operates with private memory space on the secondary PCI bus. 0 = Normal addressing mode (requires a 1.5K pull-down resistor). 1 = Private addressing enable in PCI-to-PCI bridge. (default mode, uses internal pull-up).
	6. **PRIVDEV** is a reset strap, muxed on **A[0]** (of the peripheral bus), which determines when the 80331 operates with private device enabled on the secondary PCI bus. 0 = All secondary PCI devices are accessible to Primary PCI configuration cycles (requires a 1.5K pull-down resistor). 1 = Private devices enabled (default mode, uses internal pull-up).
	7. **BRG_EN** is a reset strap, muxed on **AD[0]** (of the peripheral bus), which determines when the PCI-to-PCI bridge is enabled. 0 = Disable bridge (requires a 1.5K pull-down resistor). 1 = Enable bridge (default mode, uses internal pull-up).
	8. **ARB_EN** is a reset strap, muxed on **AD[1]** (of the peripheral bus), which determines when the integrated arbiter is enabled on the PCI interface. This signal is only valid when BRG_EN = 0. 0 = Internal Arbiter disabled (requires a 1.5K pull-down resistor). 1 = Internal Arbiter enabled (default mode, uses internal pull-up).
	9. **P32BITPCI#** is a reset strap, muxed on **A[2]** (of the peripheral bus), which identifies 80331 subsystem as 64-bit or 32-bit. 0 = 32-bit wide bus (requires a 1.5K pull-down resistor). 1 = 64-bit wide bus (default mode, uses internal pull-up).
	10. **HPI#** requires an external 8.2 K pull-up resistor.
	11. Make sure all no connect (**N/C**) signals are not connected to any signal, power or ground.

Table 1. Intel® 80331 I/O Processor Checklist (Sheet 6 of 6)

❑	Unit Checklist
Power and Ground	
	1. $V_{CCPLL[1-5]}$ and $V_{SSA[1-5]}$ require separate filters connected to 1.5 V rail. See Figure 12 in the *Intel® 80331 I/O Processor Design Guide*. R = 0.5 ohm, L = 4.7 µH and C = 22 µF. **VSSA[1-5]** must not be connected to board ground. **NOTE:** There are only four VCCPLL/VSSA pairs for the 80331. There are no VCCPLL3 and VSSA3 signals.
	2. **DDR_VREF** needs to be connected to 0.5 of the DDR (Vcc25) or DDR-II (Vcc18) voltage rail. Use a voltage divider circuit tied to Vcc25/18, and decoupling capacitors (see Figure 64 in the *Intel® 80331 I/O Processor Design Guide*).
	3. Decoupling caps are required per the *Intel® 80331 I/O Processor Design Guide*.
	4. Voltage sequencing: 80331 requires that the VCC33 voltage rail be equal to (or no less than 0.5 V below) VCC15 at all times during operation, including during system power up and power down. In other words, the following must always be true: VCC33 >= (VCC15 - 0.5 V) This can be accomplished by placing a diode (with a voltage drop < 0.5 V) between VCC15 and VCC33. The Anode is connected to VCC15 and cathode is connected to VCC33.