

80331 DDR DIMM CUSTOMER REFERENCE BOARD

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SHEET TITLE:

80331 DDR DIMM CRB

DATE MODIFIED:

12-5-2003_8:37

REVISION:

2.0

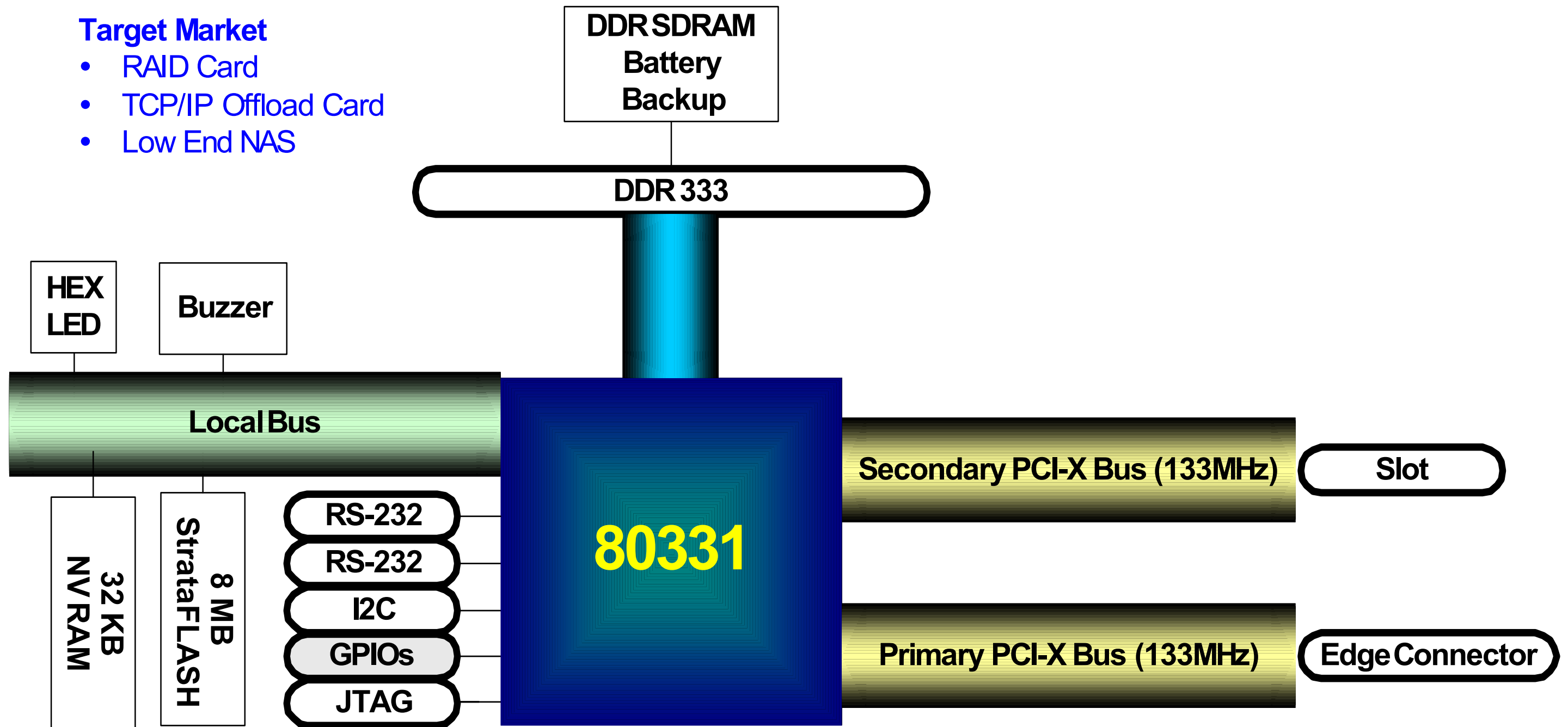
ProtoB

SHEET 1 OF 17

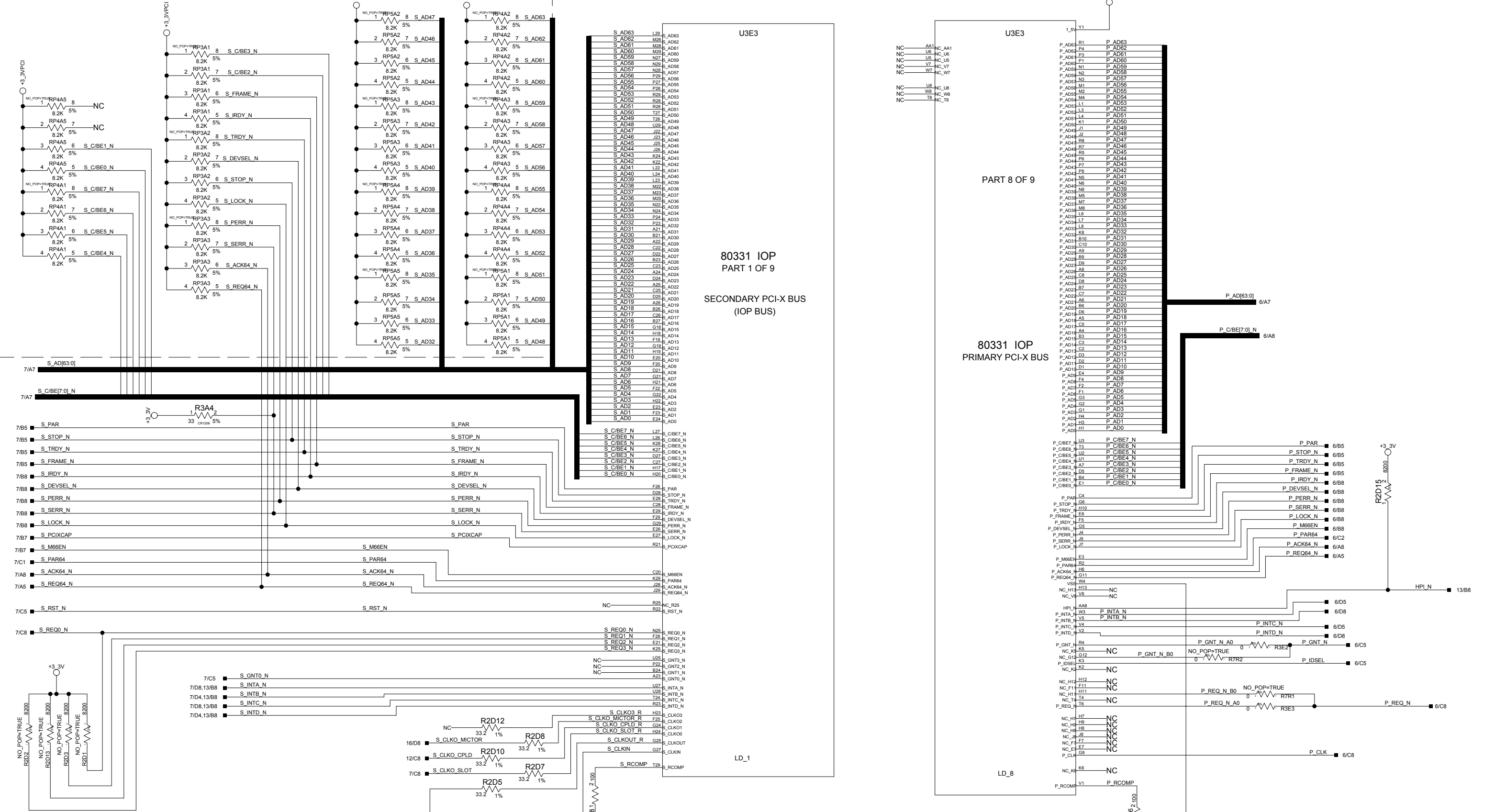
80331 DDR DIMM CUSTOMER REFERENCE BOARD

Target Market

- RAID Card
- TCP/IP Offload Card
- Low End NAS



Place Resistor Packs near PCI Connector
NO_POP RPACKS

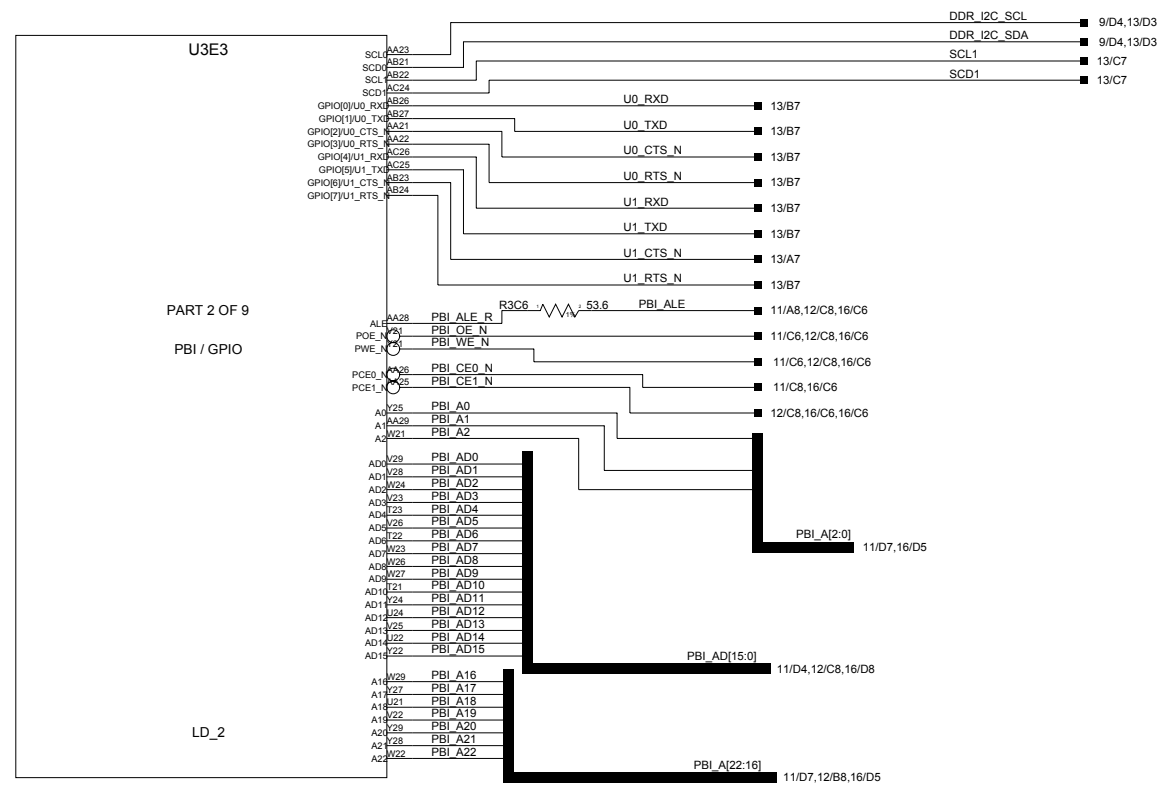


80331 IOP
PART 1 OF 9
SECONDARY PCI-X BUS
(IOP BUS)

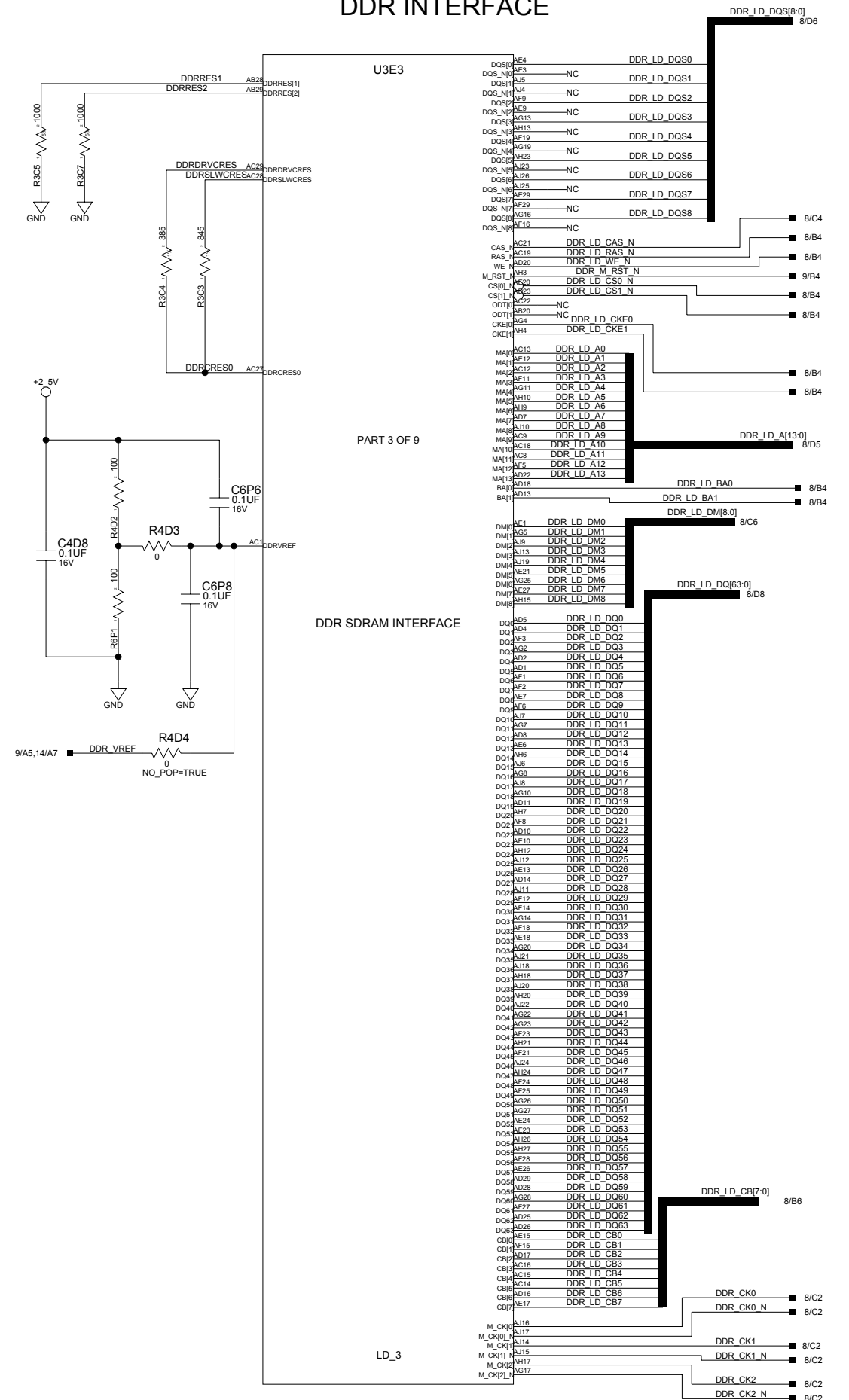
80331 IOP
PRIMARY PCI-X BUS

A0/B0 Routing of REQ/GNT	
A0 silicon	B0 silicon
R83	Populate
R85	Don't Populate
R84	Don't Populate
R82	Populate

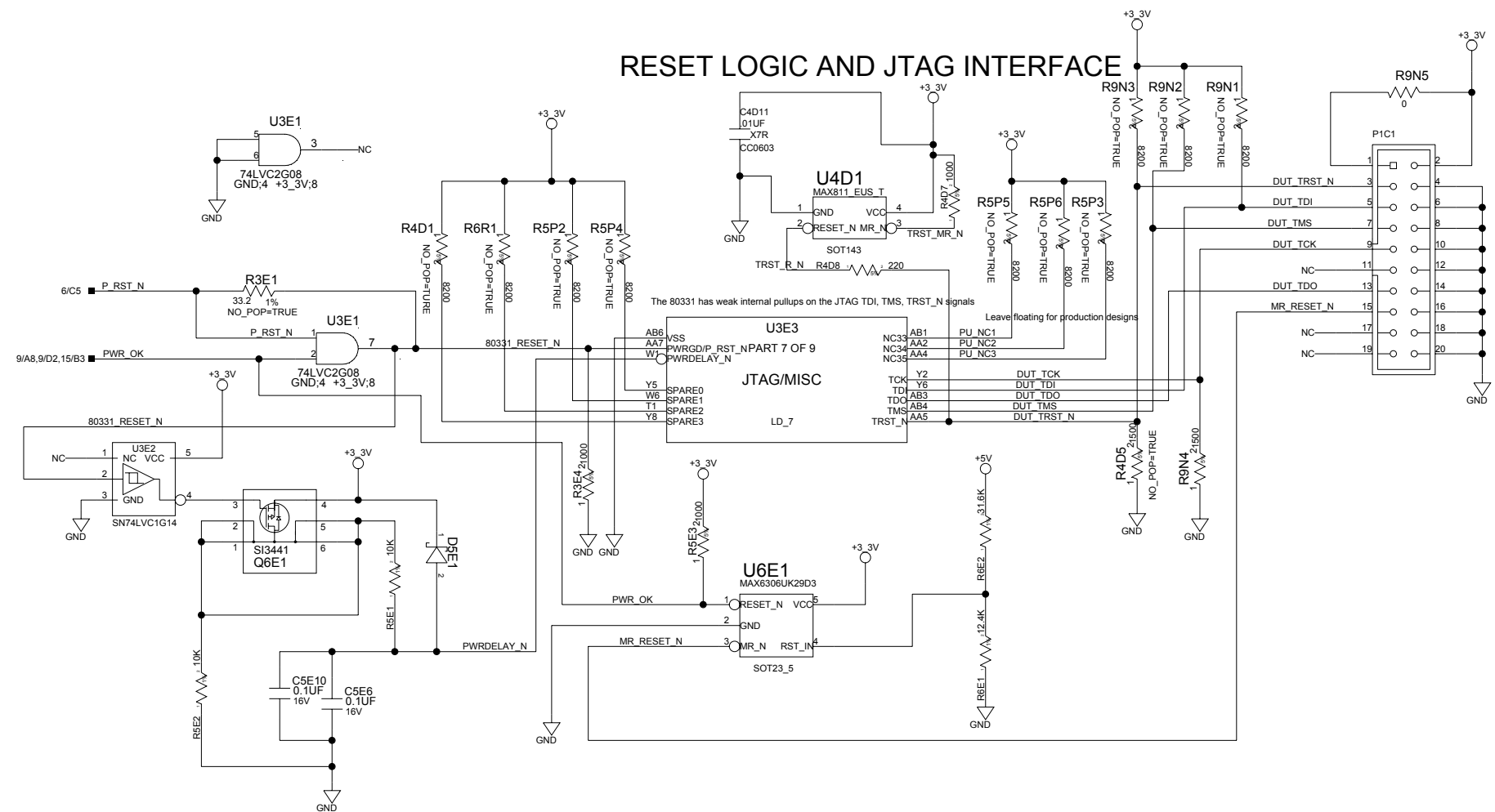
PBI INTERFACE

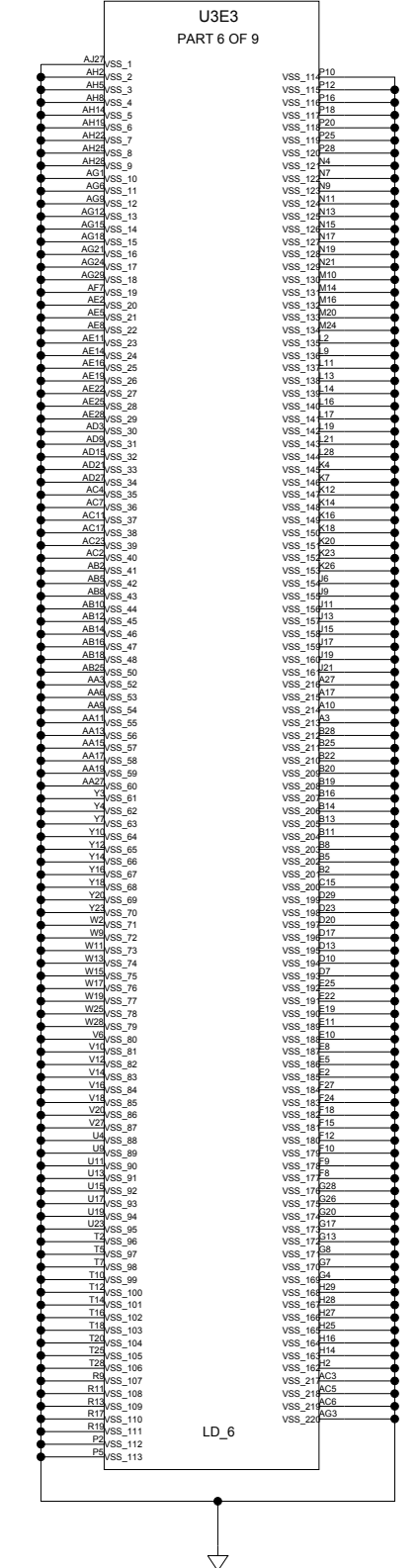
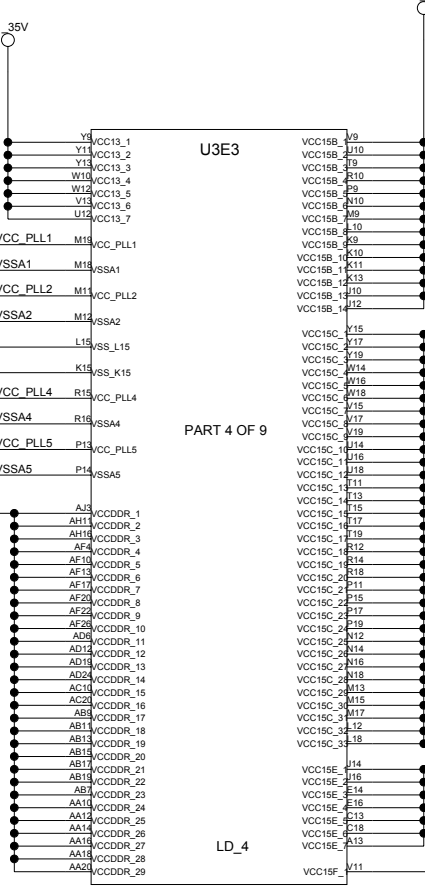
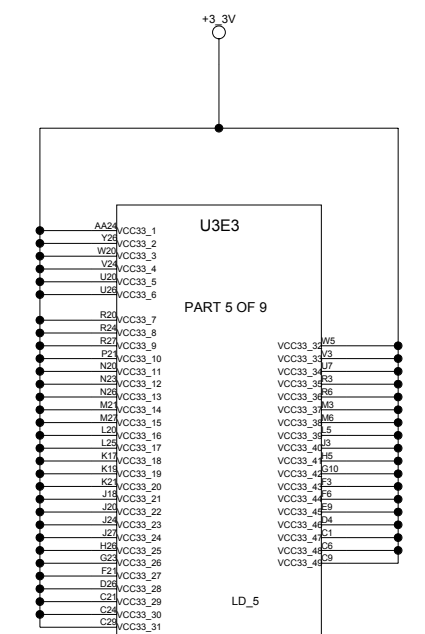
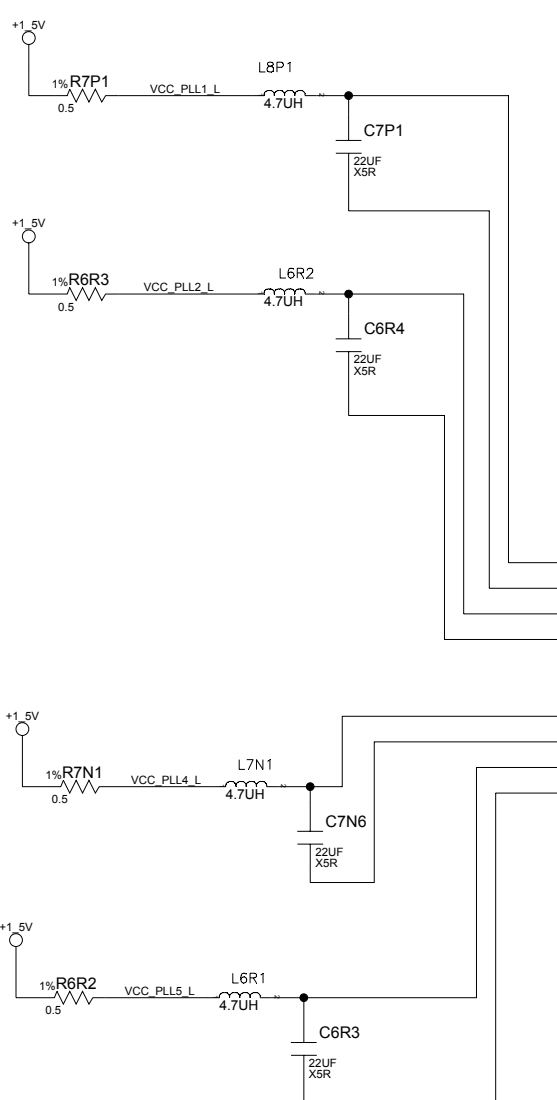
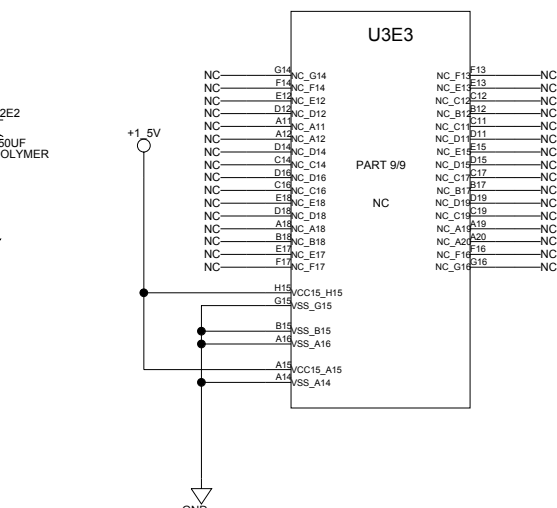
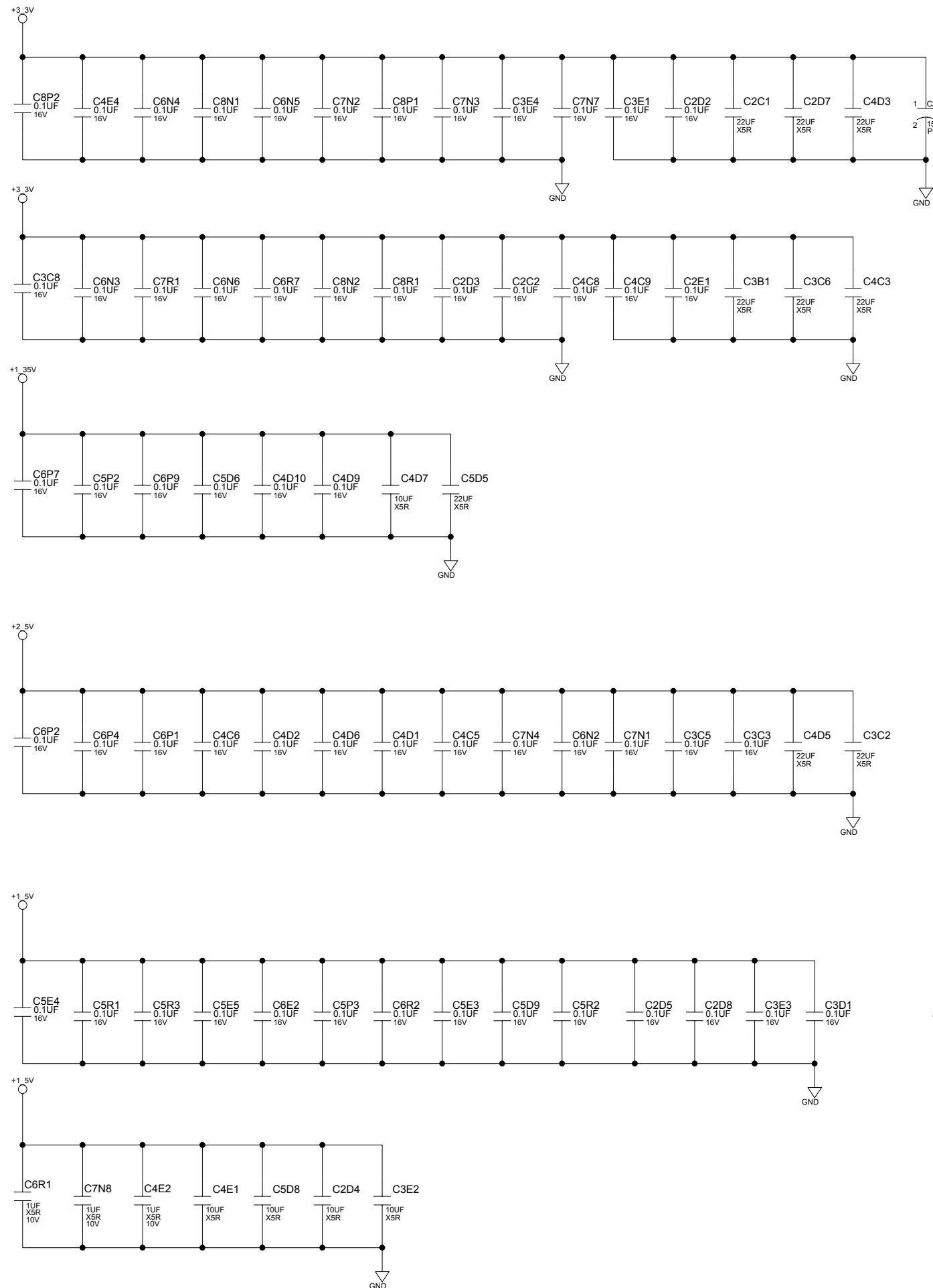


DDR INTERFACE



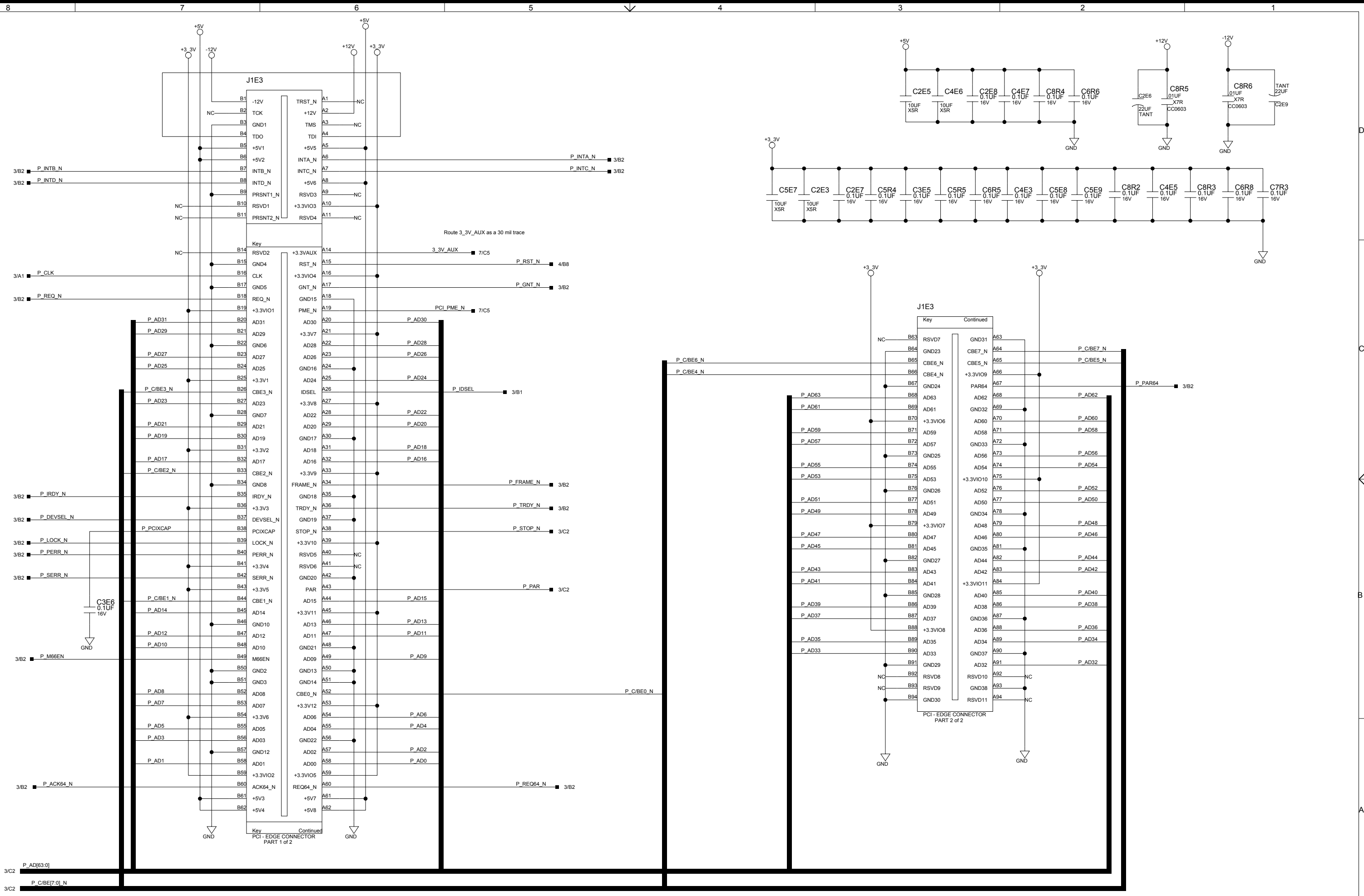
RESET LOGIC AND JTAG INTERFACE

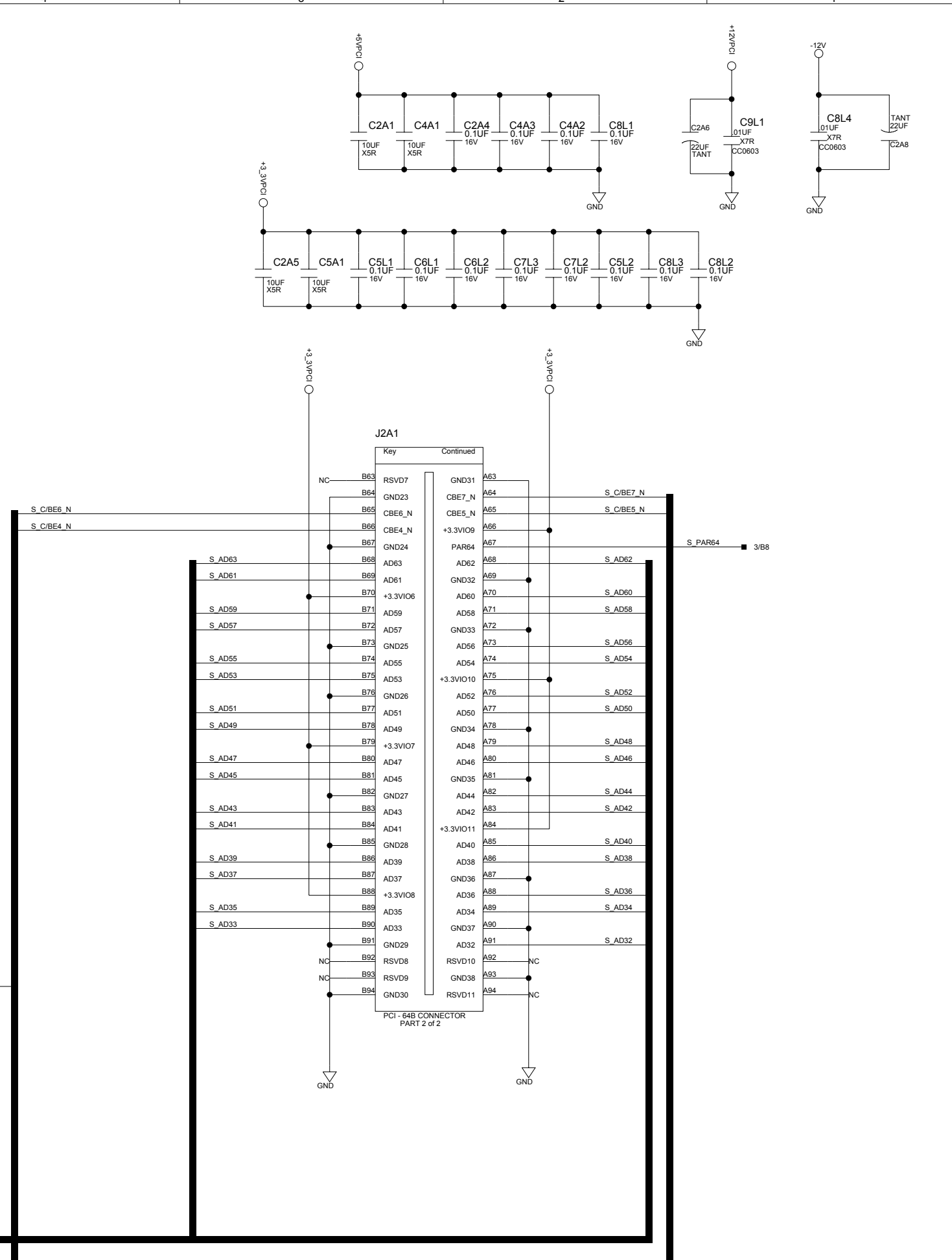
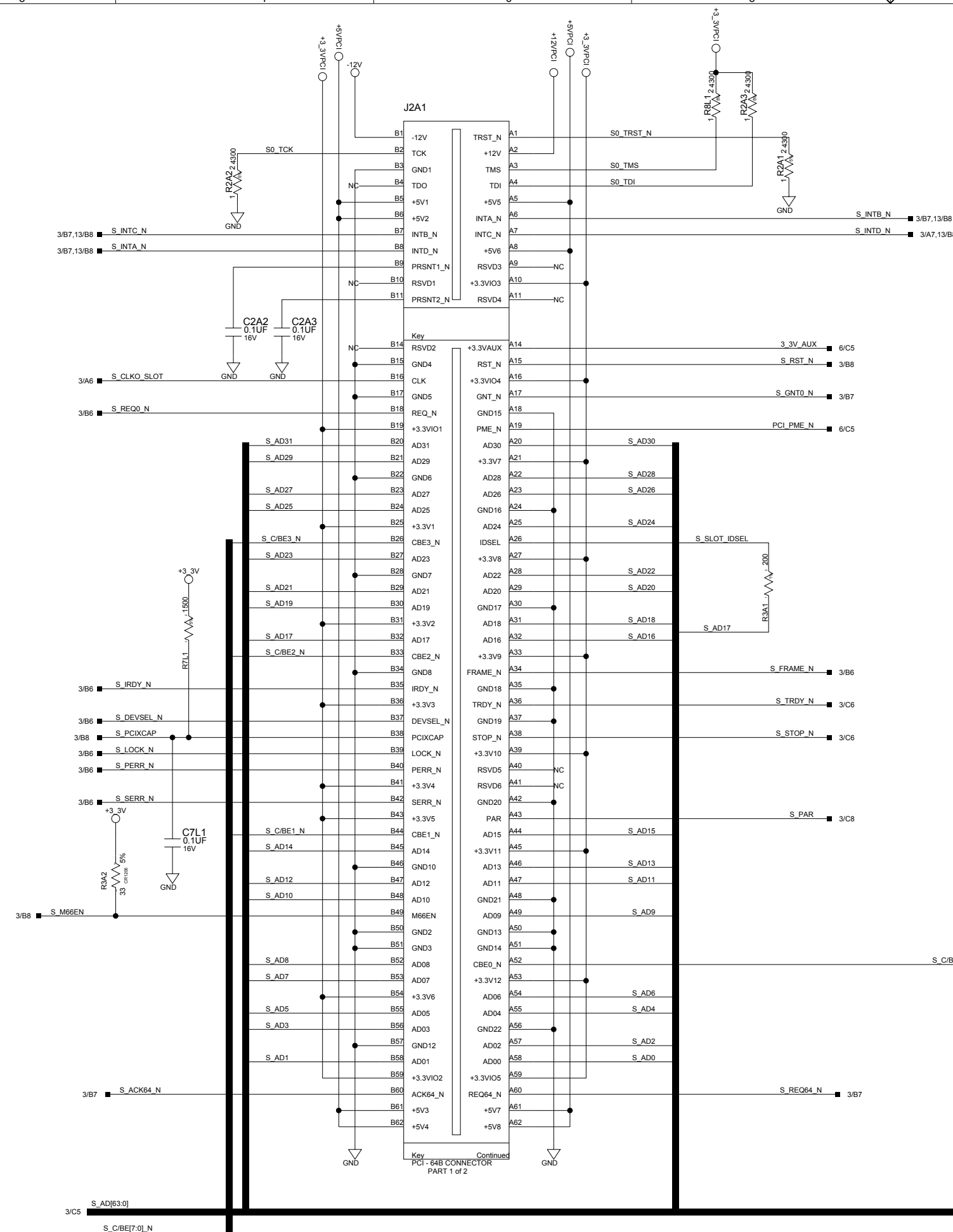


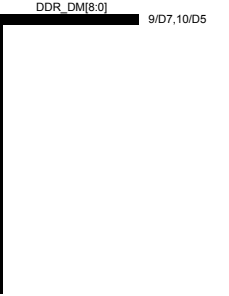
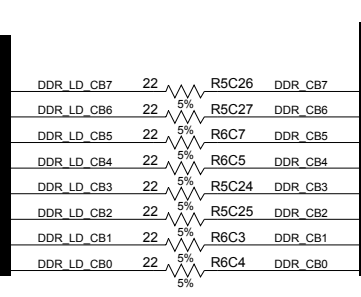
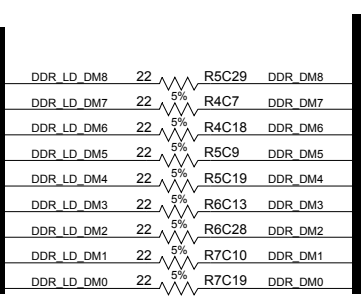
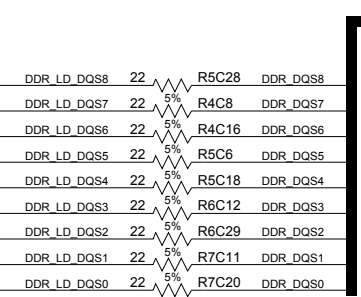
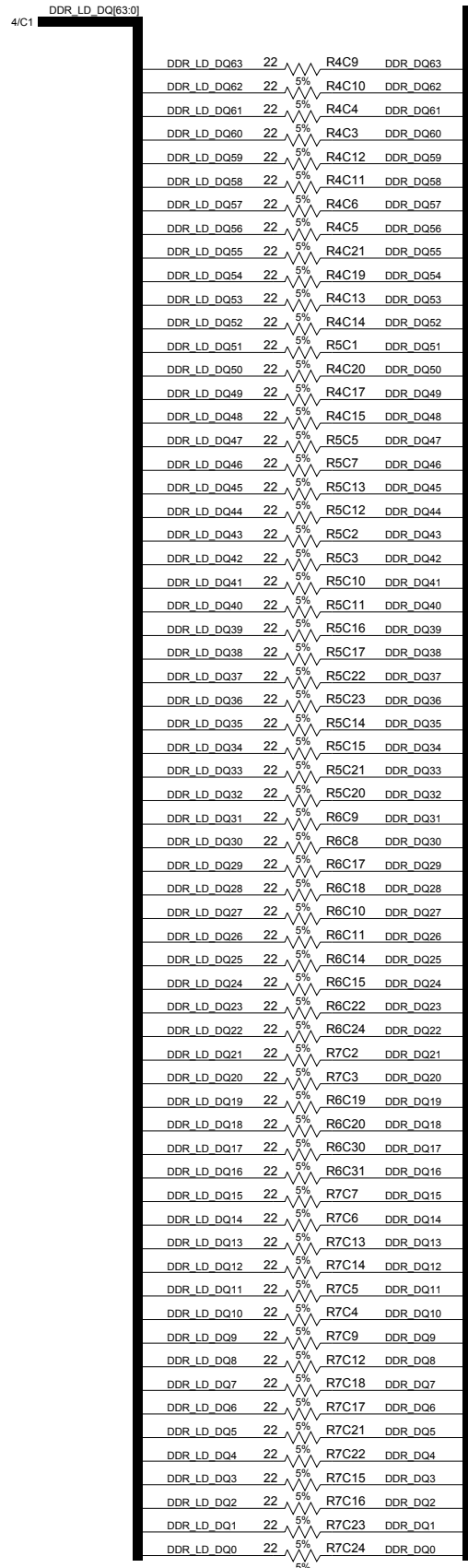


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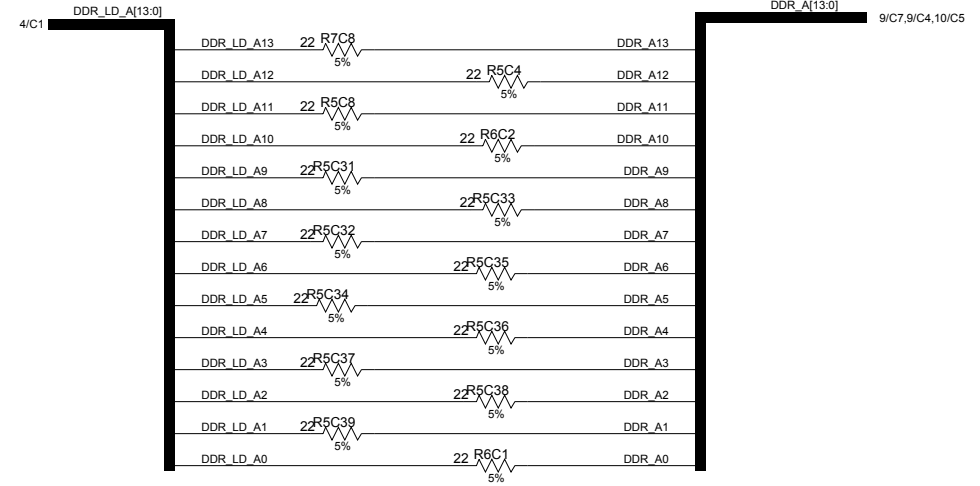
80331 POWER/GROUND



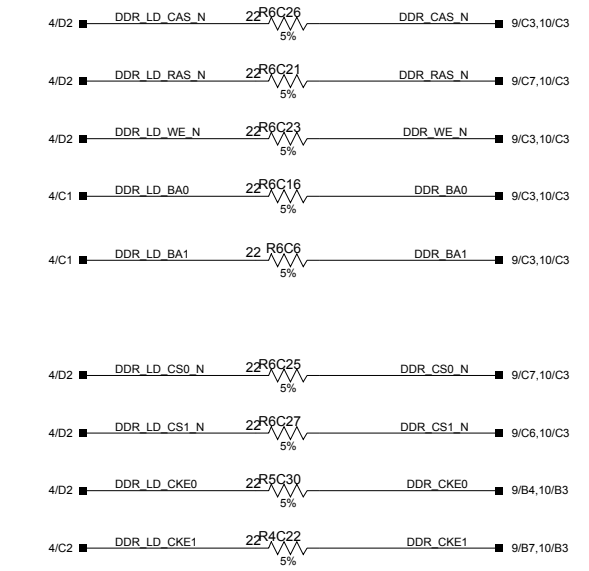


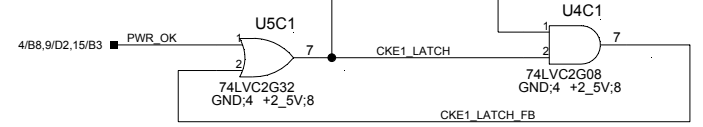
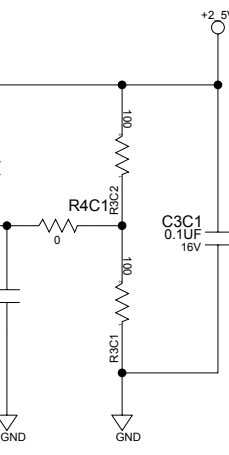
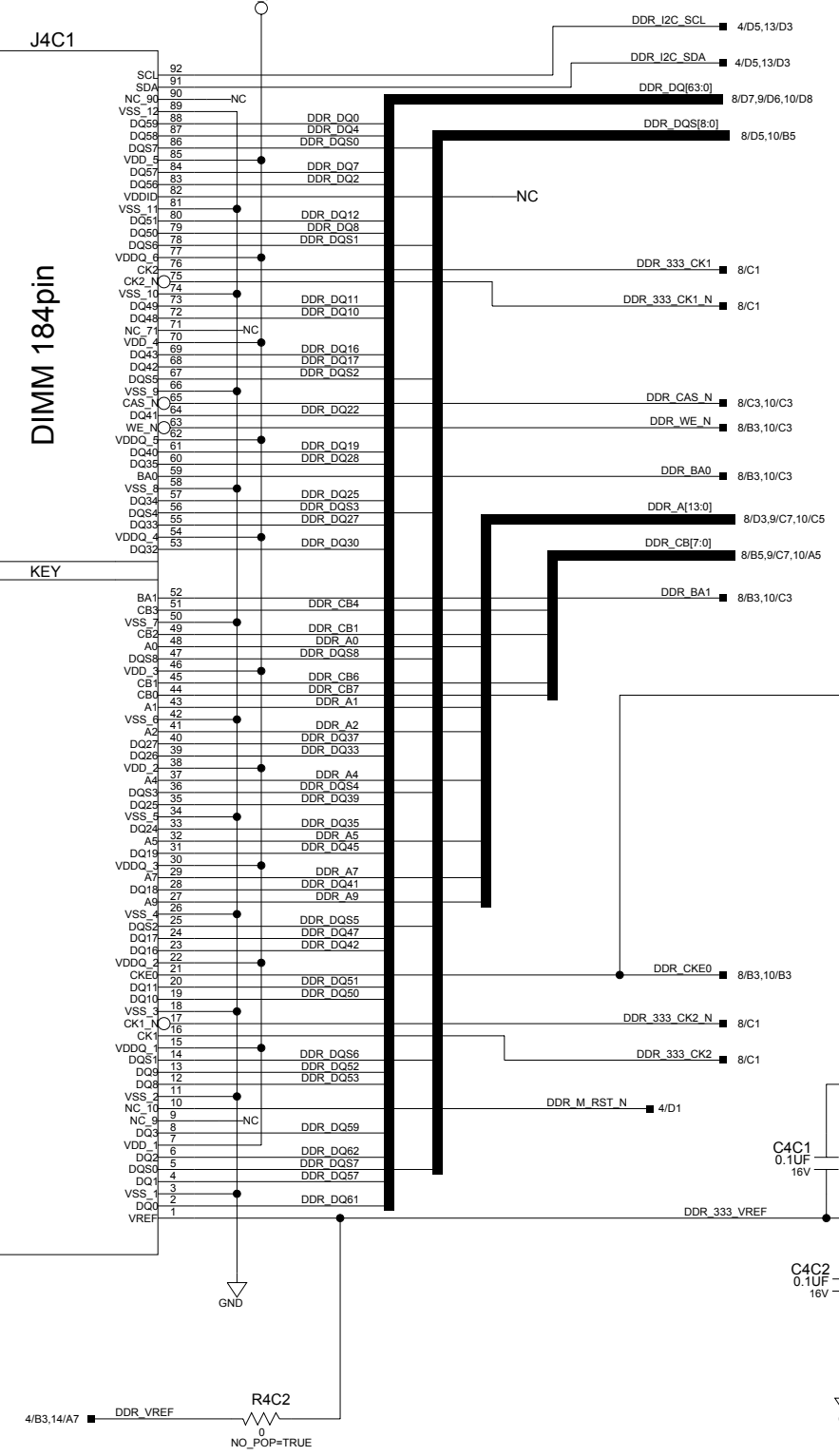
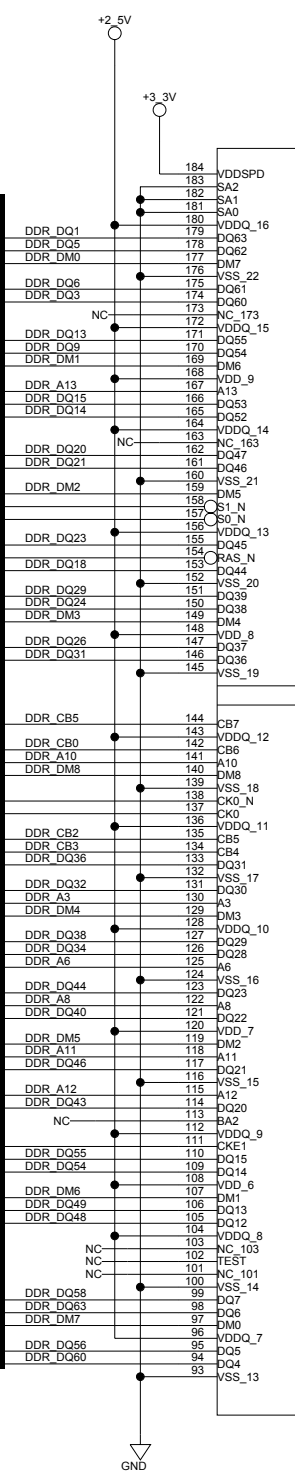
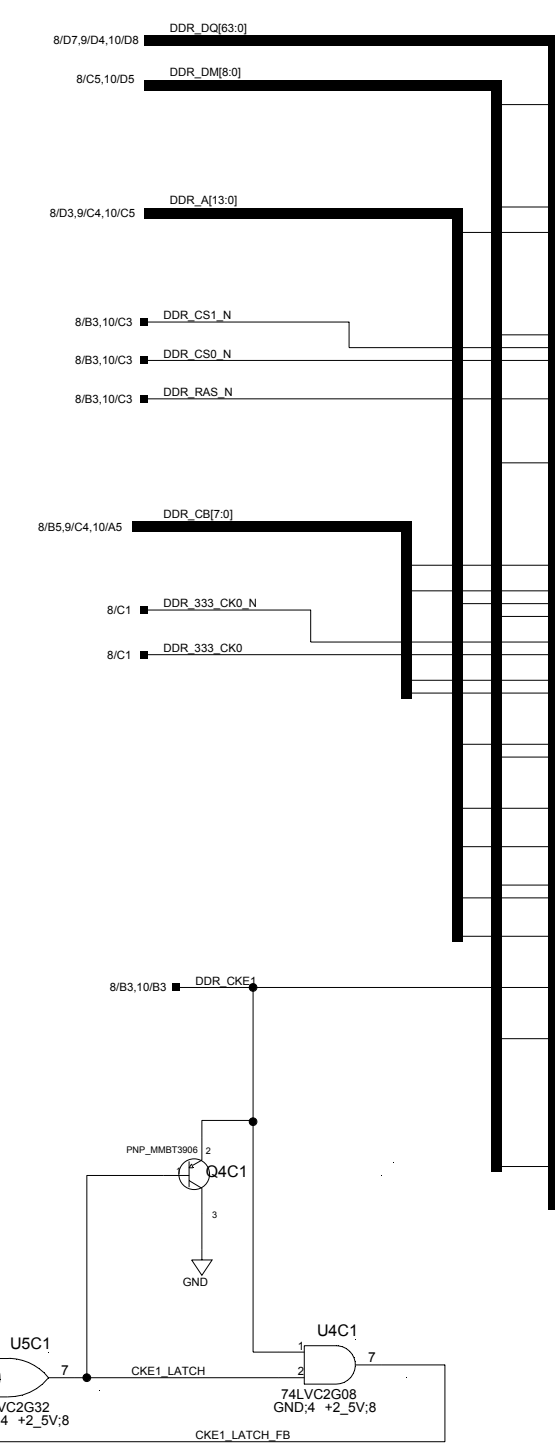
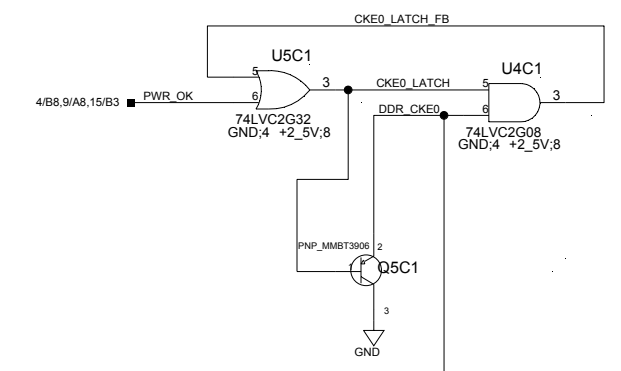
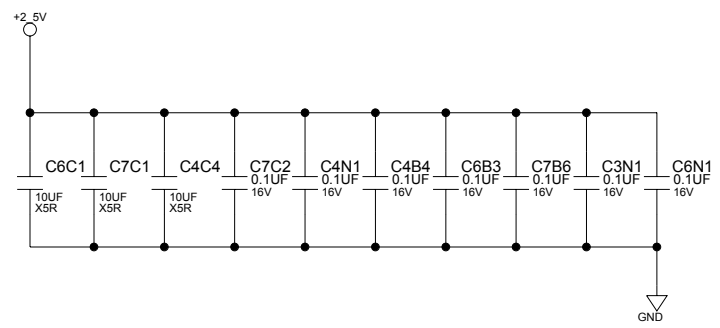


Place DDR Addr/CMD Series Resistors 0.25 to 0.5 inches of DIMM connector



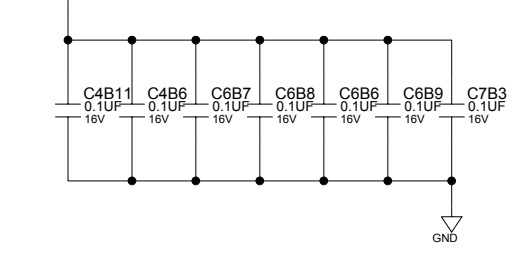
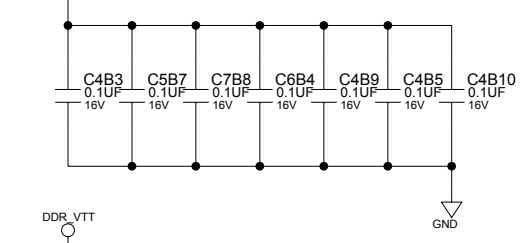
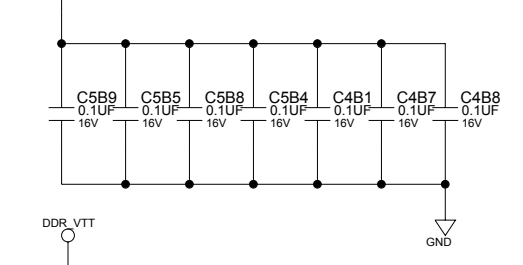
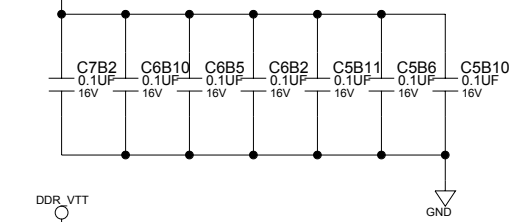
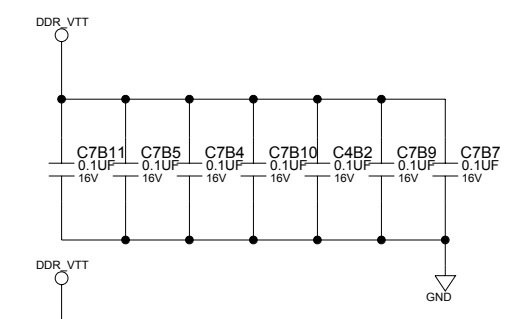
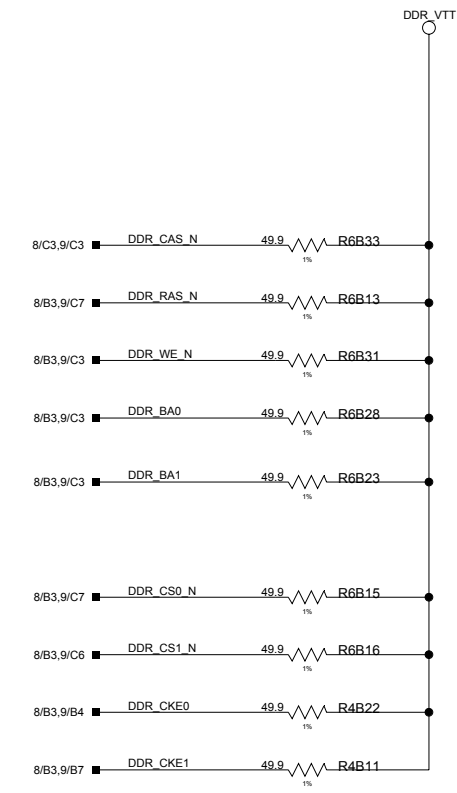
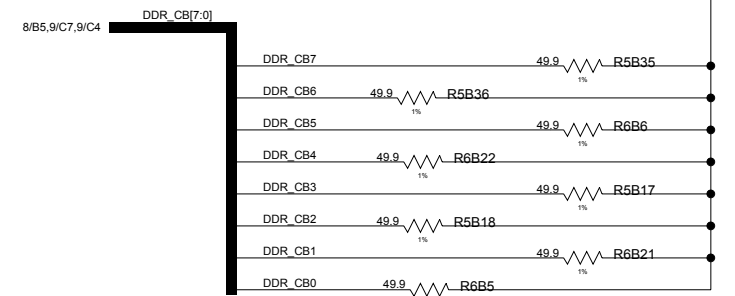
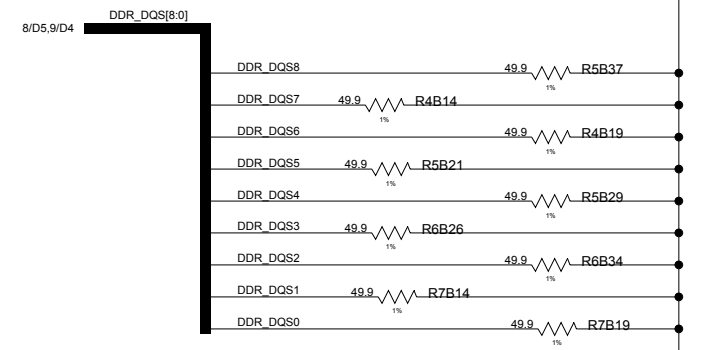
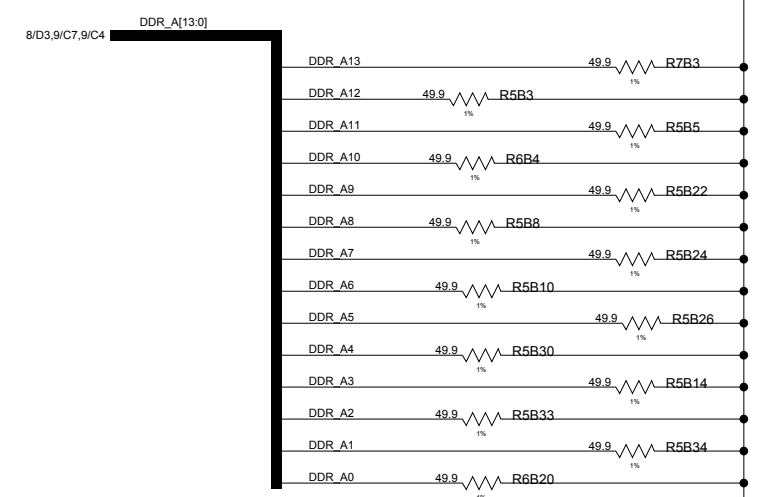
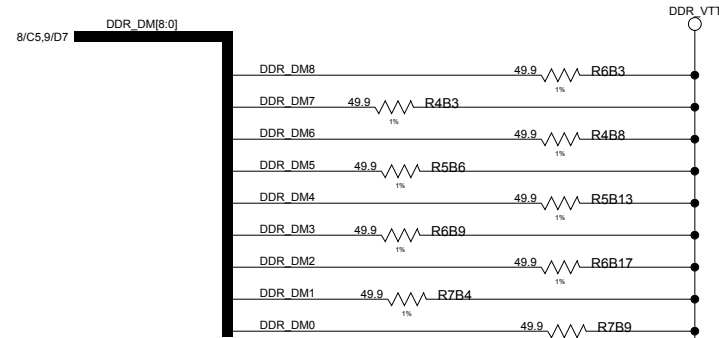
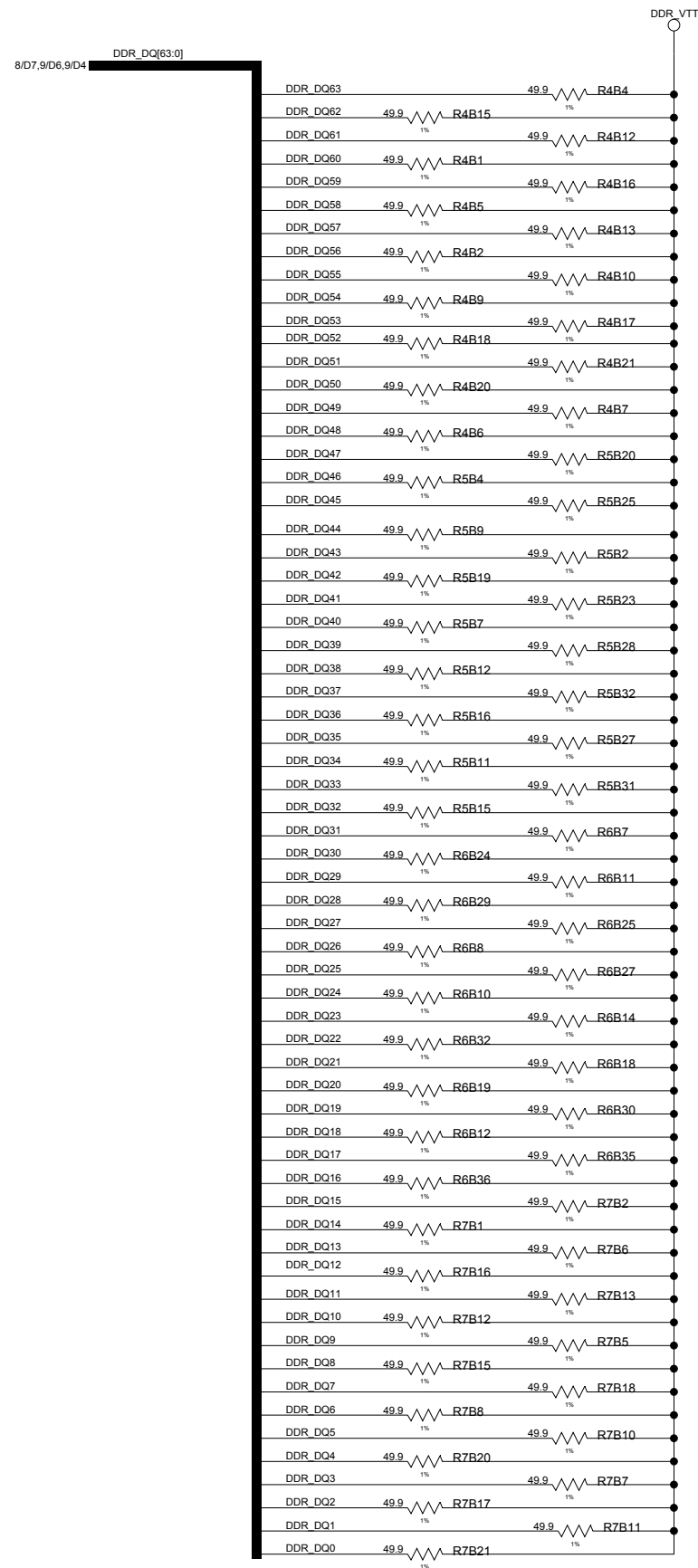
Place DDR Clock Series Resistors within 0.5 inches of 80331

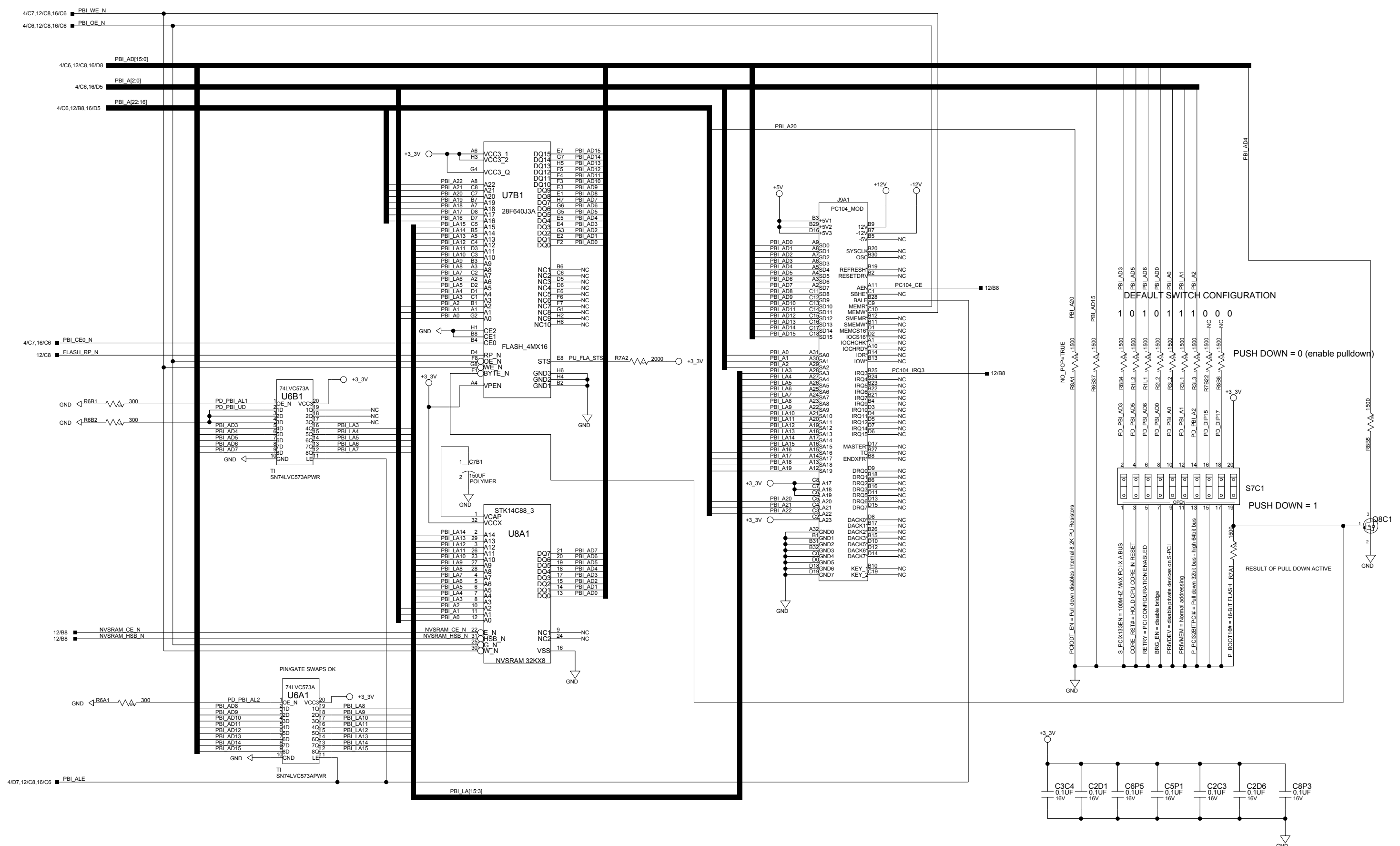


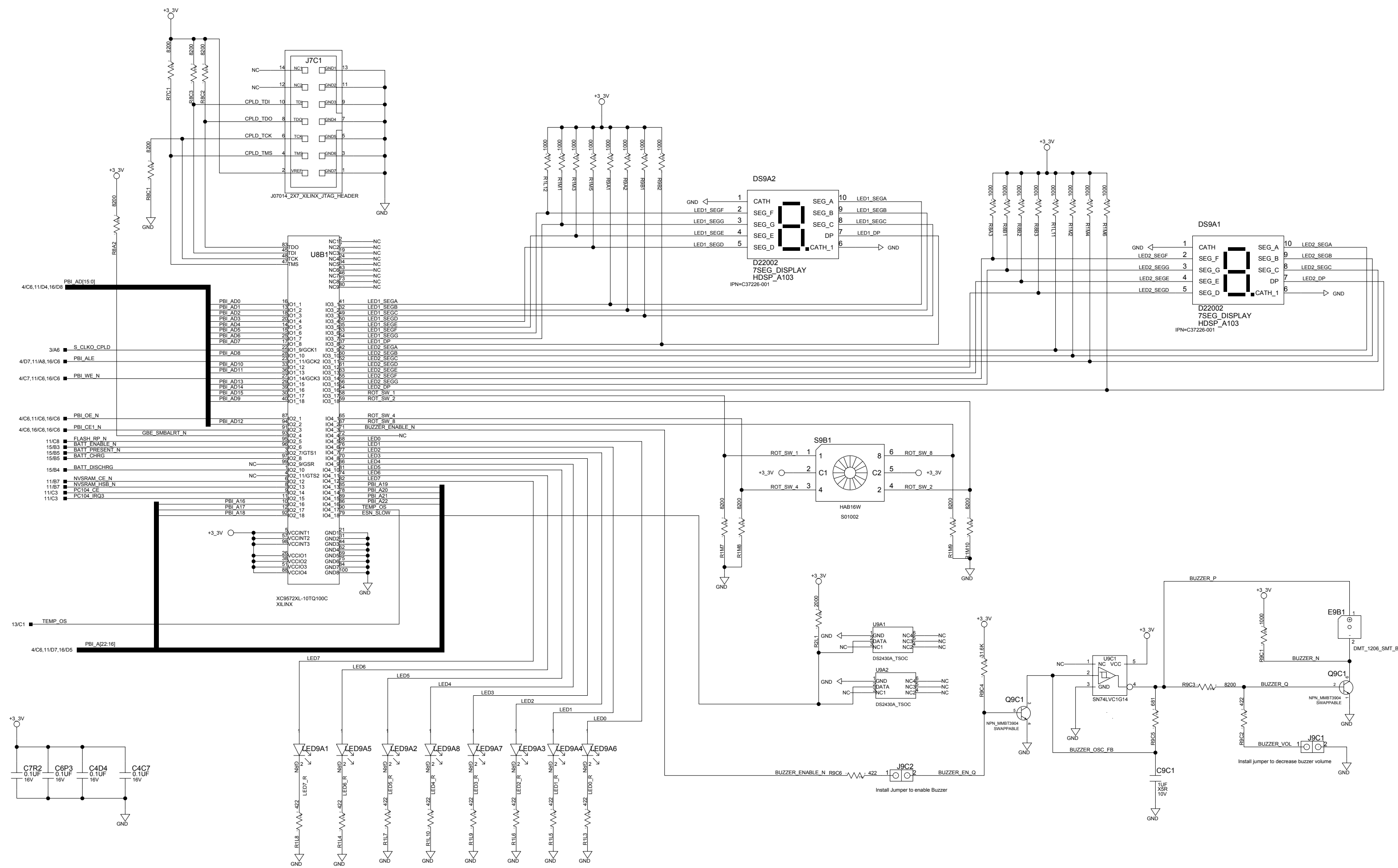


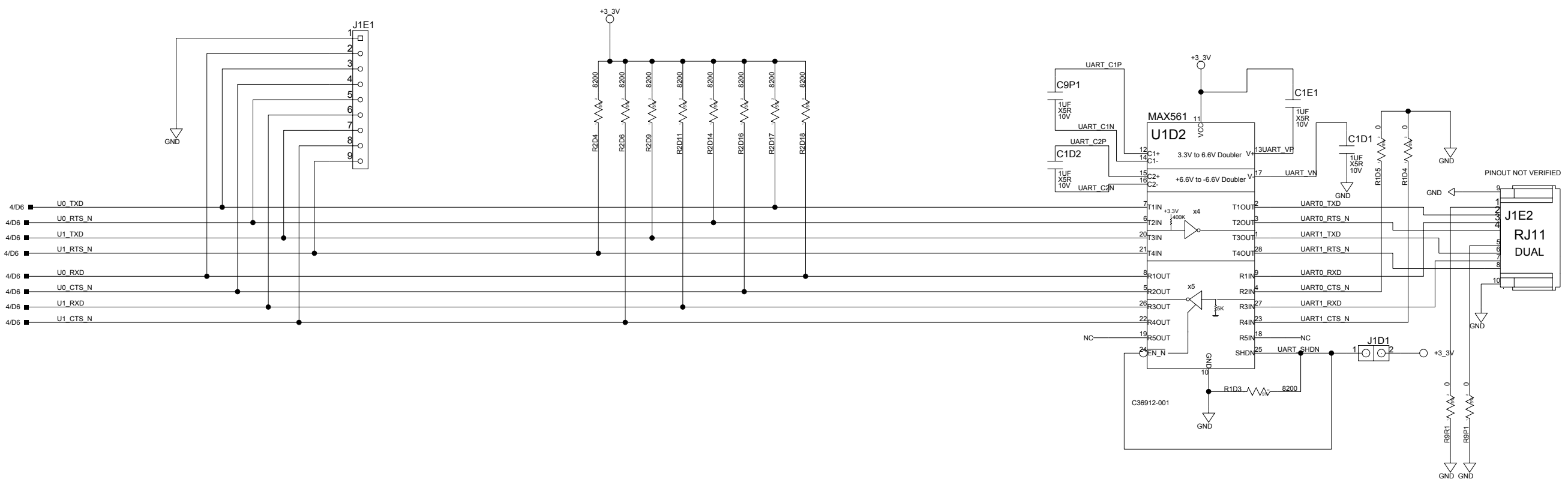
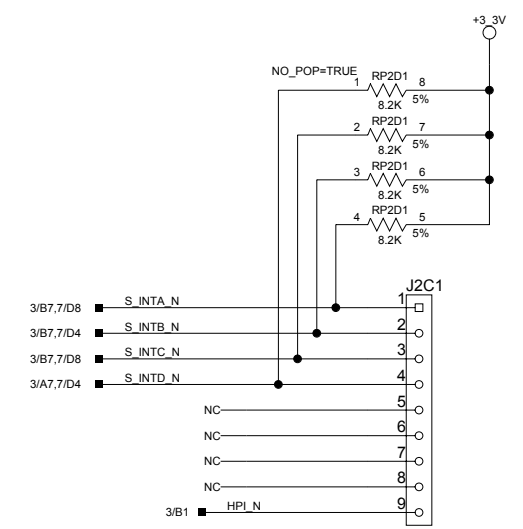
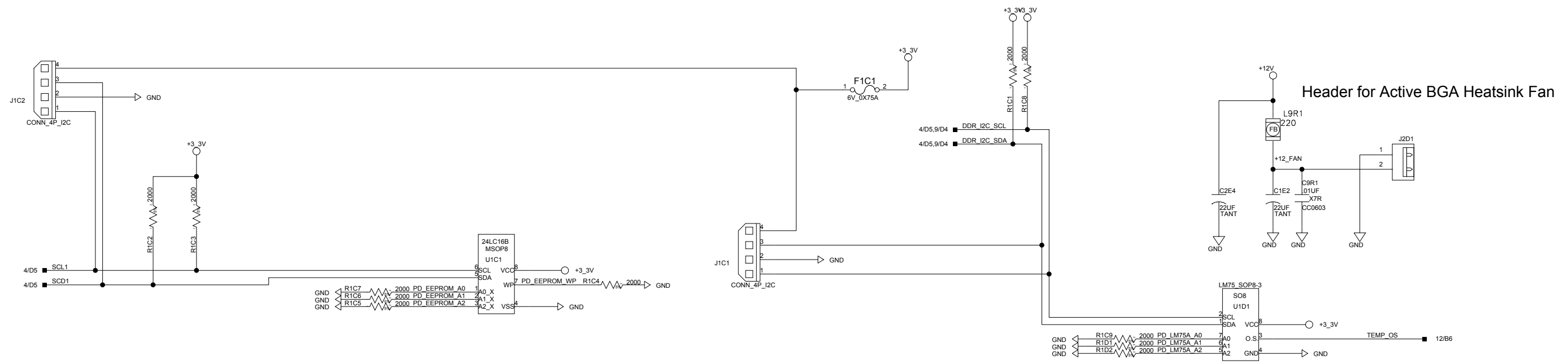
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DDR333 DIMM CONNECTOR

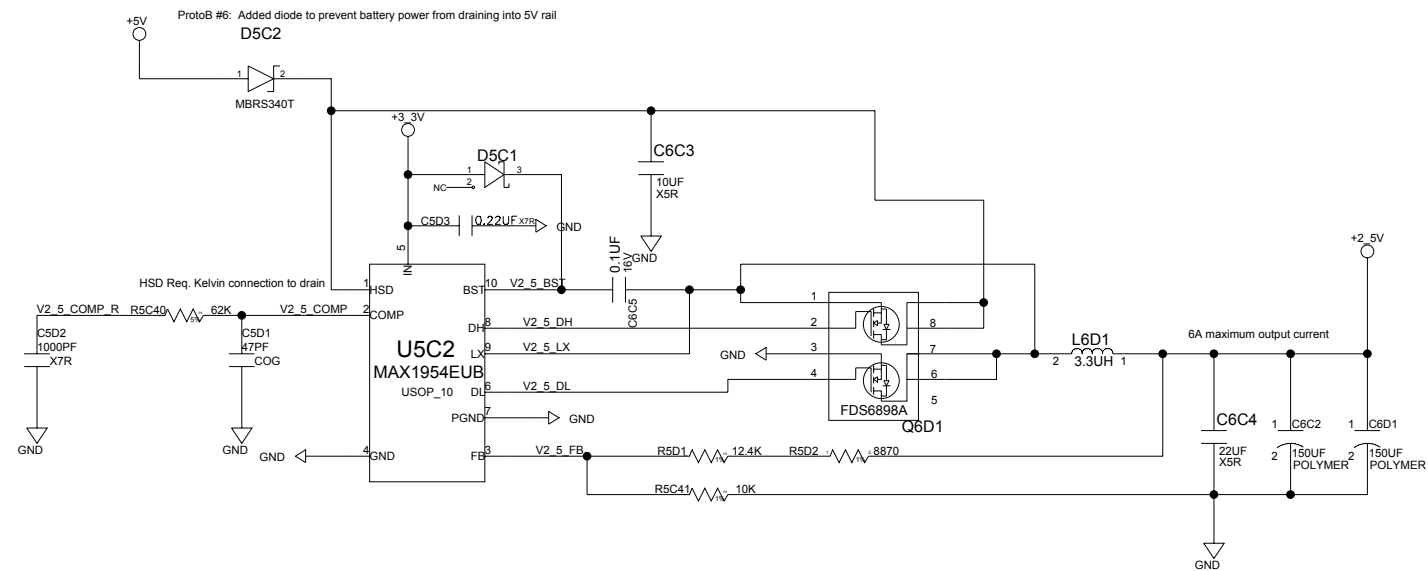




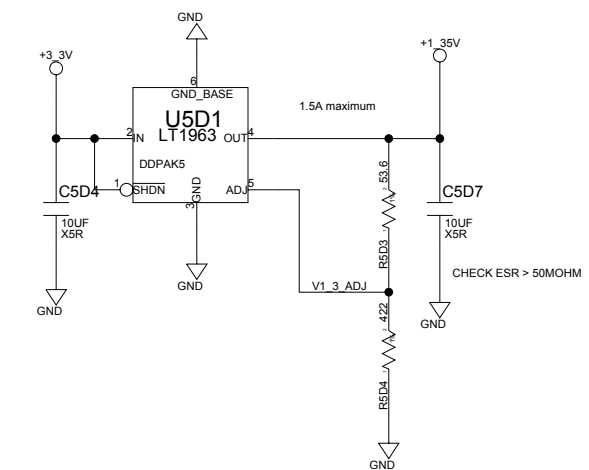




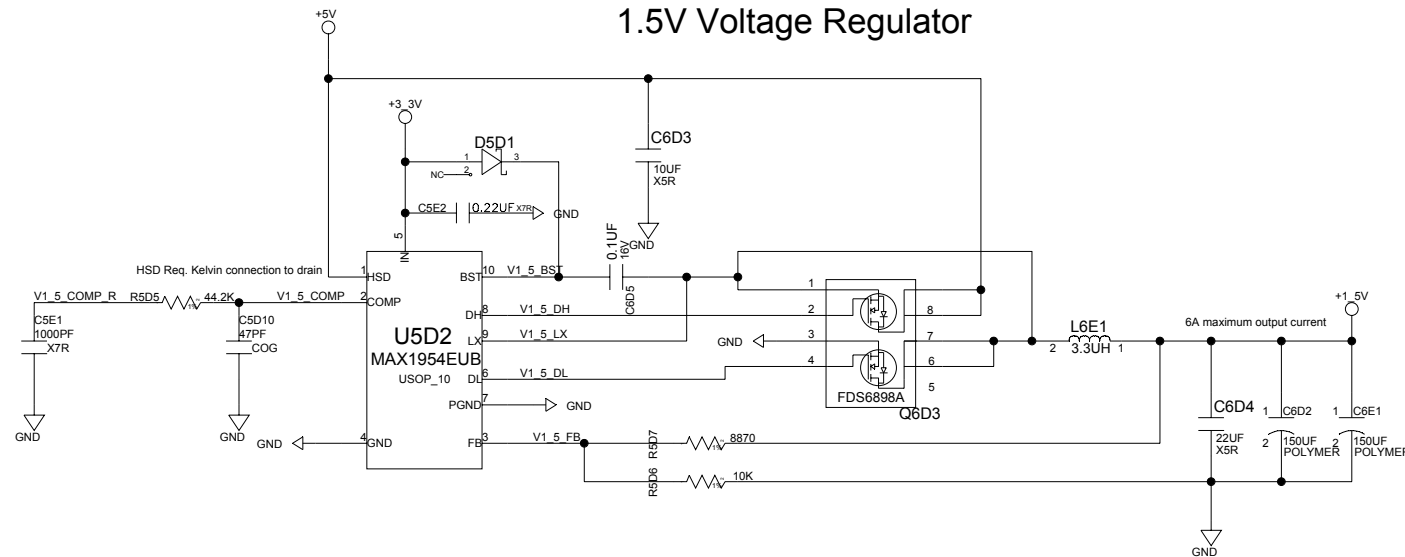
DDR Voltage Regulator



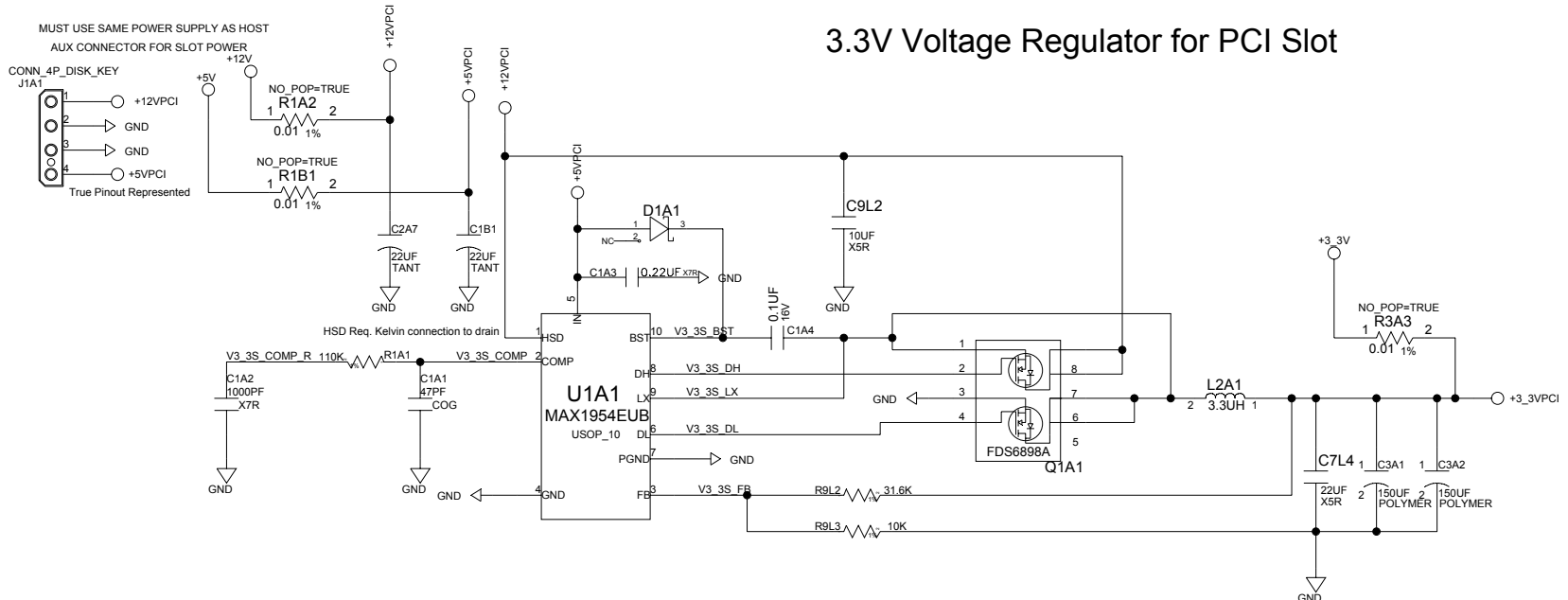
1.35V Voltage Regulator



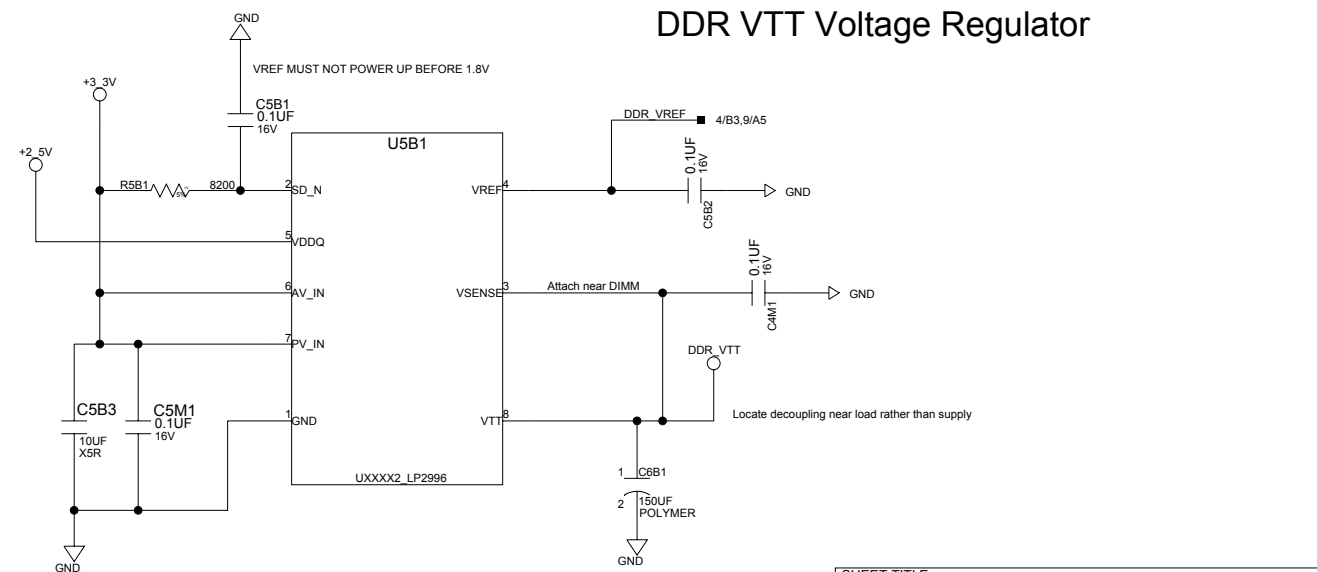
1.5V Voltage Regulator



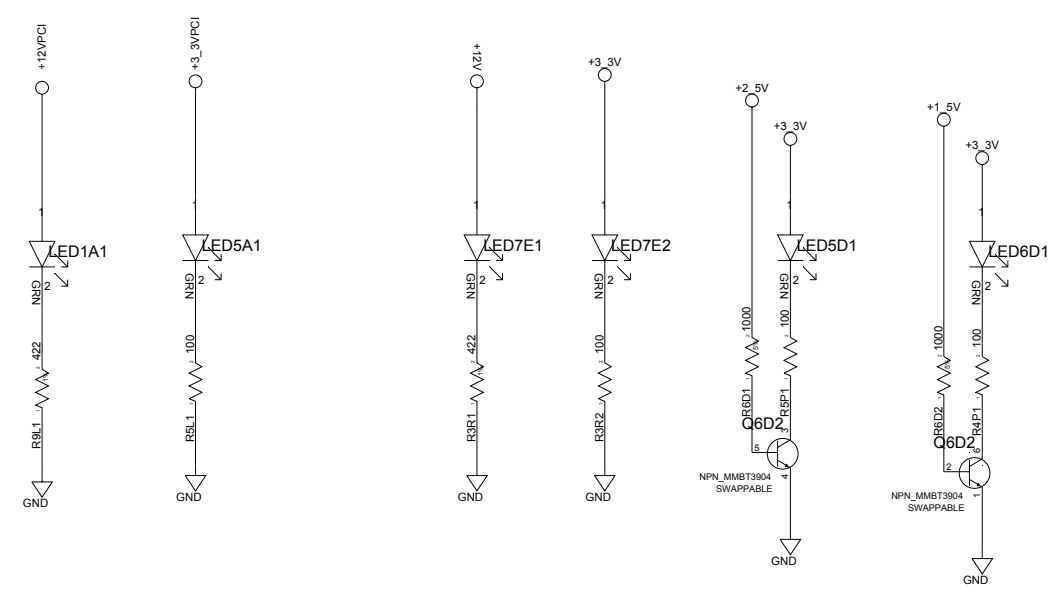
3.3V Voltage Regulator for PCI Slot

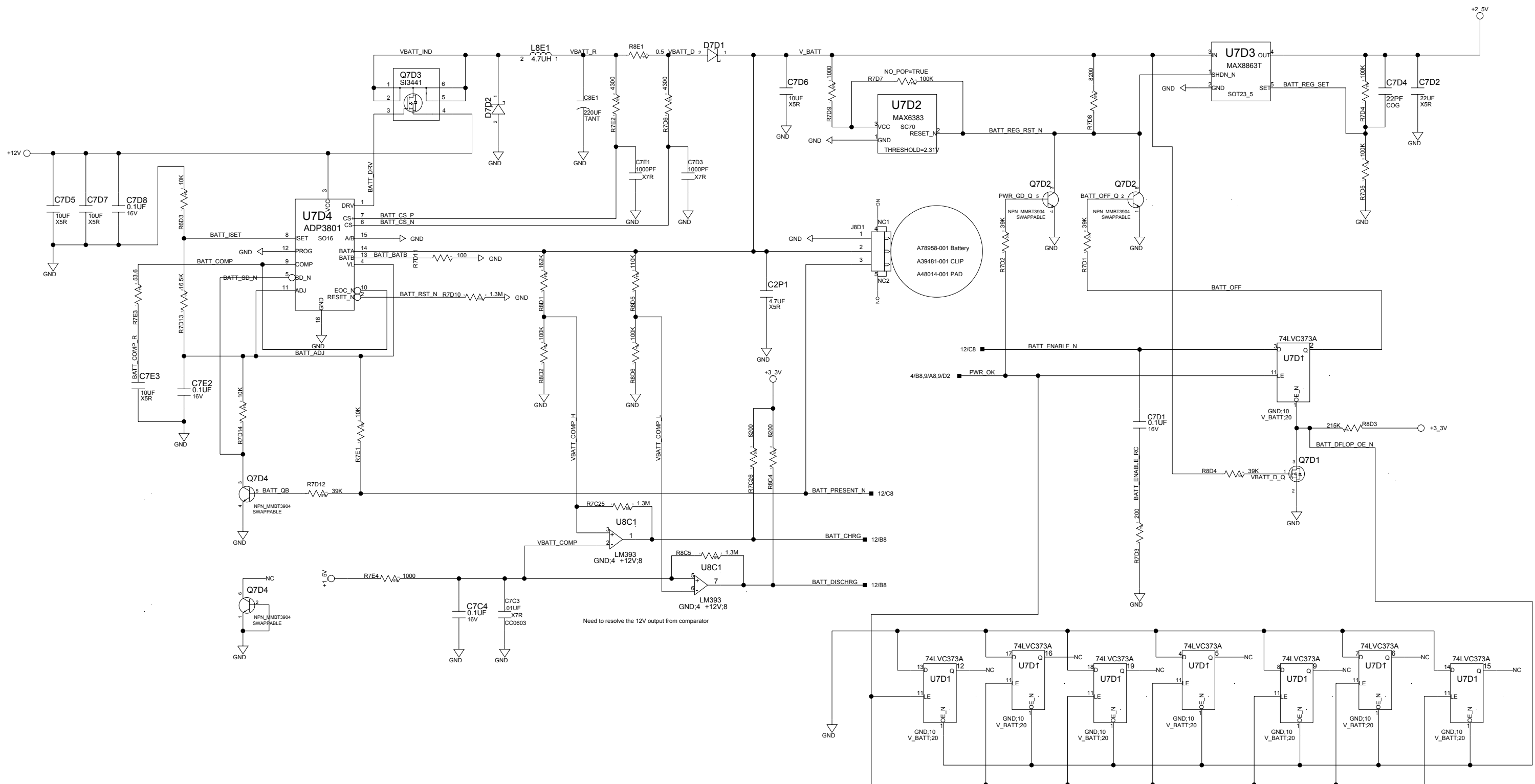


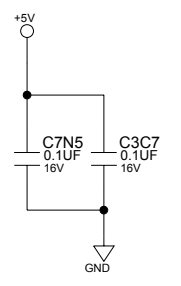
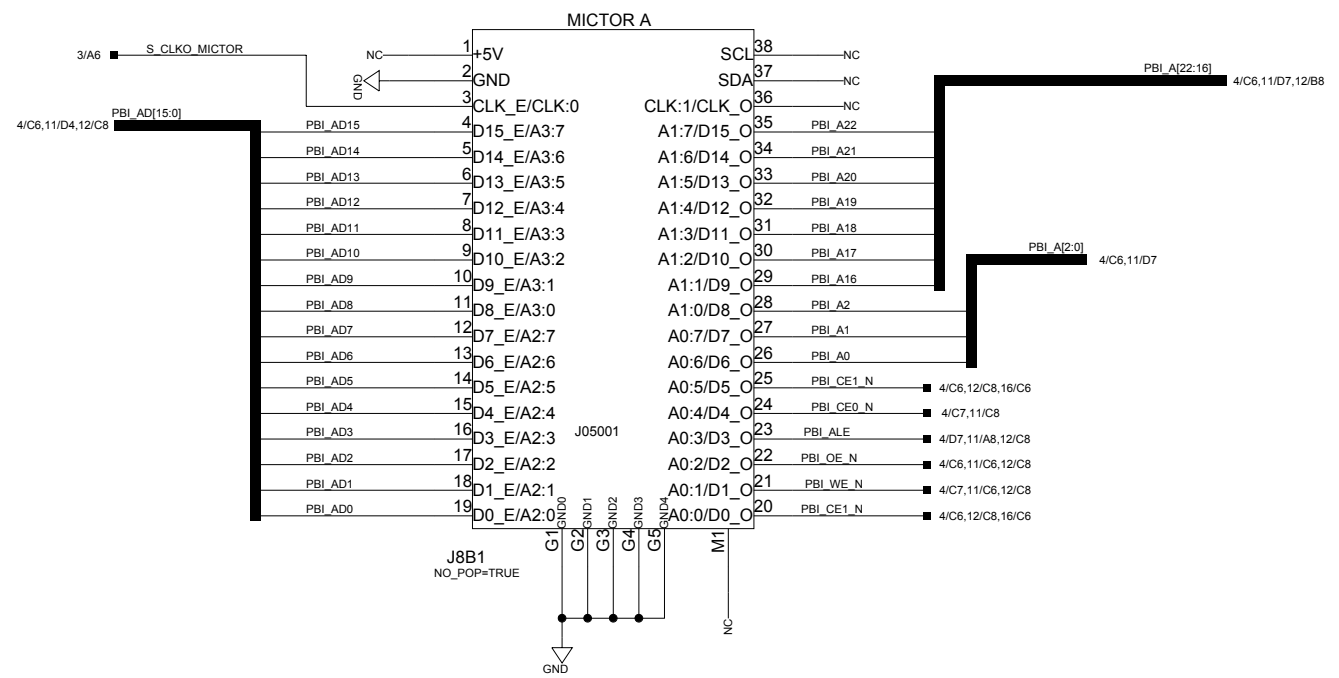
DDR VTT Voltage Regulator



LED Indicators







Mictor Connector Pin out Agilent's vs. Tektronix

Tek	Agilent		Agilent	Tek
1 GND (1)	1 +5VDC (3)	• •	2 SCL (2)	38 GND (1)
2 GND (1)	3 GND (3)	• •	4 SDA (2)	37 GND (1)
3 CLK	5 CLK _e	• •	6 CLK _o	36 CLK
4 X3:7	7 D15 _e	• •	8 D15 _o	35 X1:7
5 X3:6	9 D14 _e	• •	10 D14 _o	34 X1:6
6 X3:5	11 D13 _e	• •	12 D13 _o	33 X1:5
7 X3:4	13 D12 _e	• •	14 D12 _o	32 X1:4
8 X3:3	15 D11 _e	• •	16 D11 _o	31 X1:3
9 X3:2	17 D10 _e	• •	18 D10 _o	30 X1:2
10 X3:1	19 D9 _e	• •	20 D9 _o	29 X1:1
11 X3:0	21 D8 _e	• •	22 D8 _o	28 X1:0
12 X2:7	23 D7 _e	• •	24 D7 _o	27 X0:7
13 X2:6	25 D6 _e	• •	26 D6 _o	26 X0:6
14 X2:5	27 D5 _e	• •	28 D5 _o	25 X0:5
15 X2:4	29 D4 _e	• •	30 D4 _o	24 X0:4
16 X2:3	31 D3 _e	• •	32 D3 _o	23 X0:3
17 X2:2	33 D2 _e	• •	34 D2 _o	22 X0:2
18 X2:1	35 D1 _e	• •	36 D1 _o	21 X0:1
19 X2:0	37 D0 _e	• •	38 D0 _o	20 X0:0

- (1) Tektronix doesn't use pins 1,2,37,38 but recommends that they are grounded.
- (2) Pins 2 & 4 are not to be used they are outputs from the logic analyzer used to program emulation or analysis probes.
- (3) Pins 1 & 3 are not to be used they should be left as no connects. They are power pins for analysis/emulation probes.

Revision History

Rev 2.0 - ProtoB 12/5/2003