ECC Handling Issues on Intel XScale® I/O Processors

Technical Note

December 2003

Order Number: 300311-001

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Revision History

Date	Revision	Description
December 2003	001	This is the first release of this document.

1.0 ECC Handling Issues on Intel XScale® I/O Processors

1.1 Overview

This document presents ECC-Protected memory information specific to the Intel XScale® I/O Processors and focuses on:

- Interactions of 80200 Bus Control Unit (BCU) and Memory Control Unit (MCU) as it relates to ECC on Intel XScale® I/O Processors, including:
  - recommended setup
  - ECC transaction management and reporting
  - transaction timing/completion considerations
  - ECC, performance impact and error handling.
- 80310-specific issues regarding Intel XScale® core memory writes to ECC enabled memory regions.

Note: The 80303 is an i960-based IOP processor, so it operates slightly differently than the Intel XScale® core.

1.2 ECC Functionality in the IOP

The I/O Processor is a single functional device that integrates the Intel XScale® core with an MCU and intelligent peripherals. Table 1 shows the mapping of transaction initiator and memory transaction type:

Table 1. Mapping of Transaction Initiator and Memory Transaction Type

Memory Transaction Initiator	Memory Transaction Type	Hardware Handling ECC Calculation and Checking
Intel XScale® core	Memory read or write	Core BCU and MCU
Intelligent peripherals including PCI, DMA, AAU, etc.	Memory read or write	MCU

Discrete ECC values are calculated and stored in memory by the MCU on each 64-bit bus width memory *write*. ECC stored values are recomputed and compared with stored ECC values for accuracy by the MCU and/or BCU (80310 only) on each bus 64-bit bus *read*. Note that all sub bus width (64-bit) writes would generate an atomic read-modify-write (RMW), because the MCU is required to use the unaltered 64 bits to recalculate and store the ECC check value. Sub bus width (64-bit) writes to ECC protected memory cause RMWs, regardless of the transaction origin (Intel XScale® core, PCI, or DMA).

Note: An ECC *error* occurs when the MCU or Core BCU (80310 *only*) performs a read and determines that the stored ECC check total does not match the recalculation.

With the 80310 chipset, if the Disable Write ECC (DWE) bit is not set in the 80200 processor, a sub bus width write will generate two RMW transactions. The first is generated by the BCU and the second is generated by the MCU. Turning on the Intel XScale® core DWE eliminates the duplicate RMWs.

Note: The DWE is available on the 80200 C0 and D0 steppings.

1.3 Registers that Manage ECC

Registers are used for the management of ECC transactions. These registers are located in the MCU and 80200 BCU and perform the following functions:

- Control Register (CTL) to enable/disable: ECC generation and checking, single-bit correction, and single-bit error reporting
- ECC Log Registers: logging error types
- ECC Address Registers: logging addresses where error occurred
- 80200 ECC Disable Bit: available on C0 and D0 steppings of the 80200 processor.
- ECC Test Registers: used by software to generate data writes with incorrect ECC values written to memory for validation purposes. Subsequent memory reads of that memory generate an ECC error.

1.4 Cache Memory and ECC Error Reporting

Table 2 presents a cacheline size and relationship to Dcache Valid bit, Dcache Dirty bit, 64-bit data bus, and write buffers. A cacheline is 32 bytes in size and 32 byte-aligned. Each cacheline flush transaction is an even multiple of the 64-bit data bus, and creates only full 64-bit transactions. Therefore, cacheline flushes do *not* generate ECC errors, because no read results from an RMW; therefore, an ECC error cannot be identified.

Table 2. Data Cache line Mapping to 64-bit Data Bus and Write Buffers

Byte 29-32	Byte 25-28	Byte 21-24	Byte 17-20	Byte 13-16	Byte 9-12	Byte 5-8	Byte 1-4
One cache line/Block = 32 bytes way of set (32-Kbyte, 32-way set associative cache)							
DCache Valid Bit							
DCache Dirty Bit				DCache Dirty Bit			
Data Bus 8 bytes		Data Bus		Data Bus		Data Bus	
Write Buffer 16 bytes				Write Buffer			
Write Buffer				Write Buffer			
Write Buffer				Write Buffer			
Write Buffer				Write Buffer			

1.5 Timing Considerations on Memory Transactions

There are timing considerations whenever a memory transaction must complete before the next event. To accomplish this:

- Use a cache policy that generates a fence (see Intel XScale® I/O Processor manual)
- Perform drain write buffer followed by coprocessor wait.

Note: Drain write buffer executes as follows: before the next instruction is executed, write and fill buffers are drained and all Intel® 80200 processor data requests to external memory (including the write operations in the bus controller) have completed.

1.6 ECC Performance Impact with ECC Setup Recommendations

Calculation of ECC values does not affect performance *unless*:

- RMW is generated.
- 80310 processors *only*: for a single sub bus width memory write, the Intel XScale® core and MCU *both* generate RMWs to recalculate the ECC check value to memory if the DWE bit is not set for C0 and D0 steppings of the 80200 processor.
- An ECC error is identified during a read, and an interrupt is invoked to initiate software error handling.

There is no performance impact for the automatic correction of a single-bit error with no single-bit error reporting (a write is not generated to correct the error). Also, ECC should *not* be turned off during error processing in the interrupt handler because, for example, any incomplete DMA or inbound PCI transactions would *not* be ECC protected.

1.6.1 Recommended Setup for Performance when ECC is Required

Following is the recommended ECC setup for 80200 BCU and MCU:

80200 BCU Setup

- Enable ECC reporting, so that ECC checking for Intel XScale® core Reads is also enabled.
- 80310 processors *only*: set bit 31 in ECTST (register 8, CP13) of the *80200 processor* to Disable Write ECC (DWE); available for C0 and D0 steppings *only.* This eliminates duplicate RMWs for a single sub bus width memory write.

MCU Setup

- Enable ECC reporting
- Disable single-bit reporting, enable single-bit auto-correction, and enable multiple-bit reporting.