CK00 Clock Synthesizer/Driver

Design Guidelines

November 13, 2000

Order Number 249206-001

1. Introduction

This document provides technical specifications for development of the CK00 class of clock components, based on requirements of the Intel® Pentium® 4 processor and other Intel Architecture (IA) platforms. The CK00 is intended to be applicable to a wide variety of system implementations. The CK00 class of clocks contains new features, most notably the adoption of a new differential clock output type.

1.1 Clock Synthesizer Overview

The clock synthesizers defined here will source multiple clock types: e.g. differential Host clock, 66MHz clock, PCI clock, and others as defined by IA system requirements. These definitions deal with the Host clocks, Memory reference (Mref) clocks, 3V 66MHz clocks, 33MHz PCI clocks, 48MHz clocks, and 14.318MHz clocks.

The 3.3V input signaling specification follows the JEDEC standard for LVTTL signaling. The 3.3V power delivery specification follows the JEDEC standard range 3.3V ±5%.

This document shows examples of implementations including pin-outs. Implementations shown here include a solution contained in one package and a similar solution split into two packages. This is shown in Figure 1. Specific platforms may require implementations similar or identical to each example.

The differential host clocks have many configuration options summarized in the appendices of this document. In all cases, unless otherwise communicated, the differential clock design should be optimized for the Voh=0.7V configurations shown in the appendix.

1.2 Applicable Documents

The latest revisions of the following are used as reference documents:

JEDEC Reference

JEDEC Standard No. 8-1A, Interface Standard for 3.3±0.3 V Power Supply & Digital Integrated Circuits. Voltage and Interface Standard for Non-terminated Digital Integrated Circuit.

PCI Reference
The PCI Special Interest Group is an industry-wide group that controls the official PCI specification. You can obtain the latest copies of the PCI specification by contacting the PCI Special Interest Group at the following numbers:

(800) 433-5177 - USA
(503) 693 8344 - Fax
(503) 693 6232 - International

IBIS Reference

The IBIS Open Forum is an industry-wide forum that controls the official IBIS specification. Minutes of IBIS meetings, email correspondence, proposals for specification changes, etc. are online at "vhdl.org". To join in the email discussions , send a message to "ibis-request@vhdl.org" and request that your name be added to the IBIS mail reflector. Be sure to include your email address.

The IBIS home page can be found at http://www.eia.org/eig/ibis/ibis.htm

Audio Codec 98 Reference

The AC97 home page can be found at http://www.intel.com/pc-supp/platform/aud98

AGP Reference

AGP information can be found at http://developer.intel.com/solutions/tech/agp.htm

Intel Clock Reference

Intel CK98 definition is available at
http://developer.intel.com/design/pentiumiii/designgd/245338.htm

Rambus* Information

Information on Rambus memory technology and associated clocking architectures can be found at http://www.rambus.com

1.3 Drive Specification

The differential host clock driver output buffers are current-mode outputs and are specified by the ability to provide a determined current over a specified accuracy over a specified range of loads. The buffers are also specified as to the output di/dt which is critical in determining system rise and fall (Trise/Tfall) times.

The single-ended clock driver output buffers are specified in terms of the AC switching characteristics and their DC drive characteristics. The primary electrical parameters are the voltage to current relationship (V/I), and rise and fall time (Trise/Tfall) of the driver through its active switching range.

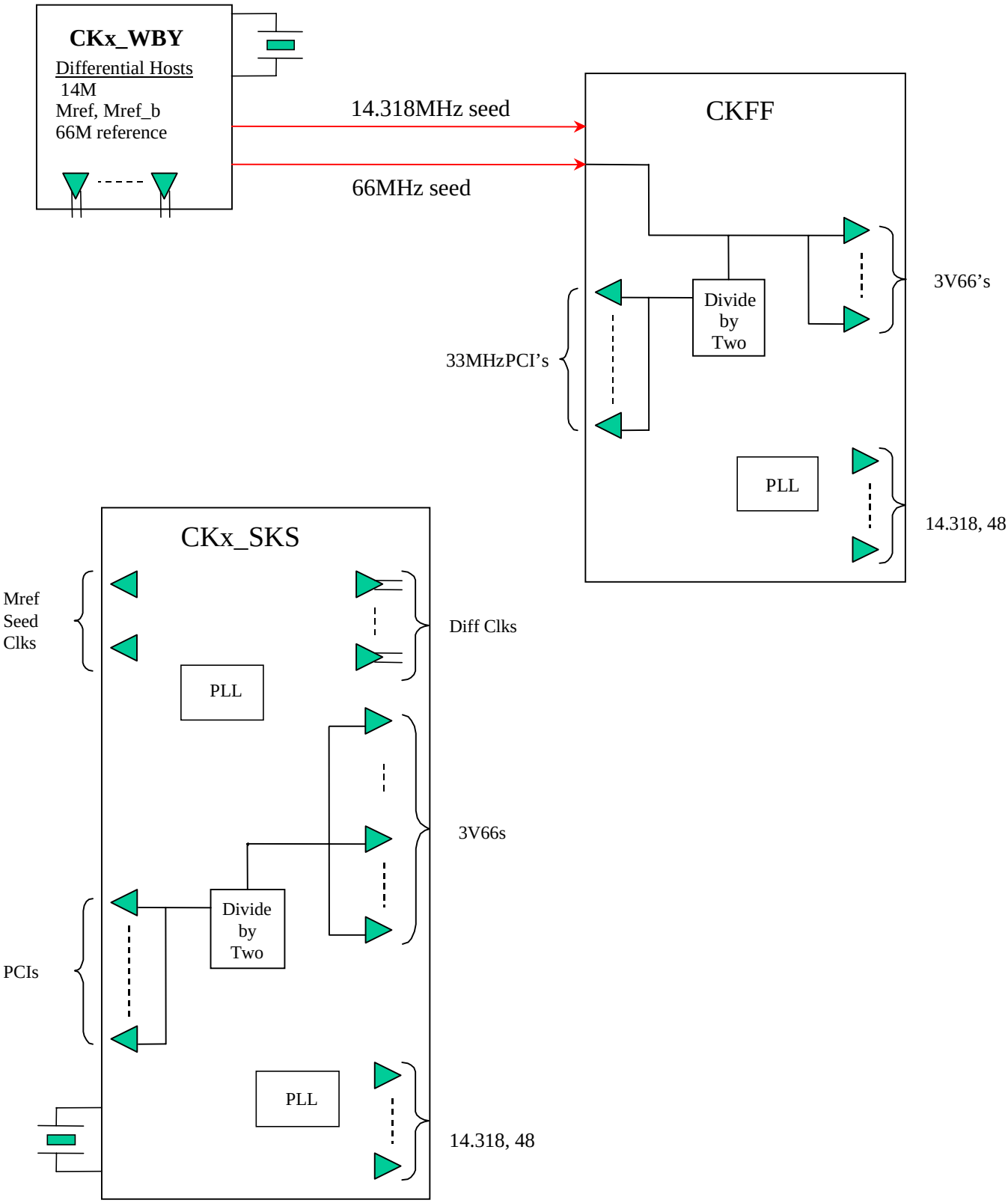


Figure 1.1 – One and Two Chip Solutions

2. Example Circuits

The differential Host clock signals are to be established by a current mode current steering buffer conceptually similar to that shown in Figure 2.1. I_{Out} is established by a mirrored and scaled copy of a reference current, I_{Ref}. The method of establishing I_{Ref} is explained in Section 2.1 in the manner believed to be the best known method.

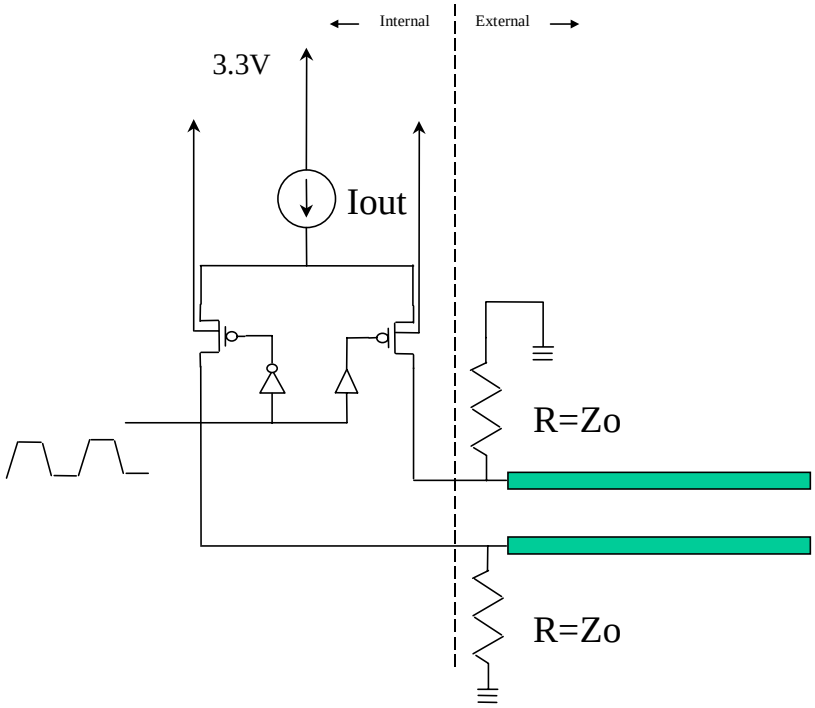


Figure 2.1 – Conceptual Output Circuit

2.1 Current Reference and Mirror Circuit

The details of the current reference circuit are shown in Figure 2.2 in the fashion believed to be the best known method using an external reference resistor. A simple current mirror connected directly to the external resistor, as shown in Figure 2.3, is not recommended due to the difficulty of establishing an accurate reference current. This inaccuracy in the reference current is due to the uncertainty of the diode-connected device voltage drop.

The operational amplifier in the current reference circuit drives the gate of M_{Iref} with feedback to establish V_{Ref}=1.1V at both inputs of the amplifier. Thus the reference current is established according to the following formula:

$$I_{Ref} = 1.1 / R_{Ref}$$

Where R_{Ref} is the external reference resistor and 1.1V was chosen for the reference voltage, according to the following reasoning:

1) The voltage is close to the voltage that will be present at the final output of the buffer when generating interesting values of Voh (ie. 0.71V). Thus, the reference voltage was chosen close to this value to provide an environment better for current mirror matching.
2) 1.1V is derivable with a clean integer ratio suitable for an accurate internal voltage divider.
3) 1.1V dictates resistor values of R_{Ref} that are available as standard quantities for the currents of interest.

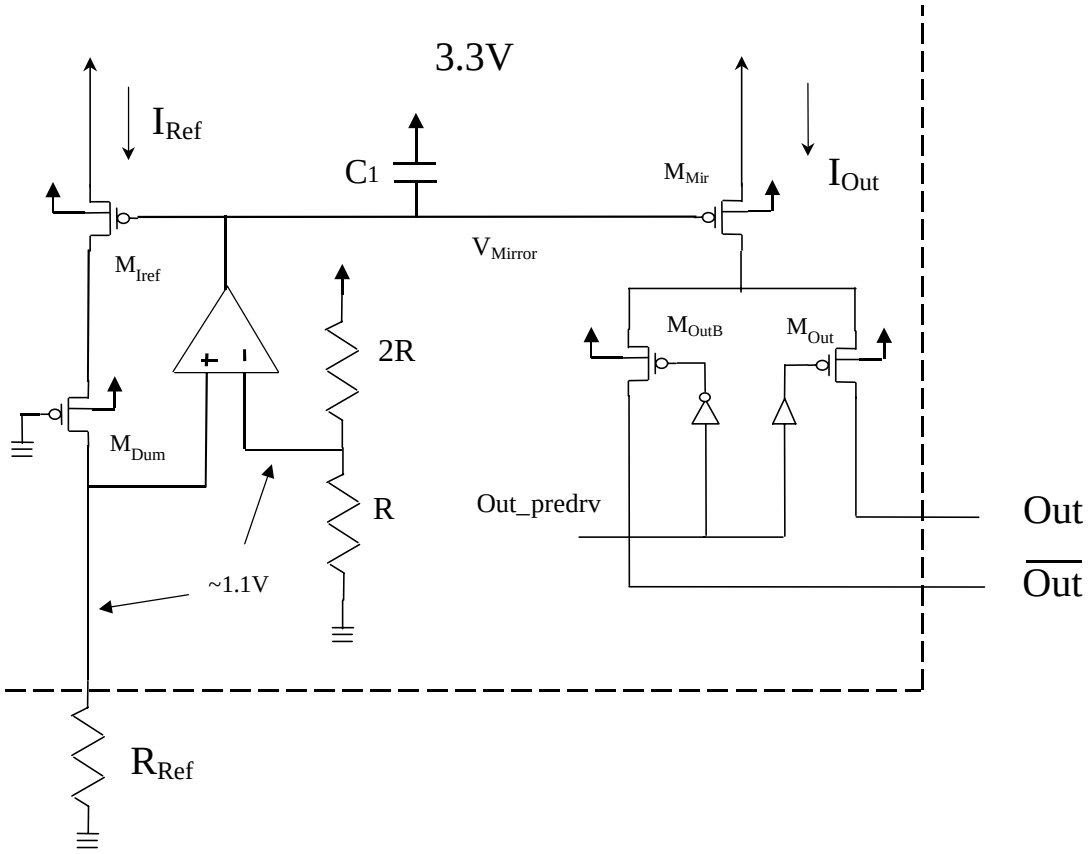


Figure 2.2 – Example Current Reference Circuit Shown with One Buffer Output

Obviously, parameters of the operational amplifier such as input offset voltage must be carefully understood by the circuit designer to ensure predicted current behavior. Furthermore, oscillation at the V_{Mirror} node could be extremely detrimental.

As shown elsewhere in this document, I_{Out} does not equal I_{Ref}. Programmable variations of the current scaling are from $I_{Out}=4*I_{Ref}$ to $I_{Out}=7*I_{Ref}$. Furthermore, chosen values of R_{Ref} are allowed to vary, which will allow for further control of the current output. Interesting values of R_{Ref} are from 200 to 500 Ohms. The principal configuration, however, will be R_{Ref} = 475 Ohms with the

scale factors set to either $I_{Out} = 5*I_{Ref}$ or $I_{Out} = 6*I_{Ref}$. As shown in Section 8.2, R_{Ref}=475 corresponds to an I_{Ref} of 2.32mA.

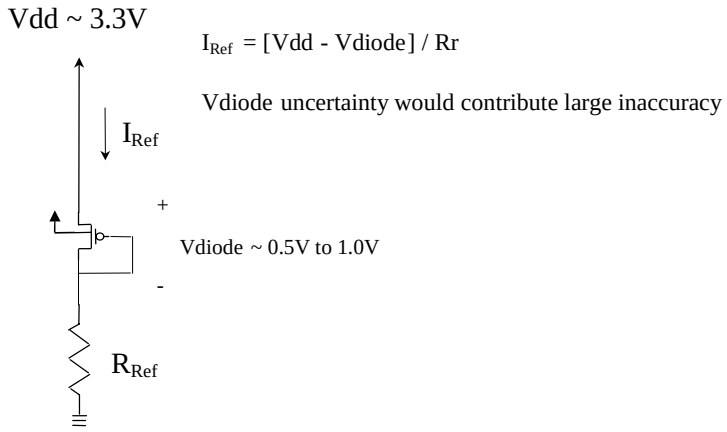


Figure 2.3 – Conventional Current Reference Circuit – *not used*

The transistor M_{Dum} was included in Figure 2.2 to imitate the drop across one of the switch transistors at the output (M_{Out} or M_{OutB} in Figure 2.2). Thus, the voltage environment seen by MI_{Ref} in Figure 2.2 is intended to be similar to M_{Mir}, which creates superior current matching potential.

The capacitor C_1 was included in Figure 2.2 to stabilize the critical current mirror node. Note that the capacitor C_1 was drawn to 3.3V rather than to ground. This was done to prevent introducing noise from ground, which would not be correlated to the noise present on the 3.3V supply of the current mirrors.

2.2 System Implementation

2.2.1 Source termination of differential HCSL type outputs

For systems implementing source termination, it has been discovered that there are significant benefits gained by adding series resistors in addition to the shunt source termination resistors. The series resistors along with the termination resistors are illustrated in Figure 2.4. The benefit is gained due to the extra isolation of the on-die and on-package capacitance from the line and forces reflected signals to terminate properly through the shunt termination resistors.

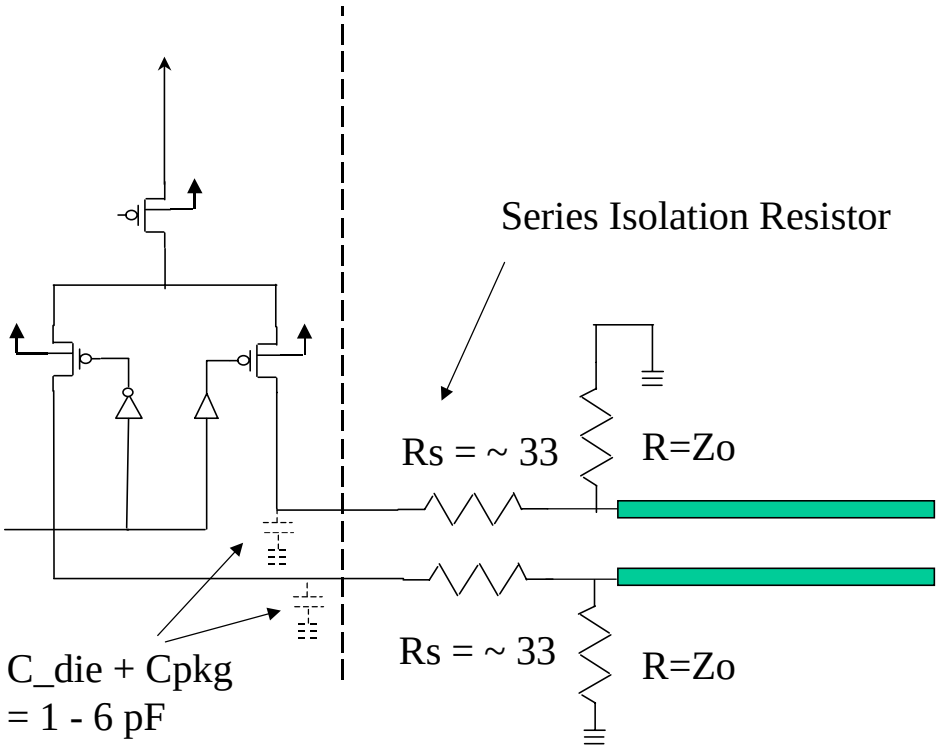


Figure 2.4 – Illustration of Series Isolation Resistance Rs

The series resistors R_S have the tradeoff of reducing the amount of voltage headroom available to the current driving circuit. For the principal Voh configuration of Voh=0.7V, the voltage at the output of the buffer will be in the range of 1.1V and be similar to the voltage at the reference resistor R_{Ref}. For configurations with Voh greater then 0.7V, it is assumed that R_S will be decreased such that the voltage present at the pin output will not exceed 1.2V neglecting overshoot. Such a decrease in R_S may result in reflections from the on-die capacitance which, depending on system implementation can cause additional reflection and ringback. The system designer should simulate this effect using realistic die and package capacitance models. The designer should also be aware that there is a trace length dependency on the effect of the reflections. To illustrate the effect of decreasing R_S below 33 Ohms in one example system, the plot shown in Figure 2.5 has been included. Figure 2.5 applies only to a specific source-terminated case with no load termination and cannot be used to make predictions of other systems. Furthermore, the plot applies only to a discrete length of clock trace. In the specific example, it is apparent that if R_S were reduced from 33 Ohms to 15 Ohms, this could cause an increase in overshoot of approximately 0.05V at the trace length simulated.

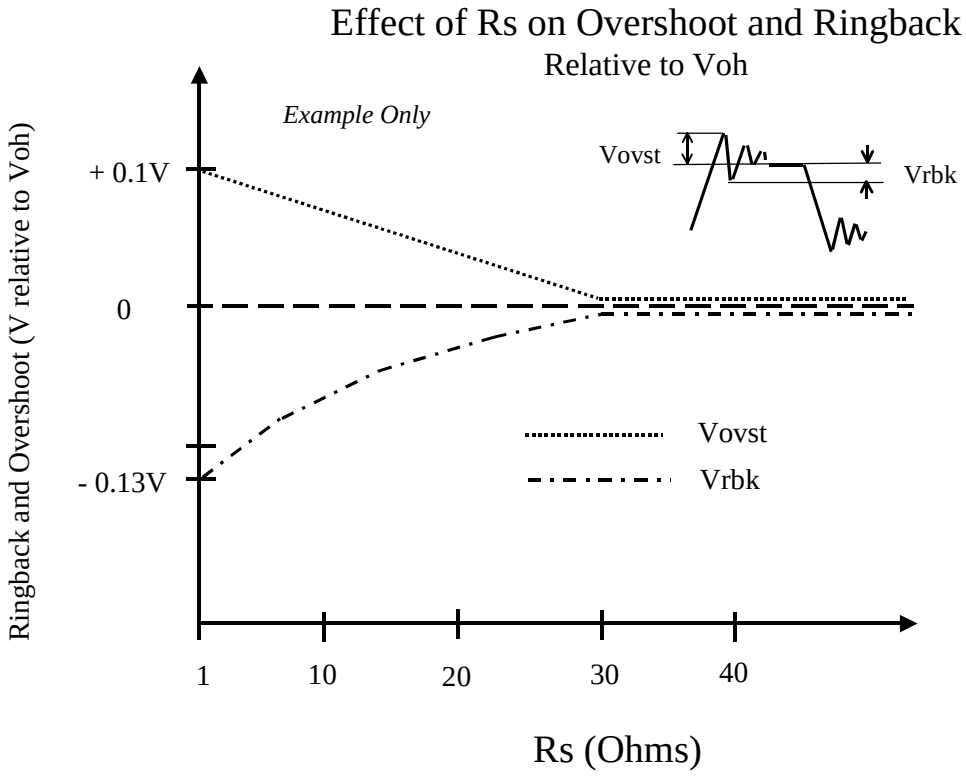


Figure 2.5 – Effect of Rs on Overshoot and Ringback for Example System

It should be noted that the voltages in Figure 2.5 could actually be much worse, depending on how the reflections are damped in the rest of the network.

It should also be noted also that for cases with matched termination at the load end of the clock trace, R_S is probably not needed since there will not be a large component of reflection terminated at the driver.

2.2.2 Pull-ups/Pull-down resistors for latched inputs

Some of the clock devices defined in this document incorporate latched or multi-function inputs. Latched inputs are both inputs and outputs of the device. Upon power-up a voltage high or voltage low is sensed at the pin of the device, after which the information is latched into the device and the pin becomes a clock output. The initial input voltage at the pin of the device will be established by a pull-up or pull-down resistor. The latched inputs should function correctly with pull-up or pull-down resistors valued between 15kOhms and 500Ohms.

3. Electrical Requirements

This section details the electrical parameters for the differential host clock buffers, multiple types of 3.3V clock output buffers, and a 5.0V-compatible 3.3V PCI clock driver output buffer. The different types of 3.3V drivers are needed to compensate for different board layout topologies.

Due to voltage and timing constraints, low-voltage differential swing outputs have been defined.

The clock driver for all clocks must generate monotonic edges through the input threshold regions as specified for each signaling environment. Many conditions exist in the design of the clock driver and the system that can affect the monotonic operation of the clock driver. Power supply noise, pin inductance and capacitance, ratio of clock signals to Vddq and Vss pins, and routing topology will affect the monotonicity of these clocks. The electrical requirements outlined here ensure components connect directly together without any external buffers or other "glue" logic. Series terminating resistors may be required to keep noise within limits on strong drivers under lightly loaded conditions. Components should be designed to operate within the "commercial" range of environmental parameters. However, this does not preclude the option of other operating environments at the vendor's discretion.

The differential clock outputs are specified in terms of their output current accuracy and transition rate over a range of loads. A default set of signaling criteria is presented along with ranges for user programmability of the swing amplitude. The driver configuration of these buffers is strongly dependent on system layout and termination. System information including layout and termination information is contained in Section 5.

Examples of possible clock driver designs are contained in the appendices.

3.1 DC Specifications

DC parameters must be sustainable under steady state (DC) conditions.

Table 3.1 Absolute Maximum DC Power Supply

Symbol	Parameter	Min.	Max.	Units	Notes
V_{DD3}	3.3V Core Supply Voltage	-0.5	4.6	V	
V_{DDQ3}	3.3V I/O Supply Voltage	-0.5	4.6	V	
Ts	Storage Temperature	-65	150	°C	2

Note: Max Vih not to exceed Vdd3 +0.7V

Table 3.2 Absolute Maximum DC I/O

Symbol	Parameter	Min.	Max.	Units	Notes
V_{ih3}	3.3V Input High Voltage	-0.5	4.6	V	1
V_{il3}	3.3V Input Low Voltage	–0.5		V	
ESD prot.	Input ESD protection	2000		V	2

Notes:
1. Maximum Vih is not to exceed maximum 0.7V above VDD.
2. Human body model.

Table 3.3 DC Operating Requirements

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{DD3}	3.3V Supply Voltage	3.3V ±5%	3.135	3.465	V	4
V_{ih3}	3.3V Input High Voltage	VDD3	2.0	V_{DD}+0.3	V	7
V_{il3}	3.3V Input Low Voltage		V_{SS}-0.3	0.8	V	7
I_{il}	Input Leakage Current	$0 < V_{in} < V_{DDQ3}$	-5	+5	µA	3, 7
V_{oh3}	3.3V Output High Voltage	Ioh = -1 mA	2.4		V	1
V_{ol3}	3.3V Output Low Voltage	Iol = 1 mA		0.4	V	1
V_{poh}	PCI Bus Output High Voltage	Ioh = -1 mA	2.4		V	1
V_{pol}	PCI Bus Output Low Voltage	Iol = 1 mA		0.55	V	1, 5
C_{in}	Input Pin Capacitance			5	pF	2
C_{xtal}	Xtal Pin Capacitance		13.5	22.5	pF	6
Ta	Ambient Temperature	No Airflow	0	70	°C	

Notes:
1. Signal edge is required to be monotonic when transitioning through this region.
2. This is a recommendation, not an absolute requirement.
3. Input Leakage Current does not include inputs with Pull-Up or Pull-down resistors. Inputs with resistors should state current requirements.
4. No power sequencing is implied or allowed to be required in the system.
5. Conforms to 5V PCI Signaling specification.
6. As seen by the crystal. Device is intended to be used with a 17-20pF AT crystal. See next section for more details.
7. All inputs referenced to 3.3V power supply.

Table 3.3 Maximum Current Draw

Part	Parameter	Min.	Max.	Units	Notes
CKx_SKS	Current from 3.3V supply	N/A	250	mA	1,2,3,4
CKx_WBY	Current from 3.3V supply	N/A	200	mA	1,2,3,4
CKFF	Current from 3.3V supply	N/A	350	mA	1,4

Notes:

1. Conditions: Max Power supply (3.465V), all active
2. Configured with 475 Ohm current reference resistor at Iout=6*Iref
3. Host = 133MHz
4. Suppliers are encouraged to design for much lower current draw then the specifications shown.

Table 3.4 Maximum Current Draw During PWRDWN#

Part	Parameter	Min.	Max.	Units	Notes
CKx_SKS	Current from 3.3V supply	N/A	60	mA	1
CKx_WBY	Current from 3.3V supply	N/A	80	mA	1
CKFF	Current from 3.3V supply	N/A	0.3	mA	

Notes:

1. Configured with 475 Ohm current reference resistor

3.1.1 Load Capacitance As Seen By External Crystal Reference

Some earlier clock definitions do not specify a target load capacitance for the clock synthesizer as seen by the crystal. Most of the clock designs targeted 12-13 pF due to historical reasons, but, few designs specified the variation in their data sheets. However, the common crystals used today are in the 17-20 pF range.

To reduce the ambiguity with this issue, this specification requires that the clock driver load capacitance (as seen by the crystal, **not the capacitance of the individual XTAL_IN and XTAL_OUT pins**) be targeted **at 18pF +/- 25%.** This specification includes the clock driver component only and does not include any capacitance associated with board vias and traces.

Doing this:

- Directs all designs to the same target load capacitance.
- Requires testing/guarantee by design of the variation.
- Eliminates external compensation capacitors if the frequency variation can be tolerated.

3.2 Buffer Specifications:

The V/I curves, and Trise/Tfall specifications are targeted at achieving acceptable switching behavior under the lumped load conditions as described in Section 4 of this specification. Pull-up and pull-down sides for each of the buffers have separate V/I curves, which are provided, in the following sections. The DC drive curve specifies steady state conditions that must be maintained, but does not indicate real output drive strength.

AC parameters must be guaranteed under transient switching (AC) conditions. The sign on all current parameters (direction of current flow) is referenced to a ground inside the component; i.e. positive currents flow into the component while negative currents flow out of the component.

Table 3.4 Buffer Types

Buffer Name	VCC Range (V)	Impedance (Ohms)	Buffer Type
48MHz, REF	3.135 - 3.465	20 - 60	Type 3
PCI, 3V66	3.135 - 3.465	12 - 55	Type 5
MRef, Mref_b	3.135 - 3.465	12 - 55	Type 5
Host/Host_bar			Type X1
14seed, 66seed	3.135 - 3.465	12 - 55	Type 5

1. CK00 single ended buffer types are a subset of previous clock driver specifications. Type 1, Type 2,and Type 4 buffer types are not required for this implementation.

3.2.1 TYPE 3: Buffer Characteristics

Table 3.5 Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.0 V	-29			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-23	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.95 V	29			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			27	mA	1
t_{rh}	3.3V Type 3 Output Rise Edge Rate	3.3V ±5% @ 0.4V – 2.4 V	0.5		2.0	V/nS	2
t_{fh}	3.3V Type 3 Output Fall Edge Rate	3.3V ±5% @ 2.4V – 0.4 V	0.5		2.0	V/nS	2

Notes:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See Waveform Figure for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC, process and temperature range.
4. Receiver logic thresholds are Vil=0.8 and Vih=2.0 Volts.
5. Ron 20-60 Ohm with a 40 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.

Pull-Up			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-29	-46	-99
1	-29	-46	-99
1.4	-27	-44	-94
1.5	-27	-43	-92
1.65	-25	-41	-89
1.8	-24	-39	-85
2	-22	-36	-79
2.4	-16	-28	-63
2.6	-12	-22	-53
3.135	0	-6	-23
3.3		0	-12
3.465			0

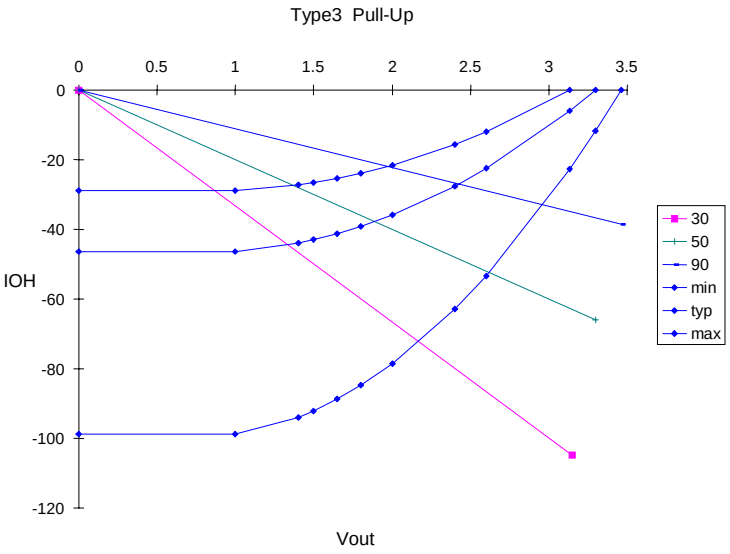


Figure 3.1 TYPE 3: Pull-Up Characteristics

Notes (Figure 3.1)**:**

1. Must meet the temperature and voltage range specified in
2. Table 3.3 DC Operating Requirements
3. This drawing is not to scale. Comparisons should be made to the data provided in the table next to this drawing and to Table 3.5 Operating Requirements. .

Pull-Down			
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	0	0	0
0.4	9	13	27
0.65	14	21	41
0.85	17	26	52
1	20	29	59
1.4	25	37	76
1.5	26	39	79
1.65	27	41	84
1.8	28	43	88
1.95	29	45	92
3.135	29	45	102
3.6		45	102

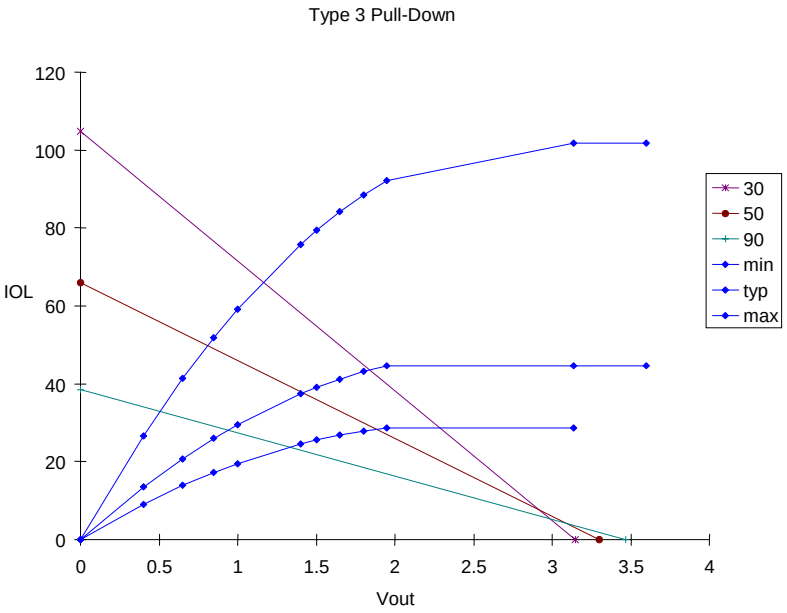


Figure 3.2 TYPE 3: Pull-Down Characteristics

Notes (Figure 3.2)**:**

1. Must meet the temperature and voltage range specified in
2. Table 3.3 DC Operating Requirements
3. This drawing is not to scale. Comparisons should be made to the data provided in the table next this drawing.

3.2.2 TYPE 5: Buffer Characteristics

Table 3.6: Operating Requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units	Notes
I_{ohmin}	Pull-Up Current	Vout = 1.0 V	-33			mA	1
I_{ohmax}	Pull-Up Current	V_{out} = 3.135 V			-33	mA	1
I_{olmin}	Pull-Down Current	V_{out} = 1.95 V	30			mA	1
I_{olmax}	Pull-Down Current	V_{out} = 0.4 V			38	mA	1
T_{rh}	3.3V Type 4 Output Rise Edge Rate	3.3V ±5% @ 0.4V - 2.4 V	1/1		4/1	V/nS	2
T_{fh}	3.3V Type 4 Output Fall Edge Rate	3.3V ±5% @ 2.4V - 0.4 V	1/1		4/1	V/nS	2

Notes:

1. Intended to approximate impedance curve below. Device should be checked against entire curve for characterization testing. Production testing is expected to be a subset of characterization testing.
2. Output rise and fall time. See for calculation / measurement information.
3. Output rise and fall time must be guaranteed across VCC , process and temperature range.
4. Receiver logic thresholds are Vil=0.8 and Vih=2.0 Volts.
5. Ron 12-55 Ohm with a 30 Ohm nominal driver impedance.
6. Ron = Vout/Ioh, Vout/Iol measured at VCC/2.
7. See PCI specification for additional PCI details.

	Pull-Up		
Voltage (V)	I (mA) min	I (mA) typ	I (mA) max
0	-34	-59	-195
1	-33	-58	-194
1.4	-31	-55	-189
1.5	-30	-54	-184
1.65	-28	-52	-172
1.8	-25.5	-50	-159
2	-22	-46	-140
2.4	-14.5	-35	-100
2.6	-11	-28	-83
3.135	0	-6	-33
3.3		0	-19
3.6			0

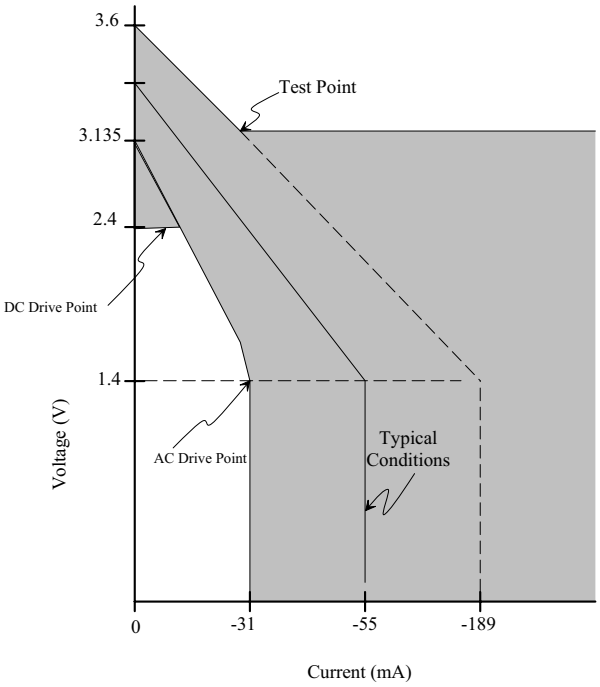


Figure 3.3 TYPE 5: Pull-Up Characteristics

Notes (Figure 3.3):

1. Must meet the temperature and voltage range specified in
2. Table 3.3 DC Operating Requirements.
3. This drawing is not to scale. Comparisons should be made to the data provided in the table next to it and to Table 3.6: Operating Requirements

Pull-Down			
Voltage (V)	I (mA) min	I(mA) typ	I (mA) max
0	0	0	0
0.4	9.4	18	38
0.65	14	30	64
0.85	17.7	38	84
1	20	43	100
1.4	26.5	53	139
1.5	28	55	148
1.65	29	56	163
1.8	30	57	175
1.95	30	58	178
3.135	31	59	187
3.6	32	59	188

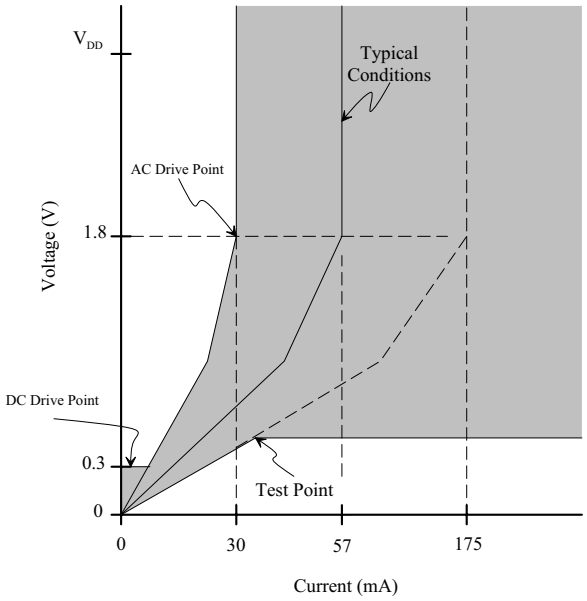


Figure 3.4 TYPE 5: PCI Clock Output Buffer Pull-Down Characteristics

Notes (Figure 3.4)**:**

1. Must meet the temperature and voltage range specified in
2. Table 3.3 DC Operating Requirements
3. This drawing is not to scale. Comparisons should be made to the data provided in the table next to it and to Table 3.6: Operating Requirements

3.2.3 Type X1 Current-mode Output Buffer Characteristics

The current-mode output buffer details and current reference circuit details are contained elsewhere in this document. For the purposes of this section, the following parameters are used to specify output buffer characteristics:

1) Output impedance of the current mode buffer circuit – Ro (See Figure 3.5)
2) Minimum and maximum required voltage operation range of the circuit – Vop (See Figure 3.1)
3) Series resistance in the buffer circuit – Ros (See Figure 3.5)
4) Current accuracy at given configuration into nominal test load for given configuration

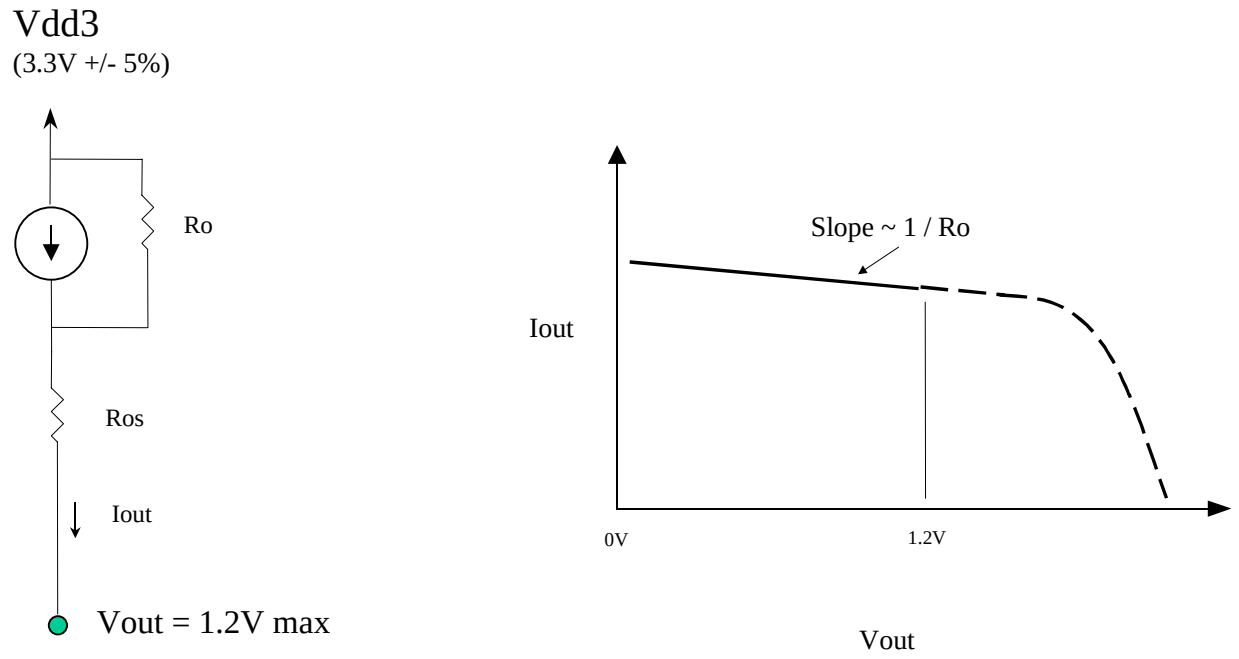


Figure 3.5

Table 3.7 - Host Clock (HCSL) Buffer Characteristics

	Minimum	**Maximum**
Ro	3000 Ohms (recommended)	N/A
Ros	unspecified	unspecified
Vout	N/A	1.2V

The reader should note that Iout is selectable depending on implementation. The parameters above, however, apply to all configurations. Vout is the voltage at the pin of the device.

The various output current configurations are shown in the appendix of this document. For all configurations, the deviation from the expected output current is +/- 7% as shown in Table 3.8.

Table 3.8 – Current Accuracy

	Conditions	Configuration	Load	**Min**	**Max**
Iout	Vdd = nominal (3.30V)	All combinations of M0, M1 and Rr shown in Table 6.9	Nominal test load for given configuration	-7% $I_{nominal}$	+7% $I_{nominal}$
Iout	Vdd = 3.30 +/- 5%	All combinations of M0, M1 and Rr shown in Table 6.9	Nominal test load for given configuration	-12% $I_{nominal}$	+12% $I_{nominal}$

Note: $I_{nominal}$ refers to the expected current based on the configuration of the device.

4. AC Timing

4.1 Timing Requirements

Table 4.1 AC Timing Requirements

		133 MHz Host		100 MHz Host			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
TPeriod	Host CLK period - average	7.5	7.65	10.0	10.2	nS	11, 14
AbsMinPeriod	Absolute minimum Host CLK Period	7.35	N/A	9.85	N/A	nS	11, 14
Ioh (Voh)	Output Current (Voltage at given load)	12.9 (0.65)	14.9 (0.74)	12.9 (0.65)	14.9 (0.74)	mA (V)	11, 13, 17
Vol		Vss = 0.0	0.05	Vss = 0.0	0.05	V	11
Vcrossover		45% Voh	55% Voh	45% Voh	55% Voh	V	11, 14
TRISE	Host/CPU CLK rise time	175	700	175	700	pS	11, 15
TFALL	Host/CPU CLK fall time	175	700	175	700	pS	11, 15
Rise/Fall Matching	Rise time and fall time matching		20%		20%		11, 16
Overshoot			Voh + 0.2V		Voh + 0.2V		11, 16
Undershoot		– 0.2V		– 0.2V			11
Tskew (One chip partition)	Pair to Pair skew for one chip partition for **CKx_SKS, CKx_RGR**		150		150	pS	11, 14
Tskew (Two chip partition)	Pair to Pair skew for two chip partition for **CKx_WBY**		100		100	pS	11, 14
Tccjitter (One chip partition)	Cycle to Cycle jitter for **CKx_SKS, CKx_RGR**		200		200	pS	11, 12, 14
Tccjitter (Two chip partition)	Cycle to Cycle jitter for two chip partition for **CKx_WBY**		150		150	pS	11, 12, 14
Duty Cycle		45%	55%	45%	55%		11, 14
TPeriod	Mref, Mref_b CLK period	15.0	15.3	20.0	20.4	nS	2, 9
THIGH	MRef, Mref_b CLK high time	5.25	N/A	7.5	N/A	nS	5, 10
TLOW	MRef, Mref_b CLK low time	5.05	N/A	7.3	N/A	nS	6, 10
TRISE	MRef, Mref_b CLK rise time	0.4	1.6	0.4	1.6	nS	8
TFALL	MRef, Mref_b CLK fall time	0.4	1.6	0.4	1.6	nS	8
TPeriod	3V66 CLK period	15.0	16.0	15.0	15.2		2, 4, 9
THIGH	3V66 CLK high time	5.25	N/A	5.25	N/A		5 ,10

TLOW	3V66 CLK low time	5.05	N/A	5.05	N/A		6 ,10
TRISE	3V66 CLK rise time	0.5	2.0	0.5	2.0		8
TFALL	3V66 CLK fall time	0.5	2.0	0.5	2.0		8
TPeriod	PCI CLK period	30.0	N/A	30.0	N/A	nS	2, 3, 9
THIGH	PCI CLK high time	12.0	N/A	12.0	N/A	nS	5 ,10
TLOW	PCI CLK low time	12.0	N/A	12.0	N/A	nS	6 ,10
TRISE	PCI CLK rise time	0.5	2.0	0.5	2.0	nS	8
TFALL	PCI CLK fall time	0.5	2.0	0.5	2.0	nS	8
tpZL, tpZH	Output enable delay (All outputs)	1.0	10.0	1.0	10.0	nS	
tpLZ, tpZH	Output disable delay (All outputs)	1.0	10.0	1.0	10.0	nS	
tstable	All clock Stabilization from power-up		3		3	mS	7

Notes:

1. Output drivers must have monotonic rise/fall times through the specified VOL/VOH levels.
2. Period, jitter, offset and skew measured on rising edge @1.25V for 2.5V clocks and @ 1.5V for 3.3V clocks.
3. The PCI clock is the Host clock divided by four at Host=133MHz. PCI clock is the Host clock divided by three at Host = 100MHz.
4. 3V66 is internal VCO frequency divided by four for Host=133MHz. 3V66 clock is internal VCO frequency divided by three for Host=100MHz
5. THIGH is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
6. TLOW is measured at 0.4V for all outputs.
7. The time specified is measured from when Vddq achieves its nominal operating level (typical condition Vddq = 3.3V) till the frequency output is stable and operating within specification.
8. TRISE and TFALL are measured as a transition through the threshold region Vol = 0.4V and Voh = 2.4V (1mA) JEDEC Specification.
9. The average period over any 1 uS period of time must be greater than the minimum specified period
10. Calculated at minimum edge-rate (1V/nS) to guarantee 45/55% duty-cycle. Pulsewidth is required to be wider at faster edge-rate to ensure duty-cycle specification is met.
11. Test load is Rs=33.2Ohms, Rp=49.9. See Section 5, and Table 6.9.
12. Must be guaranteed in a realistic system environment.
13. Configured for Ioh = 6 * Iref. See Section 5.
14. Measured at crossing points. See section 5.
15. Measured at 20% to 80%.
16. Determined as a fraction of 2*(Trp – Trn) / (Trp + Trn) where Trp is a rising edge and Trn is an intersecting falling edge.
17. These minimum and maximum voltages and currents assume a power supply of 3.30V. For system considerations, the voltages will need to be degraded to account for the +/-5% variation in the 3.3V supply.

Table 4.2 Group Skew And Jitter Limits

Output group	Pin-pin Skew Or Pair-to-Pair Skew MAX	Cycle-Cycle Jitter	Duty Cycle	Nom Vdd	Skew, jitter measure point
Host (Single Pkg Case)	150 pS	200 pS	45/55	N/A	Crossing
Host (Dual Pkg Case)	100 pS	150pS	45/55	N/A	Crossing
MRef	N/A	250 pS	45/55	3.3 V	1.5 V
48MHz	N/A	350 pS	45/55	3.3 V	1.5 V
3V66	250 pS	300 pS	45/55	3.3 V	1.5 V
PCI	500 pS	500 pS	45/55	3.3 V	1.5 V
REF	N/A	1000 pS	45/55	3.3V	1.5 V

Table 4.3 Group Offset limits

Group	Offset	Measurement loads (lumped)	Measure Points
3V66 to PCI	1.5-3.5 nS 3V66 leads	3V66@30 pF, PCI@30 pF	3V66@1.5 V, PCI@1.5 V
Host to 3V66	No Requirement		
Host to PCI	No Requirement		

Notes:
1. All offsets are to be measured at rising edges

Only offset specifications listed above are required to be guaranteed/tested. The specification should be treated as ANY output within first specified bank to ANY output of the second specified bank. Pin-pin skew is implied within offset specification; jitter is not.

4.1.1 Frequency Accuracy of 48MHz outputs

The 48 MHz nominal frequency is required to be +167ppm from 48.00MHz.

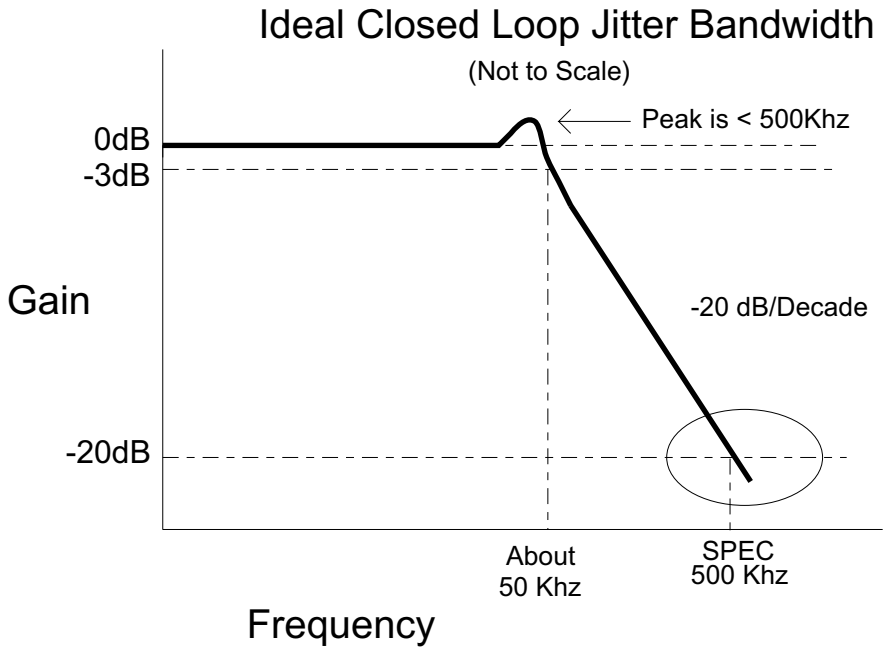
The total accuracy of the crystal and clock device over aging, temperature, and Vdd variation must be ± 500ppm around 48.000MHz. This parameter amounts to +333/-667ppm around the nominal frequency identified above.

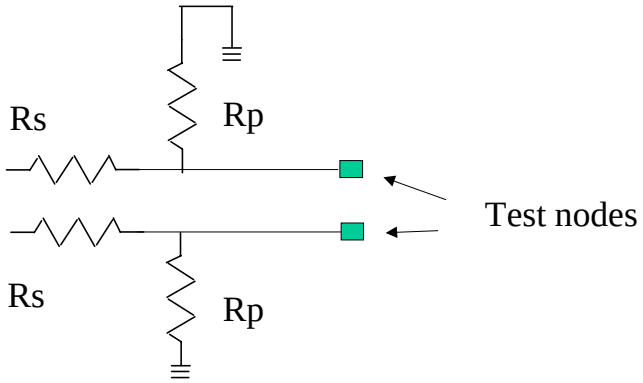
4.1.2 Multiple PLL Jitter Tracking Specification.

The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. This 1:1 relationship is critical when the clock driver drives two or more PLLs. A worst-case timing issue would occur if one PLL attenuated the jitter and another device (PLL or non-PLL) tracked the jitter completely. To reduce the possibility of this we require that the -20dB attenuation point be less than or equal to 500KHz. Most clock vendors do not specify their jitter bandwidth characteristics or specify it only at the -3dB level. To allow for greatest flexibility in loop design we require the vendor to provide the -20dB point. This specification may be guaranteed by design and/or measured with a spectrum analyzer.

This specification is intended to replace or clarify the Pentium® processor specification, which was stated as:

"To ensure a 1:1 jitter frequency relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 500 kHz and 1/3 of the clock operating frequency."





5. Test and Measurement

The tables below provide acceptable lumped load test loads over which the vendor is expected to test and guarantee all AC parameters for the clock driver. The vendor is encouraged to provide information on the correlation between lumped load performance and system performance as an applications exercise to fully describe the operation of the product.

Table 5.1 -- Lumped Capacitive Test Loads for Single Ended Outputs

Clock	Min Load	Max Load	Units	Notes
PCI Clocks (PCLK)	10	30	pF	Must meet PCI 2.1 requirements
Mref, Mref_b	10	30	pF	1 device load, possible 2 loads
3V66	10	30	pF	1 device load, possible 2 loads
48 MHz Clock	10	20	pF	1 device load
REF	10	20	pF	1 device load

Notes:

1. Maximum rise/fall times are to be guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are to be guaranteed at minimum specified load for each type of output buffer
3. Rise/fall times are specified with pure capacitive load as shown. Testing may be done with an additional 500 ohm resistor in parallel if properly correlated with the capacitive load.

The following shows lumped test load configurations for the differential Host Clock outputs.

Table 5.2 Minimum and Maximum Lumped Resistive Test Loads

Clock	Min Load	Max Load	Units	Notes
Host Clocks	20	105	Ohms	

Table 5.3 Resistive Lumped Test Loads for Differential Host Clock

Clock		Rs	Rp	Units	Notes
Host Clocks – 60 ohm configuration		33.2 1%	61.9 1%	Ohms	2, 3, 5
Host Clocks – 50 ohm configuration		33.2 1%	49.9 1%	Ohms	1, 2, 3, 5
Host Clocks – Double Terminated configuration		0	24.9 1%	Ohms	4

1. Expected test load configuration unless otherwise noted. This is a 50 Ohm environment test load. This assumes device is configured for 50 Ohm environment.
2. Test load for 60 Ohm environment. This assumes device is configured for a 60 Ohm environment.
3. Suppliers must correlate parameters measured in 50 ohm environment to a 60 ohm environment with the appropriate configurations of the device for each load.
4. Test load for dual terminated (i.e. both source and load) 50 ohm environment.
5. For configurations of the device intended to create output current greater then 14mA these test loads may not be appropriate. For such configurations, a value of Rs=0 should be used.

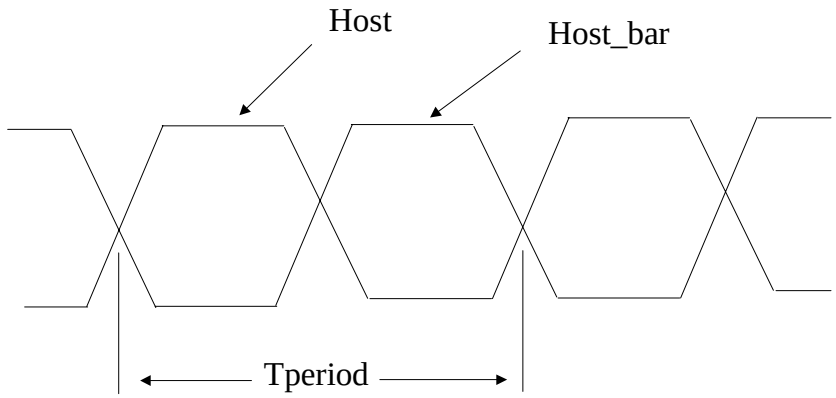


Figure 5.3 CK133 Clock Waveforms

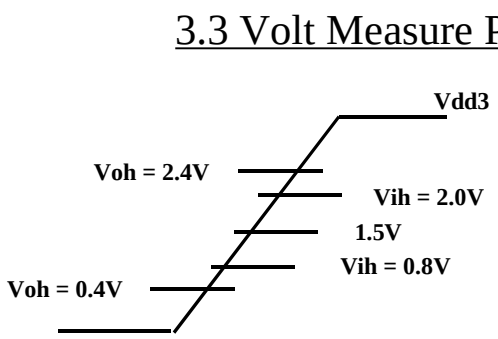


Figure 5.4 Component versus System Measure Points for Single Ended Clocks

6. Appendices

6.1 Pin-outs and Features

The following addendum defines a generic pin-out and base requirements for Intel Architecture based platforms. It is intended to be used with another clock driver or drivers to clock the memory devices.

CKx_SKS clock chip (56 SSOP and 56 TSSOP):

Description: This clock is intended to be used in single processor systems and two processor systems.

- Four Differential Host Clock Pairs
- Two 3V Single Ended memory reference clocks 180 degrees out of phase
- Four 3V, 66MHz Clocks
- Ten 3V, 33MHz PCI Clocks
- Two 48MHz Clocks
- Two 14.318MHz Reference Clocks
- Select logic for Differential Swing Control, Test mode, Hi-Z, Power-down, Spread spectrum, limited frequency select, and other
- External resistor for current reference

	GndR	1		56	3.3M
Ref/MultSel0*		2		55	3VMref
Ref/MultSel1*		3		54	3VMref_b
	3.3R	4		53	GndM
Xtal_in		5		52	Spread#
Xtal_out		6		51	Host
	GndP	7		50	Host_bar
PCI		8		49	3.3H
PCI		9		48	Host
	3.3P	10		47	Host_bar
PCI		11		46	GndH
PCI		12	SKS	45	Host
	GndP	13		44	Host_bar
PCI		14		43	3.3H
PCI		15		42	Host
	3.3P	16		41	Host_bar
PCI		17		40	GndH
PCI		18		39	I Ref
	GndP	19		38	3.3Core
PCI		20		37	GndCore
PCI		21		36	3.3L
	3.3P	22		35	3V66
Sel100/133		23		34	3V66
	GndU	24		33	GndL
48MHz/SelA		25		32	GndL
48MHz/SelB		26		31	3V66
	3.3U	27		30	3V66
PWRDWN#		28		29	3.3L

Table 6.1 CKx_SKS Pin Description Table

Pin	Type	Qty	Symbol	Description
55	3.3V output	1	3VMref	3V reference to memory clock driver
54	3.3V output	1	3VMRef_b	3V reference to memory clock driver (out of phase with 3Vmref)
52	Input	1	Spread#	Invokes Spread Spectrum functionality on the Differential Host clocks, MRef/MRef_b clocks, 66MHz clocks, and 33MHz PCI clocks. Active Low.
51,50	Buffer X1		Host/Host_b	Host pair 1
48,47	Buffer X1		Host/Host_b	Host pair 2
45, 44	Buffer X1		Host/Host_b	Host pair 3
42, 41	Buffer X1		Host/Host_b	Host pair 4
39	Special	1	I_Ref	This pin establishes the reference current for the Host pairs. This pin takes a fixed precision resistor tied to ground in order to establish the appropriate current.
35,34,31,30	3.3V output	4	3V66	66MHz 3.3V outputs
28	Input	1	PWRDWN#	Invokes power-down mode. Active Low.
26,25	Output and Latched Input	2	48MHz/SelA, 48MHz/SelB	SelA and SelB inputs are sensed on power-up and then internally latched prior to the pin being used for output of 3V 48MHz clocks.
23	Input	1	SEL100/133	Host Frequency Select. Low=100MHz, High=133MHz
21,20,18,17, 15,14,12,11, 9,8	3.3V output	10	PCI	3.3V 33MHz outputs
6	Xtal output	1	Xtal_out	14.318MHz Crystal output
5	Xtal input	1	Xtal_in	14.318MHz Crystal input
3,2	Output and Latched Input	2	Ref/MultSel0 Ref/MultSel1	MultSel0 and MultSel1 inputs are sensed on power-up and then internally latched prior to the pin being used for output of 3V 14.318MHz clocks.
56, 53	Power/Gnd		3.3M, GndM	Power and ground pins recommended for 3VMref and 3VMref_b dedicated use
49,46,43,40	Power/Gnd		3.3H, GndH	Power and ground pins recommended for Host/Host_bar dedicated use
38,37	Power/Gnd		3.3Core, GndCore	Power and ground pins recommended for dedicated core use
36,33,32,29	Power/Gnd		3.3L,GndL	Power and ground pins recommended for 3V66 dedicated use
27,24	Power/Gnd		3.3U, GndU	Power and ground pins recommended for 48MHz dedicated use
22,19,16,13, 10,7	Power/Gnd		3.3P,GndP	Power and ground pins recommended for PCI dedicated use
4,1	Power/Gnd		3.3R,GndR	Power and ground pins recommended for REF clock and Xtal dedicated use

CKx_WBY clock chip (48 SSOP Package and 48 TSSOP):

Description: This is intended as the main clock source in certain multiple-chip clock partitions. This clock is intended to be used with the FF. The WBY/FF pair is intended to be used in two-processor, and four-processor platforms.

- Six Differential Host Clock Pairs
- Two 3V Single Ended memory reference clocks 180 degrees out of phase
- One 66MHz reference output
- One14.318MHz reference output
- Select logic for Differential Swing Control, Test mode, Hi-Z, Powerdown, Spread spectrum, limited frequency select, selective clock enable.
- External resistor for current reference

GndR	1		48	3.3R	
ref_out	2		47	Gnd	
3.3R	3		46	3.3H	
Xtal_in	4		45	Host	
Xtal_out	5		44	Host_bar	
GndR	6		43	GndH	
3.3M	7		42	Host	
3VMref	8	WBY	41	Host_bar	
3VMref_b	9		40	3.3H	
GndM	10		39	Host	
3.3Core	11		38	Host_bar	
3.3Gnd	12		37	GndH	
3.3L	13		36	Host	
3V66	14		35	Host_bar	
GndL	15		34	3.3H	
Sel100/133	16		33	Host	
MultSel0	17		32	Host_bar	
MultSel1	18		31	GndH	
3.3	19		30	Host	
Gnd	20		29	Host_bar	
SelA	21		28	3.3H	
SelB	22		27	I Ref	
Spread#	23		26	GndI	
PWRDWN#	24		25	3.3I	

Table 6.2 CKx_WBY Pin Description Table

Pin	Type	Qty	Symbol	Description
45,44	Buffer X1		Host/Host_b	Host pair 1
42,41	Buffer X1		Host/Host_b	Host pair 2
39,38	Buffer X1		Host/Host_b	Host pair 3
36,35	Buffer X1		Host/Host_b	Host pair 4
33,32	Buffer X1		Host/Host_b	Host pair 5
30,29	Buffer X1		Host/Host_b	Host pair 6
27	Special	1	I_Ref	This pin establishes the reference current for the Host pairs. This pin takes a fixed precision resistor tied to ground in order to establish the appropriate current.
24	Input	1	PWRDWN#	Invokes power-down mode. Active Low.
23	Input	1	Spread#	Invokes Spread Spectrum functionality on the Differential Host clocks, MRef/MRef_b clocks, 66MHz clocks, and 33MHz PCI clocks. Active Low
22,21	Input	2	SelB, SelA	Select pins
18,17	Input	2	MultSel0, MultSel1	These pins configure the Ioh amplitude (and thus the Voh swing amplitude) of the Host pair outputs
16	Input	1	SEL100/133	Host Frequency Select. Low=100MHz, High=133MHz
14	3.3V output	1	3V66	66MHz reference clock
9	3.3V output	1	3VMref	3V reference to memory clock driver
8	3.3V output	1	3VMRef_b	3V reference to memory clock driver (out of phase with 3Vmref)
5	Xtal output	1	Xtal_out	14.318MHz Crystal output
4	Xtal input	1	Xtal_in	14.318MHz Crystal input
2	3.3V output	1	Ref_out	14.318MHz reference output
48,6,3,1	Power/Gnd		3.3R,GndR	Power and ground pins recommended for REF clock and Xtal dedicated use
43,40,37,34, 31,28	Power/Gnd		3.3H, GndH	Power and ground pins recommended for Host/Host_bar dedicated use
26,25	Power/Gnd		3.3I,GndI	Power and ground pins recommended for current reference circuit dedicated use
15,13	Power/Gnd		3.3L,GndL	Power and ground pins recommended for 3V66 dedicated use
12,11	Power/Gnd		3.3Core, GndCore	Power and ground pins recommended for dedicated core use
10,7	Power/Gnd		3.3M, GndM	Power and ground pins recommended for 3VMref and 3VMref_b dedicated use
47,20,19	Power, Gnd		3.3, Gnd	Power and ground pins

CKFF clock chip (48 SSOP and 48 TSSOP):

Description: This is a slave clock to the WBY. This can also be used as a slave clock to future variants of the WBY. **For Spread Spectrum Tracking, there must not be a PLL in the path of the 66MHz clocks or the 33MHz PCI clocks.** The 66MHz and 33MHz clocks are intended to be buffered and/or divided from the 66_in seed clock input. The pin-out of this device was chosen to allow down-bondability to 48 pins

- Six 3V66 Clocks
- Twelve 3V, 33MHz PCI Clocks
- Two 48MHz Clocks
- Two 14.318MHz Reference Clocks
- Select logic for Differential Swing Control, Test mode, Hi-Z, Power-down, Spread spectrum, limited frequency select, and other
- 66MHz reference input
- 14.318 reference input

Note: I^2C is not required for this part. However, if I^2C is not implemented, then the part should be a different part number in order to prevent applications confusion. Furthermore, if

	GndN	1		56	3.3R
14.318_in		2		55	Ref
	3.3N	3		54	Ref
66_in		4		53	GndR
	GndP	5		52	3.3L
PCI		6		51	3V66
PCI		7		50	3V66
	3.3P	8		49	GndL
	GndP	9		48	GndL
PCI		10		47	3V66
PCI		11		46	3V66
	3.3P	12		45	3.3L
	GndP	13	FF	44	3.3L
PCI		14		43	3V66
PCI		15		42	3V66
	3.3P	16		41	GndL
PCI		17		40	3.3
PCI		18		39	Gnd
	GndP	19		38	3.3U
	3.3P	20		37	48Mhz
PCI		21		36	48Mhz
PCI		22		35	GndU
	GndP	23		34	Sels
PCI		24		33	PWRDWN#
PCI		25		32	3.3S
	3.3P	26		31	GndS
Selq		27		30	Sclock
Selr		28		29	Sdata

I^2C is not implemented, pins 29 and 30 should be immune to I^2C signals to allow placement on a platform which has I^2C implemented.

Table 6.3 CKFF Pin Description Table

Pin	Type	Qty	Symbol	Description
55,54	3.3V output	2	Ref	14.318MHz 3.3V outputs
51,50,47,46,43,42	3.3V output	6	3V66	66MHz 3.3V outputs
37,36	3.3V output	2	48MHz	48MHz output. See accuracy specifications.
34,28,27	Input	3	SELq, SELr, SELs	Select Pins
33	Input	1	PWRDWN#	Invokes Power-down mode. Active Low.
30,29	Input		Sclock, Sdata	I^2C pins
25,24,22,21,18,17,15, 14,11,10,7,6	3.3V output	12	PCI	3.3V 33MHz outputs
4	Input	1	66_in	Input for 3.3V 66MHz reference clock
2	Input	1	14.318_in	Input for 14.318MHz reference clock
56,53	Power/Gnd		3.3R,GndR	Power and ground pins recommended for REF clock and Xtal dedicated use
52,49,48,45,44,41	Power/Gnd		3.3L,GndL	Power and ground pins recommended for 3V66 dedicated use
38,35	Power/Gnd		3.3U, GndU	Power and ground pins recommended for 48MHz dedicated use
32,31	Power/Gnd		3.3S, GndS	Power and ground pins recommended for I^2C dedicated use
26,23,20,19,16,13,12, 9,8,5	Power/Gnd		3.3P,GndP	Power and ground pins recommended for PCI dedicated use
3,1	Power/Gnd		3.3N, GndN	Power and ground pins recommended for dedicated input circuit use (for 14.318_in and 66_in)
40,39	Power, Gnd		3.3, Gnd	Power and ground pins

CKx_RGR clock chip Future pin-out (48 TSSOP and 48 SSOP):

Description: This clock is intended as a future spin of the SKS. This clock is intended for single processor platforms.

- Two Differential Host Clock Pairs
- Two 3V Single Ended memory reference clocks 180 degrees out of phase
- Three 3V, 66MHz Clocks
- Ten 3V, 33MHz PCI Clocks
- Two 48MHz Clocks
- Two 14.318MHz Reference Clocks
- Select logic for Differential Swing Control, Test mode, Hi-Z, Power-down, Spread spectrum, limited frequency select, and other
- External resistor for current reference

Ref/MultSel1*	1		48	Ref/MultSel0*
3.3R	2		47	GndR
Xtal_in	3		46	3.3M
Xtal_out	4		45	3VMref
GndP	5		44	3VMref_b
PCI	6		43	GndM
PCI	7		42	Spread#
3.3P	8		41	Host
PCI	9		40	Host_bar
PCI	10	RGR	39	3.3H
GndP	11		38	Host
PCI	12		37	Host_bar
PCI	13		36	GndH
3.3P	14		35	I Ref
PCI	15		34	3.3Core
PCI	16		33	GndCore
GndP	17		32	PWRDWN#
PCI	18		31	3.3L
PCI	19		30	3V66
3.3P	20		29	3V66
Sel100/133	21		28	GndL
GndU	22		27	3V66
48MHz/SelA	23		26	3.3L
48MHz/SelB	24		25	3.3U

Table 6.4 CKx_RGR Pin Description Table

Pin	Type	Qty	Symbol	Description
48,1	Output and Latched Input	2	Ref/MultSel0 Ref/MultSel1	MultSel0 and MultSel1 inputs are sensed on power-up and then internally latched prior to the pin being used for output of 3V 14.318MHz clocks.
45	Output	1	3VMref	3V reference to memory clock driver
44	Output	1	3Vmref_b	3V reference to memory clock driver (out of phase with 3VMref)
42	Input	1	Spread#	Invokes Spread Spectrum functionality on the Differential Host clocks, MRef/MRef_b clocks, 66MHz clocks, and 33MHz PCI clocks. Active Low.
41,40	Buffer X1	1	Host/Host_bar	Host pair 1
38,37	Buffer X1	1	Host/Host_bar	Host pair 2
35	Special	1	I_Ref	This pin establishes the reference current for the Host pairs. This pin takes a fixed precision resistor tied to ground in order to establish the appropriate current.
32	Input	1	PWRDWN#	Invokes power-down mode. Active Low.
30,29,27	3.3V output	3	3V66	66MHz 3.3V outputs
24,23	Output and Latched Input	2	48MHz/SelA, 48MHz/SelB	SelA and SelB inputs are sensed on power-up and then internally latched prior to the pin being used for output of 3V 48MHz clocks.
21	Input	1	SEL100/133	Host Frequency Select. Low=100MHz, High=133MHz
19,18,16,15,13,12,10, 9,7,6,	3.3V output	10	PCI	3.3V 33MHz outputs
4	Xtal output	1	Xtal_out	14.318MHz Crystal output
3	Xtal input	1	Xtal_in	14.318MHz Crystal input
46,43	Power/Gnd		3.3M, GndM	Power and ground pins recommended for 3VMref and 3VMref_b dedicated use
39,36	Power/Gnd		3.3H, GndH	Power and ground pins recommended for Host/Host_bar dedicated use
34,33	Power/Gnd		3.3Core, GndCore	Power and ground pins recommended for dedicated core use
31,28,26	Power/Gnd		3.3L,GndL	Power and ground pins recommended for 3V66 dedicated use
25,22	Power/Gnd		3.3U, GndU	Power and ground pins recommended for 48MHz dedicated use
20,17,14,11,8,5	Power/Gnd		3.3P,GndP	Power and ground pins recommended for PCI dedicated use
2,48	Power/Gnd		3.3R,GndR	Power and ground pins recommended for REF clock and Xtal dedicated use

6.2 Select Pin Logic

Table 6.5 Select Functions -- *CKx_SKS*

SEL100/133	SELA	SELB	Function
0	0	0	Active 100MHz
0	0	1	(Reserved)
0	1	0	(Reserved)
0	1	1	HI-Z all outputs
1	0	0	Active 133MHz
1	0	1	(Reserved)
1	1	0	(Reserved)
1	1	1	Test Mode

SEL 100/133	SELA	SELB		Host	MRef	3V66	3V33 PCI	48MHz	REF	Notes:
0	0	0		100MHz	50MHz	66MHz	33MHz	48MHz	14.318 MHz	
0	0	1		N/A	N/A	N/A	N/A	N/A	N/A	
0	1	0		N/A	N/A	N/A	N/A	N/A	N/A	
0	1	1		HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	
1	0	0		133MHz	66MHz	66MHz	33MHz	48MHz	14.318 MHz	
1	0	1		N/A	N/A	N/A	N/A	N/A	N/A	
1	1	0		N/A	N/A	N/A	N/A	N/A	N/A	
1	1	1		TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	

Table 6.6 Select Functions – *CKx_RGR*

SEL100/133	SELA	SELB	Function
0	0	0	Active 100MHz
0	0	1	(Reserved)
0	1	0	(Reserved)
0	1	1	HI-Z all outputs
1	0	0	Active 133MHz
1	0	1	(Reserved)
1	1	0	(Reserved)
1	1	1	Test Mode

SEL 100/133	SELA	SELB		Host	MRef	3V66	3V33 PCI	48MHz	REF	Notes:
0	0	0		100MHz	50MHz	66MHz	33MHz	48MHz	14.318 MHz	
0	0	1		N/A	N/A	N/A	N/A	N/A	N/A	
0	1	0		N/A	N/A	N/A	N/A	N/A	N/A	
0	1	1		HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	
1	0	0		133MHz	66MHz	66MHz	33MHz	48MHz	14.318 MHz	
1	0	1		N/A	N/A	N/A	N/A	N/A	N/A	
1	1	0		N/A	N/A	N/A	N/A	N/A	N/A	
1	1	1		TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	

Table 6.7 Select Functions – *CKx_WBY*

SEL100/133	SELA	SELB	Function
0	0	0	Active 100MHz
0	0	1	Active 100MHz, ref_out Low, 66_out Low, 3VMRef and 3VMRef_b Low
0	1	0	(Reserved)
0	1	1	HI-Z all outputs
1	0	0	Active 133MHz
1	0	1	(Reserved)
1	1	0	(Reserved)
1	1	1	Test Mode

SEL 100/133	SELA	SELB		Host	MRef	66M seed	14.318M seed	Notes:
0	0	0		100MHz	50MHz	66MHz	14.318MHz	
0	0	1		100MHz	Low	Low	Low	
0	1	0		N/A	N/A	N/A	N/A	
0	1	1		HI-Z	HI-Z	HI-Z	HI-Z	
1	0	0		133MHz	66MHz	66MHz	14.318MHz	
1	0	1		N/A	N/A	N/A	N/A	
1	1	0		N/A	N/A	N/A	N/A	
1	1	1		TCLK/2	TCLK/4	TCLK	TCLK	

Table 6.8 Select Functions – *CKFF*

SELq	SELr	SELs	Description	Details
0	0	0	All outputs on	All outputs on
0	0	1	Top 8 PCI off	Pins 6,7,10,11,14,15,17,18 held LOW
0	1	0	Top 6 PCI off	Pins 6,7,10,11,14,15 held LOW
0	1	1	All PCI off	All PCI outputs Held LOW
1	0	0	Hi-Z	All outputs high impedance
1	0	1	Top one 66MHz off	Pin 51 held LOW
1	1	0	All 14MHz off	Pins 55,54 held LOW
1	1	1	One 48MHz off	Pin 37 held LOW

These select pins should have priority over SMBus in conditions in which the select pins are causing an output to be in an OFF condition.

Table 6.9 Host Swing Select Functions – CKx_SKS, CKx_WBY, CKx_RGR

MultSel0	**MultSel1**	Board Target Trace/Term Z	Reference R, Iref = Vdd/(3*Rr)	Output Current	Voh @ Z, Iref=2.32mA
0	**0**	**60 ohms**	**Rr = 475 1%, Iref=2.32mA**	**Ioh = 5*Iref**	**0.70V @ 60**
0	0	50 ohms	Rr = 475 1%, Iref=2.32mA	Ioh = 5*Iref	0.59V @ 50
0	1	60 ohms	Rr = 475 1% Iref=2.32mA	Ioh = 6*Iref	0.85V @ 60
0	1	50 ohms	Rr = 475 1%, Iref=2.32mA	Ioh = 6*Iref	0.70V @ 50
1	0	60 ohms	Rr = 475 1%, Iref=2.32mA	Ioh = 4*Iref	0.56V @ 60
1	0	50 ohms	Rr = 475 1%, Iref=2.32mA	Ioh = 4*Iref	0.47V @ 50
1	1	60 ohms	Rr = 475 1%, Iref=2.32mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 ohms	Rr = 475 1%, Iref=2.32mA	Ioh = 7*Iref	0.82V @ 50

Note: The entries in boldface are the primary system configurations of interest. The outputs should be optimized for these configurations.

6.3 Spread Spectrum Clocking (SSC) Criteria:

Spread Spectrum functionality on the CK00 class of clock drivers is required and acts as an on/off switch for different forms of spread spectrum modulation techniques. Any given system design may or may not use this feature due to platform-level timing issues. The following specifications are included in the current CK00 definition:

1. No external modulation frequency source is required
2. Vendor needs to synchronously modulate the Host, PCI, 3V66, and CPU/2 output clocks. REF and fixed frequency 48MHz clock outputs are not modulated.
3. All device timings (including jitter, skew, min-max clock period, output rise/fall time) MUST meet the existing non-spread spectrum specifications
4. All non-spread Host and PCI functionality must be maintained in the spread spectrum mode (includes all power management functions.)
5. The minimum clock period cannot be violated. The preferred method is to adjust the spread technique to not allow for modulation above the nominal frequency. This technique is often called “down-spreading”. An example triangular frequency modulation profile is shown in Figure 5. The modulation profile in a modulation period can be expressed as:

$$f = \begin{cases} (1-\delta) f_{nom} + 2 f_m \cdot \delta \cdot f_{nom} \cdot t & when \quad 0 < t < \dfrac{1}{2 f_m}; \\ (1+\delta) f_{nom} - 2 f_m \cdot \delta \cdot f_{nom} \cdot t & when \quad \dfrac{1}{2 f_m} < t < \dfrac{1}{f_m}, \end{cases}$$

where f_{nom} is the nominal frequency in the non-SSC mode, f_m is the modulation frequency, δ is the modulation amount, and t is time.

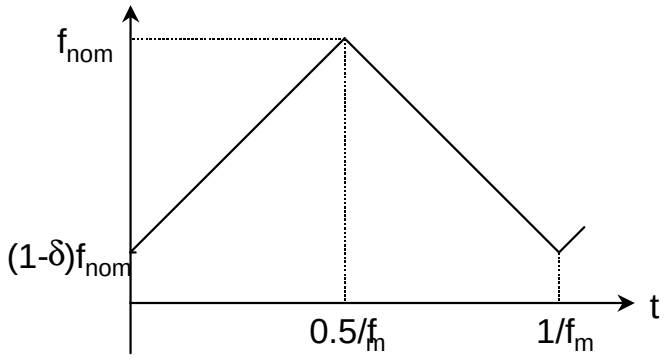


Figure 5 Triangular Frequency Modulation Profile.

6. For triangular modulation, the clock frequency deviation (δ) is required to be no more than 0.6% “down-spread” from the corresponding nominal frequency, i.e., +0%/-0.6%. The absolute spread amount at the fundamental frequency is shown in Figure 6, as the width of its spectral distribution (between the -3dB roll-off). The ratio of this width to the fundamental frequency cannot exceed 0.6%. This parameter can be measured in the frequency domain using a spectrum analyzer. The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream PLL tracking skew (see explanation in 8), which cannot exceed that of a 0.6% triangular modulation. Typically, it is about 0.5%.

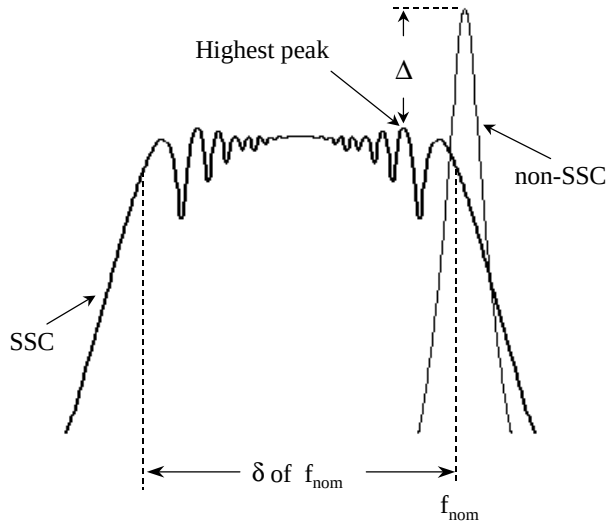


Figure 6 Spectral Fundamental Frequency Comparison

7. To achieved sufficient system-level EMI reduction, it is desired that SSC reduce the spectral peaks in the non-SSC mode by the amount specified in Table 4. The peak reduction Δ is defined, as shown in Figure 6, as the difference between the spectral peaks in SSC and non-SSC modes at the specified measurement frequency

Table 4 Desired Peak Amplitude Reduction by SSC.

CPU Clock Freq.	Peak Reduction Δ	Measurement Freq.
133 MHz	7 dB	666 MHz (5th harmonics)
100 MHz	7 dB	700 MHz (7th harmonics)

Notes:

a) The spectral peak reduction is not necessarily the same as the system EMI reduction. However, this relative measurement gives the component-level indication of SSC's EMI reduction capability at the system level.

b) It is recommended that a spectrum analyzer be used for this measurement. The spectrum analyzer should have measurement capability out to 1 GHz. The measured SSC clock needs to be fed into the spectrum analyzer via a high-impedance probe compatible with the spectrum analyzer. The output clock should be loaded with 20 pF capacitance. The resolution bandwidth of the spectrum analyzer needs to be set at 120 KHz to comply with FCC EMI measurement requirements. The video band needs to be set at higher than 300 KHz for appropriate display. 100 KHz may be used as the resolution bandwidth in case of measurement equipment limitation. The display should be set with maximum hold. The corresponding harmonic peak readings should be recorded in both the non-SSC and the SSC modes, and be compared to determine the magnitude of the spectral peak reduction.

8. The modulation frequency of SSC is required to be in the range of 30-33 KHz to avoid audio band demodulation and to minimize system timing skew. The downstream PLL tracking skew, i.e., the accumulative phase difference between the downstream PLL input and

output clocks, is shown in Figure 7, as functions of modulation frequency, modulation profile, and spread amount. This plot is obtained through PLL behavior simulations assuming a jitter-free ideal modulated input clock to the PLL. The parameters of the simulated PLL are:

(VCO gain) * (charge-pump current) = 2800 (Hz/V)(A),
feedback divider =2, 2nd-order filter: C_1 = 11 pF; C2 = 356 pF; R = 9.75 kΩ.

9. This skew should be minimized, as it reduces system timing margins. Different system implementations have different requirements and PLL characteristics, and may require tighter or looser skew. It is always true that a lower modulation frequency results in smaller tracking skew. The skew is proportional to the amount of spreading. **Any implemented modulation profile must induce less than 110 pS skew with the above PLL parameters by properly adjusting its spread amount. Sinusoidal modulation is strongly not recommended due to its low peak reduction capability.**

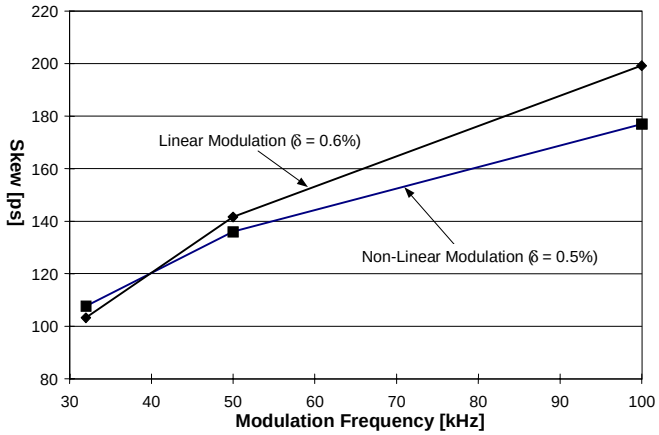


Figure 7 Downstream PLL tracking skew and modulation frequency

6.4 Non-production Frequencies for System Debug

Some system debug applications exist where CPU frequencies that are above and below the specified 100, 133 MHz are of interest for this device. The ability to use this device in a lab environment using a 10 or 20 MHz crystal is desired. Another desired feature of this product is the ability to use a function generator (in lab environment only) to drive XTAL_IN (float XTAL_OUT) in test mode to create the frequencies shown in the selection table for Test Mode.

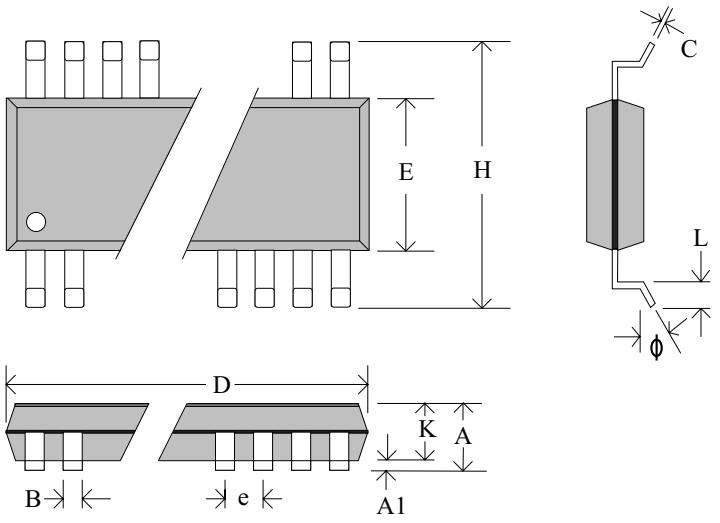
6.5 PWRDWN# Mode

When PWRDWN# is asserted, a voltage must be held across the differential outputs.

PWRDWN#	**Host / Host_bar**	**Mref / Mref_b**	**3V66**	**PCI**	**48MHz**	**Ref**	**14.318, 66 seeds**	
Asserted = 0 = low	Host = 2*Iref Host_bar = undriven	Low	Low	Low	Low	Low	Low (if applicable)	

There are no specific timing requirements for entering or exiting PWRDWN# mode.

6.6 Package Data



56 SSOP: Table of Dimensions (**inches**, unless otherwise specified)

Body		Symbol										
		E	H	C	L	ϕ	D	K	A	A1	e	B
56	Min	0.291	0.395	0.009	0.020	0°	0.720	-	0.095	0.008	0.025	0.008
(300mil)	Max	0.299	0.420	0.013	0.040	8°	0.730	-	0.110	0.016		0.012

48 SSOP: Table of Dimensions (**inches**, unless otherwise specified)

Body		Symbol										
		E	H	C	L	ϕ	D	K	A	A1	e	B
48	Min	0.291	0.395	0.009	0.020	0°	0.620	-	0.095	0.008	0.025	0.008
(300mil)	Max	0.299	0.420	0.013	0.040	8°	0.630	-	0.110	0.016		0.012

56 TSSOP: Table of Dimensions (**mm**, unless otherwise specified)

Body		Symbol							
		Body Size	Body Length	Lead Pitch	Tip to Tip	Body Thck	Stand off	Overall Height	JEDEC
56pin	Nom	6.1	14.0	0.50	8.1	0.90	0.10	1.00	MO-153

56 TSSOP: Table of Dimensions (**mm**, unless otherwise specified)

Body		Symbol							
		Body Size	Body Length	Lead Pitch	Tip to Tip	Body Thck	Stand off	Overall Height	JEDEC
56pin	Nom	6.1	12.5	0.50	8.1	0.90	0.10	1.00	MO-153

6.7 Defined option for PCI_bankSTOP# functionality

For the SKS and RGR clock devices, an option should be included such that the Spread# pin would be replaced by a PCI_bankSTOP# pin which will shut off (hold LOW) the top five PCI clocks (pins 8,9,11,12,14 for the SKS and pins 6,7,9,10,12 for the RGR). The PCI_bankSTOP# pin should be active LOW. In a system where PCI_bankSTOP# is implemented, spread spectrum will be defaulted to ON.

6.8 I^2C Considerations

I^2C has been chosen as the serial bus interface to control these clock drivers. I^2C was chosen to support the JEDEC proposal JC-42.5 168 Pin Unbuffered SDRAM DIMM. All vendors are required to determine the legal issues associated with the manufacture of I^2C devices.

1) Address assignment: Any clock driver in this specification can use the single, 7 bit address shown below. All devices can use the address if only one master clock driver is used in a system.

The following address was confirmed by Philips on 09/04/96.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	0	1	0

Note: The R/W# bit is used by the I2C controller as a data direction bit. A 'zero' indicates a transmission (WRITE) to the clock device. A 'one' indicates a request for data (READ) from the clock driver. Since the definition of the clock buffer only allows the controller to WRITE data; the R/W# bit of the address will always be seen as a 'zero.' Optimal address decoding of this bit is left to the vendor.

2) Slave/Receiver: The clock driver is assumed to require only slave/receiver functionality. Slave/transmitter functionality is optional.

3) Data Transfer Rate: 100 kbits/s (standard mode) is the base functionality required. Fast mode (400 kbits/s) functionality is optional.

4) Logic Levels: I^2C logic levels are based on a percentage of VDD for the controller and other devices on the bus. Assume all devices are based on a 3.3 Volt supply.

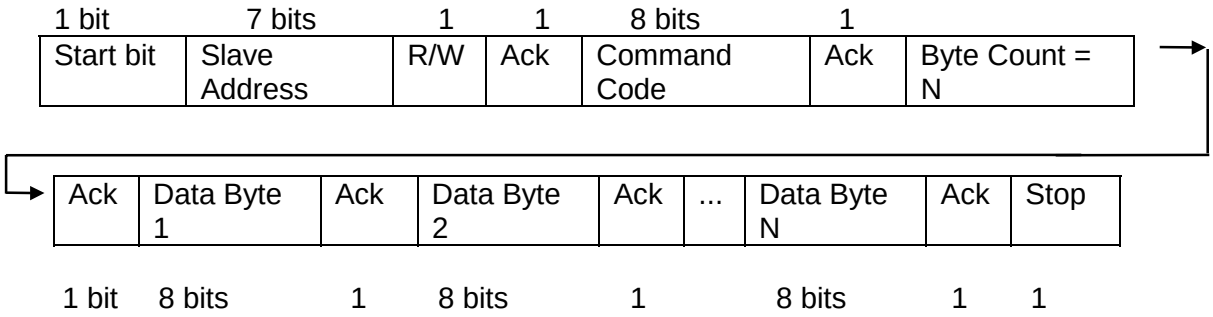
5) Data Byte Format: Byte format is 8 Bits as described in the following appendices.

6) Data Protocol:
To simplify the clock I^2C interface, the clock driver serial protocol was specified to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been

transferred. Indexed bytes are not allowed. However, the Intel controller has a more specific format than the generic I^2C protocol.

The clock driver must meet this protocol which is more rigorous than previously stated I^2C protocol. Treat the description from the viewpoint of controller. The controller "writes" to the clock driver and if possible would "read" from the clock driver (the clock driver is a slave/receiver only and is incapable of this transaction.)

"The block write begins with a slave address and a write condition. After the command code the host (controller) issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to transfer a maximum of 32 data bytes."



Note: The acknowledgment bit is returned by the slave/receiver (the clock driver).

Consider the command code and the byte count bytes required as the first two bytes of any transfer. The command code is software programmable via the controller, but will be specified as 0000 0000 in the clock specification. The byte count byte is the number of additional bytes required for the transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement.

For example:

Byte count byte	Notes:
MSB LSB	
0 0 0 0 0 0 0 0	Not allowed. Must have at least one byte.
0 0 0 0 0 0 0 1	Data for functional and frequency select register (currently byte 0 in spec)
0 0 0 0 0 0 1 0	Reads first two bytes of data. (byte 0 then byte 1)
0 0 0 0 0 0 1 1	Reads first three bytes (byte 0, 1, 2 in order)
0 0 0 0 0 1 0 0	Reads first four bytes (byte 0, 1, 2, 3 in order)
0 0 0 0 0 1 0 1	Reads first five bytes (byte 0, 1, 2, 3, 4 in order)
0 0 0 0 0 1 1 0	Reads first six bytes (byte 0, 1, 2, 3, 4, 5 in order)
0 0 0 0 0 1 1 1	Reads first seven bytes (byte 0, 1, 2, 3, 4, 5, 6 in order)
0 0 1 0 0 0 0 0	Max byte count supported = 32

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The serial controller interface can be simplified by discarding the information in both the command code and the byte count bytes and simply reading all the bytes that are sent to the clock driver after being addressed by the controller. It is expected that the controller will not provide more bytes than the clock driver can handle. A clock vendor may choose to discard any number of bytes that exceed the defined byte count.

8) Clock Stretching: The clock device must not hold/stretch the SCLOCK or SDATA lines low for more than 10 mS. Clock stretching is discouraged and should only be used as a last resort. Stretching the clock/data lines for longer than this time puts the device in an error/time-out mode and may not be supported in all platforms. It is assumed that all data transfers can be completed as specified without the use of clock/data stretching.

9) General Call: It is assumed that the clock driver will not have to respond to the "general call."

10) Electrical Characteristics: All electrical characteristics must meet the standard mode specifications found in section 15 of the I^2C specification.

a) Pull-Up Resistors: Any internal resistor pull-ups on the SDATA and SCLOCK inputs must be stated in the individual datasheet. The use of internal pull-ups on these pins of below 100K is discouraged. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5 - 6K Ohm range. Assume one I^2C device per DIMM (serial presence detect), one I^2C controller, one clock driver plus one/two more I^2C devices on the platform for capacitive loading purposes.

b) Input Glitch Filters: Only fast mode I^2C devices require input glitch filters to suppress bus noise. The clock driver is specified as a standard mode device and is not required to support this feature. However, it is considered a good design practice to include the filters.

11) PWR_DWN#: If a clock driver is placed in PWR_DWN# mode, the SDATA and SCLK inputs must be Tri-Stated and the device must retain all programming information. Idd current due to the I^2C circuitry must be characterized and in the datasheet.

For specific I^2C information consult the Philips I^2C Peripherals Data Handbook ICI2 (1996)

6.9 I²C Byte Locations for CKFF

At power up all CKFF outputs should be enabled and active. The Sdata and Sclock inputs should both have internal pull-up resistors with values above 100K Ohms for complete platform flexibility.

CKFF Serial Configuration Map

A) The serial bits will be read by the clock driver in the following order:
Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0
Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0
.
Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

B) All unused register bits (reserved and N/A) should be designed as don't care. It is expected that the controller will force all of these bits to a "0" level.

C) All register bits labeled "Initialize to 0" must be written to zero during initialization. Failure to do so may result in a higher then normal operating current. The controller will read back the last written value.

For the purposes of this section, the following labels are used to designate various outputs.

Output Type	CKFF Pin	Label
PCI	6	PCI0
PCI	7	PCI1
PCI	10	PCI2
PCI	11	PCI3
PCI	14	PCI4
PCI	15	PCI5
PCI	17	PCI6
PCI	18	PCI7
PCI	21	PCI8
PCI	22	PCI9
PCI	24	PCI10
PCI	25	PCI11
48MHz	36	48M0
48MHz	37	48M1
3V66	42	66M0
3V66	43	66M1
3V66	46	66M2
3V66	47	66M3
3V66	50	66M4
3V66	51	66M5
14.318MHz	54	14M0
14.318MHz	55	14M1

Byte 0 : CKFF Active/Inactive Register (1 = enable, 0 = disable)

Bit	Name	Description
Bit 7	PCI0	(Active/Inactive)
Bit 6	PCI1	(Active/Inactive)
Bit 5	PCI2	(Active/Inactive)
Bit 4	PCI3	(Active/Inactive)
Bit 3	PCI4	(Active/Inactive)
Bit 2	PCI5	(Active/Inactive)
Bit 1	PCI6	(Active/Inactive)
Bit 0	PCI7	(Active/Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation,

Byte 1 : CKFF Active/Inactive Register (1 = enable, 0 = disable)

Bit	Name	Description
Bit 7	PCI8	(Active/Inactive)
Bit 6	PCI9	(Active/Inactive)
Bit 5	PCI10	(Active/Inactive)
Bit 4	PCI11	(Active/Inactive)
Bit 3	48M0	(Active/Inactive)
Bit 2	48M1	(Active/Inactive)
Bit 1	14M0	(Active/Inactive)
Bit 0	14M1	(Active/Inactive)

Notes:

2. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation,

Byte 2 : CKFF Active/Inactive Register (1 = enable, 0 = disable)

Bit	Name	Description
Bit 7	66M0	(Active/Inactive)
Bit 6	66M1	(Active/Inactive)
Bit 5	66M2	(Active/Inactive)
Bit 4	66M3	(Active/Inactive)
Bit 3	66M4	(Active/Inactive)
Bit 2	66M5	(Active/Inactive)
Bit 1		(Reserved for Intel)
Bit 0		(Reserved for Intel)

Notes:

3. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation,

Byte 3 : CKFF Active/Inactive Register (1 = enable, 0 = disable)

Bit	Name	Description
Bit 7		(Reserved for Intel)
Bit 6		(Reserved for Intel)
Bit 5		(Reserved for Intel)
Bit 4		(Reserved for Intel)
Bit 3		(Reserved for Intel)
Bit 2		(Reserved for Intel)
Bit 1		(Reserved for Intel)
Bit 0		(Reserved for Intel)

Notes:

4. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation,

Byte 4 : CKFF Active/Inactive Register (1 = enable, 0 = disable)

Bit	Name	Description
Bit 7		(Reserved for clock supplier)
Bit 6		(Reserved for clock supplier)
Bit 5		(Reserved for clock supplier)
Bit 4		(Reserved for clock supplier)
Bit 3		(Reserved for clock supplier)
Bit 2		(Reserved for clock supplier)
Bit 1		(Reserved for clock supplier)
Bit 0		(Reserved for clock supplier)

Notes:

5. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation,

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