SC242 Connector Design Guidelines

August, 1998

Order Number: 243397-002

REVISION HISTORY

Date	Revision	Description
N/A	1.3	Sections 2.4 and 5.7.3: Changed weight from 250g to 400g. Changed nomenclature from processor substrate to S.E.C. cartridge. Added heat sink support mounting holes. Section 2.8.1: Added total insertion force of connector into motherboard. Section 2.8.2: Solder tail design and alignment added. Section 2.8.3: Contact backout wipe added. Section 2.9.0: Added keying feature. Section 2.9.2: Added heat sink support mounting holes. Section 2.9.3 and 2.9.4: Updated pad details to increase contact backout wipe. Section 3.1: Changed contact resistance from 5mΩ max rise per contact to 2mΩ max rise averaged over all 242 contacts. Section 3.3: Max pin self inductance from 6.0nH to 10.5nH. Section 4.18: Changed contact retention from 340g to 300g (min). Sections 4.19 and 5.9.3: Added max force on connector of 150lb. Sections 4.20 and 5.9.3: Added contact backout wipe of 0.99mm (0.039in).
5/6/97	1.4	Section 2.8.1: Clarification of requirements for retention clip and solder tail interaction during assembly. Section 2.9.0: Included additional critical to function dimensions. Sections 4.6 and 4.7: Clarification of steel gage vs. substrate. Section 4.13: Changed test procedure 53 to plating alternative (1) and 60 to plating option (2). Section 4.19: Added time duration of 30s, no movement > 0.076mm, temperature range from 15°C to 35°C.
8/15/97	1.5	Modified Revision History to highlight changes from revision 1.4 to 1.5. Added tables of board of approvals. Added “Notice for Re-Qualification” after the Revision History. Sections 2.5 and 2.6: Replaced PCB with Steel Gauge, Added Steel Gauge details and specification in the drawing form. Section 2.8.3: Removed Reference to detail B and section 2.9.4. Changed tilt tolerance from ±0.010 to 0.015 off the motherboard along short and long edges. Section 2.9: Added table of CTF dimensions. Section 2.9.0: Changed the upper tolerance on overall height of the connector. Also, changed bay lengths. Added flatness spec on top and bottom surfaces. Section 2.9.3: Drawings of primary side of substrate and detail A replaced with the drawings of S.E.C.C. showing primary side and detail A from the data sheet.

		Section 2.9.4: Secondary Side drawing shows only the contact pad pattern. Also, removed detail B showing detail around key-slot. Section 2.9.5: New section added on Critical To Function Dimensions. Section 3.1: Heading changed from "Contact Resistance" to Determination of Averaged Contact Resistance". Added description as well as sections on Bulk Contact Resistance (3.1.1), Initial Contact Resistance (3.1.2), Final Contact Resistance (3.1.3), and Voltage and Current Requirements (3.1.4). Section 3.3: Title changed from Pin Self Inductance to Effective Inductance. Section 3.3, 3.4 and 3.7: Added "Test Frequency of 20MHz". Section 4.3: Changed vibration spec from 9.0Grms, 15min/axis to 7.3Grms, 45min/axis. Section 4.6 and 4.7: Replaced "20° lead-in chamfer angle" with "70° chamfer angle". Also, added reference to **Section 2.5** for Steel Gauge. Section 4.7: Replaced "substrate" with "steel gauge" to maintain consistency with 4.6. Section 4.13: Added "Requirement: No evidence of any pores". Section 4.21: New section added on Visual Inspection of Substrate - Post Shock & Vibes. Section 5.9.3: Added two rows titled "CTF Dimensional Verification (2.9.5)" and Substrate Visual Inspection (4.21).
6/26/98	1.6	General: Changed all units to create uniformity. General: Removed all reference to MIL specifications from document. Removed section numbers 2.9.0, 2.9.1, 2.9.2, 2.9.3, 2.9.4, and 2.9.5; utilized figure numbers for each of the figures associated with the former section numbers. Combined Section 4.1.3 with Section 4.10. Removed Section 4.1.3. Section 4.3: Changed vibration spec from 7.3Grms, 45min/axis to 3.13Grms, 10min/axis and 2.2Grms, 45min/axis. Additionally, changed test frequency from '50Hz to 2000Hz' to '5Hz to 500Hz'. Added the Power Spectral Density (PSD) curved used for the vibration testing. Section 4.4: Changed the shock spec from 100G, 6ms duration, Sawtooth waveform to 50G, 11ms duration, Trapezoidal waveform. Section 4.10: Changed the temperature life spec from 500h to 240h (10 days). Removed Mixed Flow Gas section, formerly section 4.11. Section 5.1: Removed MIL-STD-1344A and MIL-STD-202F from the applicable documents list. Section 5.9.3: Changed Qualification Requirements Table, Test Group 1 from 8 samples to 16. Section 5.9.3: Qualification Requirements Table: Deleted Test Group 3 and

		Mixed Flow Gas to reflect the removal of Section 4.11, Mixed Flow Gas. Merged Sections 6.1.1 and 6.1.2 into Section 6.1. Merged Sections 7.1, 7.2, and 7.3 into Section 7. Section 7: Added "The test facility shall provide Intel and the supplier with the following document:" to complete the statement.
		Sections 3.1.2 and 3.1.3: Rephrased the requirements for contact resistance. Section 3.3: Changed Test Frequency from 20MHz to 10MHz, 100MHz, 500MHz, 1GHz, and 3GHz. Section 3.4: Changed Test Frequency from 20MHz to 1MHz, 10MHz, 100MHz, and 1GHz. Section 3.7: Changed Test Frequency from 20MHz to 100MHz, 500MHz, 1GHz, and 3GHz. Section 3.7: Added reference to Figure 11. Section 4.5: Re-worded the text; durability requirement remains unchanged. Reinstated Mixed Flow Gas Requirement as Section 4.11. Changed the test duration to 8 days total. Section 5.9.3: Qualification Requirements Table: Inserted new Test Group 3 and Mixed Flow Gas to reflect the re-instatement of Section 4.11. Section 5.9.3: Qualification Requirements Table: Moved Maximum Force on Contact and Contact Backout Wipe from Test Group 6 to Test Group 8. Re-ordered Test Group 8.
		Re-organized figures that were out of order. Section 3.7: Revised and separated impedance crosstalk coupling and propagation delay requirements. Section 4.3: Changed the frequency range for vibration because it was mis-labeled. Section 4.3: Figure 12, revised test duration data labels for clarity. Section 4.4: Re-worded shock pulse requirements to provide clarification.

Re-Qualification Notice to Connector Vendors

Any significant change to the connector will require submission of a detailed explanation of the change at least 60 days prior to the planned implementation. Intel will review the modification and establish the necessary re-qualification procedure that the connector must pass. Any testing that is required MUST be completed before the change is implemented.

Typical examples of significant changes include, **but are not limited to, the following:** Plastic material changes including base material or color; contact changes including base material, plating material or thickness; and design modifications.

For Details on qualification testing requirements, see **Section 5.**

SC242 Connector Design Guidelines

(Labeled “Slot 1” in prior revisions)

1. INTRODUCTION

This document defines a 242 contact, 1.0mm pitch, edge connector intended for high volume desktop systems based on Intel microprocessors using the Single Edge Contact (S.E.C.) cartridge, which houses a processor substrate. The connector must be low cost, low risk, robust, manufacturable, and multi-sourceable.

2. MECHANICAL REQUIREMENTS

2.1. Materials:

2.1.1. Connector Housing:

Thermoplastic, UL 94V-0 flame rating, temperature rating and design capable of withstanding reflow solder process.

Color:

Dark Brown - Pantone® 462U, 411C, 412C, or equivalent.

2.1.2. Markings:

2.1.2.1. Name:

SC242[1] (to be molded into both long sides of connector housing).

SC242 (Font type is Helvetica - 16 point Bold).

Manufacturer’s insignia (font size at supplier’s discretion).

This mark will be molded into both sides of the connector housing. Any requests for variation from this marking requires a written description (detailing size and location) to be provided to Intel for approval.

2.1.2.2. Lot Traceability:

Each header will be marked with a lot identification code that will allow traceability of all components, date of manufacture (year and week), and assembly location. This mark can be an ink mark, a heat stamp, or a laser mark, but must be able to withstand a temperature of 225°C for 40s (min). The mark must be placed on the side of the

[1] Connector housings from molds built prior to December 31, 1998 may be labeled “Slot 1” instead of “SC242”.

connector. In addition, this identification code must be marked on the exterior of the box in which the units ship.

2.1.3. Contacts:

A requirement of 100µin (min) tin lead over nickel underplate on solder tails, for all plating alternatives. The following two plating alternatives are listed to allow flexibility to connector suppliers. The absolute requirement is that the plating must meet the Qualification requirements listed in **Section 5.9**.

Alternative (1): High strength copper alloy; 15µin (min) gold plating over 50µin minimum nickel plating.

Alternative (2): High strength copper alloy, 2µin (min) gold flash over 15µin palladium-nickel over 50µin (min) nickel underplate in critical contact areas.

2.2. Number of contacts:

Total Number of Contacts: **242**

2.3. Connector Size:

The connector shall accept a processor substrate width of 127mm (5.000in), see **Figure 1**, **Figure 2**, and **Figure 3**. The connector housing shall be 132.87mm (5.231in) long, excluding the external polarization key which extends an additional 2.0mm (0.079in), see **Figure 4** and **Figure 5**.

2.4. Mechanical Supports:

The S.E.C. cartridge retention system is designed to support the S.E.C. cartridge and associated heat sink during the shock and vibration conditions outlined in **Section 4** [supported weights include: 250g (max) for the heat sink and 150g (max) for the remainder of the S.E.C. cartridge (max), for a total maximum weight of 400g]. An additional Heat Sink Support (HSS) is recommended to assist in the retention of the S.E.C. cartridge assembly during shock and vibration conditions, and to provide additional stability. The motherboard mounting holes for the S.E.C. cartridge retention system and the HSS are shown in **Figure 6**. The S.E.C. cartridge has a positive tactile response when complete substrate engagement is achieved. The S.E.C. cartridge retention system and manufacturing tolerances limit substrate backout to 0.99mm (0.039in) from the SC242 connector within the retention system.

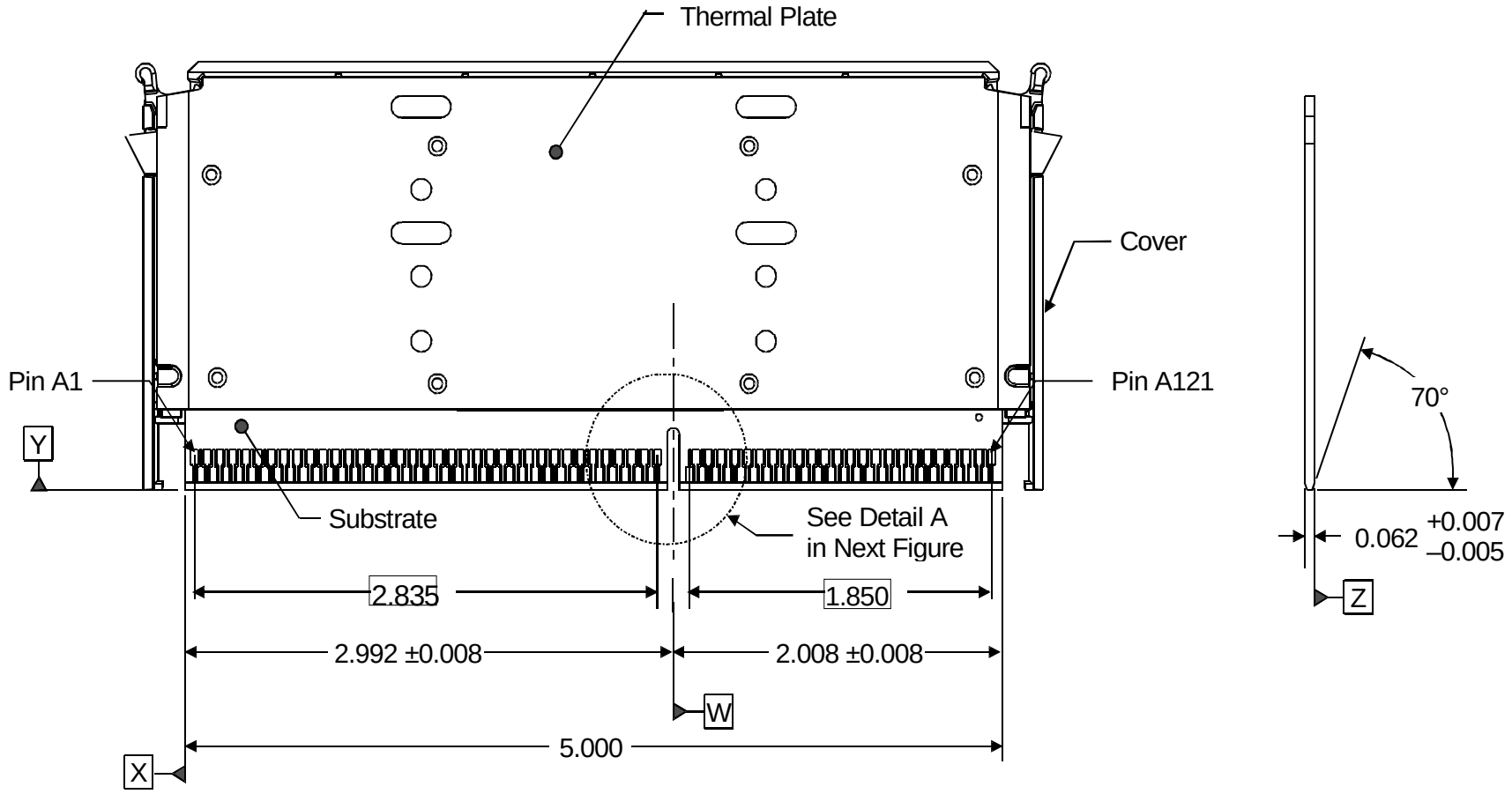
2.5. Insertion Force of Steel Gauge into SC242 Connector:

25lb (max). Applies only to the test conditions detailed in **Section 4.6**. See **Figure 7** for details and specifications of Steel Gauge.

2.6. Extraction Force of Steel Gauge from SC242 Connector:

15lb (max). See **Figure 7** for details and specifications of the Steel Gauge.

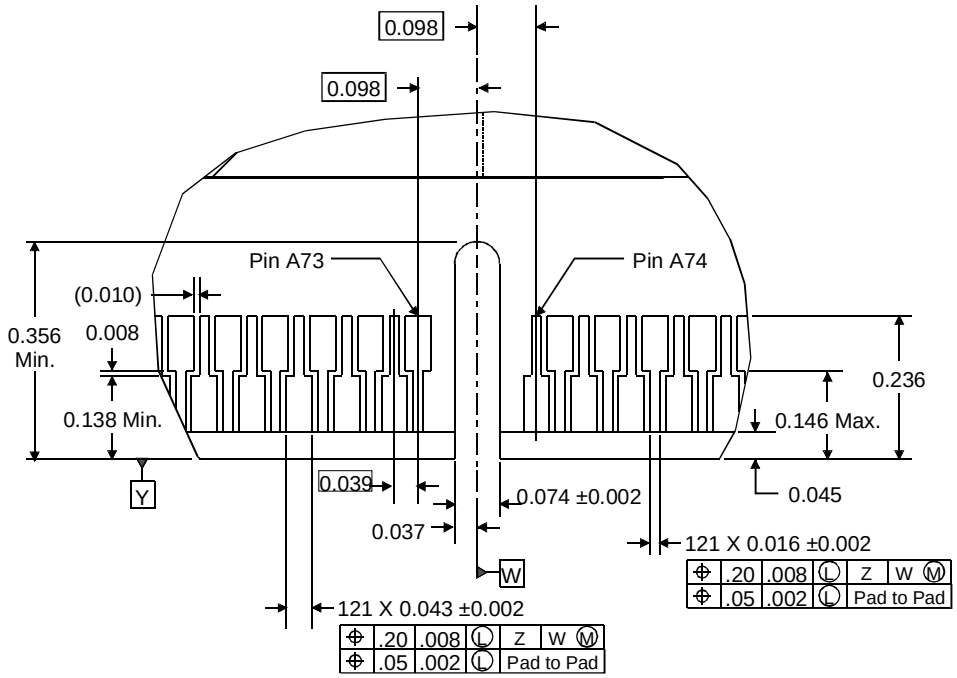
The following drawing is given for reference only. Please refer to the document number **243341** which contains the latest revision of the original drawing (Figure 11-9, page 11-10) titled S.E.C. Cartridge Substrate Dimensions (Skirt not shown for clarity.)



Note: All dimensions without tolerance information are considered reference dimensions only

Figure 1: Substrate Form Factor - Primary Side

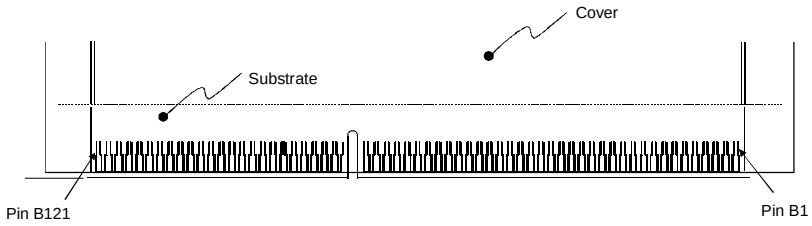
The following drawing is given for reference only. Please refer to document number **243341** which contains the latest revision of the original drawing (Figure 11-11, page 11-1) titled S.E.C. Cartridge substrate - Detail A.



Note: All dimensions without tolerance information are considered reference dimensions only

Figure 2: Enlargement of Substrate Form Factor - Primary Side

The contact pattern on the secondary side of the substrate is shown below. It is given for reference only. Please refer to document number **243341** which contains the latest revision of the original drawing (Figure 11-10, page 11-10) titled S.E.C. Cartridge Substrate Dimensions, Cover Side View.



Note: Cover not completely shown to allow for substrate details to be
This drawing show the pin details of the cover side of the S.E.C.

Figure 3: Substrate Form Factor - Secondary Side

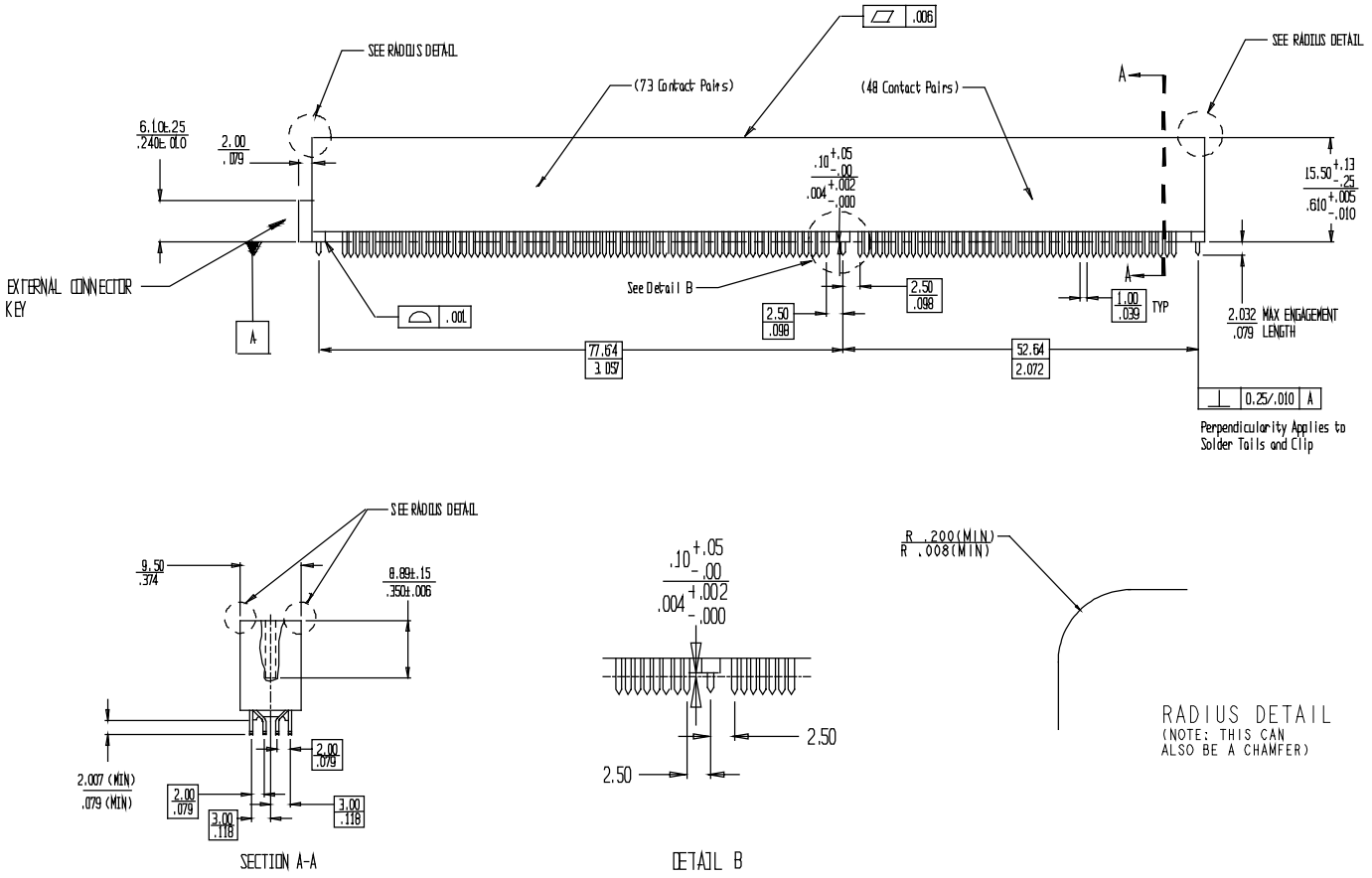


Figure 4: Connector Dimensions

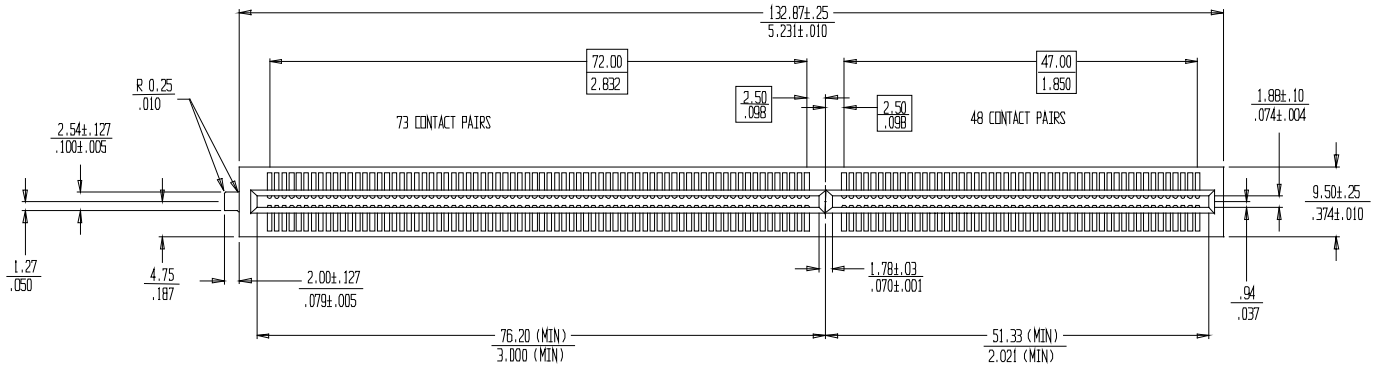


Figure 5: Connector Dimensions, con't.

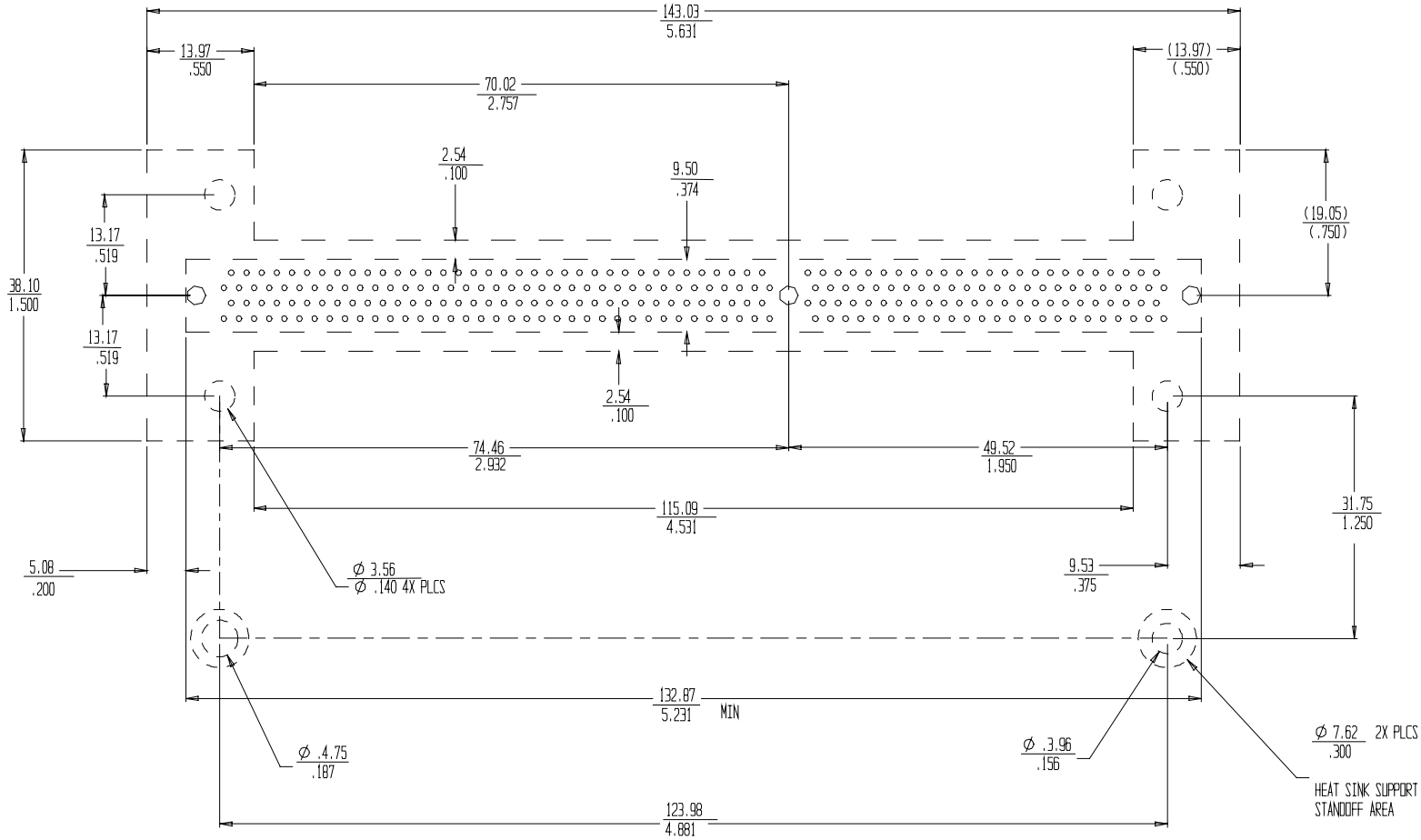


Figure 6: Mechanical Keep-Out Area Around Connector

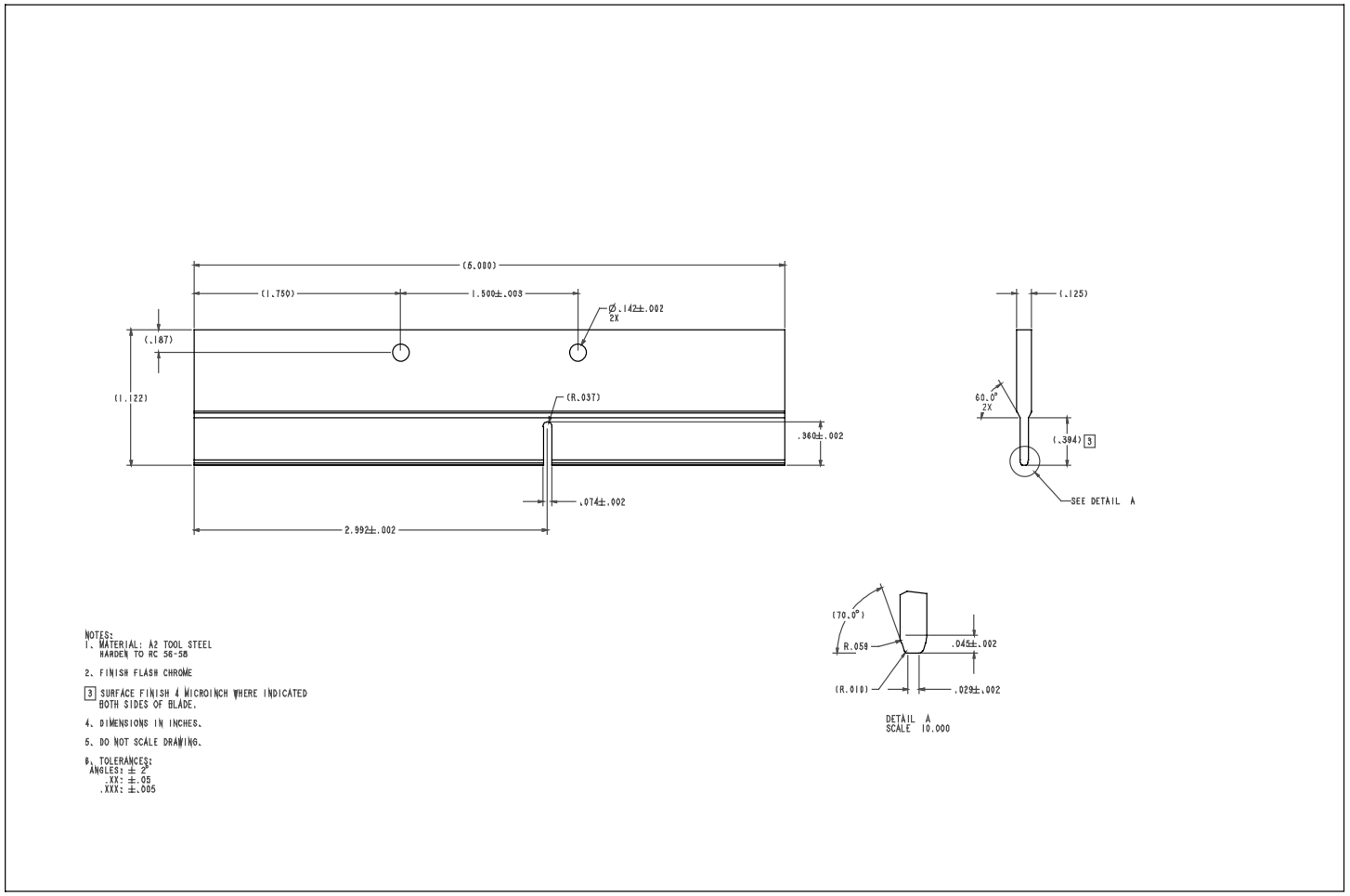


Figure 7: Steel Guage Details and Specifications

2.7. Durability:

The connector shall withstand a minimum of 50 insertion/withdrawal cycles with an S.E.C. cartridge.

2.8. Assembly Requirements to Motherboard:

2.8.1. Pre-Solder Attachment:

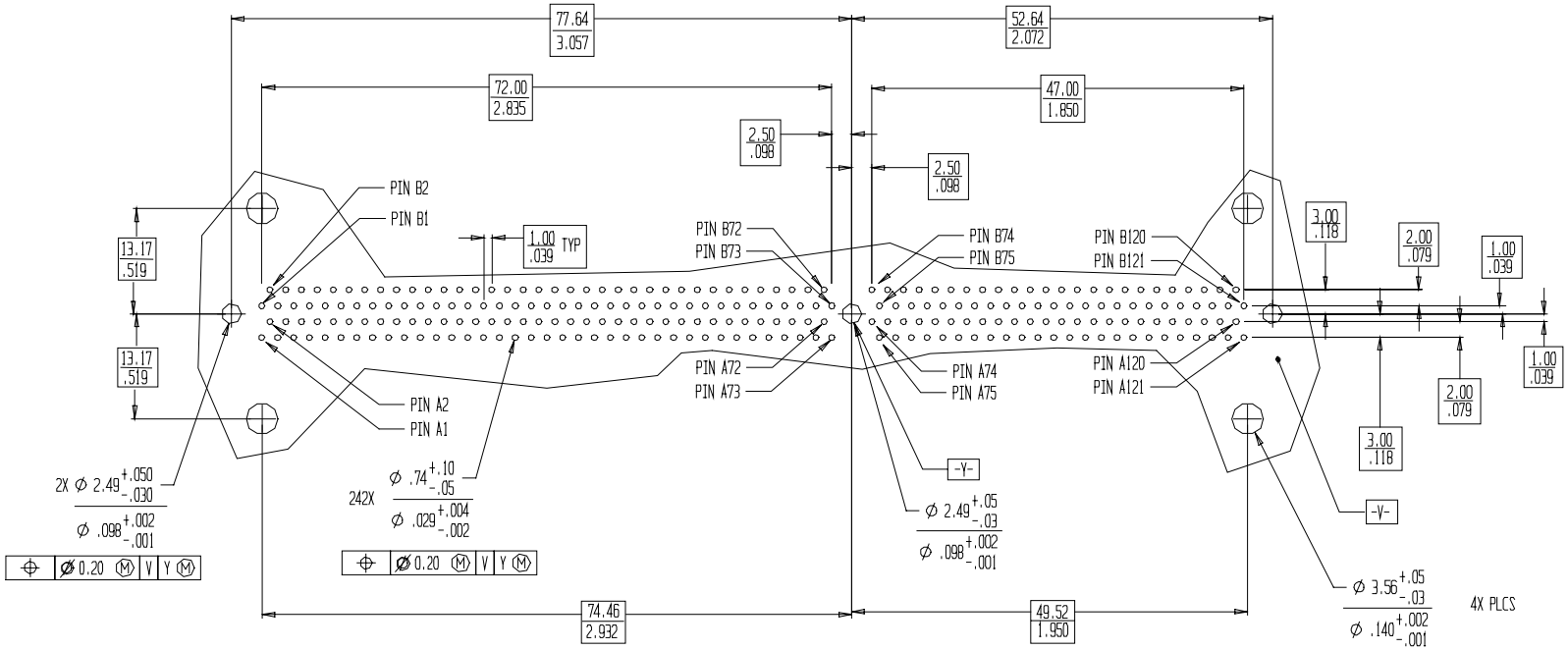
A method of fastening the connector to the motherboard is required to assist in the manufacturing process. The fastening method shall be consistent with low-cost, high-volume printed circuit board assembly lines. The recommended approach is to use three snap-in clips that require a total insertion force of 3lb to 15lb to install the SC242 connector into the motherboard. The clip length can be longer than the solder tail pins for purposes of alignment, but must not interfere with or misdirect the alignment and penetration of the solder tails into the motherboard during the assembly process.

2.8.2. Solder Tail Design and Alignment:

The connector solder tails must be designed and aligned such that the end of the solder tails must enter a virtual condition hole that is 0.48mm (0.019in) in diameter. The virtual condition solder tail holes result from the true positional tolerance dimensions specified in the motherboard layout shown in **Figure 6** and **Figure 8.** The solder tails and retention clips must not bind when inserted into the motherboard layout. The solder tails and clips have a 0.25mm (0.010in) perpendicularity requirement with respect to Datum A, see **Figure 4**.

2.8.3. Contact Backout Wipe:

The minimum contact backout wipe within the connector for the upper and lower contacts on the gold finger pads shown in details “A” in **Figure 2** is 0.99mm (0.039in). The purpose of this requirement is to allow for assembly and manufacturing tolerances in the S.E.C. cartridge retention system, as outlined in **Section 2.4.** Included in the tolerances mentioned above, is a SC242 manufacturing assembly tilt tolerance of 0.375mm (0.015in) maximum above the motherboard along both the short and long sides of the connector. This results in a post assembly parallelism of 0.51mm (0.020inches) between the SC242 connector Datum A (**Figure 4** and **Figure 5**) and the motherboard.



Recommended clearances around 3.56 mm DIA (0.140 inch DIA) mounting Holes:

7.62 mm DIA (0.300 inch DIA) trace keepout - all external layers

6.35 mm DIA (0.250 inch DIA) trace keepout - all internal layers

Note: Conversion from Metric to English units rounded to 3 significant digits

Figure 8: Connector Motherboard Layout

2.9. Connector Drawings:

The SC242 connector shall hold the processor substrate at right angles to the motherboard. All dimensions are in metric. Dimensions in inches are shown for reference only. The connector must accommodate a 1.57mm + 0.18mm / - 0.13mm (0.062in + 0.007in / - 0.005in) thick processor substrate (see **Figure 1**, **Figure 2**, and **Figure 3**). The upper outer edges of the connector housing must include a minimum radius (radius shown) or chamfer as shown in **Figure 4** and **Figure 5**. The connector key width dimension of 1.78mm (0.070in) is measured prior to the draft. (All dimensions are measured prior to draft unless otherwise specified.) The purpose of the internal key is to properly align the S.E.C. substrate within the SC242 connector, and to prevent the cartridge from being inserted backwards (rotated 180 degrees) into the connector.

There is an additional external key on one end of the connector (see **Figure 4** and **Figure 5**) that works in conjunction with an internal key within the S.E.C. cartridge retention mechanism. This keying scheme prevents improper installation of the S.E.C. cartridge retention mechanism to the motherboard.

Critical to function dimensions are identified in **Figure 9**. Each of the dimensions must meet the requirements given below. Note that dimensions B and D are measured at the bottom of card cavity as shown in **Figure 9**.

Dimension	Minimum (inch)	Maximum (inch)
A	0.070	0.078
B	1.9855	N/A
C	0.069	0.071
D	2.9645	N/A
E	0.095	0.105
F	5.221	5.241
G	0.344	0.356
H	0.364	0.384
J	0.600	0.615

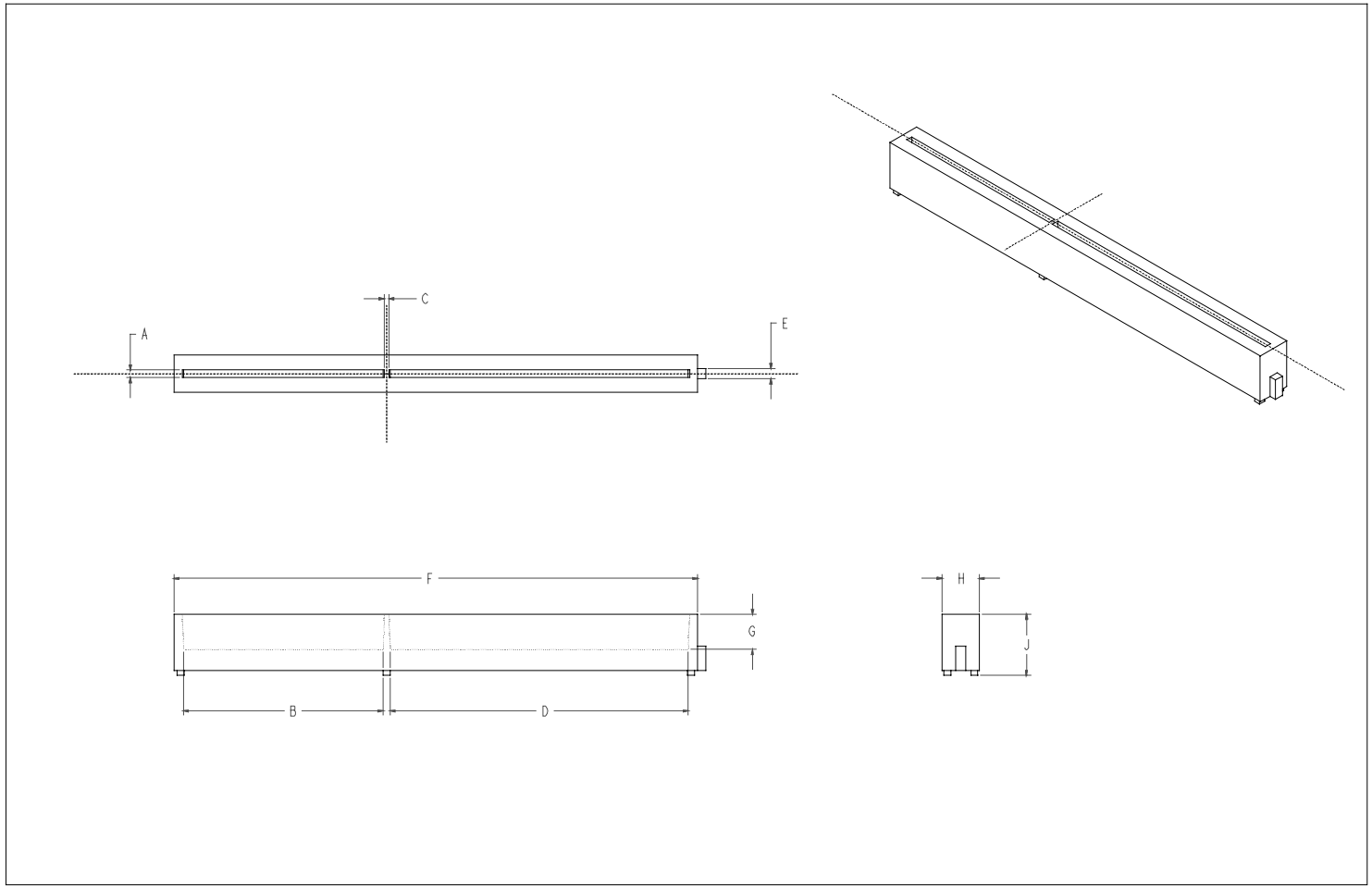


Figure 9: Critical To Function Dimensions

3. ELECTRICAL REQUIREMENTS

3.1. Determination of Averaged Contact Resistance:

Measure Total Contact Resistance $\mathbf{R_{AB}}$ for each of the 242 contacts.

Measure Bulk Contact Resistance $\mathbf{R_{AC}}$ for each of 121 lower contacts.

Determine Contact Resistance for each of the 242 contacts using either

$\mathbf{R_{CB} = R_{AB}}$ for upper contacts or

$\mathbf{R_{CB} = R_{AB} - R_{AC}}$ for lower contacts.

To determine Average Contact Resistance, sum up $\mathbf{R_{CB}}$ for all contacts and divide by the number of contacts. That is, for SC242 connector:

$$\mathbf{R_{averaged} = (\sum R_{CB})/242}$$

3.1.1. Bulk Resistance:

It is the resistance of the thin pad connecting a common bus and the lower contact pad on the mating substrate. Bulk Resistance is measured between point **A** on a common bus and point **C** at the junction of the thin pad and the contact pad as shown in the **Figure 10**.

3.1.2. Initial Contact Resistance:

There are three requirements: (a) Initial contact resistance averaged over 242 contacts not to exceed 10mΩ. (b) No pin can exceed the initial contact resistance of 500mΩ. (c) No more than one pin can exceed the initial contact resistance of 50mΩ.

3.1.3. Final Contact Resistance:

There are three requirements: (a) Final contact resistance averaged over 242 contacts not to exceed 12mΩ. (b) No pin can exceed the final contact resistance of 500mΩ. (c) No more than one pin can exceed the initial contact resistance of 50mΩ.

3.1.4. Test Voltage & Current Rating:

Test to be performed at 1.0A per contact. Voltage can vary to a maximum of 5.0V during test to attain 1.0A.

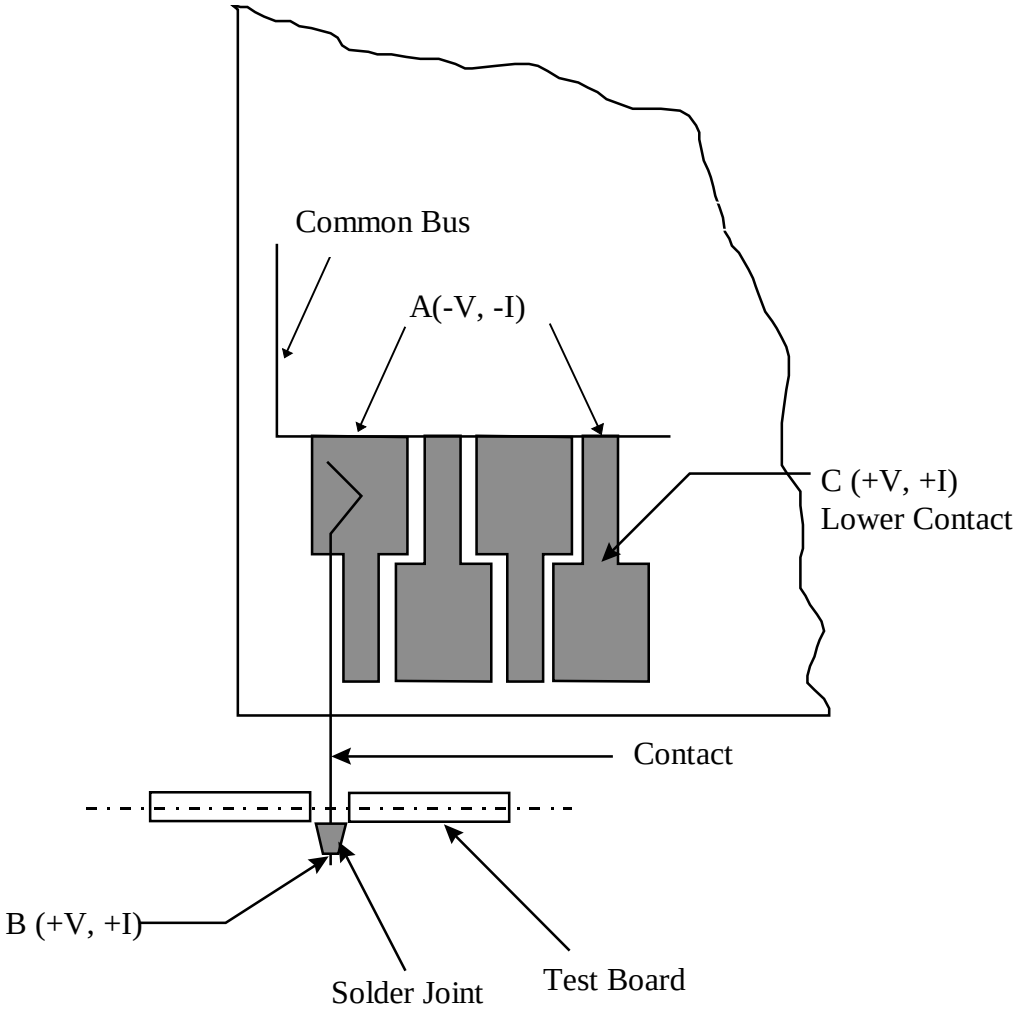


Figure 10: Electrical Testing Schematic

3.2. Contact Current Rating:

1.0A/contact.

3.3. Effective Inductance:

10.5nH (max). Measured between two adjacent pins which have their solder tails shorted together (using a shorting bar or other mechanism), probed at a location within 0.25mm (0.010in) from the top of the contact area. Test frequencies: 10MHz, 100MHz, 500MHz, and 1GHz.

3.4. Pin to Pin Capacitance:

2pF (max) at each of the test frequencies: 1MHz, 10MHz, 100MHz, and 1GHz. Measured between two adjacent pins that are not shorted together, probed at a location within 0.25mm (0.010in) from the top of the contact area.

3.5. Pin to Pin Insulation Resistance:

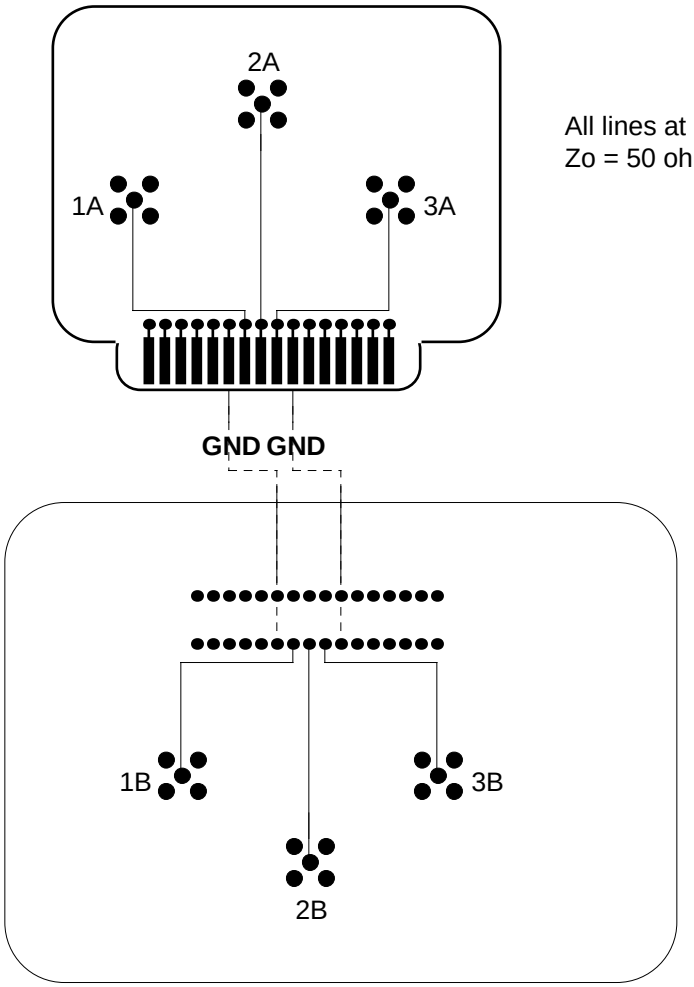
800MΩ (min), as measured per EIA 364, Test Procedure 21.

3.6. Dielectric Withstand Voltage:

400Vac per EIA 364, Test Procedure 20.

3.7. Characteristic Impedance, Propagation, and Crosstalk Coupling:

35Ω < Zo < 80Ω, Delay < 150ps, Crosstalk Coupling < 10%, using the TDR measurements described in **Sections 3.7.1** and **3.7.2**. For propagation delay measurement, the assumed rise time shall not exceed 80ps with an edge rate (10% - 90%) incident at the connector. Use a test rise time of 1ns with an edge rate (10% - 90%) for characteristic impedance and crosstalk coupling measurements. Instead of TDR, the Network Analyzer can be used to measure characteristic impedance at test frequencies of: 100MHz, 500MHz, and 1GHz. The test structure for connector impedance, propagation delay, and crosstalk measurements is shown in **Figure 11**.



All lines at same length (+/- 0.1 in),
Zo = 50 ohms, +/- 5%

Figure 11: Test Structure

3.7.1. Impedance and Propagation delay

Measurement Conditions (see Figure 11):

TDR/TDT measurement (or equivalent technique)

Signal:ground ratio = 3:1

Test board Zo = 50Ω ± 5%

Connector delay measured from substrate via to motherboard via (substrate via to be within 0.25mm (0.010in) of the top of the edge finger).

Measurements made on each line while others floating.

Zo: 35Ω ≤ Zo ≤ 80Ω **Delay: Tpd < 150ps**

3.7.2. Crosstalk

Measurement Conditions (see Section 3.7.1):

TDR/TDT measurement (or equivalent technique)

Signal driven into line 1, response measured on line 2

Magnitude:

Coupled voltage ≤ 10% of input voltage

4. ENVIRONMENTAL REQUIREMENTS

Design, including materials, shall be consistent with the manufacture of units that meet the following environmental reference points.

4.1. Temperature Range:

4.1.1. Operating:

0ºC to +85ºC.

4.1.2. Shipping and Storage:

-40ºC to + 105ºC.

4.2. Visual Inspection:

Connector must meet mechanical requirements as specified in **Section 2.**

4.3. Vibration, Random:

Frequency Range: 5Hz to 500Hz

Vibration test to be performed for two durations:

Duration 1: 10min/axis (derived from Intel Corporation customary board vibration specifications).
Power Spectral Density (PSD) Profile: 3.13GRMS.

Figure 12 presents the PSD curves used for the vibration testing.
Sample Size: 4 for contact resistance, 4 for electrical discontinuity.

Duration 2: 45min/axis for long term reliability from fretting corrosion perspective (10min test PSD reduced by S-N factor for extended time).
PSD Profile: 2.2GRMS.

Figure 12 presents the PSD curves used for the vibration testing.
Sample Size: 4 for contact resistance, 4 for electrical discontinuity

Axes Orientation: Schematic of X, Y and Z axes orientation in connector/SECC assembly is shown in **Figure 13**.
Input Accelerometer Location: Input (Control) accelerometer to be mounted on the vibration table.
Connector to be mounted to ATX motherboard. The layout details of the ATX motherboard are shown in **Figure 14**. The motherboard thickness is 0.062in + 0.008in / - 0.005in.

Connector must meet all the electrical contact resistance requirements following random vibration test. No electrical discontinuities > 1.0µs. The connector must be mated with the mechanical sample outlined in **Section 5.7.3** and retained with mechanical supports outlined in **Section 2.4**.

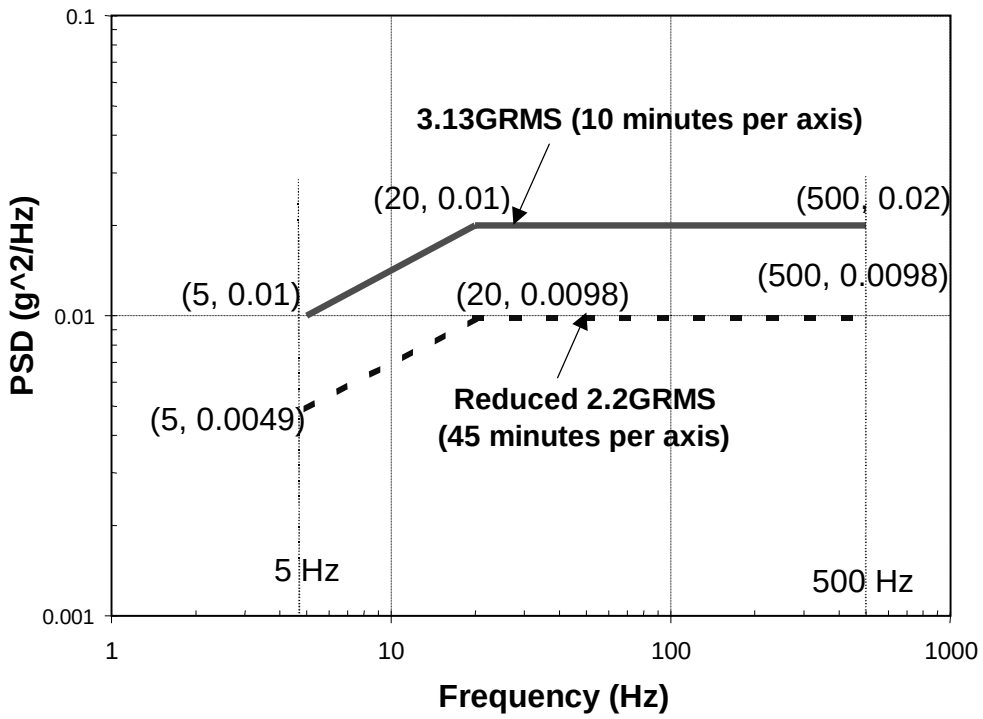


Figure 12: Power Spectral Density Curve

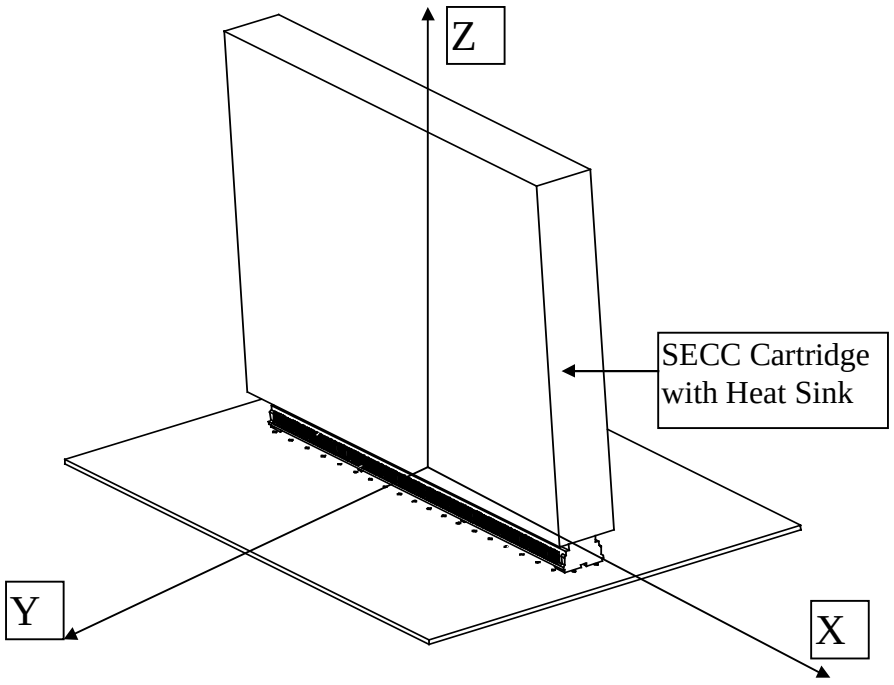


Figure 13: Schematic of Axes Orientation for Vibration Test

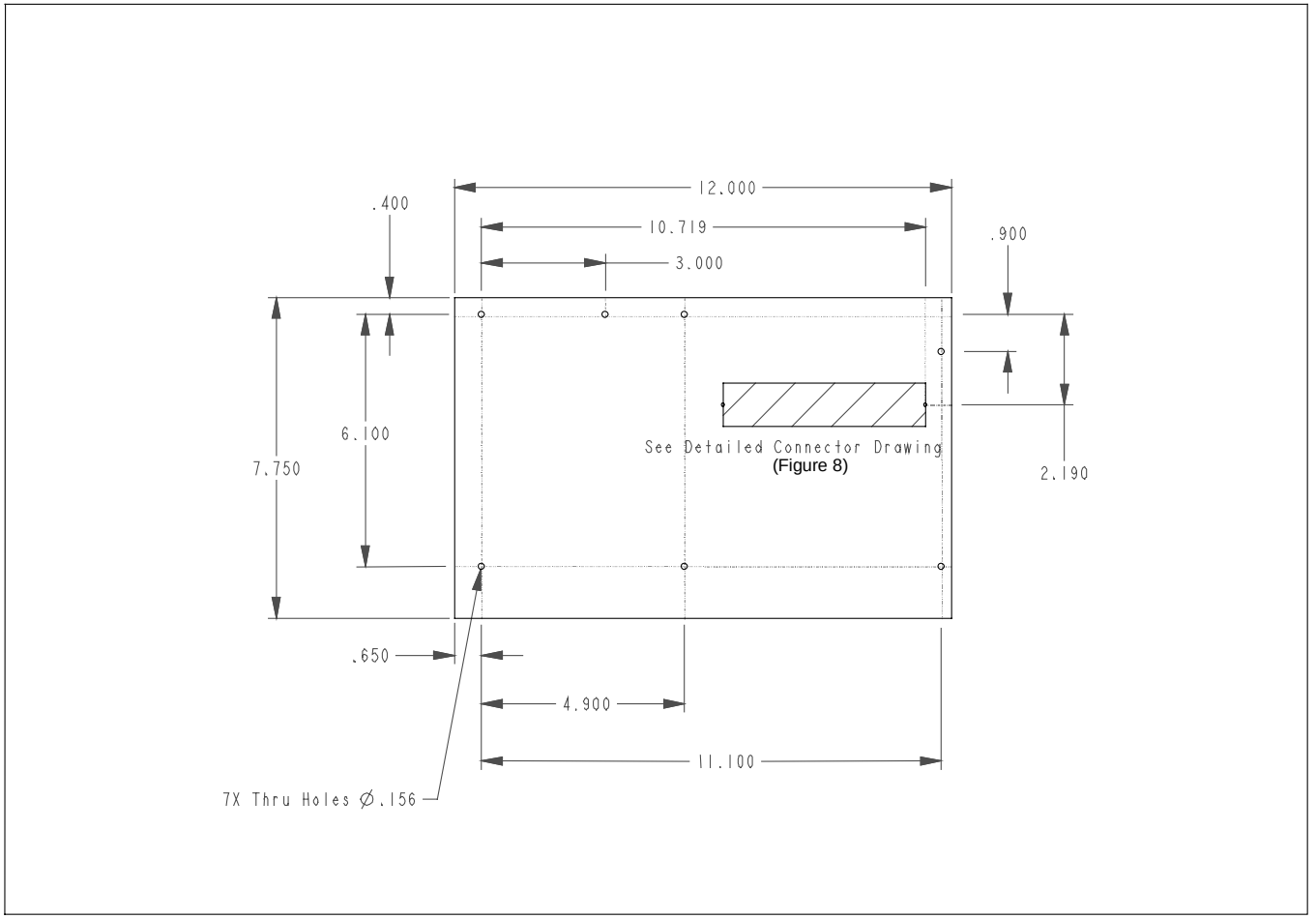


Figure 14: ATX Motherboard Layout Details

4.4. Shock:

Tested at 50G, 11ms duration, Trapezoidal waveform. Three shocks applied in each of three perpendicular axes (18 total). No electrical discontinuities > 1.0µs. The connector must be mated with the mechanical sample outlined in **Section 5.7.3** and retained with mechanical supports outlined in **Section 2.4**. The total minimum velocity change shall be 170in/s. **Figure 15** provides the schematic for this requirement.

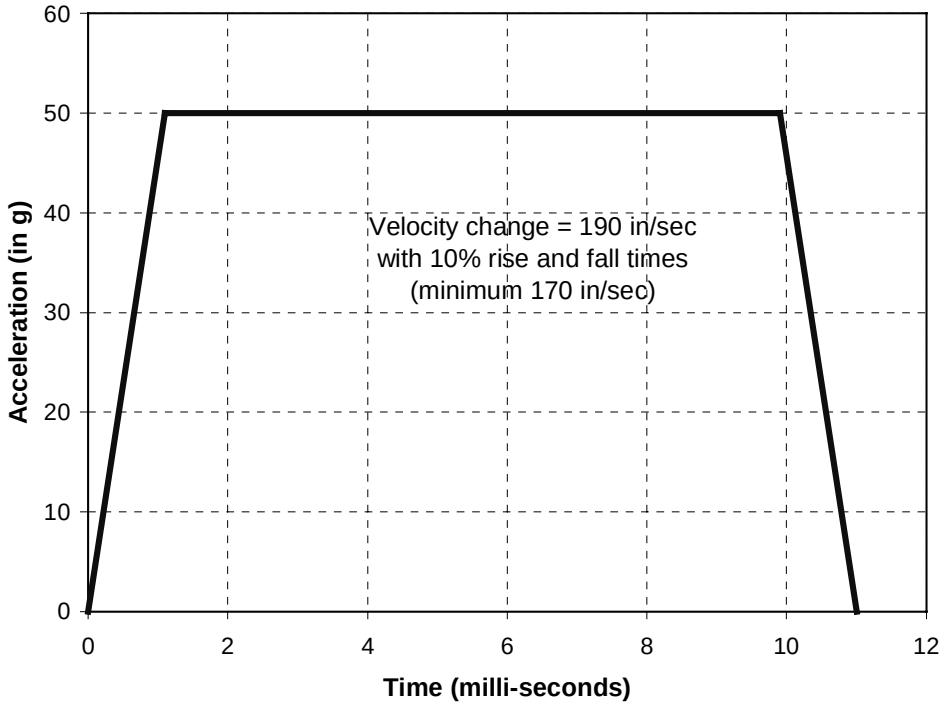


Figure 15: Shock Pulse Curve

4.5. Durability:

Mate and unmate samples for 50 cycles at a rate of 500cph (max), using the same substrate. Same substrate to be used for 1st and 51st cycles. Measure contact resistance when mated in 1st and 51st cycles. A spare substrate is used for 2nd through 50th cycles. **A pair of New Substrates to be used for each of the connector samples**.

4.6. Mating Force:

EIA 364, Test Procedure 13: Force necessary to mate steel gauge to samples at a maximum rate of 0.5in/min. 3.3oz average initial insertion force per opposing pair of contacts using steel gauge (see **Section 2.5**), except 1.58mm (0.062in) thick with 70° chamfer angle (see **Figure 1** side view of substrate). Total force < 25lb, per **Section 2.5**.

4.7. Unmating Force:

Force necessary to unmate steel gauge from samples at a maximum rate of 0.5in/min. Test performed similar to **Section 4.6**, except steel gauge is extracted. 1.98oz average initial extraction force per opposing pair of contacts using steel gauge (see **Section 2.6**), except 1.58mm (0.062in) thick with 70° chamfer angle (see **Figure 1** side view of substrate). Total extraction force < 15lb, per **Section 2.6**.

4.8. Thermal Shock:

-55ºC to +85ºC, 5 cycles per EIA 364, Test Procedure 32: Test Group 4 (see **Section 5.9.3**) unmated and unmounted for this test. Test group 5 mated and mounted for this test.

4.9. Humidity Temperature Cycling:

25ºC to 65ºC at 90% to 95% RH (non-condensing) for 10 days per EIA 364, Test Procedure 31, Method 3.

4.10. Temperature Life:

Mated samples shall be exposed to 105ºC air temperature (the maximum operating temperature plus the maximum recommended temperature rise for the contact due to electrical heating. Normally, this is 85ºC plus 20ºC rise = 105ºC.) for 240h (10 days). Precondition samples with three insertion/extractions (min).

4.11. Mixed Flow Gas:

Precondition samples with three insertion and extractions (min) using a new substrate that has not gone through the mixed flowing gas test. Testing shall be performed in accordance with EIA 364, Test Procedure 65, Class 2A. The test is to be performed as follows: The samples are exposed unmated to the mixed flowing gas for one day, and then mated for the remaining seven days of the test.

4.12. Withstand Temperature:

Ramp temperature at rate of 1ºC/sec to 3ºC/sec to 145ºC for 2min, then ramp to 225ºC for 40s. Test per EIA 364, Test Procedure 56, Procedure 5.

4.13. Porosity:

For plating outlined in **Section 2.1.3** (1), use EIA 364, Test Procedure 53, Nitric acid test. For plating outlined in **Section 2.1.3** (2), use EIA 364, Test Procedure 60, Procedure 1.1.2 Sulfur Dioxide test. Test to be performed for randomly selected 10 contacts from each level. That is, 10 contacts from lower and upper rows (levels) of the contact pattern. That is, total of 20 contacts per connector.
Requirement: Maximum of **one pore** per set of 10 contacts. That is, only one pore allowed for each of the 10 contacts randomly selected from the lower and upper rows.

4.14. Plating Thickness:

Record thickness of plating on contact surface per EIA 364, Test Procedure 48, Method C.

4.15. Solvent Resistance:

Requirement: No damage to ink markings if applicable.
EIA 364, Test Procedure 11.

4.16. Normal Force:

Requirement: Calculate normal force using nominal thickness processor substrate.
EIA 364, Test Procedure 4.

4.17. Solderability:

Requirement: 95% coverage.
EIA 364, Test Procedure 52, Class 2, Category 3.

4.18. Contact Retention:

Requirement: No movement > 0.38mm (.015in).
EIA 364, Test Procedure 29, 300g (min) load per individual contact.

4.19. Maximum Force on Connector:

No physical damage to connector after application of 150lb to fully seated S.E.C. cartridge. Time duration for test is 30s. Force applied to top surface of S.E.C. cartridge, perpendicular to the motherboard, after the cartridge is fully mated and bottomed out in the connector. No movement > 0.076mm (0.003in). Test performed within a 15°C to 35°C temperature range.

4.20. Contact backout Wipe:

0.99mm (0.039in) minimum. There shall be no discontinuities or improper connections after withdrawing an S.E.C. cartridge 0.99mm (0.039in), after the cartridge is first bottomed out in the connector.

4.21. Visual Inspection of Substrate - Post Shock & Vibration:

Remove the substrate from the S.E.C. cartridge. To pass shock & vibration, there shall be no "evidence of fretting corrosion - i.e. black spots" on any of the contact pads of the substrates. When a pass/fail decision can not be made based on visual inspection of the substrate (fret corrosions is suspected), i.e., plating wear through and black spots, substrate surface analysis under SEM must be done.

5. Qualification Testing Requirements

This section of the document outlines the tests that must be successfully completed in order for the connector supplier's connector to pass the qualification process. It provides the test plan and procedure required to reach and maintain a qualified test status.

5.1. Applicable Documents

EIA-364-C
Pentium® II Processor data sheet, Intel Order Number 243335

5.2. Production Lot Definition

A production lot is defined as a separate process run through the major operations including molding, contact stamping, contact plating, and assembly. These lots should be produced on separate shifts or days of the week. Lot identification marking needs to be provided to Intel as verification of this process.

5.3. Testing Facility

Testing will be performed by Intel's designated test facility.

5.4. Funding

Connector supplier will fund connector qualification testing for their connector. Any additional testing that is required due to design modifications will also be at the expense of the supplier.

5.5. Reporting

Test reports of the connector qualification testing will be provided directly from the independent test facility to Intel. Intel will also be given access to contact the test facility directly to obtain connector qualification status, explanation of test results and recommendations based on the test results.

5.6. Process Changes

Any significant change to the connector will require submission of a detailed explanation of the change at least 60 days prior to the planned implementation. Intel will review the modification and establish the necessary re-qualification procedure that the connector must pass. Any testing that is required MUST be completed before the change is implemented.

Typical examples of significant changes include, **but are not limited to, the following:** Plastic material changes including base material or color; contact changes including: base material, plating material or thickness; and design modifications.

5.7. Connector Test Plan

5.7.1. Test Flow

The test flow is outlined in **Section 5.9.3**. Sample sizes and test requirements are given for each test group. For specific test procedures, please refer to the applicable test specifications referenced in **Section 5.1**.

5.7.2. Retest Restrictions

Failures of particular sections of the test plan for a given connector footprint will require re-testing of at least a portion of the test flow defined in **Section 5.9.3**. The definition of the tests required will be at Intel's discretion. The modifications that will be made to the connector to improve a failing condition must be provided to Intel in writing and must be approved by Intel® prior to retest. If failures occur after retest, further testing will be at Intel's discretion.

5.7.3. Mechanical Samples

A mechanical sample of the S.E.C. cartridge, processor substrate, and heat sink (or suitable mockups that approximate size and mass of the planned heat sink) will be used during the mated connector qualification testing. The weight of the S.E.C. cartridge processor is 150g. The recommended maximum weight for an S.E.C. cartridge processor heat sink is 250g. See the Pentium® II processor data sheet and related documentation for further information on heat sinks, thermal solutions and mechanical support.

5.8. Connector Qualification Notification

Upon completion of the test flow and receipt of test data, Intel will prepare a summary report for the connector supplier that will provide notification as to whether the connector has passed or failed connector qualification testing.

5.9. Connector Qualification

5.9.1. Sample size per group: (shown at bottom of each test group in Section 5.9.3)

Test samples are to be taken from two different lots. Example: if 8 samples are required, 4 samples will be used from two different lots. Each sample shall be prepared in accordance to the documents specified in **Section 5.1,** and selected at random per **Section 5.2**.

5.9.2. Test Sequence: Each group of samples is tested per the number sequence as outlined in Section 5.9.3.

The following is an example of how the test sequence works: In Test Group 8, the first test is (1), visual inspection, followed by test (2), contact retention, followed by test (3), solvent resistance. Four samples are tested in this test group, as outlined in **Section 5.9.1.**

5.9.3. Qualification Test

Test Description Sequence (Reference Section Location)	Test Group								
	1	2	3	4	5	6	7	8	9
Visual Inspection (4.2)	1,11	1,6	1,6	1,9	1	1,6	1	1	1
CTF Dimensional Verification (2.9)	2	2	2	2	2	2	2	2	2
Termination Resistance (3.1)	4,6,9	3,5	3,5		3,5,7				
Adjacent Pair Inductance (3.3)									3
Pin to Pin Capacitance (3.4)									4
Insulation Resistance (3.5)				3,7					
Dielectric Withstand Voltage (3.6)				4,8					
Characteristic Impedance, Propagation, and Crosstalk Coupling (3.7)									5
Vibration (4.3)	8								
Shock (4.4)	7								
Durability (4.5)	5								
Mating Force (0)	3								
Unmating Force (4.7)	10								
Thermal Shock (4.8)				5	4				
Humidity Temperature Cycling (4.9)				6	6				
Temperature Life (4.10)		4							
Mixed Flowing Gas (4.11)			4						
Resistance to Solder Heat (4.12)						3			
Porosity (4.13)							3		
Plating Thickness (4.14)							4		
Solvent Resistance (4.15)								6	
Normal Force (4.16)							5		
Solderability (4.17)							6		
Contact Retention (4.18)								5	
Maximum Force on Connector (4.19)								3	
Contact Backout Wipe (4.20)								4	
Substrate Visual Inspection (4.21)	12								
Sample Size per Test Group	16	8	4	8	8	4	4	4	4

6. SAFETY REQUIREMENTS

6.1. Design:

Design, including materials, shall be consistent with the manufacture of units that meet the following safety standards:

UL Recognition.

CSA Certified.

7. DOCUMENTATION REQUIREMENTS

The connector supplier shall provide Intel with the following documentation:

Multi-Line SPICE models for connector.

Product specification incorporating the requirements of these specifications.

Recommended board layout guidelines for the connector consistent with low cost, high volume printed circuit board technology.

The test facility shall provide Intel and the supplier with the following document:

Qualification Testing and Test Report supporting successful compliance with these specifications.

UNITED STATES, Intel Corporation
2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119
Tel: +1 408 765-8080

JAPAN, Intel Japan K.K.
5-6 Tokodai, Tsukuba-shi, Ibaraki-ken 300-26
Tel: + 81-29847-8522

FRANCE, Intel Corporation S.A.R.L.
1, Quai de Grenelle, 75015 Paris
Tel: +33 1-45717171

UNITED KINGDOM, Intel Corporation (U.K.) Ltd.
Pipers Way, Swindon, Wiltshire, England SN3 1RJ
Tel: +44 1-793-641440

GERMANY, Intel GmbH
Dornacher Strasse 1
85622 Feldkirchen/ Muenchen
Tel: +49 89/99143-0

HONG KONG, Intel Semiconductor Ltd.
32/F Two Pacific Place, 88 Queensway, Central
Tel: +852 2844-4555

CANADA, Intel Semiconductor of Canada, Ltd.
190 Attwell Drive, Suite 500
Rexdale, Ontario M9W 6H8
Tel: +416 675-2438