330-Contact Slot Connector (SC330) Design Guidelines

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Order Number: 244428-001

1. INTRODUCTION

This document defines a connector for server and workstation platforms based on Intel microprocessors. The connector has 330 contacts with a pitch of 0.030in.

1.1. Purpose:

To define functional, quality, and material (that is, visual, dimensional and physical) requirements and specifications of the SC330 connector. To provide SC330 connectors that meet or exceed applicable system design and manufacturing criteria.

1.2. Scope:

This specification applies to all SC330 connectors purchased to the requirements of this specification.

2. MECHANICAL REQUIREMENTS

2.1. Cosmetics (Look and Feel) :

2.1.1. Visual Inspection:

Connectors should be inspected at 10X magnification with top-lit fluorescent ring lighting. Reference examination may be performed with magnification of 20X.

2.1.1.1. Incomplete Fill or Damaged Housing:

Incomplete fill is an area of the housing missing plastic due to reduced or incomplete mold fill. Damaged housing is misformed, chipped, broken areas in the housing.
Requirement: No incomplete fill or damaged housing.

2.1.1.2. Mold Flash:

Mold flash is excess plastic material extruded at the mold parting line.
Requirement: No mold flash > 0.005in (0.127mm) should be present on the solder tails and no mold flash > 0.010in (0.254mm) should be present on the connector housing.

2.1.1.3.

Foreign Material, Contamination and Discoloration:

Foreign material is defined as the material adhering to or within the material surface, not present by design.
Contamination is a surface coating which is not present by design.
Discoloration is a variation in color due to chemical change; not due to surface finish, grain size structure or grain size.
Requirement: No foreign material, contamination or discoloration in the contact area. No foreign material, contamination or discoloration larger than 0.254mm (0.010in) in major dimension on the connector housing and larger than 0.127mm (0.005in) on the solder tails.

2.1.1.4.

Burrs:

A Burr is a mechanically displaced metal that is still attached to a metallic part.
Requirement: No evidence of burrs in contact area and on solder tails when viewed at 10X magnification.

2.1.1.5.

Damaged, Missing, or Misaligned Solder Tails:

Requirement: No damaged, malformed, missing or misaligned solder tails. Note that dimensional measurement of solder tail true position in **Section 2.9.2** is the primary means of solder tail alignment.

2.1.1.6.

Missing Plating:

Requirement: No missing plating on contact area and solder tail.

2.2. Materials:

2.2.1. Connector Housing:

Thermoplastic, UL 94V-0 flame rating, temperature rating and design capable of withstanding reflow solder process (See **Section 4.11**).

Color: Black

2.2.2. Markings:

2.2.2.1. Name:

SC330[1] (to be molded or laser marked into both long sides of connector housing.). It must pass Solvent Resistance Test of **Section 4.14**.

SC330 (Font type is Helvetica - 16 point Bold).

Manufacturer's insignia (font size at supplier's discretion). This mark will be molded or laser marked into both sides of the connector housing. It must pass Solvent Resistance Test of **Section 4.14**. Any requests for variation from this marking requires a written description (detailing size and location) to be provided to Intel for approval.

2.2.2.2. Lot Traceability:

Each connector will be marked with a lot identification code that will allow traceability of all components, date of manufacture (year and week), and assembly location. This mark can be an ink mark, a heat stamp, or a laser mark but must be able to withstand a temperature of 225°C for 40s (min). The mark must be placed on the side of the connector.

2.2.3. Contacts:

A requirement of 100µin (min) tin lead over nickel underplate on solder tails, for all plating alternatives. The following two alternatives are listed to allow flexibility. **The absolute requirement is that the plating meet the Qualification requirements listed in Section 6.9.**

Alternative (1): High strength copper alloy; 30µin (min) gold plating over 50µin (min) nickel underplate in critical contact areas.

Alternative (2): High strength copper alloy; 2µin (min) gold flash over 30µin (min) palladium-nickel over 50µin (min) nickel underplate in critical contact areas.

[1] Connector housings from molds built prior to December 31, 1998 may be labeled "Slot Type 2" instead of "SC330".

2.3. Number of contacts:

Total number of contacts: 330

2.4. Connector Size:

The connector shall accept a processor substrate width of 5.535in (140.59mm). The connector housing shall be 5.660in (143.76mm) long. The tolerance on the connector for overall dimensions not to exceed ± 0.005in.

2.5. Mechanical Supports:

The substrate must have a positive tactile response when complete substrate engagement is achieved. The maximum backout allowable for the substrate to ensure reliable electrical continuity of the assembly is 0.020in (0.5080mm) from the completely engaged position. A retention system to isolate the weight of the Single Edge Contact cartridge (S.E.C.C.) and the associated heat sink (total module weight of 1100gms), from the connector during the shock and vibration conditions during shipping and handling is the responsibility of the system designer. The connector is not expected to bear any weight from the S.E.C.C. However, it must pass the MIL-STD-C-55302 condition with the associated weight of 1100g as specified by Intel.

2.6. Insertion Force:

Insertion force of the steel gauge into the connector not to exceed 35lb. This applies only to test conditions detailed in **Section 4.6**. The steel gauge details are shown in **Figure 1**.

2.7. Extraction Force:

Extraction force of the steel gauge from the connector not to exceed 20lb. This applies only to test conditions detailed in **Section 4.7**.

2.8. Durability:

The connector shall withstand a minimum of 50 insertion/withdrawal cycles with a substrate.

2.9. Assembly Requirements to the Motherboard:

2.9.1. Pre- Solder Attachment:

A method of securing the connector to the motherboard is required to assist in the manufacturing process. The securing method shall be consistent with low cost, high volume printed circuit assembly lines. Four metal forklocks are required to achieve this goal. The combined insertion force for all metal forklocks shall not exceed 20lb (max). The retention force of a fully seated

connector to the motherboard shall be between 3lb and 20lb. The forklock lead-in length can be longer than the solder tail pins for the purpose of alignment, but must not engage with the motherboard or alter the alignment of the connector to the motherboard layout until the solder tails have penetrated the motherboard. In addition, the forklocks must be designed and toleranced such that they will not skew or turn the connector as it is assembled to the motherboard. There is a zero insertion force of the clips to the motherboard until the pins have penetrated the motherboard. The lead length of the solder tail pins is 0.090in + 0.010in / - 0.005in from the seating plane of the connector.

2.9.2. Solder Tail Design and Alignment:

The connector solder tails must be designed and aligned such that the tip of the solder tails must enter a virtual condition hole that is 0.021in (0.533mm) in diameter. The virtual condition solder tail holes result from the true positional tolerance dimensions specified in the layout shown in **Figure 2**. The solder tails must not bend when fully inserted into this motherboard layout. The solder tails have 0.012in (0.30mm) perpendicularity and true position requirements with respect to Datums C and D, see **Figure 3**. The forklocks have a 0.015in (0.38mm) true position requirement with respect to Datum E and a 0.006in (0.15mm) true position requirement with respect tot Datum D, see **Figure 3**

2.10. Connector Drawings:

The SC330 connector shall hold the substrate at right angles to the motherboard. All dimensions are in inches; metric dimensions are shown for reference only. The connector must accommodate a 0.062in thick substrate (tolerance + 0.007in / - 0.005in with a maximum substrate board warpage of 0.010in/in). Key width dimension of 0.060in ± 0.002in (1.52mm ± 0.005mm) measured at bottom of card slot prior to draft. All dimensions are measured prior to draft unless otherwise specified. The purpose of internal keys is to properly align the S.E.C.C. within the SC330 connector and to prevent the cartridge from being inserted backwards (rotated 180 degrees) into the connector.

Critical to function (CTF) dimensions are identified in **Figure 4**. Each of the dimensions must meet the requirements given in the **Table 1**. These dimensions will be verified as part of the qualification process, see **Table 4**. Also, supplier will provide and maintain Critical Process Parameters controlling these CTFs or will provide direct measurements to meet ongoing quality requirements.

Table 1: Critical To Function Dimensions

Dimension	Minimum (in)	Maximum (in)
Housing Bay (Card Slot) Length (Left) - A	1.887	1.897
Housing Bay (Card Slot) Length (Middle) - B	1.923	1.933
Housing Bay (Card Slot) Length (Total) - C	5.545	5.555
Housing Width (Lower Shoulder)- D	0.485	0.495
Housing Width (Bottom)- E	0.535	0.545
Housing Height - F	0.754	0.764
Housing Flatness - Bottom Standoffs	0.000	0.002
Solder Tail (Lead) True Position (With respect to Datums C and D)	0.000	0.012
Retention Feature (Forklocks) - True Position (With respect to Datum E)	0.000	0.015
Retention Feature (Forklocks) - True Position (With respect to Datum D)	0.000	0.006
Retention Feature (Forklocks) – Width	0.077	0.081
Card Slot (Substrate Slot) Width - G	0.069	0.073
Cartridge Seating Plane Height (Depth) - H	0.361	0.371
Solder Tail (Lead) Length - J	0.085	0.100
Contact True Position	0.000	0.002
Terminal Gap	0.018	0.030

Manufacturer is required to monitor these CTFs as a part of on-going Quality Control.
Dimensions A, B and C are measured at the Cartridge Seating Plane.

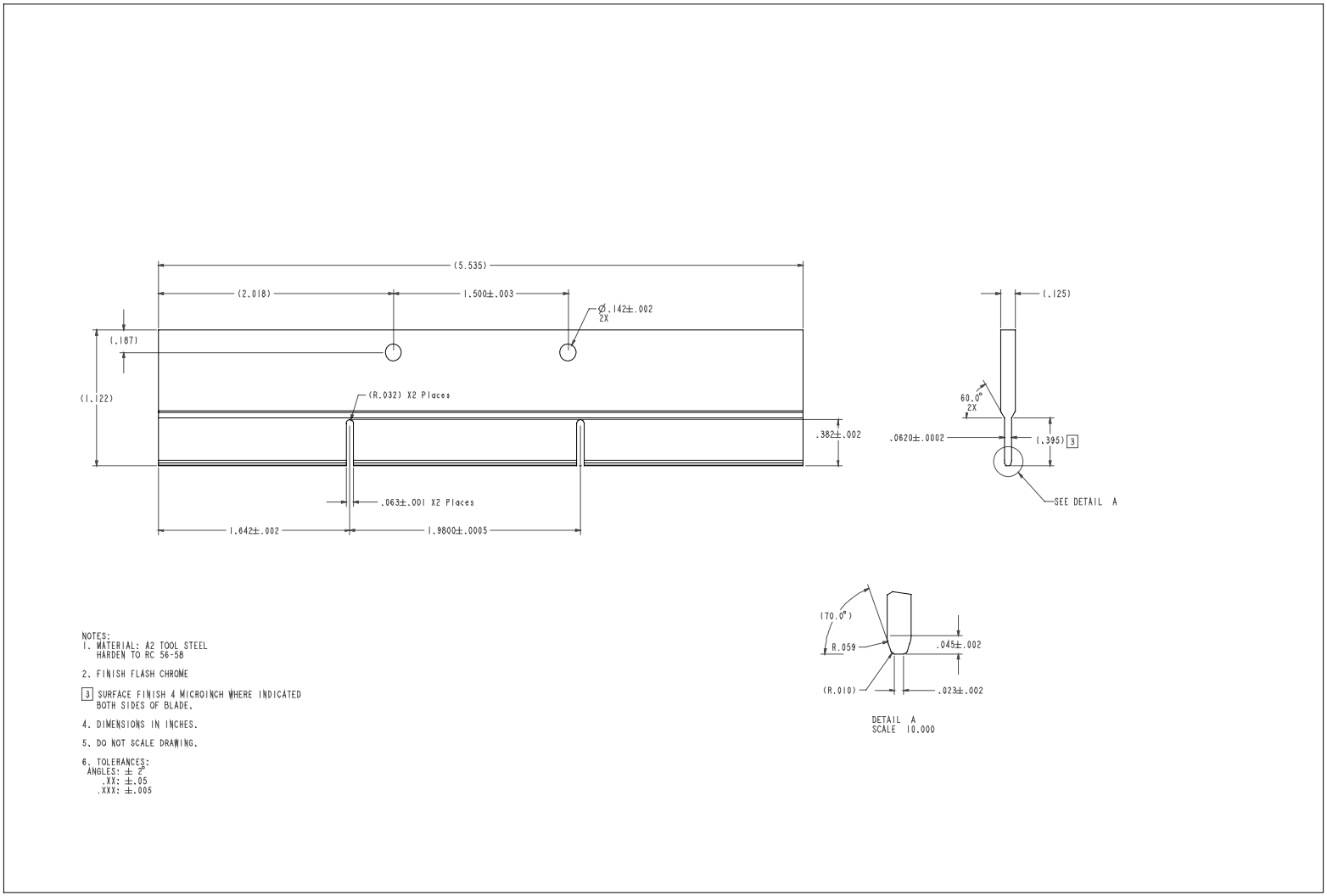


Figure 1: Steel Gauge Specifications

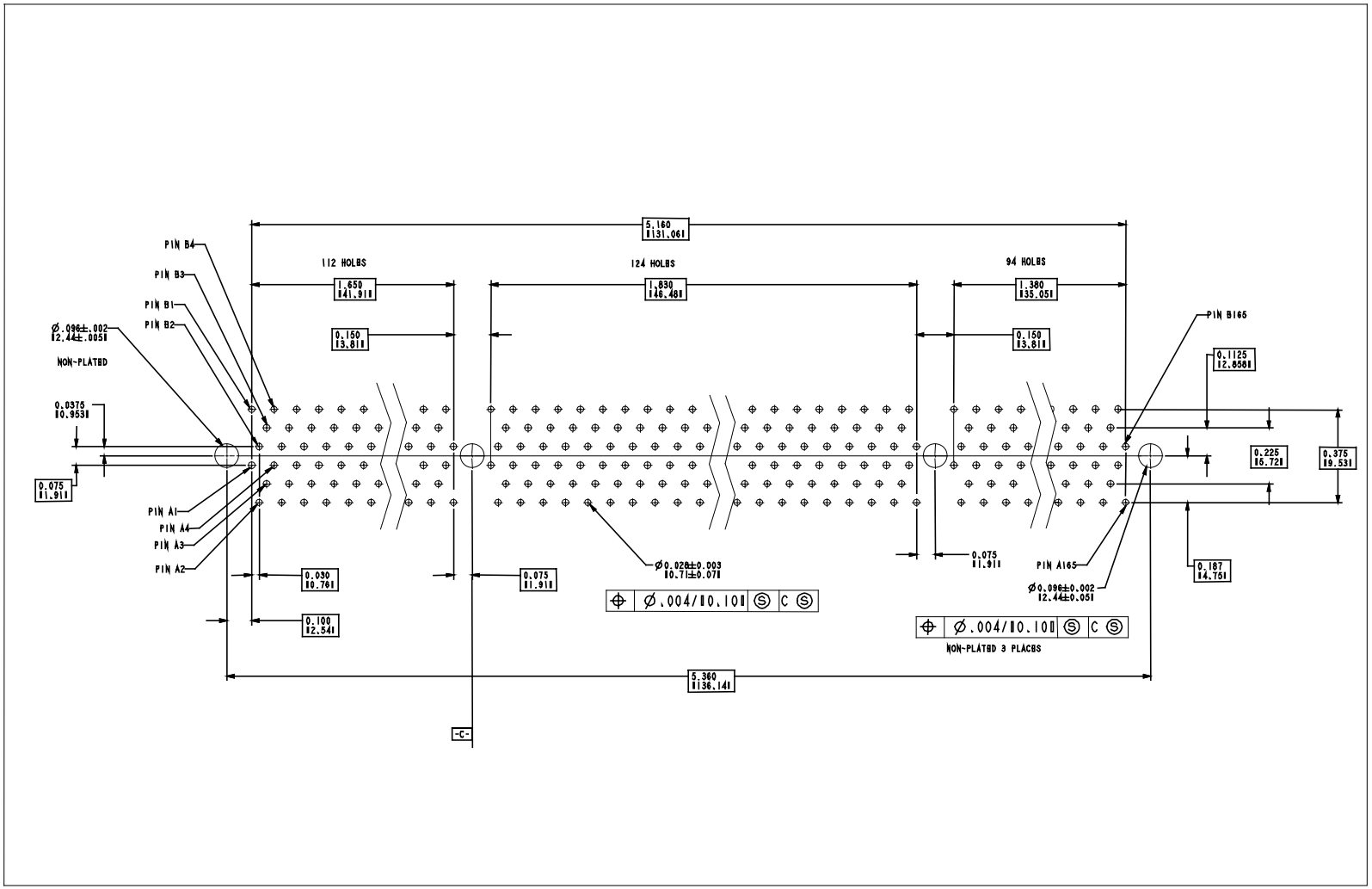


Figure 2: Motherboard Layout

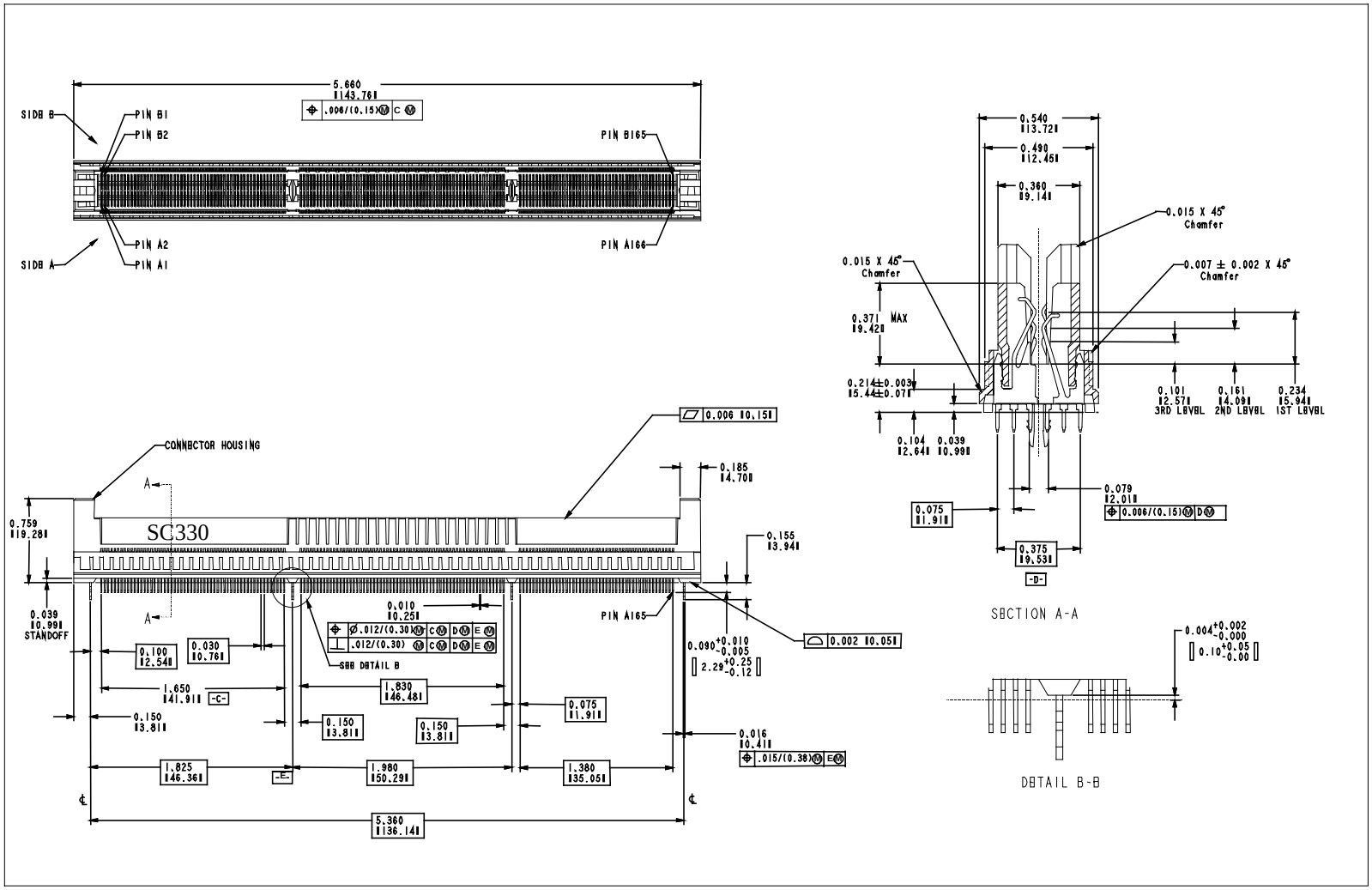


Figure 3: Connector Dimensions

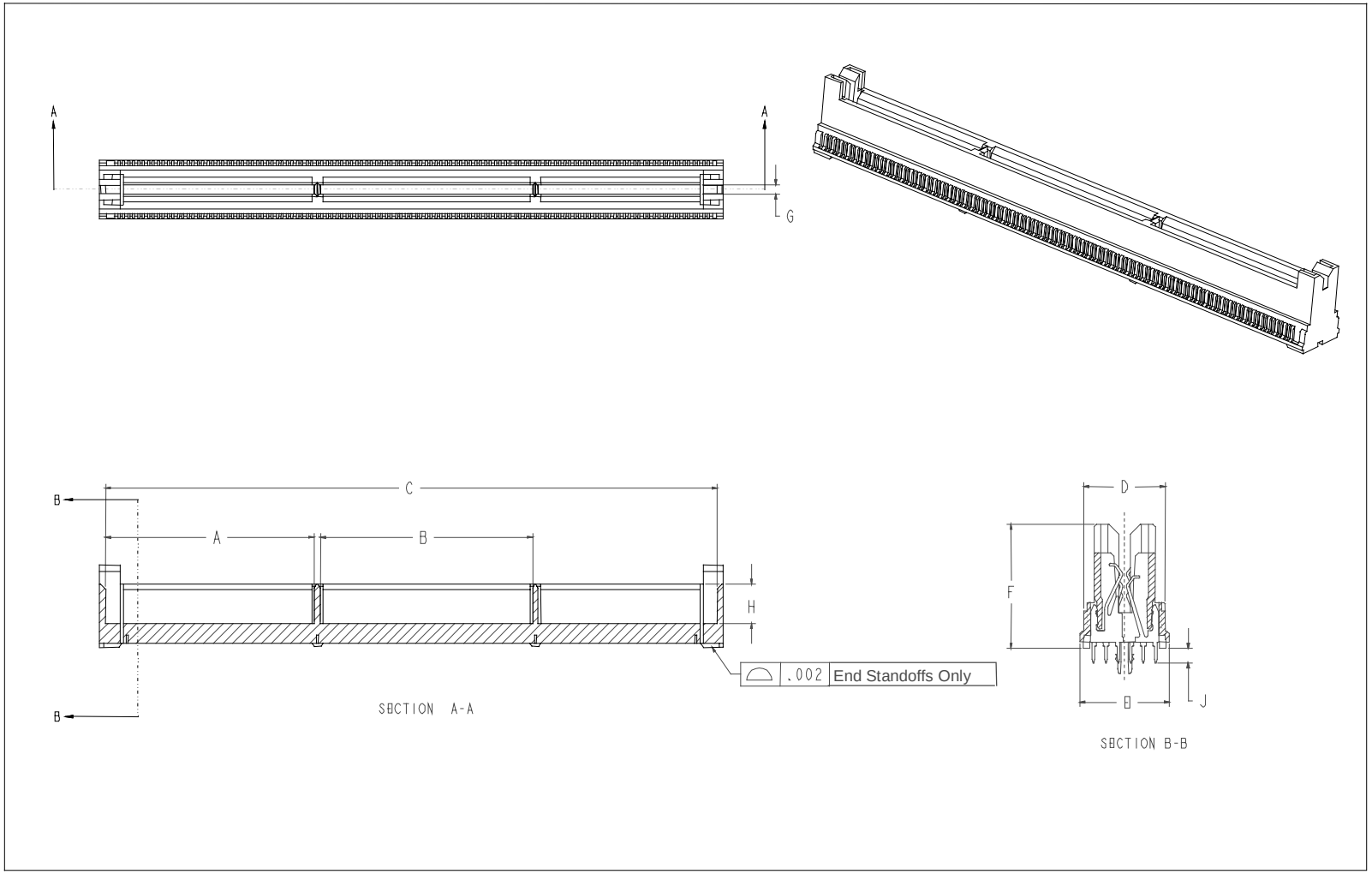
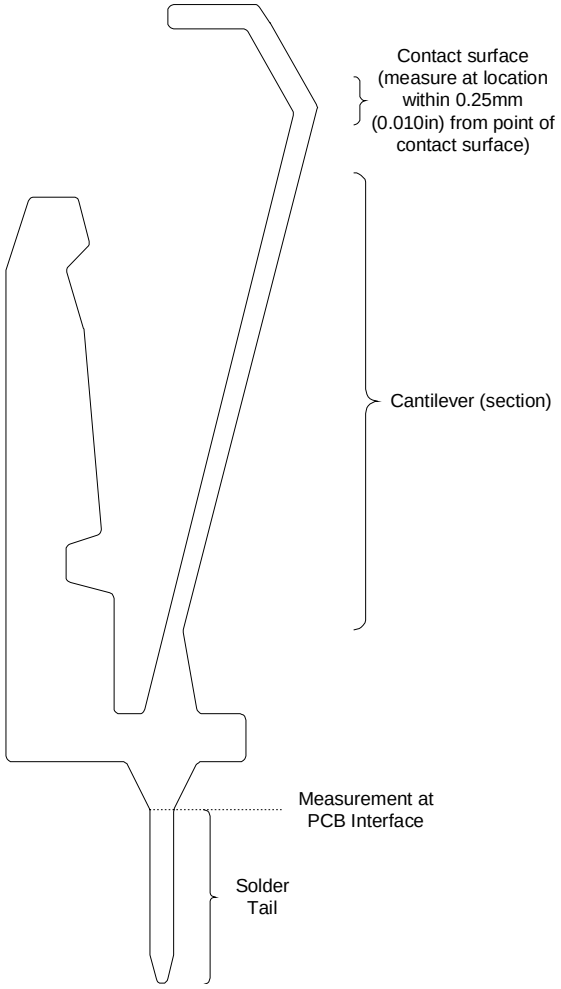


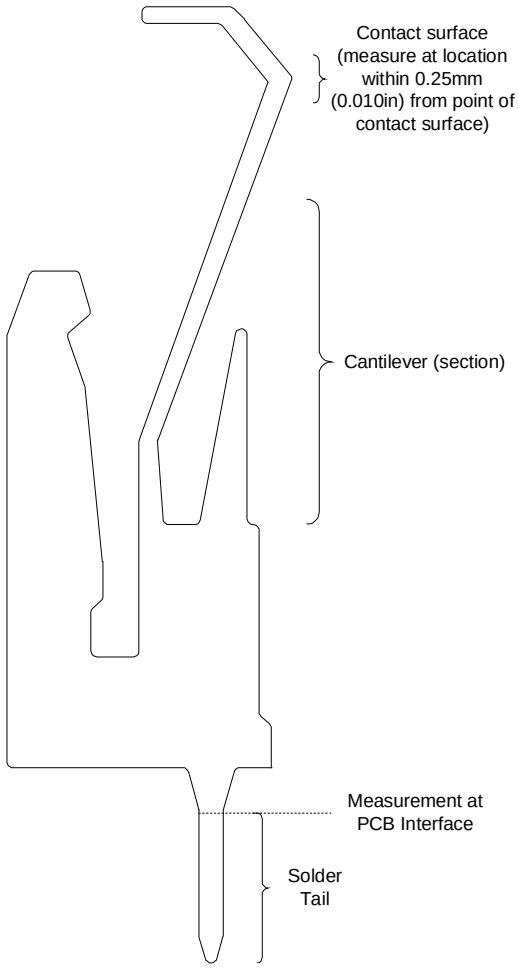
Figure 4: Critical To Function Dimensions

3. ELECTRICAL REQUIREMENTS

Figure 5 provides examples of typical signal and power/ground pins.



Typical Signal Pin
(Middle and Lower Pins)



Typical Power/Ground Pin
(Upper Pins)

Figure 5: Typical Connector Pins

3.1. Determination of Averaged Contact Resistance:

Measure the Total Contact Resistance $\mathbf{R_{AB}}$ for each of the 330 pins.

Measure the Bulk Resistance $\mathbf{R_{AC}}$ for each of 110 traces over the middle pads.

Measure the Bulk Resistance $\mathbf{R_{AD}}$ for each of 110 traces over the lower pads.

Determine the Contact Resistance for each of the 330 pins using:

$\mathbf{R_{CB} = R_{AB}}$ for upper (power/ground) 110 pins

$\mathbf{R_{CB} = R_{AB} - R_{AC}}$ for middle 110 pins

$\mathbf{R_{CB} = R_{AB} - R_{AD}}$ for lower 110 pins.

To determine Average Contact Resistance, sum up $\mathbf{R_{CB}}$ for all pins and divide by the total number of pins. That is, for SC330 connector,

$R_{averaged} = (\sum R_{CB})/330$ for all pins

$R_{averaged} = (\sum R_{CB})/8$ for V_{tt} pins only.

V_{tt} pins are identified as A5, A6, A156, A157, B6, B7, B156, B157.

3.1.1. Bulk Resistance:

This is the resistance of the thin pad connecting a common bus and the middle contact pad or the lower contact pad on the mating substrate. The Bulk Resistance is measured between point **A** on a common bus and a junction point of the thin pad and the lower or middle contact pads as shown in the **Figure 6**. Thus, $\mathbf{R_{AC}}$ and $\mathbf{R_{AD}}$ represent the Bulk Resistance for thin pads connecting common bus and the middle and lower contact pads, respectively.

3.1.2. Initial Contact Resistance:

There are five requirements: (a) Initial contact resistance averaged over 330 pins not to exceed 10mΩ. (b) Initial contact resistance averaged over 8 $\mathbf{V_{tt}}$ pins not to exceed 10mΩ. (c) No pin can exceed a contact resistance of 100mΩ. (d) Only one pin can have contact resistance between 50mΩ - 100mΩ. (e) Only two pins can have the contact resistance between 25mΩ - 50 mΩ.

3.1.3. Final Contact Resistance:

Final contact resistance is the end-of-life resistance taken after each of the environmental stress tests.
There are five requirements: (a) Final contact resistance averaged over 330 pins not to exceed 15mΩ. (b) Final contact resistance averaged over 8 $\mathbf{V_{tt}}$ pins not to exceed 15mΩ. (c) No pin can exceed a contact resistance of 100mΩ. (d) Only one pin can have contact resistance between 50mΩ - 100mΩ. (e) Only two pins can have the contact resistance between 25mΩ - 50mΩ.

3.2. Pin Current Rating:

Requirement:

Current Rating: 0.5A IDC per pin without exceeding the applied voltage of 5.0Vdc.
Temperature Rise (above the ambient at 0.5A IDC): Not to exceed 20°C.

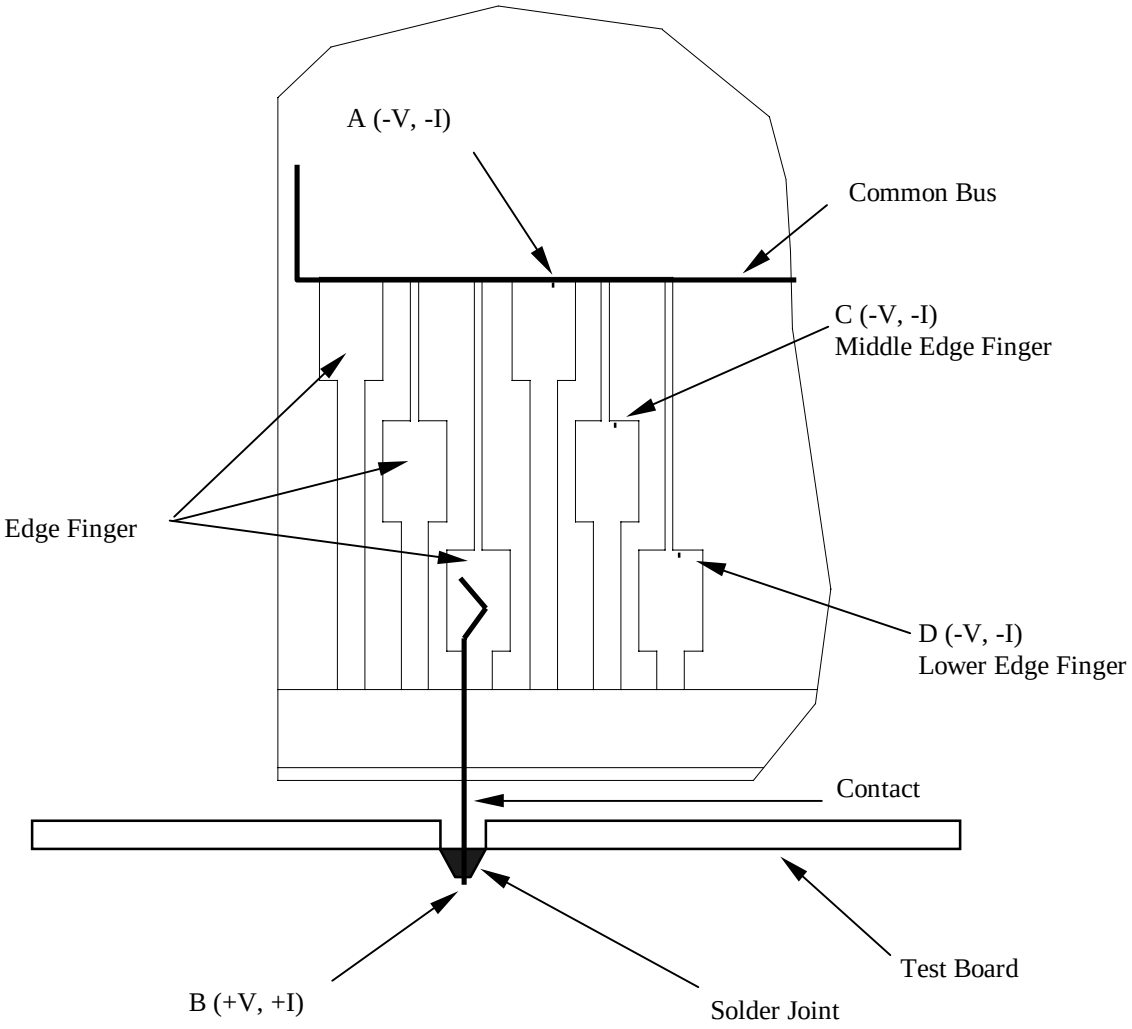


Figure 6: Schematic of Contact Resistance Measurements

Procedure:

Once the current rating of 0.5A IDC is established, monitor the contact temperature for 5min. Measure the temperature rise after stabilization has occurred. Stabilization occurs when three successive readings, over a span of five or more minutes, have a

change of temperature less than ±2°C. Pin current rating shall be randomly measured for five pins from each of the three styles, power/ground, long signal (middle pins), and short signal (lower pins), for a total of 15 pins. Testing shall be measured as per EIA 364, test procedure 70, method 13. See **Figure 7**.

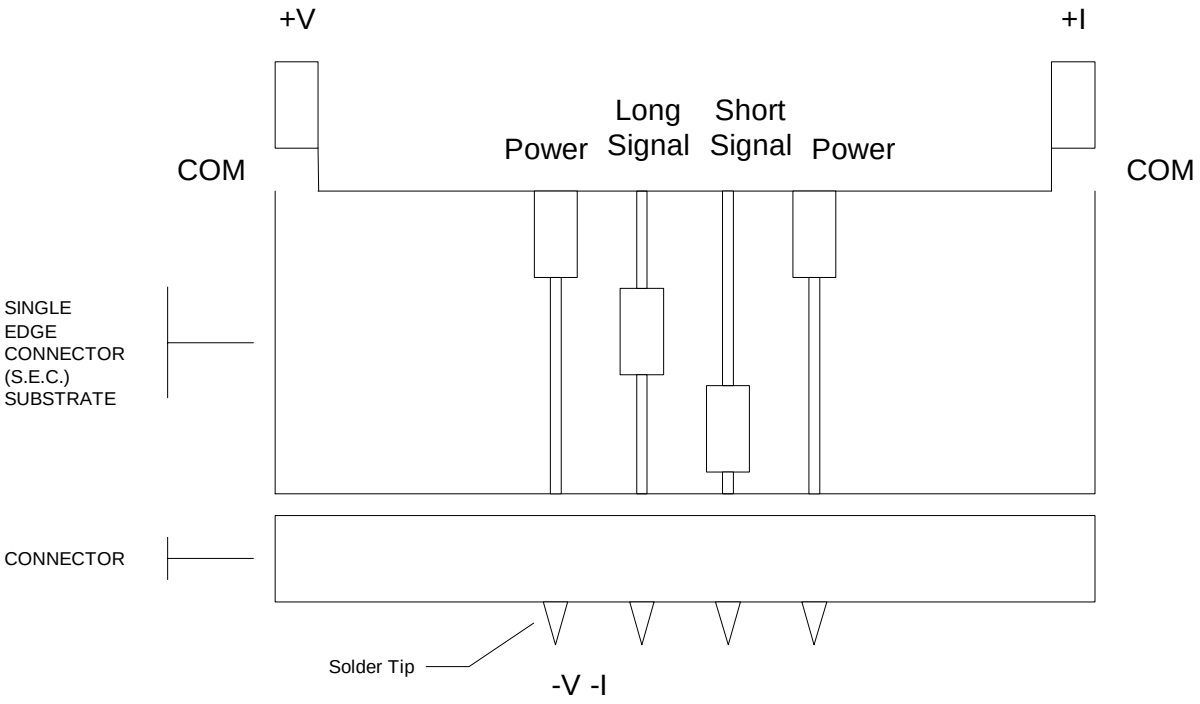


Figure 7: Schematic of Pin Current Measurements

3.3. Pin Self Inductance (Inductance in Free Air):

Requirement:

Pin Self Inductance in Free Air at all test frequencies: not to exceed 8nH

Procedure:

Pin self inductance shall be measured in free air (with contact removed from connector housing) at the measurement planes indicated in **Figure 5**, at a location within 0.010in (0.25mm) from the point of the contact surface. Inductance measurements shall be taken at the following test frequencies: 200, 500, 700 and 1000MHz. Pin inductance in free-air shall be randomly measured for five pins from each of the three styles, power/ground, long signal (middle pins), and short signal (lower pins), for a total of 15 pins. Refer to high frequency bridge setup manual of HP4191A/B, HP4291A/B, or equivalent.

3.4. Pin to Pin Capacitance:

Requirement:

Pin to Pin Capacitance: not to exceed 2pF at 1MHz.

Procedure:

Pin to pin capacitance shall be measured as per EIA 364, Test Procedure 30 (Under Revision). Pin to pin contact capacitance shall be measured between adjacent long and short signal pins (signal to signal), between short signal pin and adjacent ground pin and between long signal pin and ground pin, at a location within 0.010in (0.25mm) from the top of the contact area. Measurements shall be randomly taken for five pairs from each of the three sets listed above, for a total of 15 measurements. The schematic for this test is shown in **Figure 8**. This measurement is on connector only in unmated condition (no substrate mated).

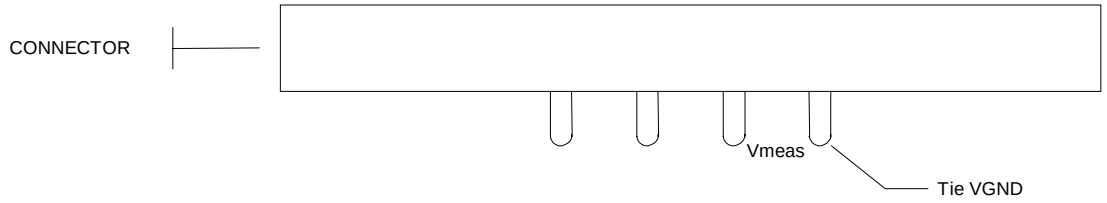


Figure 8: Schematic of Pins

3.5. Pin to Pin Insulation Resistance:

Requirement:

Pin to Pin Insulation Resistance: Minimum of 1000MΩ

Procedure:

Contact insulation resistance shall be measured as per EIA 364, Test procedure 21. Pin to pin insulation resistance shall be measured between adjacent long and short signal pins (signal to signal), between short signal pin and adjacent ground pin and between long signal pin and ground pin. Pin to pin insulation resistance shall be randomly measured for five pins from each of the three styles, power/ground, long signal (middle pins), and short signal (lower pins), for a total of 15 pins. The schematic for this test is shown in **Figure 8**. This measurement is on connector only in unmated condition (no substrate mated).

3.6. Pin Dielectric Withstand Voltage:

Requirement:

Pin Dielectric Withstand Voltage: Minimum 400Vac

Procedure:

Pin Dielectric Withstand voltage shall be measured as per EIA 364, Test Procedure 20. Pin dielectric withstand voltage shall be measured between adjacent long and short signal pins (signal to signal), between short signal pin and adjacent ground pin and between long signal pin and ground pin. Pin Dielectric Withstand Voltage shall be randomly measured for five pins from each of the three styles, power/ground, long signal (middle pins), and short signal (lower pins), for a total of 15 pins. The schematic for this test is shown in **Figure 8**. This measurement is on connector only in unmated condition (no substrate mated).

3.7. Pin Characteristic Impedance

Requirement:

Typical signal pin impedance at post filter rise time of 1ns: Shall be $52.5\Omega \pm 7.5\Omega$, with pin termination $Z_L = 50\Omega$, mounted within 3in from the tip of the daughter board pad.
Typical signal pin impedance at post filter rise time of 200ps: Shall be $52.5\Omega \pm 10.0\Omega$, with pin termination $Z_L = 50\Omega$, mounted within 3in from the tip of the daughter board pad. Any impedance measurements which are outside the specified range are allowed if the duration of the "out of spec" TDR pulse is less than TDR time of 100ps (50ps real time).
Board trace impedances: $Z_0 = 50\Omega \pm 10\%$.
All terminations: Shall not exceed tolerance of $\pm 5\%$ of the specified values.

Procedure:

Use a TDR measurement with less than 50ps rise time steps at launch and post processing filter rise time of 200ps and 1ns. Impedance shall be measured at 200ps and 1ns rise time. All ground/power pins should be tied to all ground planes. The adjacent short and long signal pin should be terminated to 50Ω. The schematic for this test is shown in **Figure 9**. 12 measurements (6 long signal pins, LS, and 6 short signal pins, SS) per connector shall be taken. These measurements will be equally divided on side A and side B of the mating card

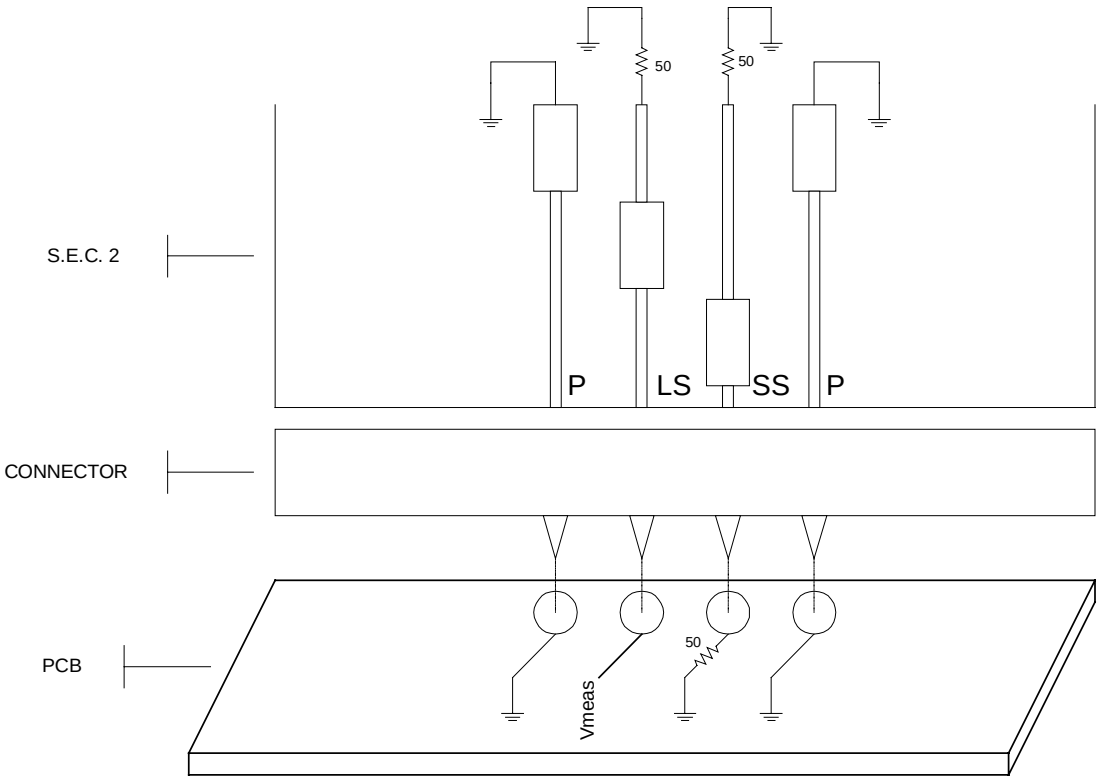


Figure 9: Schematic of Impedance Measurements

3.8. Pin to Pin Crosstalk Coupling:

Requirement:

Pin to Pin Crosstalk: Not to exceed 6% baseline to peak of the aggressor's signal.
Board trace impedances: $Z_0=50\Omega \pm 10\%$.
All terminations: Shall not exceed tolerance of ± 5% of the specified values.
Test rise time: 1ns with an edge rate (10% - 90%).

Procedure: (For Test Board configuration, see **Section 3.10**)

Measure crosstalk in the time domain with a 1ns edge rate. Crosstalk shall be measured as per EIA Test Procedure 90 (under approval). The schematic for this test is shown in **Figure 10**. Pin to pin crosstalk shall be observed at the NEXT (near source termination) and FEXT (on other side of connector from source driver, far end termination). Pin to pin crosstalk shall be terminated at NEXT with 50Ω to ground. Pin to pin crosstalk shall be terminated at FEXT end with 50Ω to ground.

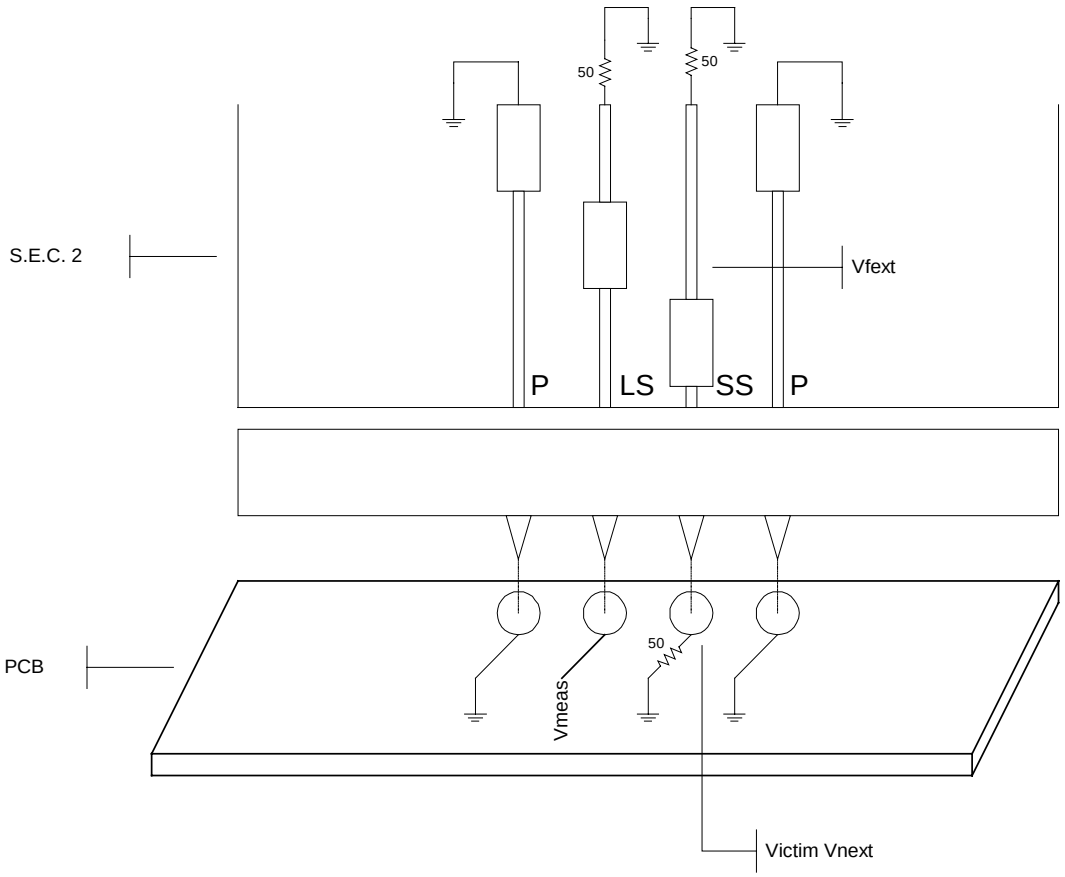


Figure 10: Schematic of Crosstalk Coupling and Propagation Delay Measurements

Drive the short signal pin from a 50Ω source, through the connector into a 50Ω load.
Measure the victim long pin at the NEXT and FEXT ends.
Drive the long signal pin from a 50Ω source, through the connector into a 50Ω load.
Measure the victim short pin at the NEXT and FEXT ends.
Adjacent short and long signal pins shall be tied through 50Ω to ground on both pin ends. Adjacent ground/power pins shall be grounded.

3.9. Connector Propagation Delay

Requirement:

Propagation Delay across the mated connector with the prescribed test fixturing calibrated out leaving only the connector at the established measurement planes indicated in **Figure 5**: Not to exceed 110ps at the 50% source amplitude level.
Board trace impedances: $Z_0 = 50\Omega \pm 10\%$
All terminations: Shall not exceed tolerance of ± 5% of the specified value.
Test rise time: Not to exceed 100ps with an edge rate (10% - 90%).

Procedure:

Measure Propagation Delay in the time domain with an edge rate of less than 100ps. Propagation delay shall be measured as per EIA Test Procedure 103 (under approval). The schematic for this test is shown in **Figure 10**.

All ground/power pins should be tied to all ground planes. The adjacent short and long signal pin should be terminated to 50Ω. Drive the short signal pin from a 50Ω source, through the connector into a 50Ω load. Drive the long signal pin from a 50Ω source, through the connector into a 50Ω load.

3.10. Test Board Configuration

Figure 11, **Figure 12**, and **Figure 13** provide examples of the Mother and CPU Test Board Layouts.

On board masks: include test board rev # & SC330 connector p/n 71109-5005.
Board construction: 6-layer embedded, 50Ω stripline construction.
Trace impedance's: 50Ω +/- 10%.
Label all test traces.
Connect all ground pins to all ground planes.
Transmission Cal trace length: 1X signals trace length.
Reflection Cal trace: 2X signal trace.
Label L (inductance) Cal, C (capacitance) Cal, Trans(transmission) Cal, and Reflection Cal traces.
Traces between LS & SS signals lines should be separated as soon as possible once away from the connector.
All signal traces should be approx. 2in to 3in long. All traces are the same length.
Nominal space between SMA centers = .8in.
Label each launch connector.
Via's in ground planes every 0.3in; filled via's okay.
SMA interface spec is 50Ω +/- 20% within a 200ps exception window at a Tr = 200ps.
All connector ground pins are connected directly to all ground planes with no thermal relief
Daughter board thickness is 0.062in + 0.007in / - 0.005in.
Backplane board thickness is 0.062in + 0.008in / - 0.005in.
Via's between signal trace connections and pads to be 0.010in (0.25mm) from top of pad to bottom of signal trace via, in-accordance with yellow book specs.

SC330 Mother Test Board Layout

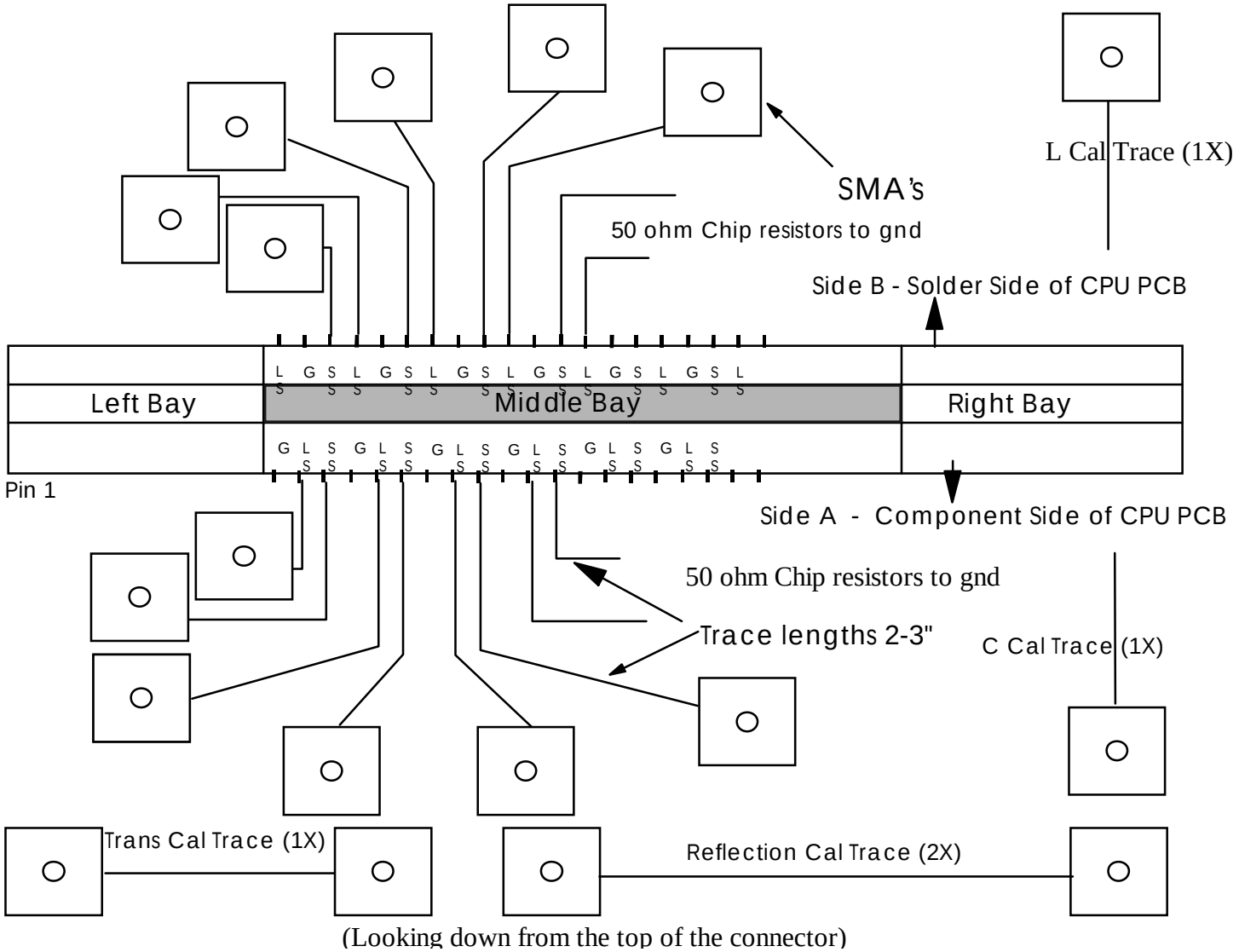


Figure 11: Mother Test Board Layout

SC330 CPU Test Board Layout:

Primary (Processor) Side

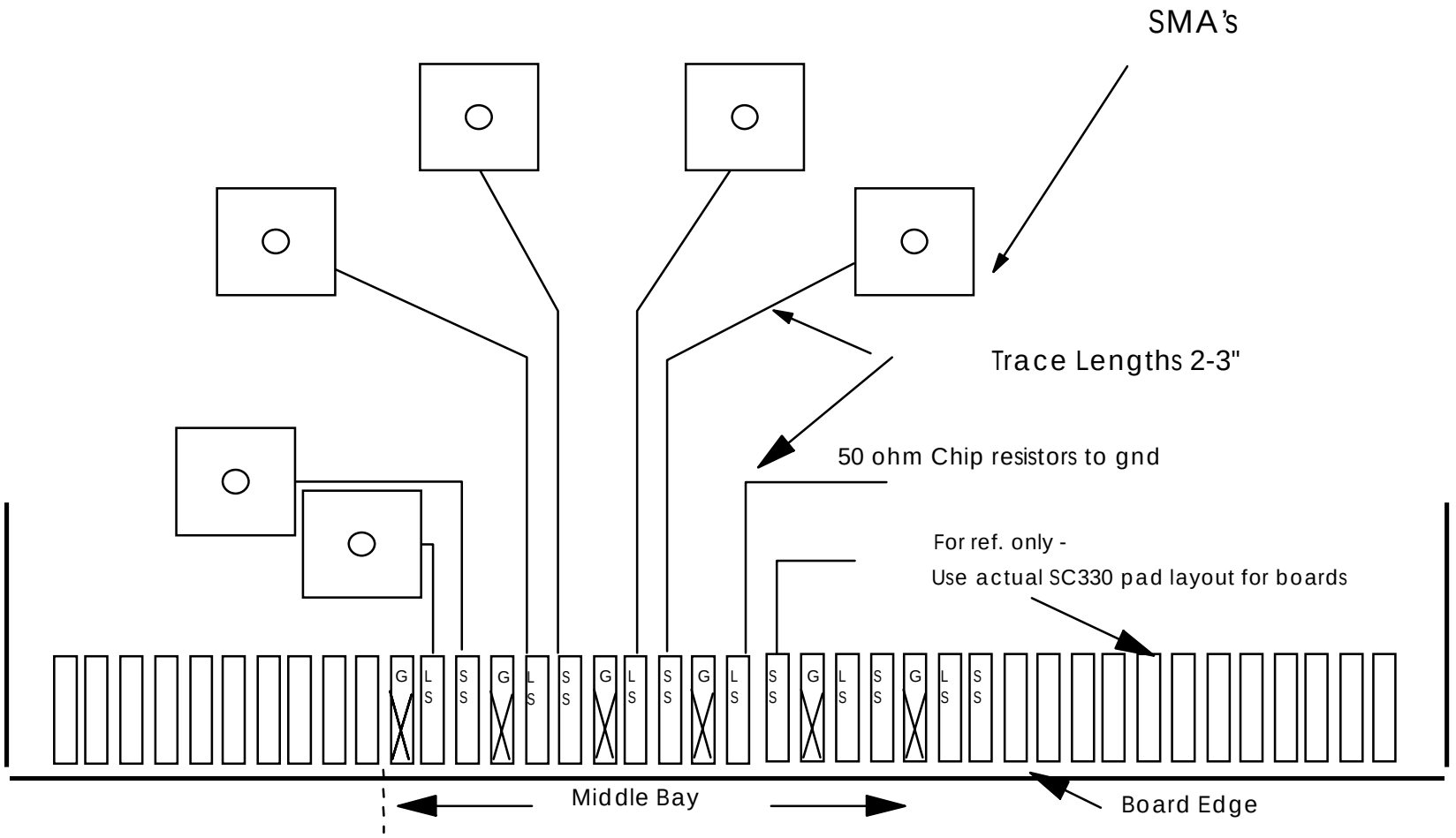


Figure 12: CPU Test Board Layout: Primary (Processor) Side

SC330 CPU Test Board Layout:

Secondary Side

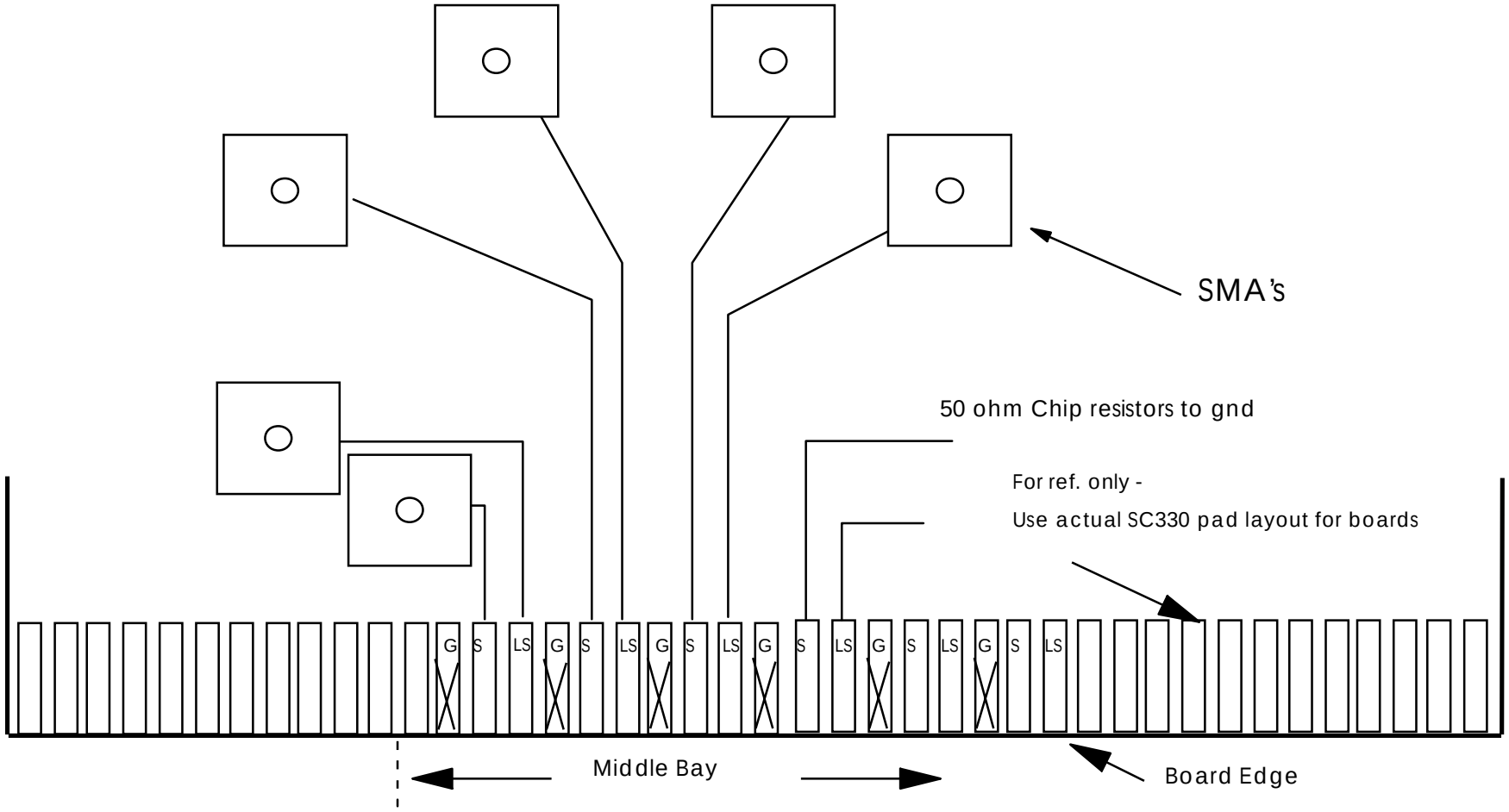


Figure 13: CPU Test Board Layout: Secondary Side

4. ENVIRONMENTAL REQUIREMENTS

Design, including materials, shall be consistent with the manufacture of units that meet the following environmental reference points:

4.1. Temperature Range:

4.1.1. Operating:

0ºC to + 85ºC.

4.1.2. Shipping and Storage:

-40ºC to + 105ºC.

4.1.3. Temperature Life:

This test to be performed as per EIA 364, Test Procedure 17. Precondition samples with three insertion/extractions (min). The connectors (mated) shall withstand a minimum of 240h of the maximum operating temperature (85°C) plus the maximum recorded temperature rise for the contact due to electrical heating in **Section 3.2** plus 2°C. For example, if Maximum Temperature Rise is 8°C, then Temperature Life will be performed at (85°C + 8°C + 2°C) = 95°C. **The Test Temperature MUST be recorded.**

4.2. Visual Inspection:

Connector must meet mechanical requirements as specified in **Section 2.**

4.3. Vibration, Random:

Frequency Range: 5Hz to 500Hz

Vibration test to be performed for two durations:

Duration 1: 10min/axis (derived from Intel Corporation customary board vibration specifications).
Power Spectral Density (PSD) Profile: **Table 2** presents the PSD profile used for the vibration testing. (Logarithmic interpolation is used in **Table 2**.)
Sample Size: 4 for contact resistance, 4 for electrical discontinuity.

Duration 2: 45min/axis for long term reliability from fretting corrosion perspective (10min test PSD reduced by S-N factor for extended time).
PSD Profile: **Table 3** presents the PSD profile used for the vibration testing. (Logarithmic interpolation is used in **Table 3**.)
Sample Size: 4 for contact resistance, 4 for electrical discontinuity

Axes Orientation: Schematic of X, Y and Z axes orientation in connector/SECC assembly is shown in **Figure 14**.
Input Accelerometer Location: Input (Control) accelerometer to be mounted at midlength of the connector housing on the side opposite the heatsink.

Connector must meet all the electrical contact resistance requirements following random vibration test. No electrical discontinuities > 1.0µs. The connector must be mated with the mechanical sample outlined in **Section 6.7.3** and retained with mechanical supports per MIL-STD-C-55302.

Table 2: PSD Data for Vibration Test - 10min/axis

X Axis		Y Axis		Z Axis	
Freq. (Hz)	PSD (g^2/Hz)	Freq. (Hz)	PSD (g^2/Hz)	Freq. (Hz)	PSD (g^2/Hz)
5	0.01	5	0.01	5	0.01
50	0.02	20	0.02	20	0.02
350	0.03	100	0.02	100	0.05
500	0.07	130	0.035	130	0.25
		470	0.035	220	0.23
		500	0.1	350	0.015
				500	0.015
GRMS = 3.98		GRMS = 4.05		GRMS = 6.33	

Table 3: PSD Data for Vibration Test – 45min/axis

X Axis		Y Axis		Z Axis	
Freq. (Hz)	PSD (g^2/Hz)	Freq. (Hz)	PSD (g^2/Hz)	Freq. (Hz)	PSD (g^2/Hz)
5	0.0049	5	0.0049	5	0.0049
50	0.0098	20	0.0098	20	0.0098
350	0.0147	100	0.0098	100	0.0245
500	0.0343	130	0.0172	130	0.123
		470	0.0172	220	0.113
		500	0.049	350	0.00735
				500	0.00735
GRMS = 2.79		GRMS = 2.84		GRMS = 4.43	

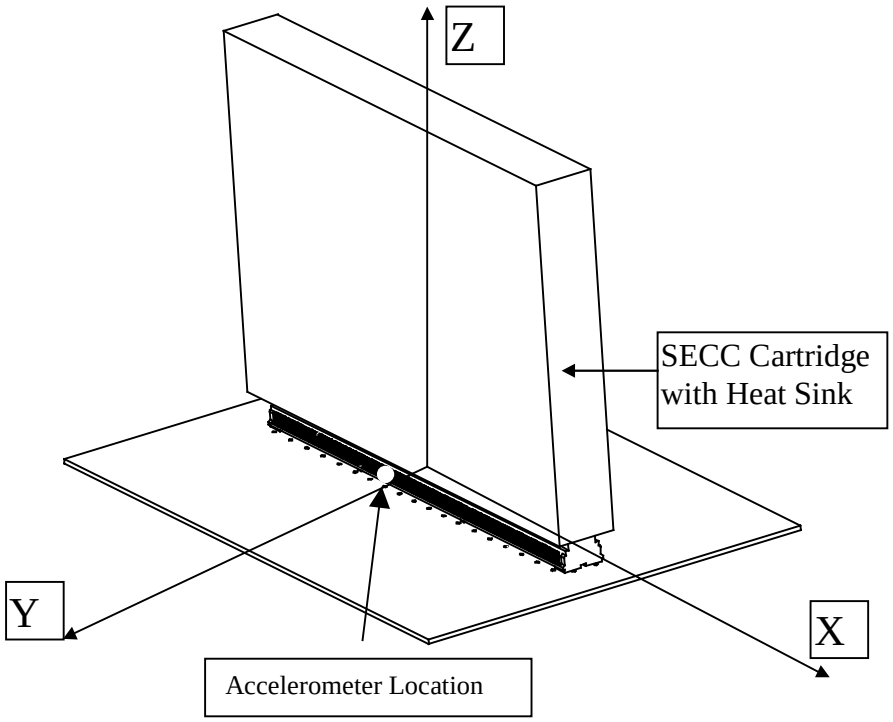


Figure 14: Schematic of Axes Orientation for Vibration Test

4.4. Shock:

Tested per EIA 364, Test Procedure 27, Test Condition A: 100G, 6ms duration, Sawtooth waveform. Three shocks applied in each of three perpendicular axes (18 total). No electrical discontinuities > 1.0μs. The connector must be mated with the mechanical sample outlined in **Section 6.7.3** and retained with mechanical supports per MIL-STD-C-55302.

4.5. Durability:

Mate and unmate samples for 50 cycles at a rate of 500cph (max), using the same substrate. Same substrate to be used for 1st and 51st cycles. Measure contact resistance when mated in 1st and 51st cycles. A spare substrate is used for 2nd through 50th cycles. **A pair of New Substrates to be used for each of the connector samples**.

4.6. Mating Force:

EIA 364, Test Procedure 13: Force necessary to mate Steel Gauge (see **Figure 1**) to samples at a maximum rate of 0.5in/min. **Total force < 35lb, per Section 2.6.**

4.7. Unmating Force:

Force necessary to unmate Steel Gauge (see **Figure 1**) from samples at a maximum rate of 0.5in/min. Test performed similar to **Section 4.6** except Steel Gauge is extracted. **Total extraction force < 20lb, per Section 2.7.**

4.8. Thermal Shock:

-55ºC to +85ºC, 5 cycles per EIA 364, Test Procedure 32. Test Group 4 (see **Table 4**) unmated and unmounted for this test. Test group 5 mated and mounted for this test.

4.9. Humidity Temperature Cycling:

25ºC to 65ºC at 90% to 95% RH (non-condensing) for 10 days per EIA 364, Test Procedure 31, Method 3.

4.10. Mixed Flowing Gas:

Precondition samples with three insertion and extractions (min) using a new substrate that has not gone through the mixed flowing gas test. Testing shall be performed in accordance with EIA 364, Test Procedure 65, Class 2A. The test is to be performed as follows: The samples are exposed unmated to the mixed flowing gas for one day, and then mated for the remaining ten days of the test.

4.11. Solder Withstand Temperature:

Ramp temperature at rate of 1ºC to 3ºC/s to 145ºC for 2min, then ramp to 225ºC for 40s. Test per EIA 364, Test Procedure 56, Procedure 3.

4.12. Porosity:

For plating outlined in **Section 2.2.3 (1),** use EIA 364, Test Procedure 53, Nitric acid test. For plating outlined in **Section 2.2.3 (2),** use EIA 364, Test Procedure 60, Procedure 1.1.2 Sulfur Dioxide test. Test to be performed for randomly selected 10 contacts from each level. That is, 10 contacts from lower, middle and upper rows (levels) of the contact pattern. That is, total of 30 contacts per connector. Requirement: Maximum of **one pore** per set of 10 contacts. That is, only one pore allowed for each of the 10 contacts randomly selected from the lower, middle and upper rows.

4.13. Plating Thickness:

Record minimum thickness of plating on contact surface per EIA 364, Test Procedure 48, Method C. Test to be performed for randomly selected 10 contacts from each level. That is, 10 contacts from lower, middle and upper rows (levels) of the contact pattern. That is, total of 30 contacts per connector.

4.14. Solvent Resistance:

As per EIA 364, Test Procedure 11.

Requirement: No damage to ink markings if applicable.

4.15. Normal Force:

As per EIA 364, Test Procedure 4. Test to be performed for randomly selected 5 contacts from each level. That is, 5 contacts from lower, middle and upper rows (levels) of the contact pattern. That is, total of 15 contacts per connector.

Requirement: Record normal force at a nominal deflection for a substrate thickness of 0.062in + 0.007in / – 0.005in.

4.16. Solderability:

As per EIA 364, Test Procedure 52, Class 2, Category 3.

Requirement: 95% coverage.

4.17. Contact Retention:

As per EIA 364, Test Procedure 29, 300g (minimum) load per individual contact in the direction to unseat the contacts from the housing.

Requirement: No movement > 0.015in (0.38mm)

4.18. Maximum Force on Connector:

No physical damage to connector after application of 150lb to fully seated Substrate. Force applied to top surface of substrate, perpendicular to the motherboard, after the substrate is fully mated with the connector. The force requirement is to accommodate extra load during substrate insertion in a manufacturing assembly environment. This test is independent from the vibration and shock conditions outlined in **Sections 4.3** and **4.4**.

4.19. Contact Backout Wipe:

The maximum contact backout wipe within the connector for the three rows of contacts on the gold finger pads, shown in **Figure 15** and **Figure 16**, is 0.020in (0.5080mm). There shall be no discontinuities or improper connections upon withdrawal of the substrate after the substrate is first bottomed out in the connector. The purpose of this requirement is to allow for assembly and manufacturing tolerances and facilitate in design of the substrate retention system.

4.20. Visual Inspection of Substrate:

Remove the substrate from the S.E.C. cartridge. Inspect for visual evidence of fretting corrosion - i.e. black spots - on contact pads of the substrate. When a pass/fail decision can not be made based on visual inspection of the substrate, one or both of the following two methods will be used as surface analysis for Nickel and/or Copper detection in the contact area.

Method 1: Exposure (dipping into) to Dimethylglyoxime (DMG) solution

Method 2: SEM analysis

Requirement: No visual evidence of fretting corrosion on any contact pad.

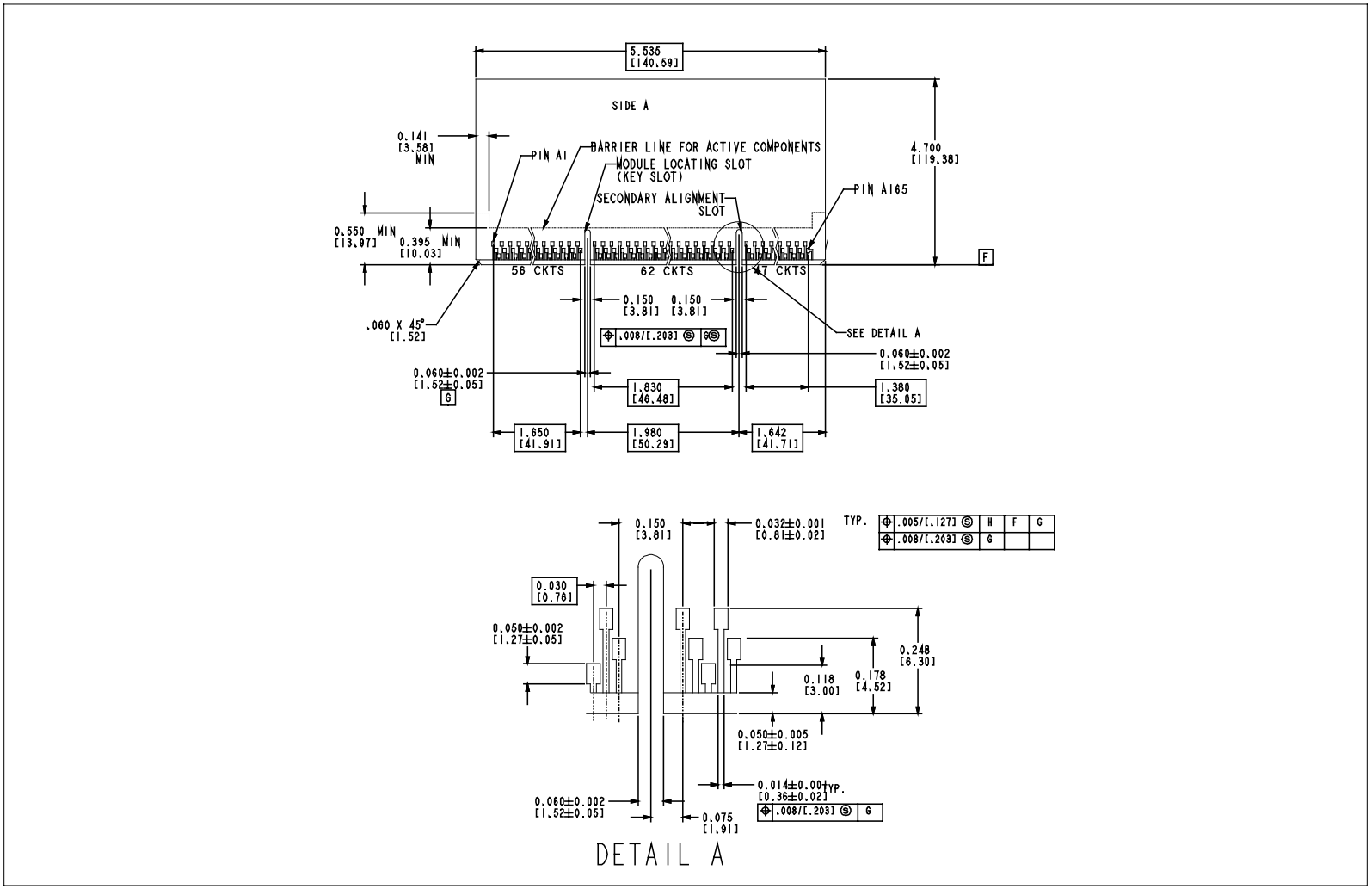


Figure 15: Substrate Form Factor, Primary Side and Key Slot

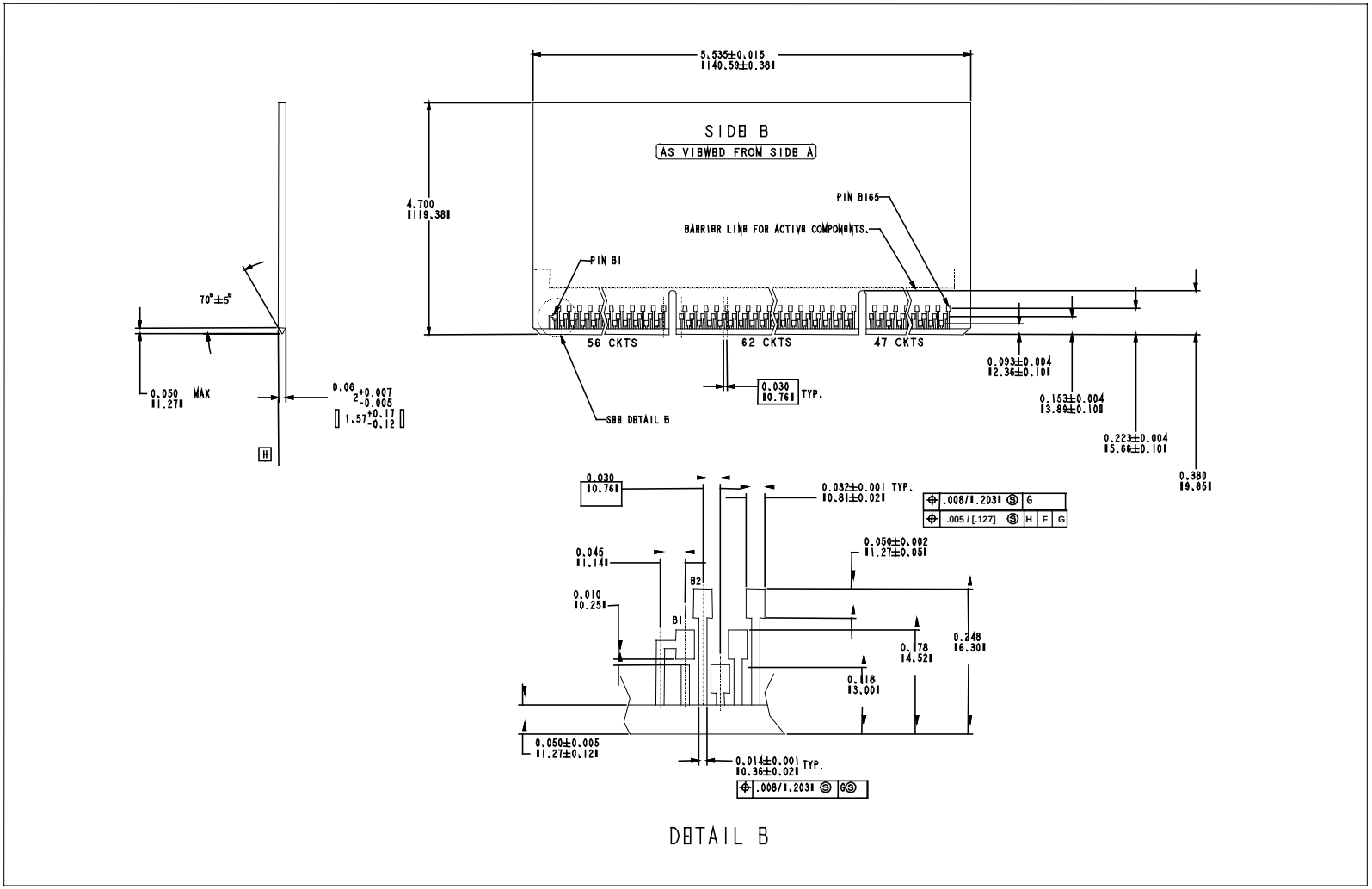


Figure 16: Substrate Form Factor, Secondary Side and Edge Fingers

5. QUALITY ASSURANCE REQUIREMENTS:

Failure to conform to the specifications will result in Corrective Action. The extent of re-qualification (partial or full) will be decided by the customer and supplier.

The supplier shall have, and supply documented measurement procedures and proven measurement capability for all parameters defined in this specification. The supplier shall have documented maintenance and calibration records for all equipment. The supplier shall also have documented records that reflect equipment performance over time and equipment performance to specifications. These records shall be made available to Intel upon request.

Deviation from the inspection methods indicated may be performed for correlated alternative methods. Acceptable correlation data will be furnished to and approved by Intel. The supplier must be able to track the equipment used and show that it is stable and capable.

6. QUALIFICATION TESTING REQUIREMENTS:

This section of the document outlines the tests that must be successfully completed in order for the connector supplier's connector to pass the qualification process. It provides the test plan and procedure required to reach and maintain a qualified test status.

6.1. Applicable Documents:

MIL-STD-C-55302

EIA-364

EIA-364-C

6.2. Production Lot Definition:

A production lot is defined as a separate process run through the major operations including molding, contact stamping, contact plating and assembly. These lots should be produced on separate shifts or days of the week. Lot identification marking needs to be provided to Intel as verification of this process.

6.3. Testing Facility:

Testing will be performed by Intel's designated test facility.

6.4. Funding:

Connector supplier will fund connector qualification testing for their connector. Any additional testing that is required due to design modifications will also be at the expense of the supplier.

6.5. Reporting:

Test reports of the connector qualification testing will be provided directly from the independent test facility to Intel and the Supplier. Intel will also be given access to contact the test facility directly to obtain: connector qualification status, explanation of test results and recommendations based on the test results. Intel and the Supplier will be notified, by the test facility, of any test failure. Intel will also be notified, by the supplier, of any corrective action.

6.6. Process Changes:

By Supplier:

Any significant change to the connector will require submission of a detailed explanation of the change at least 60 days prior to the planned implementation. Intel will review the modification and establish the necessary re-qualification procedure that the connector must pass. Any testing that is required MUST be completed before the change is implemented.

Typical examples of significant changes include, **but are not limited to, the following:** Plastic material changes including base material or color; contact changes including base material, plating material or thickness; and design modifications.

By Intel:

Supplier needs to acknowledge change request within 5 days and submit a plan within10 days. The implementation should comprehend normal and accelerated lead times.

6.7. Connector Test Plan:

6.7.1. Test Flow:

The test flow is outlined in **Section 6.9**. Sample sizes and test requirements are given for each test group. For specific test procedures, refer to the applicable test specifications referenced in **Section 6.1**.

6.7.2. Retest Restrictions:

Failures of particular sections of the test plan for a given connector footprint will require re-testing of at least a portion of the test flow defined in **Section 6.9**. The definition of the tests required will be at Intel's discretion. The modifications that will be made to the connector to improve a failing condition must be provided to Intel in writing and must be approved by Intel prior to retest. If failures occur after retest, further testing will be at Intel's discretion.

6.7.3. Mechanical Samples:

Mechanical samples of the substrate and heat sink (or suitable mockups that approximate size, center of gravity and mass of the assembly) will be used during the mated connector qualification testing. The target weight for the assembly is 1100g (max). This assembly will be specified by Intel.

6.8. Connector Qualification Notification:

Upon completion of the test flow and receipt of test data, Intel will prepare a summary report for the connector supplier that will provide notification as to whether the connector has passed or failed connector qualification testing.

6.9. Connector Qualification:

6.9.1. Sample size per group:

See **Table 4**. Test samples are to be taken from two different lots. Example: if 8 samples are required, 4 samples will be used from two different lots. Each sample shall be prepared in accordance to the documents specified in **Section 6.1**, and selected at random per **Section 6.2**.

6.9.2. Test Sequence:

Each group of samples is tested per the number sequence as outlined in **Table 4**.

Table 4: Qualification Test Sequence:

Test Description Sequence (Reference Section Location)	Test Group										
	1	2	3	4	5	6	7	8	9	10	11
Visual Inspection (4.2)	1,11	1,6	1,6	1,9	1,8	1,5	1,4	1	1	1	1
CTF Dimensional Verification (2.10)	2	2	2	2	2	2	2	2	2	2	2
Contact Resistance (3)	4,6,9	3,5	3,5		3,5,7						
Adjacent Pair Inductance (3.3)										3	
Pin to Pin Capacitance (3.4)										4	
Insulation Resistance (3.5)				3,7							
Dielectric Withstand Voltage (3.6)				4,8							
Characteristic Impedance (3.7), Crosstalk Coupling (3.8), and Propagation Delay (3.9)										5	
Vibration (4.3)	8										
Shock (4.4)	7										
Durability (4.5)	5										
Mating Force (4.6)	3										
Unmating Force (4.7)	10										
Thermal Shock (4.8)				5	4						
Humidity Temperature Cycling (4.9)				6	6						
Temperature Life (4.1.3)		4									
Mixed Flowing Gas (4.10)			4								
Resistance to Solder Heat (4.11)							3				
Porosity (4.12)								3			
Plating Thickness (4.13)								4			
Solvent Resistance (4.14)									4		
Normal Force (4.15)								5			
Solderability (4.16)								6			
Contact Retention (4.17)									3		
Maximum Force on Connector (4.18)						3					
Contact Backout Wipe (4.19)						4					
Contact Current Rating (3.2)											3
Substrate Visual Inspection (2.1.1)	12										
Sample Size per Test Group	16	8	4	8	8	4	4	4	4	4	4

7. SAFETY REQUIREMENTS

Design, including materials, shall be consistent with the manufacture of units that meet the following safety standards:

UL Recognition.

CSA Certified.

8. DOCUMENTATION REQUIREMENTS

The connector supplier shall provide Intel with the following documentation:

Multi-Line SPICE models for connector.

Product specification incorporating the requirements of this specification.

Recommended board layout guidelines for the connector consistent with low cost, high volume printed circuit board technology.

The test facility shall provide Intel and the supplier with the following document:

Qualification Testing and Test Report supporting successful compliance with this specification.

UNITED STATES, Intel Corporation
2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA 95052-8119
Tel: +1 408 765-8080

JAPAN, Intel Japan K.K.
5-6 Tokodai, Tsukuba-shi, Ibaraki-ken 300-26
Tel: + 81-29847-8522

FRANCE, Intel Corporation S.A.R.L.
1, Quai de Grenelle, 75015 Paris
Tel: +33 1-45717171

UNITED KINGDOM, Intel Corporation (U.K.) Ltd.
Pipers Way, Swindon, Wiltshire, England SN3 1RJ
Tel: +44 1-793-641440

GERMANY, Intel GmbH
Dornacher Strasse 1
85622 Feldkirchen/ Muenchen
Tel: +49 89/99143-0

HONG KONG, Intel Semiconductor Ltd.
32/F Two Pacific Place, 88 Queensway, Central
Tel: +852 2844-4555

CANADA, Intel Semiconductor of Canada, Ltd.
190 Attwell Drive, Suite 500
Rexdale, Ontario M9W 6H8
Tel: +416 675-2438

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