



Dual Memory Clock Generator Design Guidelines

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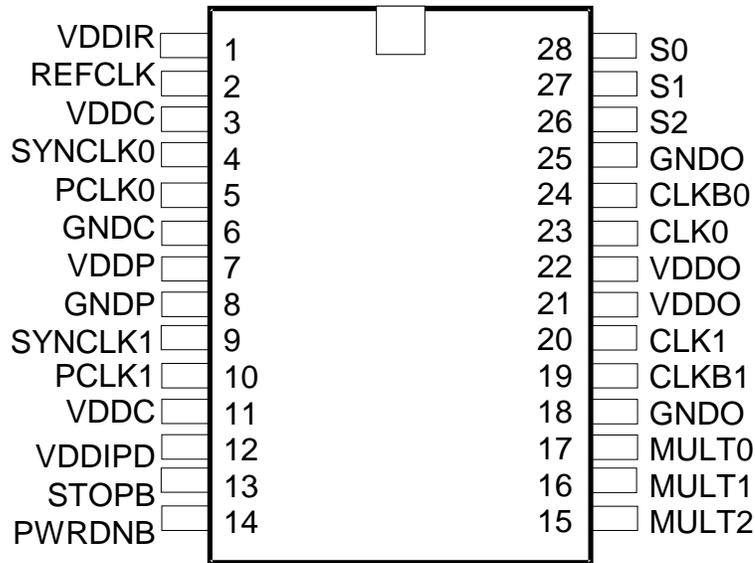
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Pin-out**Pin Description Table**

Pin	Type	Symbol	Description
28	Input	S0	Mode select
27	Input	S1	Mode select
26	Input	S2	Mode select
13	Input	STOPB	Active Low Output Disable for CLK[0:1]/CLKB[0:1]
14	Input	PWRDNB	Active Low Power Down
17	Input	MULT0	PLL Multiplier Select
16	Input	MULT1	PLL Multiplier Select
15	Input	MULT2	PLL Multiplier Select
2	Input	REFCLK	Reference Clock
5	Input	PCLK0	Phase Detector
10	Input	PCLK1	Phase Detector
4	Input	SYNCLK0	Phase Detector
9	Input	SYNCLK1	Phase Detector
23	Output	CLK0	Output Clock
24	Output	CLKB0	Output Clock complement
20	Output	CLK1	Output Clock
19	Output	CLKB1	Output Clock complement
1	Reference	VDDIR	Reference voltage for REFCLK
12	Reference	V _{DD} IPD	Reference Voltage for Phase Detector Inputs and STOPB
7	Power	VDDP	VDD for PLL
8	Ground	GNDP	Ground for PLL
3, 11	Power	VDDC	Power for phase aligners
6	Ground	GNDC	Ground for phase aligners
21, 22	Power	VDDO	Power for output clocks
18, 25	Ground	GNDO	Ground for output clocks

Electrical Characteristics

The Dual Memory Clock Generator is a functional extension of the Direct Rambus* Clock Generator (DRCG) and maintains memory channel signal integrity. For DRCG details, please see www.rambus.com. The DMCG definition allows higher supply currents than the DRCG:

Supply Current Projections

Symbol	Parameter	Minimum	Maximum	Unit
I _{POWERDOWN}	Current in Power-down state (PWRDNB = 0)	---	200	μA
I _{CLKSTOP}	Current in Clk Stop state (STOPB = 0)	---	140	mA
I _{NORMAL}	Current in Normal state (STOPB = 1)	---	200	mA

Gear Ratio Select

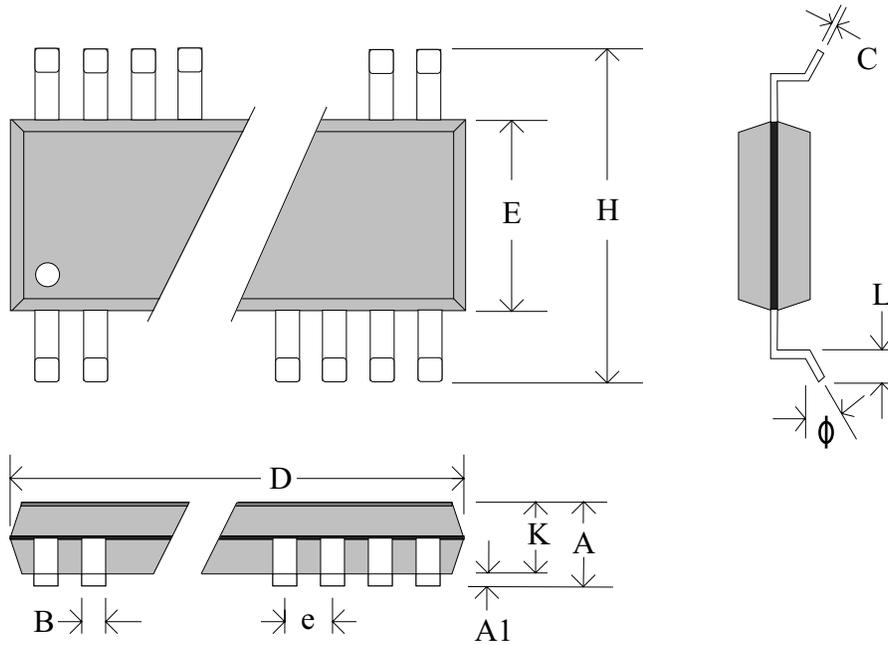
MULT0	MULT1	MULT2	GEAR RATIO
0	0	0	4:1
0	0	1	9:2
0	1	0	6:1
0	1	1	TBD by Intel
1	0	0	8:3
1	0	1	16:3
1	1	0	8:1
1	1	1	TBD by Intel

Bypass and Test Mode Select

S0	S1	S2	Mode	CLK[0:1]	CLKB[0:1]
0	0	0	Normal	CLK	CLKB
0	0	1	Supplier Test		
0	1	0	OE	Hi-Z	Hi-Z
0	1	1	OE	Hi-Z	Hi-Z
1	0	0	Bypass	Non-aligned CLK	Non-aligned CLKB
1	0	1	Supplier Test		
1	1	0	Test	REFCLK	REFCLKB
1	1	1	Reserved		

Mechanical Package Outline Drawings

Devices should be made available in a 28-pin TSSOP. Other package options can include 28-pin SSOP and 28-pin QSOP packages.



28 TSSOP: Table of Dimensions (mm, unless otherwise specified)

Body		Symbol										
		E	H	C	L	ϕ	D	K	A	A1	e	B
28 pin (9.7mm)	Min	4.3	6.25	0.09	0.5	0°	9.6		-	0.05	0.65	0.19
	Max	4.5	6.50	0.20	0.7	8°	9.8	1.10	-	0.15		0.30