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PGA370 Processor Bus Terminator Design Guidelines

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1.0 INTRODUCTION

Intel$^®$ Pentium$^®$ III processor has termination circuitry for the processor's AGTL+ bus. In a two-processor platform, each end of the bus must be properly terminated, whether or not both processor socket locations have processors installed. This document describes the design considerations for a PGA370 termination package to occupy the second PGA370 socket location and terminate the bus when there is only one processor installed in a two-processor platform.

Although there are other possible methods to implement a bus termination package, Intel recommends that designs adhere to the bus guidelines in Section 3. The resistor and decoupling network schematics in this document are examples only. Other resistor and decoupling designs are also feasible. This document does not provide detail on variations to the specific design solution presented.

2.0 TERMINATION PACKAGE REFERENCE SCHEMATICS

Figures 1 shows the names of the corresponding signals that interface through the PGA370 socket.

Figures 2 and 3 are examples of 68-ohm termination resistor networks implemented with four-resistor packages that have two separate connections for each resistor element. Note that the maximum power for each resistor is 0.06 W (i.e., 0.20 W/four-pack of resistors) and that this is the maximum power per resistor that will need to be dissipated.

Figure 4 is a capacitor decoupling network between V_{TT} and ground to prevent V_{TT} noise interference (voltage drop) on the bus signals. This interference is caused by the potentially large current draw through the V_{TT} power distribution plane (or trace) to the termination resistors.
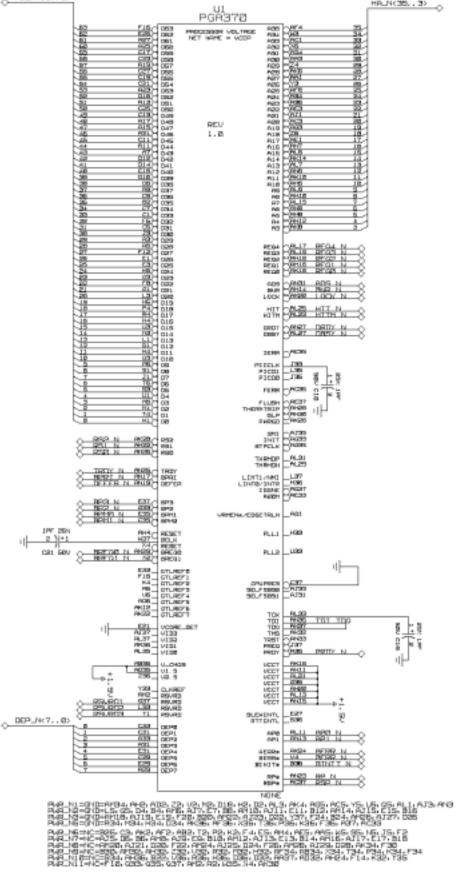
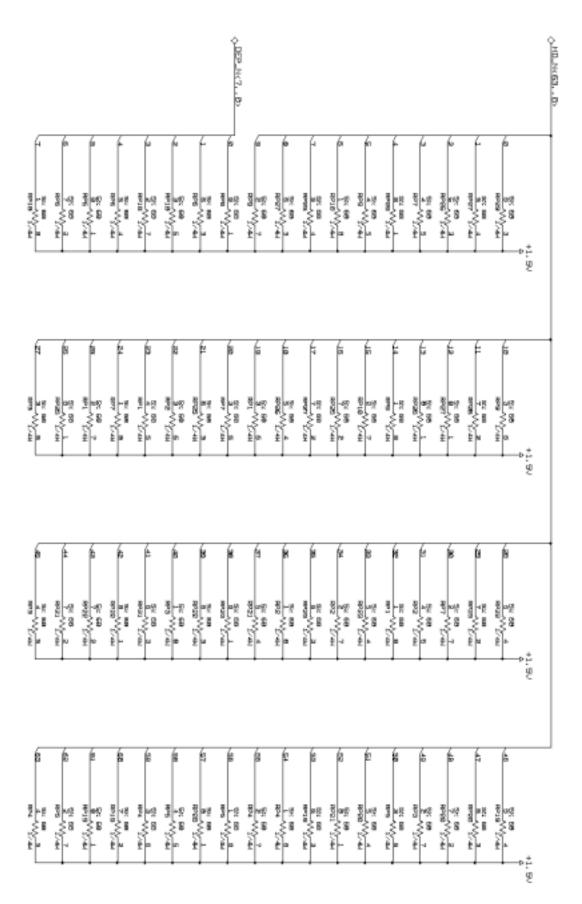**Figure 1 Signals on PGA370 Connector**

Figure 2 68-Ohm Termination Resistors

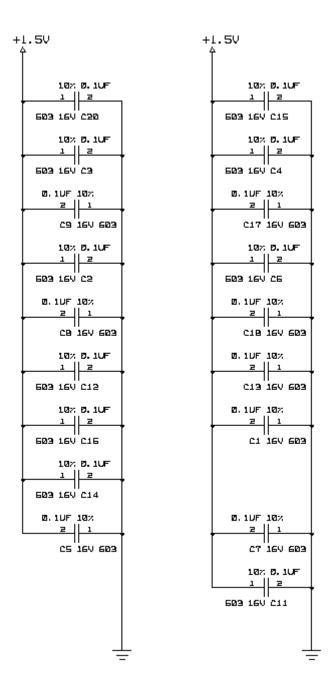Figure 3 68-Ohm Termination Resistors

Figure 4 Termination Decoupling

3.0 Stack-up

This section defines the thickness and functionality (type) of each layer. The section on routing provides specific routing rules for each group of nets.   The preferable stack-up is a 4-layer substrate (shown in Figure 5, below). The thicknesses of the metal and dielectric layers are given in Table 1 below. These thicknesses are representative and can be altered by various substrate suppliers as long as the characteristic impedance (Zo) target of 60 Ohms ± 15% is met. The total thickness of the substrate shall be 0.063 + 0.007/- 0.005 inches.
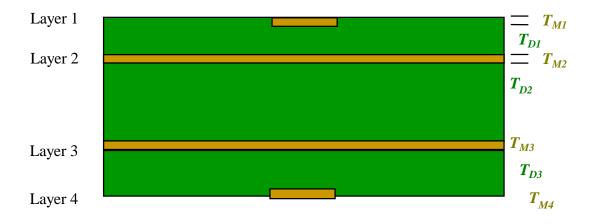
Layer 1 T_{M1}

                T_{D1}

Layer 2 T_{M2}

                T_{D2}

Layer 3 T_{M3}

                T_{D3}

Layer 4 T_{M4}

Figure 5   Reference Substrate Stack-Up

Material		Thickness (mils)	Layer Type
Metal: 1-oz copper	T_{M1}	1.4	Signal 1
Dielectric: FR4-CORE	T_{D1}	6.0*	
Metal: 1-oz copper	T_{M2}	1.4	VCCT
Dielectric: PRE-PREG	T_{D2}	44.0*	
Metal: 1-oz copper	T_{M3}	1.4	GND
Dielectric: FR4-CORE	T_{D3}	6.0*	
Metal: 1-oz copper	T_{M4}	1.4	Signal 2

Table 1: Thickness of Metals and Dielectrics of the Substrate Stack-Up

*This can be whatever thickness is required to reach a target Zo of 60 Ohms. Even the copper thickness can be 0.5 oz as long as Zo condition is met. The total board thickness is to be 62 mils. If this is less than 62 mils, the PRE_PREG thickness can be decreased accordingly.

4.0 AGTL+ Bus Guidelines

The design should follow the AGTL+ layout guidelines specified in the *Pentium® II Processor Developer's Manual*. Some of these guidelines include:

- Use a four layer stack-up to get the desired controlled impedance. Route the highest frequency signal traces on the bottom signal layer (BCLK is a must). The ground plane will prevent the signals on the bottom from radiating during EMI testing.

- Limit trace routing on the package from 0.1 to 1.0 inch.

- Add a 1 pF capacitor to the ends of the BCLK, PICCLK, and TCLK clock lines, after 0.5" to 1" of trace.

- Distribute V_{TT} by a dedicated plane. A plane is recommended; however, a 50 mil minimum width trace may also be used.

- Closely control the characteristic line impedance, Z_0, to a 51Ω - 69Ω range. A ground plane will be needed to maintain the proper characteristic line impedance. This impedance reflects the motherboard target impedance for the Pentium® III FC-PGA processor.

- The 35 R-packs(for terminating 140 AGTL+ lines) must be distributed equally on either side of the substrate inside the socket cavity area with a minimum spacing of 125 mils from the pins on the secondary side. The capacitors must also be distributed equally. Due to space constraints while routing, 1206 resistor packs and 0603 capacitors are recommended.

- Make sure power routings are decoupled correctly. Due to severe space constraints, it is necessary to put 1 Vtt decoupling capacitor for every two R-packs.

- A PCB signal velocity of 1.6 to 2.0 ns/ft should be used as the signal layers are fast microstrips.

- The following have to be set in the termination package:
    1. TDI and TDO have to be connected together.
    2. The VID signals have to be no-connects.
    3. The Vtt (1.5V) and Vcmos pins have to shorted through a wide trace (preferably about 1000 um wide, or at least the width of the pin pad rings).
    4. The Vtt pins of the R-packs have to be close to the capacitors.
    5. Use short and wide traces for Vtt and Vss for the escapes on the signal layers.
    6. The VcoreDet pin and the CPUPreset pin have to be tied to ground.
    7. The SELFSB pins must be no-connects.
    8. VRMEN# (AG1) must be a no-connect.
    9. RESET# (AH4, AM2 and X4) must be no-connects.
    10. CLKREF (Y33 and X34) must be no-connects.

- Minimize cross talk:

    1. Maximize line-to-line spacing (at least 10 mils between traces). Use a 5/15 rule where possible.

    2. Keep the dielectric constant used on the termination card between 4.2 and 4.6.

    3. Minimize the cross sectional area of the traces, (5 mil lines with 1/2 ounce/ft^2 copper – but beware of higher resistively traces).

    4. Isolate AGTL+ signals in groups. That is, route the data signals in one group, the control signals in one group, and the address signals in another group. If the groups are routed together over a plane, provide at least 25 mils separation between the groups.

Conventional "pull-up" resistor networks may not be suitable for termination. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). The packages generally have too much inductance to maintain the voltage and current needed at each resistive load. Platforms usually get better results with discrete resistors, resistor packages with two separate pins for each resistor, or other resistor networks with acceptable characteristics.

For additional information on the how to properly route the AGTL+ bus, please refer to the *Pentium*® *II Processor AGTL+ Guidelines.*

5.0 Termination Package Physical Description

The terminator pins must properly mate with the PGA370-pin socket shown in Figure 6 (see *PGA370 Connector Design Guidelines)*. Figure 7 shows a physical format template for the termination package.
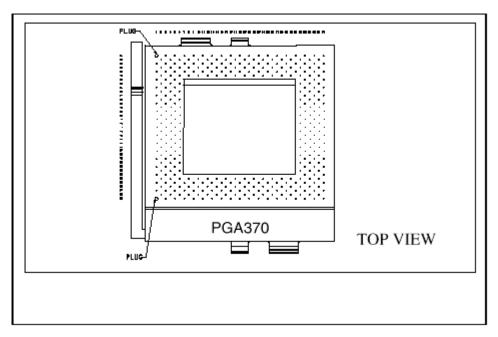

Figure 6 PGA-370 socket

6.0 TERMINATION PACKAGE RETENTION

Original Equipment Manufacturers (OEM) install retention mechanisms on their platforms to ensure the mechanical integrity of systems with PGA370 socket processors. Depending on OEMs' specific shock and vibration specifications, the bus termination package may require a retention mechanism to remain secure. The requirements for such a mechanism are determined by each computer OEM.

The bus termination package should be physically compatible with the same retention mechanism used for current PGA370 processors. For specifics on Intel-defined retention mechanisms, OEMs should request the appropriate drawings from their preferred suppliers.
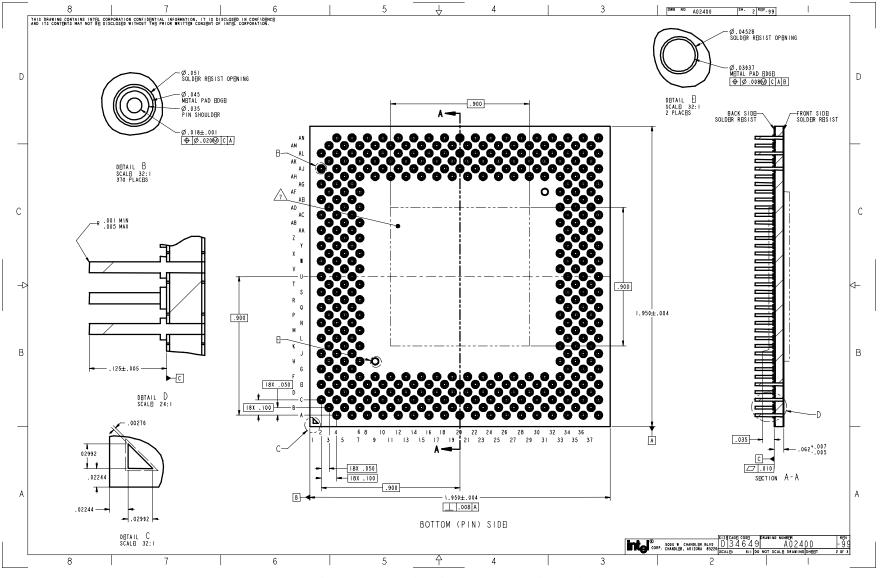
Figure 7 Termination Package Dimensions