Intel® Pentium® III Processor with 512KB L2 Cache Dual Processor Platform Design Guide

June 2001

Document Number 249658-001

Contents

Index of Figures

Index of Tables

Revision History

Revision	Draft/Changes	Date
-001	Initial Version	June 2001

This page intentionally left blank

Design Guide Introduction 1

This design guide documents Intel's design recommendations for dual-processor systems based on the Intel® Pentium® III Processor with 512KB L2 Cache and the Intel® Pentium® III Processor (CPUID 068xh) with AGTL signalling capability for use with the ServerWorks* HE-SL chipset. In addition to providing motherboard design recommendations such as layout and routing guidelines, this document will also address possible system design issues such as processor power delivery, layout considerations for mechanical pieces, EMI design impacts and system bus decoupling.

Please note that this document describes the design recommendations that are driven by the Intel® Pentium® III Processor with 512KB L2 Cache's specifications. Because of this, the recommendations explicity mentioned the Intel® Pentium® III Processor with 512KB L2 Cache in most places. The Intel® Pentium® III Processor (CPUID 068xh) with AGTL signalling capability is compatible with systems designed to the recommendations in this document and will operate in its AGTL compatible mode when placed in the system.

Carefully follow the design information, board schematics, debug recommendations and system checklist presented in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two categories below.

- **Design Recommendations** are items based on Intel's simulations and lab experience to date and are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- **Design Considerations** are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as an example, but may not be applicable to your particular design.

1.1 Audience

This document is targeted at the following audience:

- Intel® Pentium® III Processor with 512KB L2 Cache system developers;
- System developers modifying an existing PGA370 socket dual-processing platform to be Intel® Pentium® III Processor with 512KB L2 Cache ready.

1.2 Related Documents

The reader of this specification should also be familiar with the material and concepts presented in the following documents [1,2]:

Document	Intel Order Number
P6 Family of Processors Hardware Developer's Manual	244001
IA-32 Processors and Related Products 1999 Databook	243565
370-Pin Socket (PGA370) Design Guidelines	244410
Intel® Pentium® III Processor with 512KB L2 Cache Datasheet	249657

Document	Intel Order Number
Intel® Pentium® III Processor in the FC-PGA2 Package Thermal Design Guidelines	249660
VRM 8.5 DC-DC Converter Design Guidelines	249659
Intel® Pentium® III Processor with 512KB L2 Cache Bus Terminator Design Guide	249661
Intel® Pentium® III Processor (CPUID 06Bxh) BSDL Files	
Intel® Pentium® III Processor with 512KB L2 Cache DP I/O Buffer Models	

NOTE:
1. Unless otherwise noted, this reference material can be found on the Intel Developer's Website located at http://developer.intel.com.
2. For a complete listing of Intel® Pentium® III processor reference material, please refer to the Intel Developer's Website at http://developer.intel.com/design/PentiumIII/

1.3 Conventions and Terminology

For this document, the following terminology applies.

- **Intel® Pentium® III Processor (CPUID 068xh) with AGTL Capability** - Intel® Pentium® III Processor based on Intel's 0.18-micron technology with AGTL (1.25 V_{TT}) interface support. This processor contains 256KB of L2 cache and is dual-processor capable.
- **Intel® Pentium® III Processor with 512KB L2 Cache** - Intel® Pentium® III Processor based on Intel's 0.13-micron (i.e. 1.25V V_{TT} / AGTL) technology. This processor contains 512KB of L2 cache and is dual-processor capable.
- **PGA370 socket** - 370-pin Zero Insertion Force (ZIF) socket which a FC-PGA or FC-PGA2 packaged processor plugs into.
- **FC-PGA** - Flip Chip Pin Grid Array. The package technology used on Intel® Pentium® III Processor (CPUID 068xh) for the PGA370 socket. The FC-PGA package has the processor die exposed.
- **FC-PGA2** - Flip Chip Pin Grid Array 2. The package technology used on the Intel® Pentium® III Processor with 512KB L2 Cache and some Intel® Pentium® III Processors (CPUID 068xh) for the PGA370 socket. The FC-PGA2 package contains an Integrated Heat Spreader which covers the processor die.
- **Keep-out zone** - The area on or near a FC-PGA packaged processor that system designs can not utilize.
- **Processor** - For this document, the term processor is the generic form of the Intel® Pentium® III Processor with 512KB L2 Cache for the PGA370 socket in the FC-PGA2 package.
- **Integrated Heat Spreader (IHS)** - The Integrated Heat Spreader (IHS) is a metal cover on the die and it is an integral part of the CPU. The IHS promotes heat spreading away from the die backside to ease thermal constraints.
- **AGTL compatible processor** - Generic term for Intel® Pentium® III Processors which are compatible with AGTL signalling voltage levels (1.25V). These processors are the Intel® Pentium® III Processor (CPUID 068xh) with AGTL Capability and the Intel® Pentium® III Processor with 512KB L2 Cache.
- **AGTL+ only processor** - Generic term for Intel® Pentium® III Processors which can only use AGTL+ signalling voltage levels (1.5V). These processors are Intel® Pentium® III Processors (CPUID 068xh) which do not have AGTL compatibility.

1.4 State of the Data

The data contained within this document are based on near-production validation testing and silicon characterization.

This page intentionally left blank

General Design Considerations 2

This section documents motherboard layout and routing guidelines for Intel® Pentium® III Processor with 512KB L2 Cache platforms. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Even when the guidelines are followed, critical signals are recommended to be simulated to ensure proper signal integrity and flight time. Any deviation from the guidelines should be simulated.

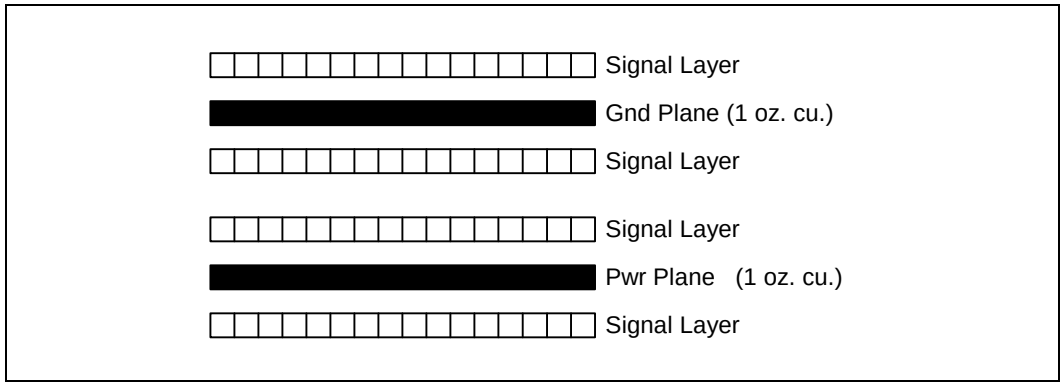
The trace impedance typically noted (i.e., 60Ω +/- 15%) is the “nominal” trace impedance for a 5-mil wide trace. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

2.1 Nominal Board Stackup

An example of a 6-layer stack-up is shown in Figure 2-1. The impedance of all the signal layers should be 60Ω +/- 15%. A lower trace impedance reduces signal edge rates, overshoot, and undershoot, and has less crosstalk than a higher trace impedance. A higher trace impedance increases edge rates and may slightly decrease signal flight times. Please note that thicker core may help reduce board warpage issues.

Figure 2-1. Sample Board Stackup



Additional guidelines on board stack-up, placement, and layout include the following.

- The board impedance (Z) should be between 55 Ω and 75 Ω (65 Ω ± 15% is recommended).
- The dielectric process variation in the PCB fabrication should be minimized.
- The ground plane should not be split on the ground plane layer.
- Keep vias for decoupling capacitors as close to the capacitor pads as possible.

2.2 Socket 370 Component Keepout

Figure 2-2. Socket 370 Component Keepout

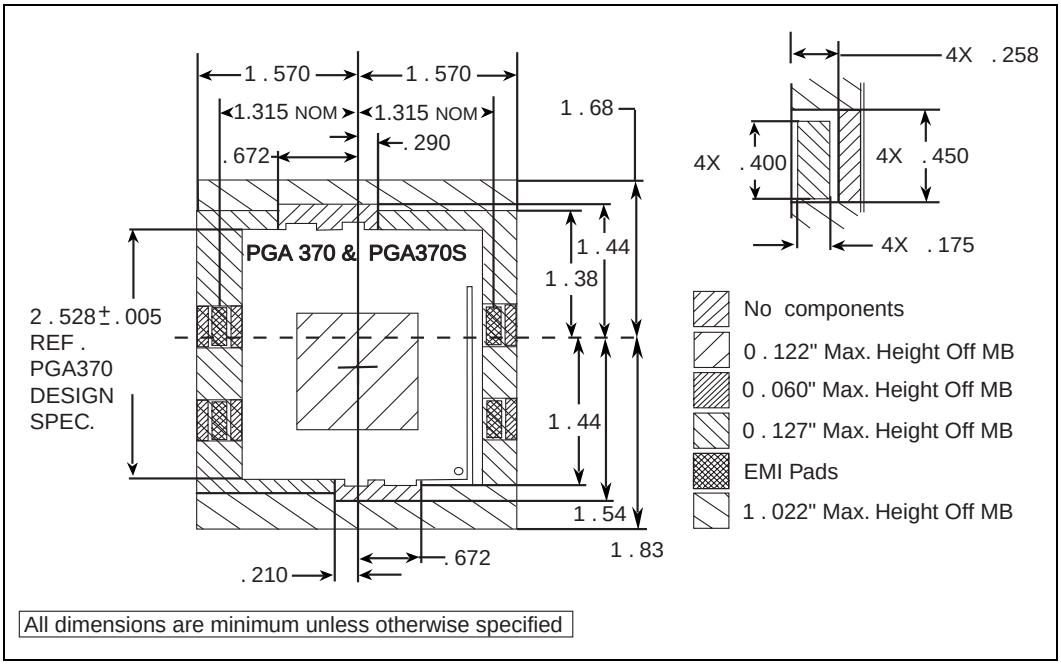
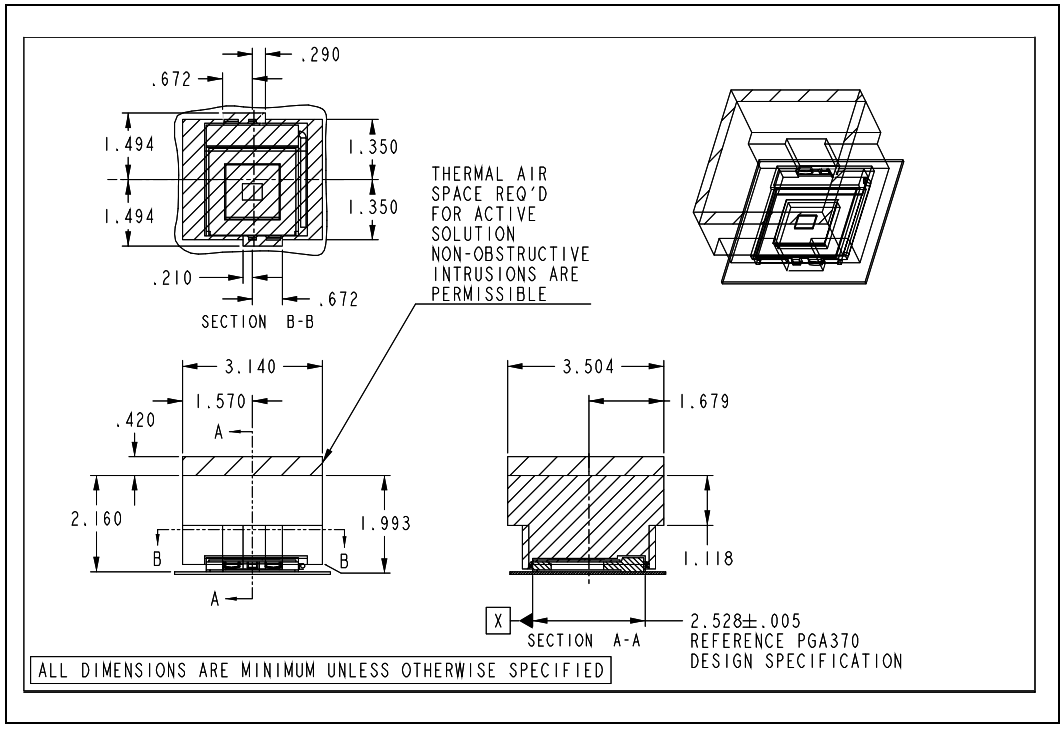


Figure 2-3. Socket 370 Volumetric Keepout



This page intentionally left blank

Processor Host Bus Design 3

3.1 Initial Timing Analysis

To determine the available flight time window, perform an initial timing analysis. Analysis of setup and hold conditions will determine the minimum and maximum flight time bounds for the system bus. Use the following equations to establish the system flight time limits.

Table 3-1. System Timing Equations

Equation
$T_{flight,min} >= T_{hold} - T_{co,min} + T_{skew}$
$T_{flight,max} <= T_{cycle} - T_{co,max} - T_{su} - T_{skew} - T_{jit} - T_{adj}$

Table 3-2. System Timing Terms

Term	Description
T_{cycle}	System cycle time, defined as the reciprocal of the frequency.
$T_{flight,min}$	Minimum system flight time.
$T_{flight,max}$	Maximum system flight time.
$T_{co,max}$	Maximum driver delay from input clock to output data.
$T_{co,min}$	Minimum driver delay from input clock to output data.
T_{su}	Minimum setup time. Defined as the time for which the input data must be valid prior to the input clock.
T_{hold}	Minimum hold time. Defined as the time for which the input data must remain valid after the input clock.
T_{skew}	Clock generator skew. Defined as the maximum delay variation between output clock signals from the system clock generator, the maximum delay variation between clock signals due to system board variation and chipset loading variation, and skew due to delay in the PGA370 socket.
T_{jit}	Clock jitter. Defined as the maximum edge to edge variation in a given clock signal.
T_{adj}	Multi-bit timing adjustment factor. This term accounts for the additional delay that occurs in the network when multiple data bits switch in the same cycle. The adjustment factor includes such mechanisms as package and PCB crosstalk, high inductance current return paths, and simultaneous switching noise.

Component timings for the Intel® Pentium® III Processor with 512KB L2 Cache are available in the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet*. Please contact your chipset vendor for documentation concerning the chipset component timing.

Recommended values for system timings are contained in Table 3-3. Skew and jitter values for the clock generator device come from the clock driver datasheet. The PCB skew specification is based on the results of extensive simulations at Intel. The T_{adj} value is based on Intel's experience with systems that use previous generations of processors.

Table 3-3. System Bus Timing Parameters

Timing Term	Value
T_{skew} [ns]	0.250
T_{jit} [ns]	0.2
T_{adj} [ns]	0.5
T_{cycle} [ns]	7.5

The flight time requirements for CPU to CPU transfers that result from using the component timing specifications and recommended system timings are summarized in Table 3-4. All component values should be verified against the latest specifications before proceeding with analysis.

Table 3-4. Sample CPU to CPU flight time calculations

Driver	Receiver	Calculation
CPU	CPU	$T_{flight,min}$ >= 1.0 - 0.4 + 0.25 = 0.85 ns
CPU	CPU	$T_{flight,max}$ <= 7.5 - 3.25 - 0.95 - 0.25 - 0.2 - 0.5 = 2.35 ns

3.2 General Topology and Layout Guidelines

Intel is recommending that all Intel® Pentium® III Processor with 512KB L2 Cache dual-processing platforms use a system bus T-topology. Figure 3-1 shows a high level diagram of this topology. The pull-up resistors shown inside the processor packages are the processor's on-die AGTL termination. Since the processor has on-die termination, a dual processor capable system must either have two processors installed, or one processor and one terminator.

Figure 3-1. System Bus T-Topology

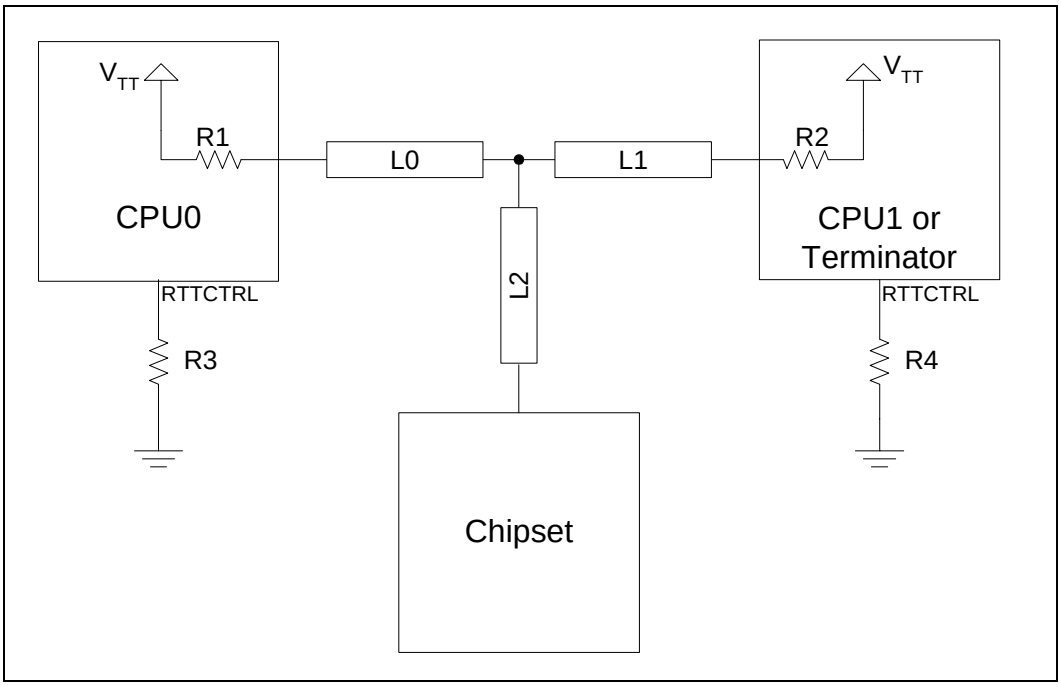


Table 3-5 contains the length specifications for the segments of the T-topology. Please note that lengths L0 and L1 must be length matched to within 0.25 inches. Table 3-6 contains the component values which should be used for this topology.

Table 3-5. Trace Lengths for T Topology (ServerWorks Chipset)

Segment	Min Length (inches)	Max Length (inches)
L0	3.25	3.75
L1	3.25	3.75
L2	1.75	2.5

Table 3-6. Component Values for T Topology

Reference	Value	Tolerance
R1 (on chip)	68Ω	10%
R2 (on chip)	68Ω	10%
R3	68Ω	1%
R4	68Ω	1%

3.3 Terminator-less T Topology

For dual processor platform designs without a terminator, the following new T topology is recommended. A new segment (L3) with a pull-up resistor to Vtt has been added to provide termination when the CPU1 socket is not populated. The L3 segment should be connected as close to the CPU1 pin as possible, preferably after the L1 segment connects to the CPU1 pin. The R4 value for CPU1 uses a 100Ω resistor pulled down to Vss instead of the 68Ω that is normally recommended. CPU0's R3 value should remain 68Ω.

Please Note: Intel will not be validating the terminator-less T topology design. This design is based on extensive simulation results that have been performed by Intel. It is provided as a reference for designs seeking to not require a terminator when the system is operating with one processor. Intel recommends that any implementation of this topology be simulated and validated carefully.

Figure 3-2. Terminator-less System Bus T Topology

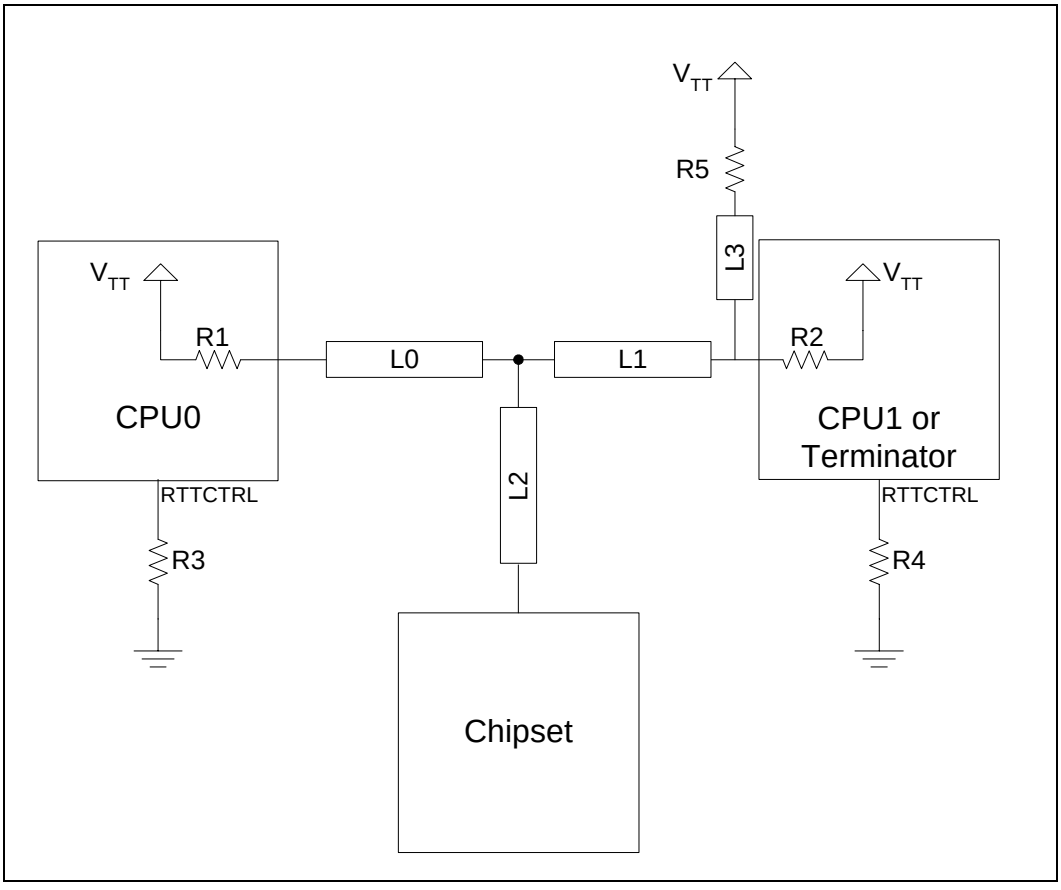


Table 3-7. Trace Lengths for Terminator-less T Topology (ServerWorks Chipset)

Segment	Min Length (inches)	Max Length (inches)
L0	3.25	3.75
L1	3.25	3.75
L2	1.75	2.5
L3	0.0	1.0

Table 3-8. Component Values for Terminator-less T Topology

Reference	Value	Tolerance
R1 (on chip)	68Ω	10%
R2 (on chip)	100Ω	15%
R3	68Ω	1%
R4	100Ω	1%
R5	100Ω	10%

3.4 Wired-OR Signal Considerations

The Wired-OR signals of the processor's host bus require additional consideration. The Wired-OR signals in an Intel® Pentium® III Processor with 512KB L2 Cache system are HIT#, HITM#, BNR#, AERR#, BERR#, and BINIT#. The Wired-OR signals may be driven by multiple bus agents at the same time, such as both processors asserting the HIT# signal to signify a cache hit on a line they both contain. With multiple driving agents, these signals are susceptible to being overdriven which results in excessive overshoot and ringback on these signals.

Terminating the Wired-OR signals at the chipset branch of the T topology will reduce the effect of multiple driving agents on these signals. Intel recommends that system designers carefully examine the signal integrity of these signals and optionally implement the circuit shown in Figure 3-3. This recommendation will work correctly for systems designed with the standard T topology or the terminator-less T topology.

Please note that the incorporation of Wired-OR termination is optional. Intel has not seen any failures on systems which do not implement the Wired-OR termination recommendations. Therefore, systems which are already in the latter phases of design may wish to forego implementing these recommendations until an opportunity presents itself to incorporate them. However, it is the responsibility of the system designer to ensure that the signal quality of these signals meet the component specifications.

Figure 3-3. Wired-OR Termination Topology

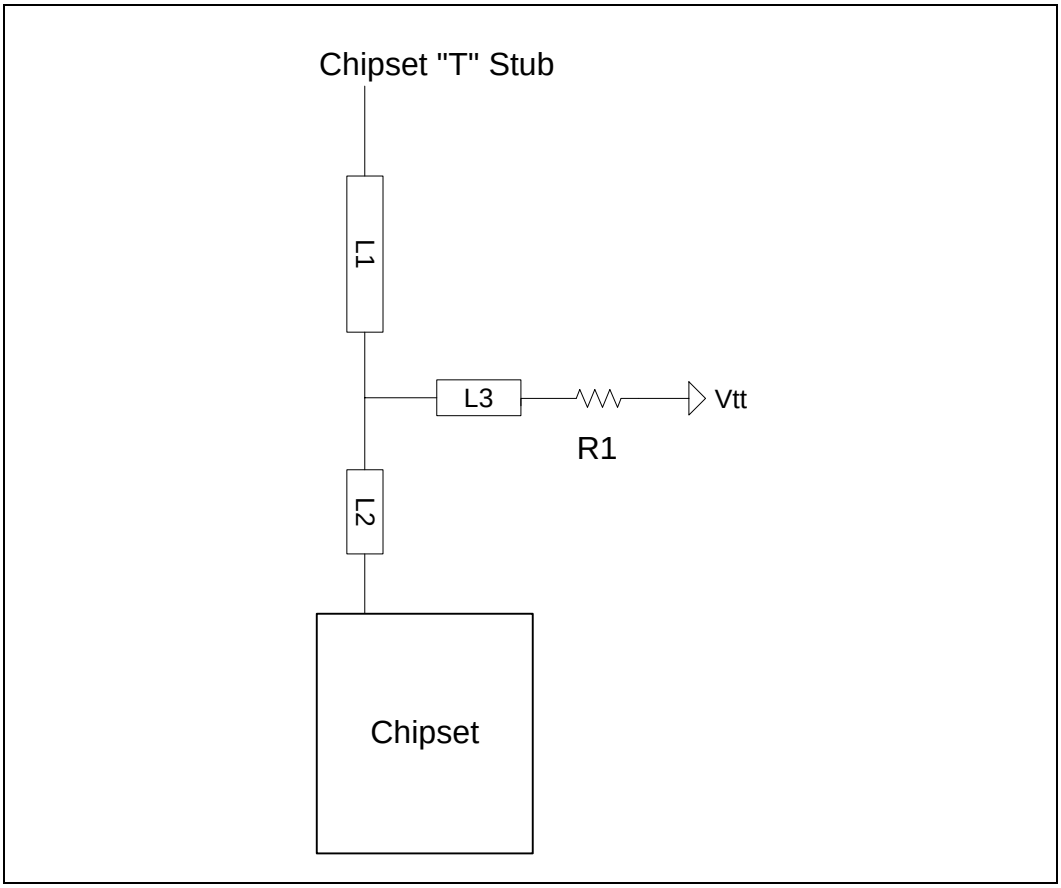


Table 3-9. Wired-OR Values

Item	Value	Notes
L1	1.75 to 2.5 inches	Same as L2 lengths in Section 3.2 and Section 3.3
L2	Less than 0.25 inches	Should be as short as possible. Optimal case is to make this value zero, making the L3 stub come after the chipset pin.
L3	Less than 1.5 inches	
R1	100 to 220 Ω	The range of values has trade-offs in flight time and dampening effects. 150Ω +/- 10% is a base recommendation.

Please note that the value range for R1 present a set of trade-offs for flight time and dampening effects. Choosing a value near the upper end of the range (around 200Ω) will impact the flight times the least, but will also provide minimal dampening. Choosing a value at the lower end of the range (around 100Ω) will provide optimal dampening but has a larger impact on the signal flight times. Intel recommends a value of 150Ω +/- 10% as a reasonable trade-off between dampening and flight time.

3.5 Simulation Methodology

Analog simulations are recommended for high-speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working “solution space” that meets flight time and signal quality requirements. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulations can be reduced.

Intel recommends running simulations at the device pads for signal quality and at the device pins for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

Intel® Pentium® III Processor with 512KB L2 Cache DP I/O buffer models are available from the Intel Developer website.

3.6 Trace Routing

The following guidelines should be followed when routing the AGTL host bus signal traces:

- Traces should have an impedance of 60Ω +/- 15%
- The nominal trace width should be 5 mils.
- The L0 and L1 lengths in Table 3-5 should be matched to within 0.25 inches.
- Minimize the number of vias and layer transitions.

3.7 Layout Rules for AGTL Signals

3.7.1 Ground Reference

It is strongly recommended that AGTL signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane.

3.7.2 Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance. For optimal signal integrity, high-speed signals should not be routed over power plane splits.

3.7.3 CPU Connector Breakout

It is strongly recommended that AGTL signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the connector on the same layer. If routing is tight, breakout from the connector on the opposite routing layer over a ground reference and cross over to main signal layer near the CPU connector.

Note: Following the above layout rules is critical for AGTL signal integrity.

3.7.4 Minimizing Crosstalk

The following general rules will minimize the impact of crosstalk in the high speed AGTL bus design:

- Maximize the space between traces. Maintain a minimum of 10 mils (assuming a 5 mil trace) between trace edges wherever possible. It may be necessary to use tighter spacing when routing between component pins. When traces have to be close and parallel to each other, minimize the distance that they are close together, and maximize the distance between the sections when the spacing restrictions relaxes.
- Avoid parallelism between signals on adjacent layers if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL is a low signal swing technology, it is important to isolate AGTL signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings, such as 3.3 V system memory.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes the crosstalk.
- Route AGTL address, data and control signals in separate groups to minimize crosstalk between groups. Keep at least 25 mils between each group of signals.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
- Minimize the dielectric process variation used in the PCB fabrication.
- Minimize the cross sectional area of the traces. This can be done by narrower traces and/or by using thinner copper, but the trade-off for this smaller cross sectional area is a higher trace resistivity that can reduce the falling edge noise margin because of the I*R loss along the trace.

3.8 Layout Rules for Non-AGTL (CMOS) Signals

The following layout rules should be used for all CMOS signals:

- The trace impedance should be 60Ω +/- 15%.
- External termination resistors should be placed in the middle of the trace to prevent long reflection times and reduce reflection ledges.
- Do not route CMOS traces next to AGTL traces. Switching noise on the AGTL traces may attack the nearby CMOS traces.
- Route a CMOS trace on one signal layer. If layer switching is unavoidable, try minimize the number of layer switches.
- Try to use only one reference plane for a trace (either Vcc or Vss).
- Although CMOS signals are slow, they may still have speed path problems. This is especially true for APIC clock and APIC data. Try to avoid long routes.

3.9 Undershoot/Overshoot Requirements

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below VSS. The overshoot guideline limits transitions beyond VCC or VSS due to the fast signal edge rates. The processor can be damaged by repeated overshoot events on buffers if the charge is large enough (i.e., if the overshoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline will also make satisfying the ringback specification difficult.

When performing simulations to determine impact of overshoot and undershoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modeled within Intel I/O buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the processor performance, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O buffer model will impact results and may yield excessive overshoot/undershoot.

Refer to the latest *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet* for detailed undershoot/overshoot requirements.

3.10 Debug Port Routing Guidelines

This section describes the processor debug port, in-target probe (ITP) platform design guidelines. The data in this chapter must be used with the information found in the "Debug Tool Specifications" chapter of the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet* to complete the design and layout of the debug port.

3.10.1 Target System Implementation

The implementation guidelines given in this section will ensure a fully functional ITP debug system. The signals involved in the ITP debug system are high speed signals and must be routed with high speed design considerations in mind. The implementation offers flexibility in areas such as JTAG routing (i.e., scan chain), addition of non-ITP compliant parts, and clock rate. However, the implementation is not flexible in system and execution signal connections.

Intel will use an ITP for internal debug and system validation and recommends that all system designs include a debug port.

3.10.1.1 Signal Layout Guidelines

The Debug Port (TAP) is a part of the processor scan chain. It will need to be connected to the bus clock and system bus signals. This implies that the designer will place the Debug Port within 12 inches of the nearest processor.

There are three signal groups within the debug port as mentioned in the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet*. Each group has a different set of layout requirements. The system signals are special ITP-specific signals and are both inputs and outputs. The JTAG signals are system

resources and may be shared with local JTAG tools. Input and output signals are available. The execution signals are a combination of CMOS and AGTL level signals. They are both inputs and outputs to the ITP.

The ITP TCK and TMS signals must be routed with a maximum trace resistance of 2.0 ohm to reduce the amount of DC shifting on these signals. This is due to the small termination values that are recommended for these signals.

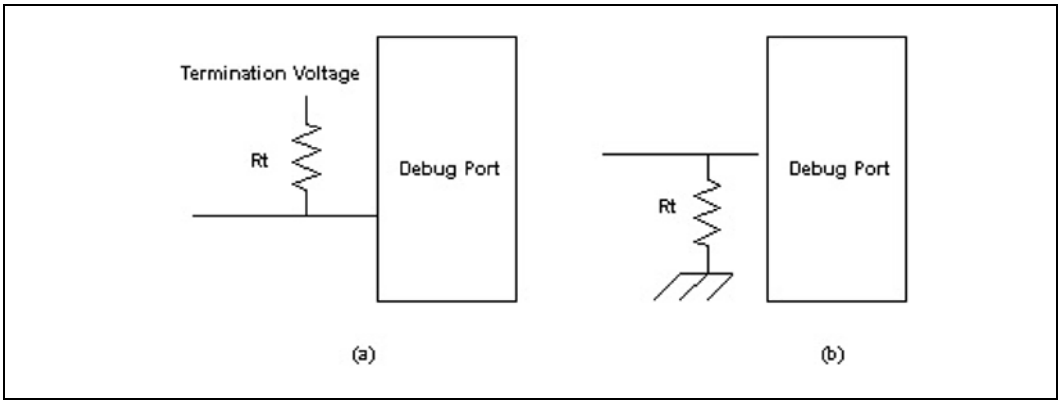
3.10.1.1.1 System Signal Layout Guidelines

Table 3-10 provides the system signal layout guidelines. See Table 3-13 for termination values.

Table 3-10. System Signal Layout Guidelines

Signal	Routing Notes	Sample Layout
POWERON	Route with normal trace 2 to 6 inches to the debug port connector	Figure 3-4a
BCLK, BCLK#	Refer to BCLK system requirements documentation for proper termination values and routing requirements	N/A
DBRESET#, BSEN#, DBINST#		Figure 3-4a

Figure 3-4. Simple Terminations



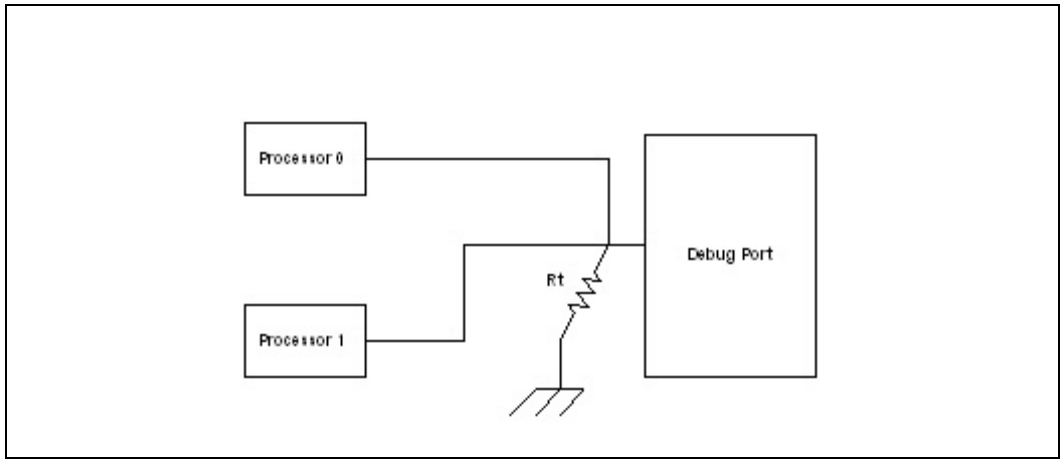
3.10.1.1.2 JTAG Signal Layout Guidelines

Reflections on TCK that cause mid-threshold ringing will render the primary system debug tool inoperative. Simulate the behavioral model, and verify signal integrity using your system bus signal analysis tools. The following table provides the JTAG signal layout guidelines. It is highly recommended that TCK be simulated to ensure proper signal quality is maintained.

Table 3-11. JTAG Signal Layout Guidelines

Signal	Routing Notes	Sample Layout
TCK	Critical JTAG signals which requires timing and signal integrity considerations, driver is 74VCX16245 with external edge rate control on TCK	Figure 3-5
TMS, TDI, TDO	Critical JTAG signal which requires timing and signal integrity considerations. ITP driver is 74VCX16245. TMS must be routed with TCK.	Figure 3-4a
TRST#	On target resistors should be used to force TRST# assertion (low).	Figure 3-4b

Figure 3-5. TCK Termination, DP System



3.10.1.1.3 Execution Signal Layout Guidelines

Table 3-12. Execution Signals Routing Guidelines

Signal	Routing Notes	Sample Layout
PREQx#	AGTL signal routing guidelines apply	Figure 3-4a
PRDYx#		Figure 3-6
RESET#	The flight time of the RESET# signal from the closest processor must be added to the arrival time of BCLK at the Debug Port.	Figure 3-7

Figure 3-6. PRDYx# Signal Termination

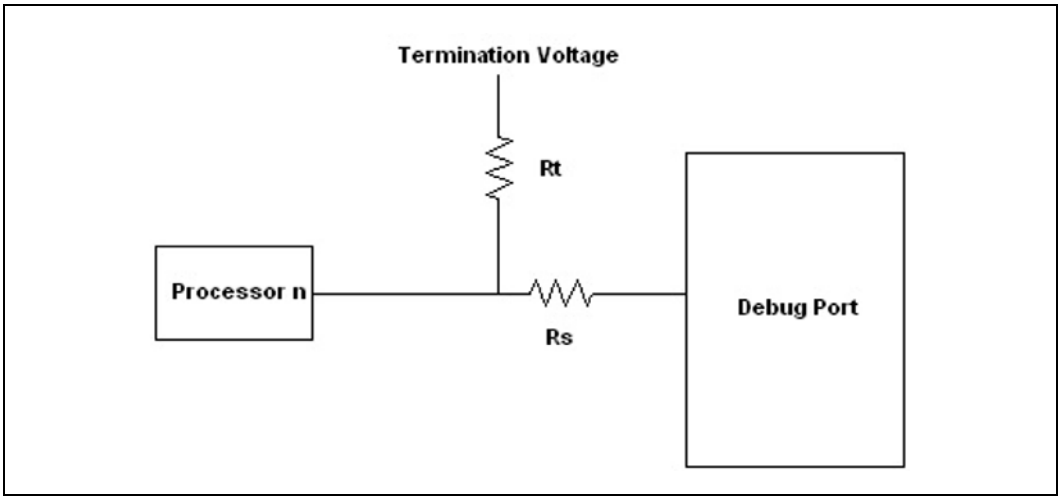
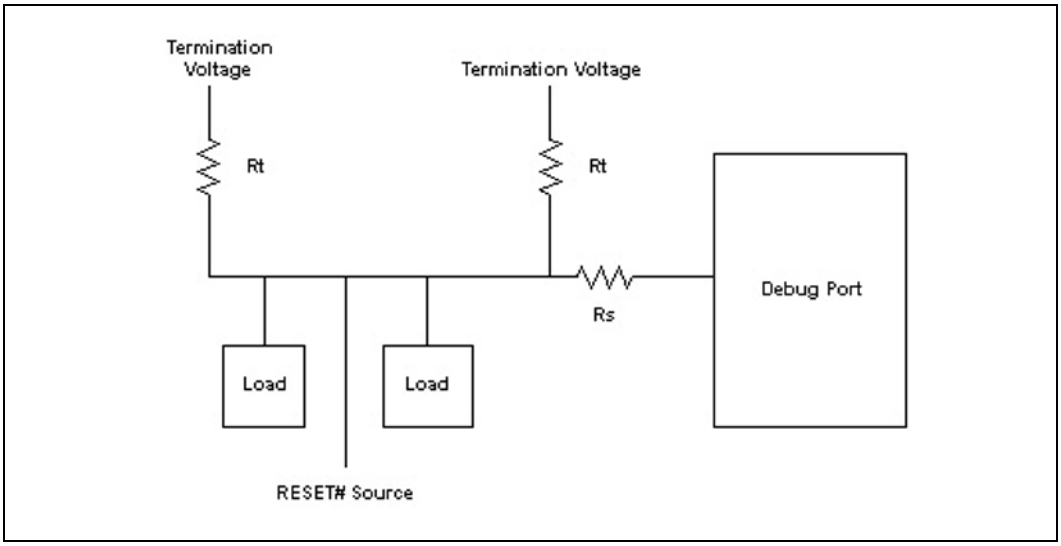


Figure 3-7. RESET# Signal Termination



3.10.1.2 Signal Termination Requirements

Table 3-13 lists signal termination requirements for the debug port signals.

Table 3-13. Debug Port Termination Requirement

Signal	Signal Termination Value (Rt)	Termination Value (Rs)	Termination Voltage
System Signal			
POWERON	1.5 KΩ	N/A	V_{TT}
BCLK, BCLK#	Refer to BCLK system requirements documentation for proper termination values and routing requirements		
BSEN#	240 Ω	N/A	V_{CC}
DBRESET#	240 Ω	N/A	V_{CC}
DBINST#	10 KΩ	N/A	V_{CC}
JTAG Signals			
TCK	39 Ω		GND
TDI	200 - 300 Ω	N/A	$VCC_{CMOS1.5}$
TDO	150 Ω	N/A	$VCC_{CMOS1.5}$
TMS	39 Ω	N/A	$VCC_{CMOS1.5}$
TRST#	500 - 680 Ω	N/A	GND
Execution signals			
RESET#	Match to AGTL characteristic impedance	240 Ω	V_{TT}
PREQx#	200 - 300 Ω	N/A	$Vcc_{CMOS1.5}$
PRDYx#	Match to AGTL characteristic impedance	240 Ω	V_{TT}

3.10.1.3 Routing Guidelines

Table 3-14. Routing Guidelines

Parameter	Reference Figure	Description
TCK	Figure 3-5	1" max from debug port to RT AND 12" max from debug port to processor VERY SENSITIVE TO NOISE -- please route accordingly
TMS, TDO, TDI, POWERON, DBRESET#, BSEN#, DBINST#, PREQx#	Figure 3-4a	1" max from debug port to RT AND 12" max from debug port to processor

Table 3-14. Routing Guidelines

Parameter	Reference Figure	Description
TRST#	Figure 3-4b	1" max from debug port to RT AND 12" max from debug port to processor
PRDYx#	Figure 3-6	1" max from debug port to RS AND 1" max from debug port to RT AND 12" max from debug port to processor (AGTL guidelines)
RESET#	Figure 3-7	1" max from debug port to RS AND 1" max from debug port to RT AND 12" max from debug port to processor

3.10.1.4 System Implementation

Figure 3-8 demonstrates the expected route of the JTAG data link for a processor only cluster. It is obligatory to pull up TDI/TDO for each signal, however. Note that when the number of processors is changed, a bypass must be used for the empty sites.

Figure 3-9 and Figure 3-10 illustrate possible bypass configurations with a three pin jumper and a four-pin jumper.

Figure 3-8. JTAG Signals TDI/TDO for Processor Only

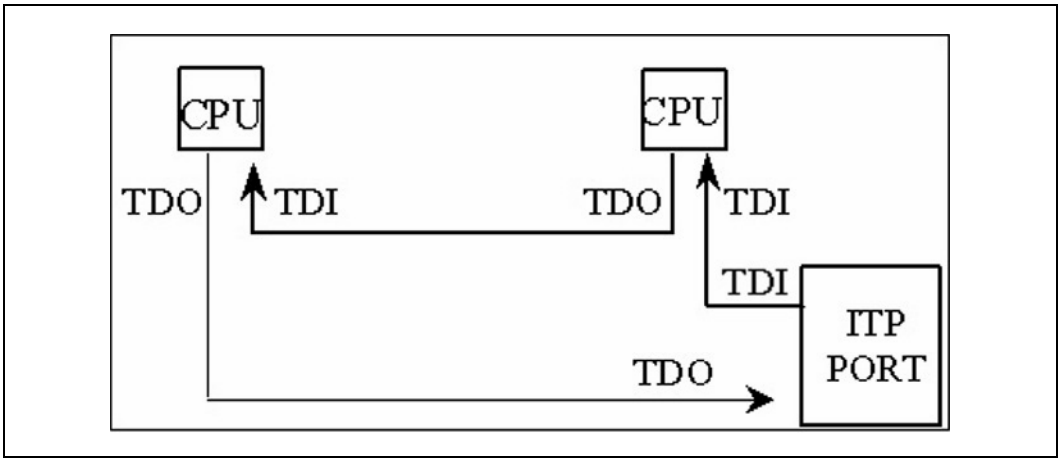


Figure 3-9. TDO 3-Pin Jumper Bypass

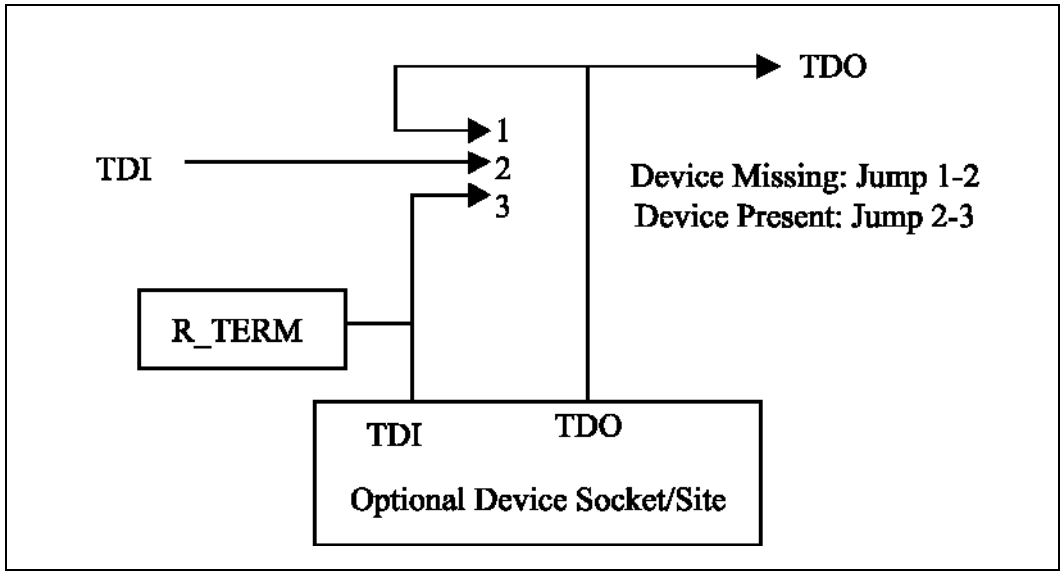
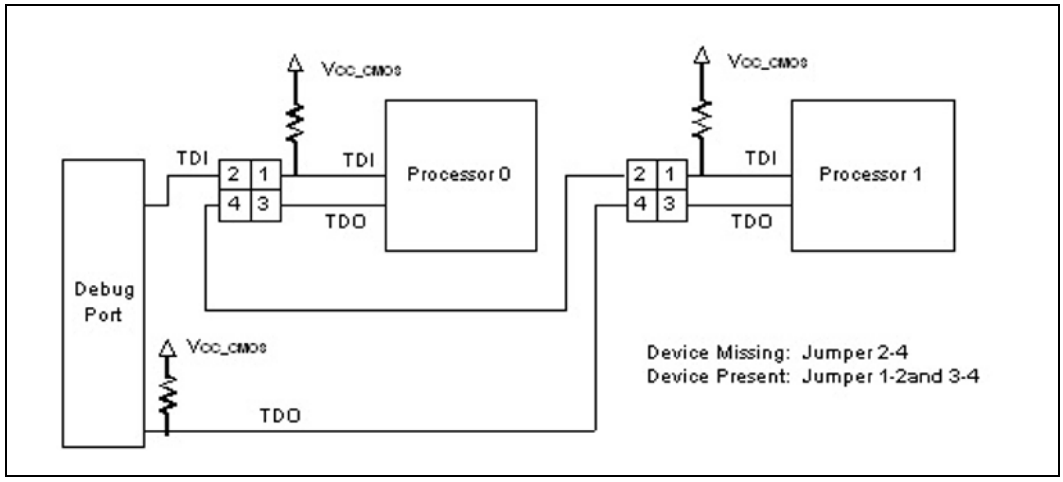


Figure 3-10. 4-Pin Jumper Bypass



This page intentionally left blank

Clocking 4

4.1 General Clocking Considerations

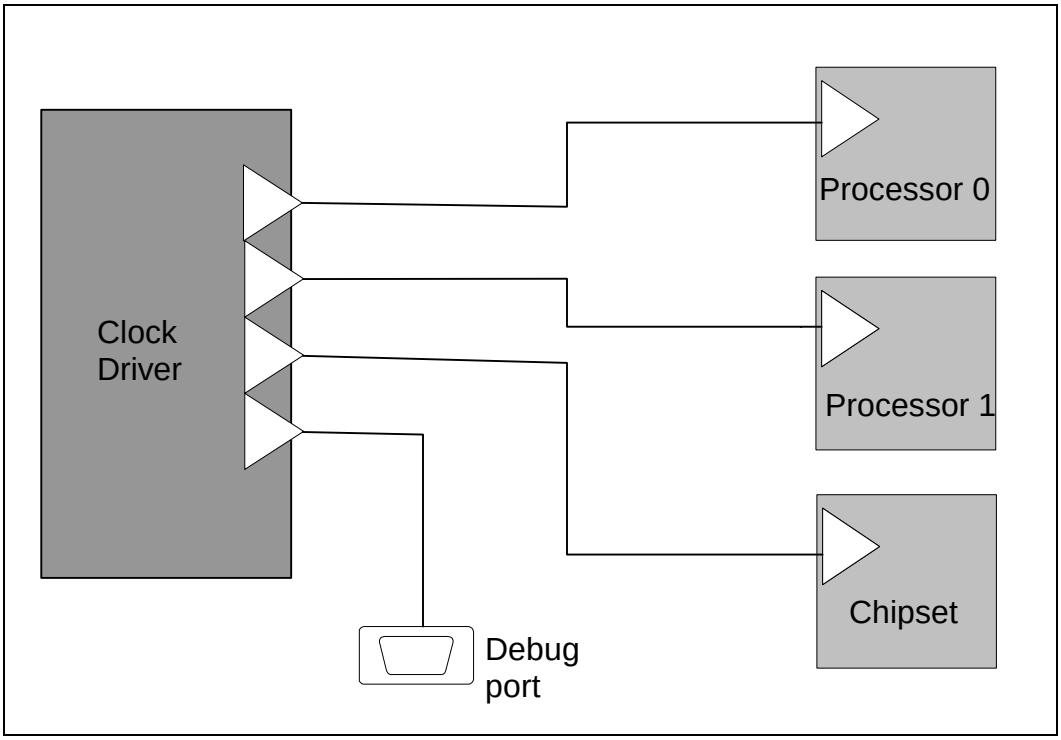
The host bus clock signals are critical signals in a platform design. The signal integrity and timing of these signals should be carefully evaluated and simulated. The following sections provide host clocking recommendations for the two supported Intel® Pentium® III Processor with 512KB L2 Cache clocking methodologies: single-ended clocking and differential clocking.

In general, the following layout recommendations should be followed for the host bus clocks:

- It is recommended that system bus clocks be routed on the signal layer next to the ground layer (referenced to ground).
- It is strongly recommended that system bus clocks do not traverse multiple signal layers.
- System clock routing over power plane splits should be minimized.
- If necessary, grounded guard band traces can be routed next to clock traces to reduce crosstalk to other signals.

Figure 4-1 shows the host bus clocking connections that must be made in a dual-processor system. Detailed information regarding the routing, layout, and termination of the processor and chipset connections can be found in Section 4.2 and Section 4.3. The debug port routing has special requirements and are covered in Section 4.4.

Figure 4-1. Host Bus Clock Connections



The clocking requirements and timing information for the Intel® Pentium® III Processor with 512KB L2 Cache can be found in the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet*. For additional information about the timing and clocking requirements of the chipset component, please contact your chipset vendor for the appropriate documentation.

4.2 Single Ended Host Bus Clocking Routing

Intel® Pentium® III Processor with 512KB L2 Cache dual-processor platforms have support for using single-ended host bus clock drivers. When using this clocking method, the BCLK signal (pin W37) is used as the single-ended clock input to the processor. The BCLK#/CLKREF signal (pin Y33) is used as a reference voltage and must be connected to the appropriate filter circuit described in Section 4.2.1.

Figure 4-2 shows the topology that should be used for the processor clock traces. Please note that L0, L1, and L2 refer to trace lengths between the illustrated components. Table 4-1 contains the recommended lengths and component values for this topology.

Figure 4-2. Single Ended Clocking Topology - CPU

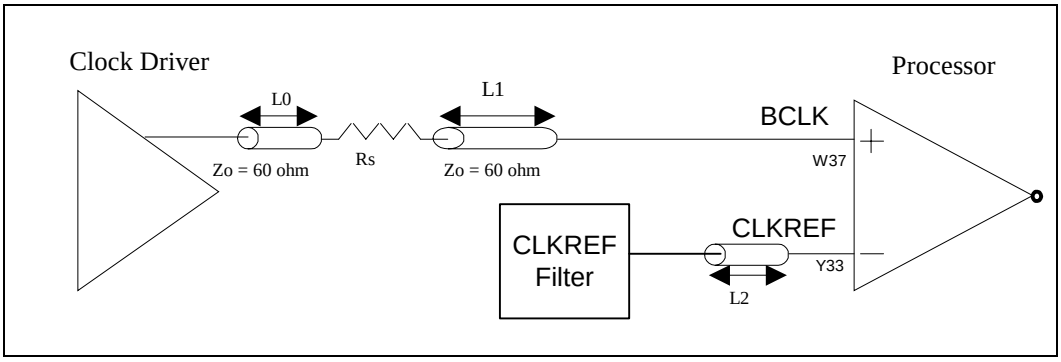


Table 4-1. Component Values for SE Clocking Topology - CPU

Reference	Value	Notes
L0	0.25 to 0.5 inches	All L0s should be matched
L1	Chipset L1 + 1” +/- 0.125 Chipset L1 + 0.5” +/- 0.125	Use this processor L1 length if the chipset L1 is 5”-7” Use this processor L1 length if the chipset L1 is 7”-12”
L2	0.0 to 1.0 inches	L2 should be as short as possible.
Rs	22 to 33 Ω	1% Tolerance

Figure 4-3 shows the topology that should be used for the chipset clock traces. Please note that L0 and L1 refer to trace lengths between the illustrated components. Table 4-2 contains the recommended lengths and component values for this topology.

Figure 4-3. Single Ended Clocking Topology - Chipset

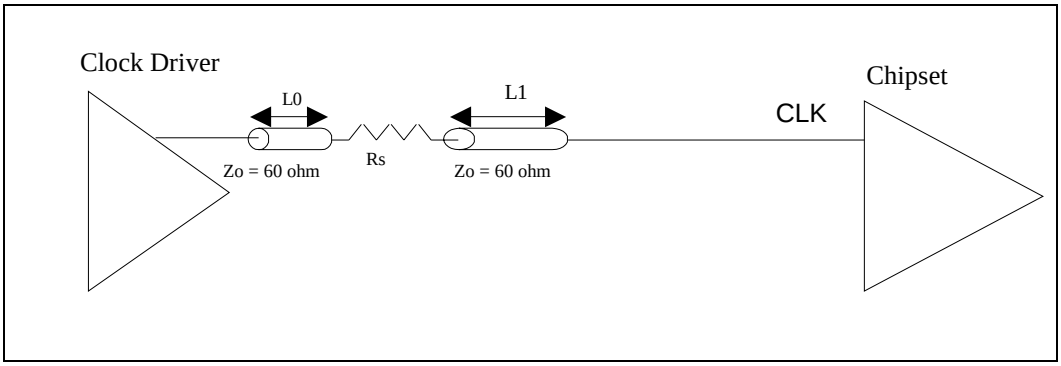


Table 4-2. Component Values for SE Clocking Topology - Chipset

Reference	Value	Notes
L0	0.25 to 0.5 inches	All L0s should be matched
L1	5 inches to 12 inches	Effects processor lengths.
Rs	22 to 33 Ω	1% Tolerance

The following guidelines should also be followed for single-ended clock implementations:

- BCLK must be routed through trace impedance of 60 ohm +/- 10%.
- Use 5 mil wide traces.
- Place all serial termination resistors within 0.50 inches to clock driver pins.
- Place all other signals at least 20 mils from the clock traces.
- All the termination resistors are rated at 1% accuracy.
- The two processor clock traces should be matched to within 0.250 inches.

4.2.1 CLKREF Filter Implementation

When using single-ended clocking mode, the BCLK#/CLKREF signal on the processor serves as a reference voltage to the clock input. To provide a steady reference voltage, a filter circuit must be implemented and attached to this pin. Figure 4-4 shows the recommended CLKREF filter implementation. The CLKREF filter should be placed as close as possible (less that 1.0 inch) to the processor's CLKREF pin.

Figure 4-4. CLKREF Filter Implementation

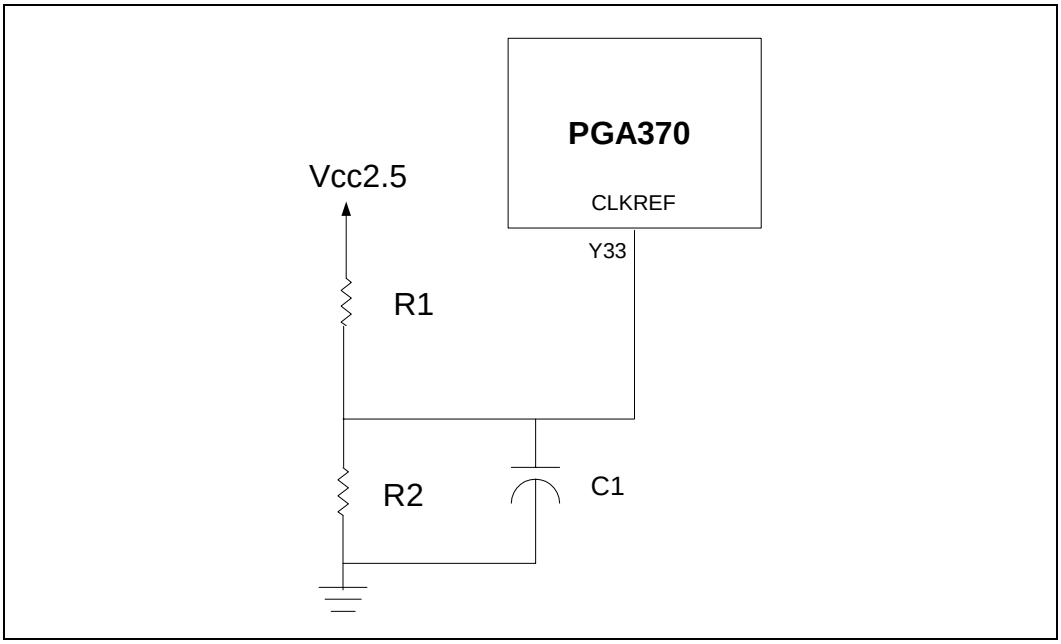


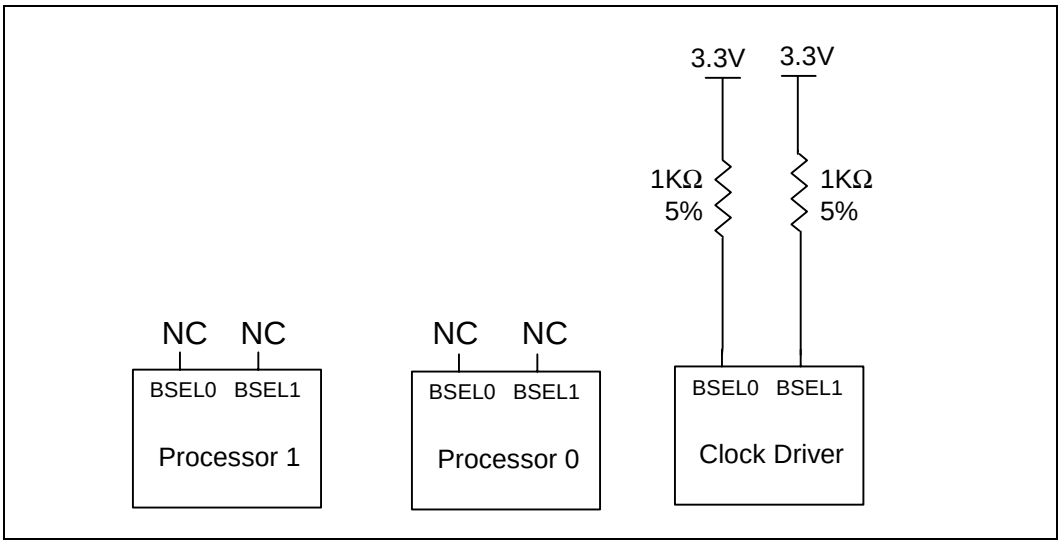
Table 4-3. CLKREF Component Values

Reference	Value	Notes
R1	150 Ω	1% Tolerance
R2	150 Ω	1% Tolerance
C1	4.7 µF	

4.2.2 Single-Ended Clocking BSEL[1:0] Implementation

In an Intel® Pentium® III Processor with 512KB L2 Cache platform that is using single-ended (SE) clocking or a clock source that does not support the VTT_PWRGD protocol, the normal BSEL frequency selection process will not work. Since the clock generator is not compatible with dynamic BSEL assertions, all BSEL[1:0] signals should not be connected together. Instead, the BSEL pins on the clock generator should be pulled-up to 3.3 V through a 1 KΩ, 5% resistor. This strapping will force the clock generator into 133 MHz clocking mode and will only support 133 MHz capable processors.

Figure 4-5. Single Ended Clock BSEL Circuit



4.3 Differential Host Bus Clocking Routing

Intel® Pentium® III Processor with 512KB L2 Cache dual-processor platforms support differential host bus clock drivers. When operating in differential clocking mode, the BCLK and BCLK#/CLKREF form a differential pair of clock inputs. The differential pair of traces should be routed with special care and using standard differential signalling techniques. The following sections contain the recommended topology and routing for differential clocking for these platforms.

4.3.1 Differential Clocking Topology

Figure 4-6 shows the topology that should be used for the processor and chipset traces. Please note that L0 and L1 refer to trace lengths between the illustrated components. Table 4-4 contains the recommended lengths and component values for this topology.

Figure 4-6. Differential Clocking Topology

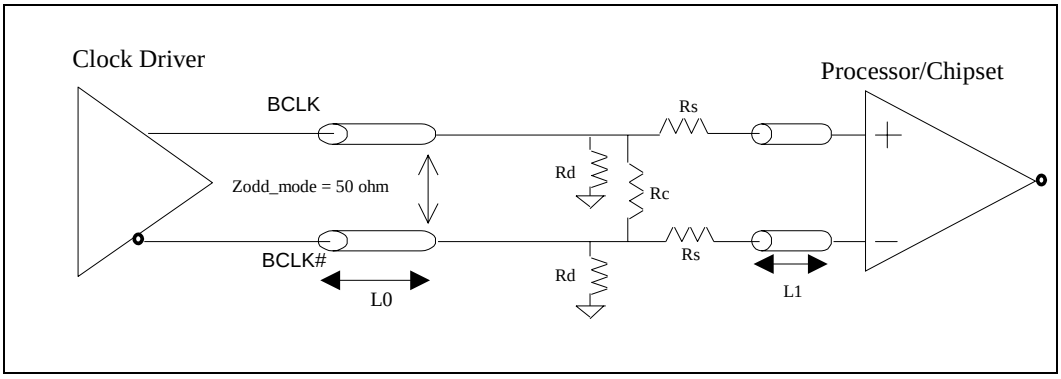


Table 4-4. Component Values for Differential Clocking

Reference	Value	Notes
L0 (Processor)	5 to 9 inches	Match each processor differential pair to within 0.250 inches
L0 (Chipset)	Processor L0 + 1 inch +/- 0.125 inches	Match to the processor L0 and add 1 inch for package loading
L1	0.0 to 0.4 inches	Should be as short as possible
Rd	63.4Ω	1% Tolerance
Rs	33.2Ω	1% Tolerance
Rc	475Ω	1% Tolerance

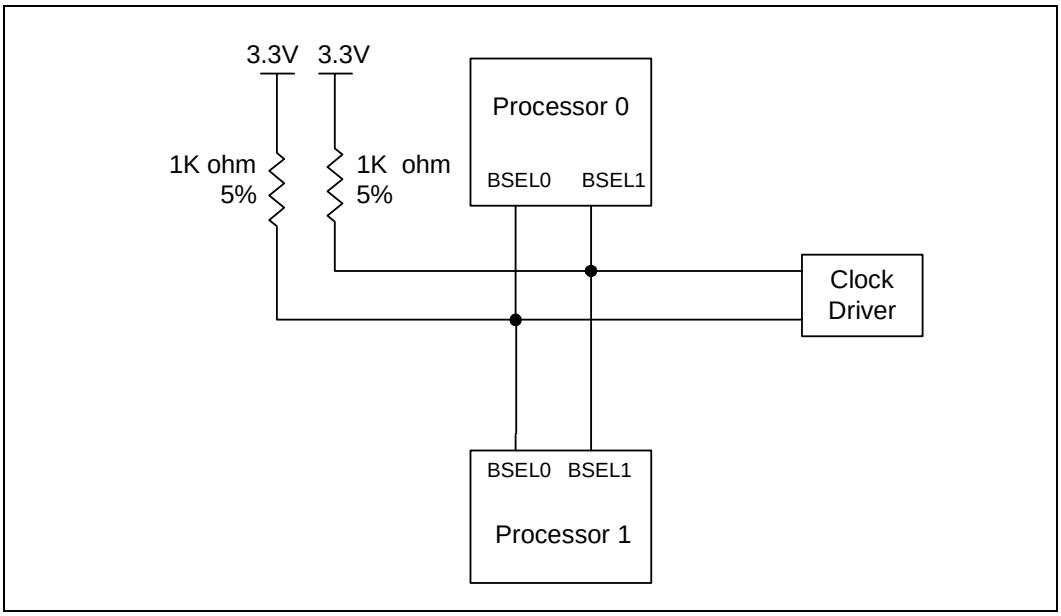
The following guidelines should also be followed for differential clock implementations:

- Match BCLK and BCLK# in length, width and impedance.
- BCLK and BCLK# should be coupled to achieve odd mode impedance of 50 ohm.
- Use 5 mil traces, routed differentially.
- Place all termination resistors within 0.40 inches of BCLK/BCLK# pins at the receiver.
- Other should be spaced at least 20 mils away from clock lines.
- All the termination resistors are rated as 1% accuracy.
- Minimize stubs to passive components.
- Clock to chipset is 1 inch longer than the clock to CPU (to compensate for CPU package load).

4.3.2 Differential Clocking BSEL[1:0] Implementation

The System Bus Frequency Select Signals (BSEL [1:0]) are used to select the system bus frequency for the host bus agents. The frequency selection is determined by the processor(s) and driven out to the host bus clock generator. All system bus agents must operate at the same 133MHz frequency. The BSEL pins for the processor are open drain signals and rely on a 3.3V pull-up resistor to set the signal to a logic high level. Figure 4-7 shows the recommended implementation for a differentially clocked system.

Figure 4-7. Differential Clock BSEL Circuit



4.4 Debug Port Host Clock Connection

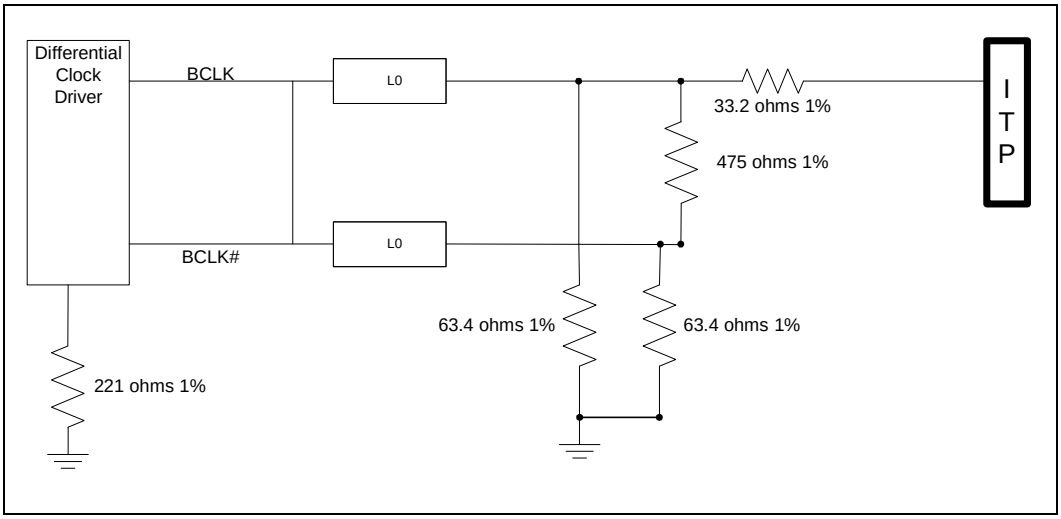
In order to recover full front side bus speed BPM[5:0]# and RESET# data with the ITP, the Debug Port should be placed as close as is physically reasonable to the system bus and no further than 1.5 ns flight time (as measured by trace length of the BPM[5:0]# and RESET# signals) from the nearest front side bus agent. System designers should record the flight time of the BPM[5:0]# and RESET# signals from the nearest front side bus agent to the Debug Port. This value will be important during the routing of several other Debug Port signals.

Assuming BCLK (and BCLK# in differential clocked systems) signals are routed from the system clock buffer to each of the synchronous clock agents with a matched length, the copy of this signals from the system clock buffer to the ITP Debug Port must have a flight time equal to the matched length of the other synchronous clock agents plus the flight time of the BPM[5:0]# signals from the nearest bus agent to the Debug Port noted above. This will ensure that the same BCLK to BPM[5:0]# phase relationship seen at the closest system bus agent will be present at the Debug Port pins. Clock trace lengths may be adjusted to center the recovery of BPM[5:0]# and RESET# at the Debug Port within the ITP receiver setup an hold window.

For a single-ended clock driver design, the topology illustrated in Figure 4-3 should be used. In this case, the “chipset” in the illustration is actually the debug port pin. The trace length L0 and the Rs value are the same as recommendations for the chipset in Table 4-2. However, the length of the trace segment L1 should be chosen so that it complies with the requirements described in the previous paragraph. This means that the L1 for the debug port is at least as long as the L1 for the processor clock traces.

The circuit recommendations for a differential clock driver design are shown in Figure 4-8. The length, L0, should be chosen to complies with the flight time requirements mentioned in this section. Please note that these requirements will make the length L0 longer than the processor clock trace’s L0 lengths. The terminating resistors should be placed as close the ITP socket as possible.

Figure 4-8. Debug Port Differential Host Clock Implementation



4.5 Clock Driver Decoupling and Power Delivery

The decoupling and power delivery requirements of the system clock driver are dependent on the clock driver and chipset used in the system implementation. Because of this, no specific information can be provided in this document. However, since proper decoupling and noise-free power delivery are critical to the clock driver’s operation, Intel encourages system implementors to carefully follow the chipset and clock driver vendor’s recommendations in these areas. An incorrect implementation of these circuits can easily cripple a clock driver’s ability to produce reliable clock signals and lead to system instability. Please refer to the appropriate clock driver and chipset vendor information for more details.

Power 5

The intent of this section is to familiarize the reader with the processor power requirements for an Intel® Pentium® III Processor with 512KB L2 Cache dual processor platform, and to show simulation model and power implementation techniques. Only specific power distribution and control issues pertaining to Intel® Pentium® III Processor with 512KB L2 Cache platforms are discussed in this section. It is assumed that the reader is familiar with power distribution issues of the Intel® Pentium® III processors.

5.1 Terminology

"*Power-Good*" or **"*PWRGOOD*"** (an active high signal) indicates that all of the supplies and clocks within the system are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.

"V_{CC}" or **"Vcc_{CORE}"** refers to Intel® Pentium® III Processor with 512KB L2 Cache core and cache supply voltages.

"V_{TT}" refers to the AGTL termination voltage.

"*AGTL*" refers to Intel® Pentium® III Processor with 512KB L2 Cache's Assisted Gunning Transceiver Logic supply voltage. "AGTL" is the bus between the processor and its chipset. The terms "AGTL" and "System Bus" are synonymous.

"*VRM 8.5*" refers to the DC-DC design guidelines for Intel® Pentium® III Processors with 512KB L2 Cache. These voltage regulator design supplies the required voltage and current to a single processor.

5.2 Typical Power Delivery

Power distribution is generally thought of as *supplying power to the components that require it*. Most digital designers typically assume that an ideal supply will be provided. The printed circuit board (PCB) designers attempt to create this ideal supply with two power planes in the PCB or by using large width traces to distribute power. High frequency noise created when logic gates switch is typically controlled with high frequency ceramic capacitors, which are recharged from lower frequency bulk capacitors. Various *rule of thumb* methods exist for determining the amount of each type of capacitance that is

required. For Intel® Pentium® III Processor with 512KB L2 Cache dual processor designs, the system designer needs to design beyond the rule of thumb and architect a power distribution system that meets the processor specifications. Figure 5-1 shows the ideal power model.

Figure 5-1. Ideal Processor Power Supply Scheme

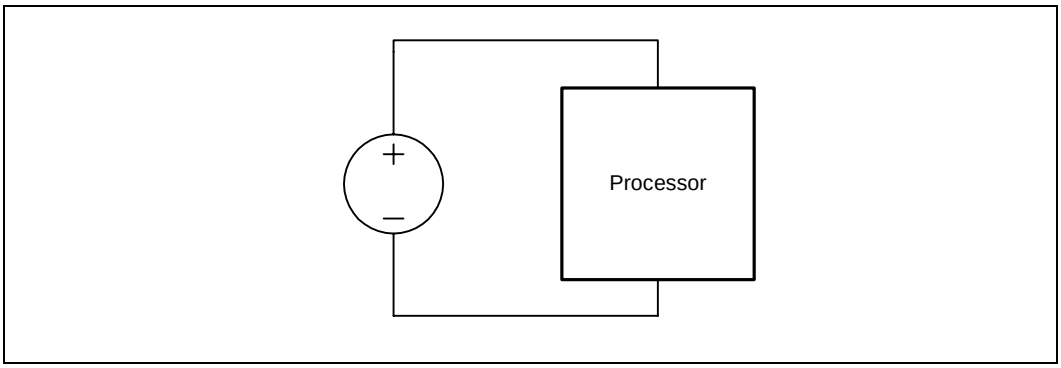


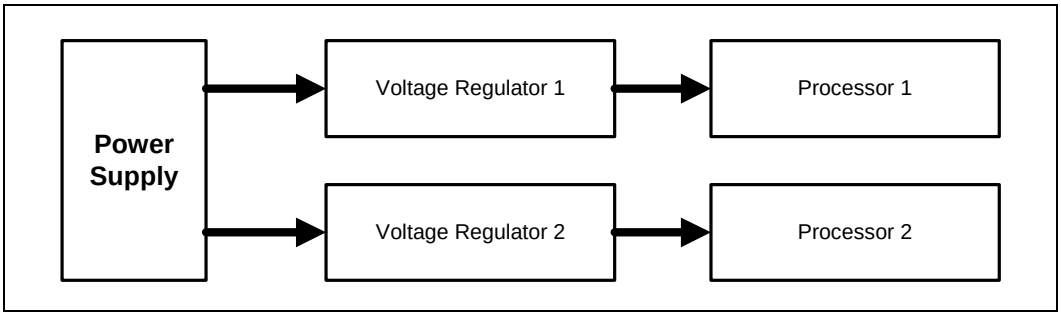
Figure 5-2 shows the recommended system baseboard solution involving local voltage regulators. Each voltage regulator solution can be either a voltage regulator module (VRM) or an embedded voltage regulator (VRD) depending upon the specific requirements of the board designs. It is recommended that board designers follow the guidelines in VRM 8.5 DC-DC converter design guidelines document.

Each regulator circuit should be placed as close as possible to the corresponding processor and aligned to the side of the socket with the higher density of power and ground pins.

In previous generation Pentium® III dual processor based systems, there existed the possibility of sourcing the combined voltage and current requirements for both processors from one large voltage regulator. **However, due to the load-line characteristics specified by the Intel® Pentium® III Processor with 512KB L2 Cache, Intel recommends that separate power planes be utilized**. This configuration of voltage regulators is shown in Figure 5-2.

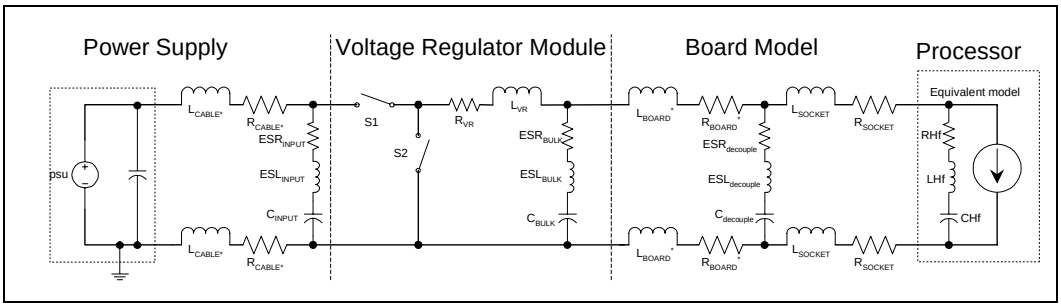
.

Figure 5-2. Power Distribution for a DP System Motherboard



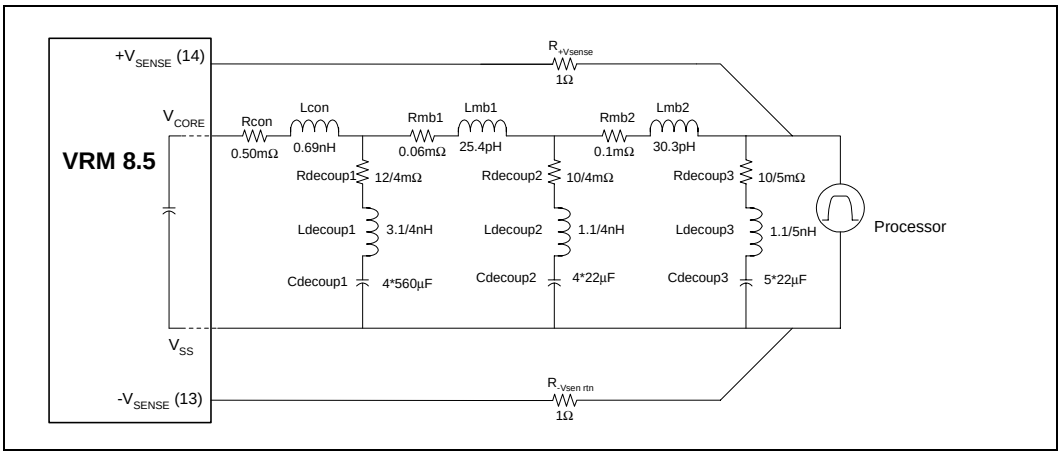
To completely model the motherboard system, one must include the inductance and resistance which exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor socket and voltage regulator. A more detailed model showing these effects is shown in Figure 5-3 below.

Figure 5-3. Detailed Power Distribution Model for System with VRM



Both VRD and VRM solutions should be designed in conjunction with the recommended load model referenced in Figure 5-4.

Figure 5-4. VRM 8.5 Board Power Distribution Model



5.3 Dual Processor Power Requirements

This section describes the issues related to supplying power to an Intel® Pentium® III Processor with 512KB L2 Cache. For detailed electrical specifications, please refer to the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet*.

5.3.1 Voltage Tolerance

Refer to the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet* for voltage tolerance specifications. Failure to meet these specifications on the low-end tolerance results in transistors slowing down and not meeting timing specifications. Not meeting the specifications on the high-end tolerance can cause damage or reduce the life of the processor.

5.3.2 Multiple Voltages

The VRM 8.5 module or embedded voltage regulator, which provides the Vcc_{CORE} supply to the Intel® Pentium® III Processor with 512KB L2 Cache, has the capability of supplying voltages from +1.05V to +1.825V. The voltage regulator solutions designed to the *VRM 8.5 DC-DC Converter Design Guidelines* can provide adequate power for all speed versions of Intel® Pentium® III Processors with 512KB L2 Cache.

Multiple voltages required for an Intel® Pentium® III Processor with 512KB L2 Cache dual processor system are Vcc_{CORE}, V_{REF}, V_{TT}, $Vcc_{CMOS1.5}$, $Vcc_{CMOS1.8}$, $Vcc_{CMOS2.0}$, and V_{SS}. Refer to the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet* for the pin location of these voltages.

5.3.3 Voltage Sequencing

When designing a system with multiple voltages, there is always the issue of ensuring that no damage occurs to the system during voltage sequencing. Voltage sequencing is the timing relationship between two or more voltages. Sequencing applies to the power voltage levels and the levels of certain other crucial signals when the user turns on or off the power supply, or the system enters a failure condition. Systems should be designed such that neither supply stays on for extended time while the other is off. Excessive exposure to these conditions can compromise long-term component reliability. Please refer to the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet* for the voltage sequencing requirements.

5.4 Meeting Power Requirements

Intel recommends using VRM 8.5 compliant modules or embedded regulator designs for Intel® Pentium® III Processor with 512KB L2 Cache dual processor system board designs. The system board designer should properly place high frequency and bulk decoupling capacitors as needed between the voltage regulator and processor to ensure voltage fluctuations remain in specification.

Intel® Pentium® III Processor with 512KB L2 Cache dual processor power distribution designs require trade-offs between power supply, distribution and decoupling technologies. This section discusses how to do a step by step design of a system using the more accurate power distribution model shown in Figure 5-3.

5.4.1 Supplying Voltage

Local (point of load) regulation is recommended for the Intel® Pentium® III Processors with 512KB L2 Cache to satisfy their higher current requirements and to maintain power converter output voltage tolerance. For example, a DC-to-DC converter, placed close to the load, converts a higher DC voltage to a lower level using either a linear or switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R) and localizes losses to the planes between the converter and the processor sockets.

It is recommended that voltage regulator solutions (VRD or VRM) employ differential remote sense (as illustrated in Figure 5-4) to compensate for voltage drops between the regulators and the socket pins. The sense lines should be terminated as close to the center of the socket as possible and should not have an impedance greater than 1Ω.

5.4.2 Decoupling Technology and Transient Response

The inductance of the system due to cables and power planes slows the power supply's ability to respond quickly to a current transient. Decoupling a power plane can be broken into several independent parts. The closer to the load the capacitor is placed, the more inductance that is bypassed. By bypassing the inductance of leads, power planes, etc., less capacitance is required. However, closer to the load there is less room for capacitance. Therefore trade-offs must be made.

The Intel® Pentium® III Processor with 512KB L2 Cache causes large switching transients. These sharp surges of current occur at the transition between low power mode and high power mode. It is the responsibility of the system designer to provide adequate high frequency decoupling to manage the highest frequency components of the current transients. To lower total board inductance and resistance, the processor is designed with approximately 74 Vcc_{CORE} and 74 V_{SS} (ground) pins. Larger bulk storage (C_{BULK}), such as electrolytic (OSCON) capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition.

Power bypassing is required due to the relatively slow speed at which a DC-to-DC converter can react, that is the loop response time of the converter feedback circuit in comparison to the processor load change and frequency. Bulk capacitance supplies energy from the time the high frequency decoupling capacitors are drained until the power supply can react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate that it is able to supply, while the high frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate that they can supply.

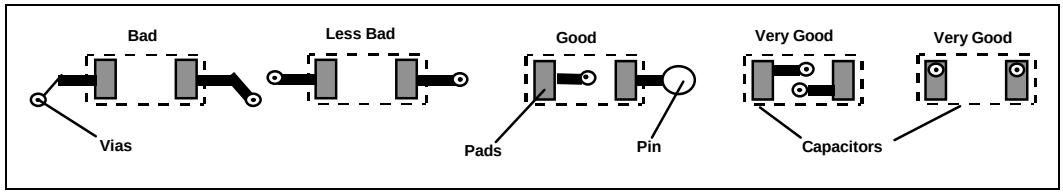
A load-change transient occurs when coming out of or entering a low power mode. These are not only quick changes in current demand, but also long lasting average current requirements. Maintaining voltage tolerance during these changes in current requires high-density bulk capacitors with low Effective Series Resistance (ESR) and low Effective Series Inductance (ESL). Use thorough analysis when choosing these components.

5.4.2.1 Location of High Frequency Decoupling

A system designer for Intel® Pentium® III Processors with 512KB L2 Cache should properly design for high frequency decoupling. High frequency decoupling should be placed as close to the power pins of the processor as physically possible. Use both sides of the board if necessary for placing components in order to achieve the optimum proximity to the power pins. This is vital as the inductance of the board's metal plane layers could cancel the usefulness of these low inductance components.

Another method to lower the inductance that should be considered is to shorten the path from the capacitor pads to the pins that it is decoupling. If possible, place the vias connecting to the planes within the pad of the capacitor. If this is not possible, keep the traces as short and wide as is feasible. Possibly one or both ends of the capacitor can be connected directly to the pin of the processor without the use of via. Even if simulation results look good, these practical suggestions can be used to create an even better decoupling situation where they can be applied in layout. Figure 5-5 illustrates these concepts..

Figure 5-5. 1206 Capacitor Pad and Via Layouts



5.4.2.2 Location of Bulk Decoupling

The location of bulk capacitance is not as critical as the high frequency decoupling components. However careful placement is still important for these components to minimize the effects of parasitic board impedances impacting transient response capability. Further, location and component impedances are useful in simulation of the power conversion circuit. Bulk components should typically be placed close to the processor sockets to minimize AC delays.

It should be further noted that bulk capacitors on VRMs are effectively electrically located behind the inductance of the converter pins. As a result bulk capacitors need to be utilized close to the processor socket.

The recommended number of bulk decoupling components and board load model for use with VRMs is illustrated in Table 5-1 and Figure 5-4.

Table 5-1. Bulk Capacitance Recommendations

Design Type	Bulk Capacitance	ESR	ESL	RMS Current Rating
On-board design	4 OSCON, 560 µF	12mΩ	3.1 nH max	5.04 A_{rms}

5.5 Recommendations

Intel recommends using simulation to design and verify Intel® Pentium® III Processor with 512KB L2 Cache dual processor based systems. With the estimates provided in the previous section, a model of the power source, and the model of the processor, system developers can begin analog modeling. The following sections contain Intel's design recommendations.

5.5.1 Decoupling Guidelines

5.5.1.1 Vcc_{CORE} Decoupling Design

Table 5-2 contains the quantities and values for the Vcc_{CORE} supply high frequency decoupling. All capacitors should be placed within the PGA370 socket cavity and mounted on the primary side of the motherboard. The capacitors are arranged to minimize the overall inductance between Vcc_{CORE} and V_{SS} power pins, as shown in Figure 5-6.

Figure 5-6. PGA370 Decoupling Capacitor Placement

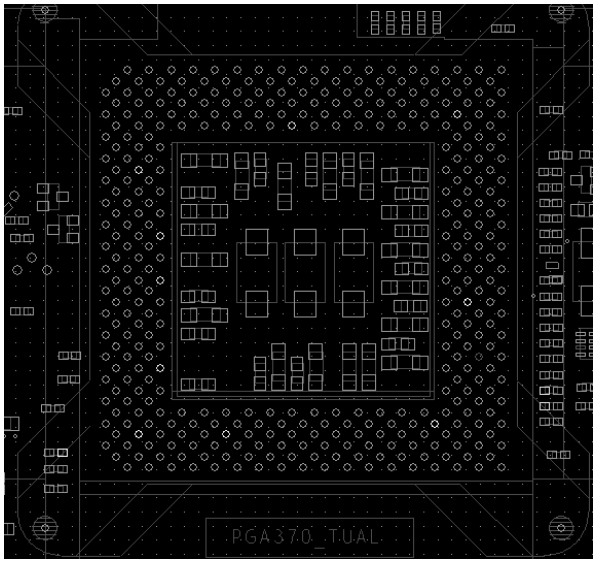


Table 5-2. Vcc_{CORE} High Frequency Capacitance Recommendations

Capacitance	ESR	ESL
9 1210 package, 22µF or 16 1206 package, 4.7µF	10mΩ	1.1 nH

5.5.1.2 V_{TT} Decoupling Design

Twenty 0.1-µF capacitors in 0603 packages should be placed within 200 mils of each PGA370 socket. As many of these capacitors should be placed inside the PGA370 socket cavity.

5.5.1.3 AGTL V_{REF} Decoupling Design

Three 0.1-µF capacitors in 0603 packages should be placed within 500 mils of the V_{REF} pins. Two should be connected between V_{TT} and V_{REF}, and one should be connected between V_{REF} and ground. If this circuit is far from the processor, add a 0.1-uF capacitor for decoupling.

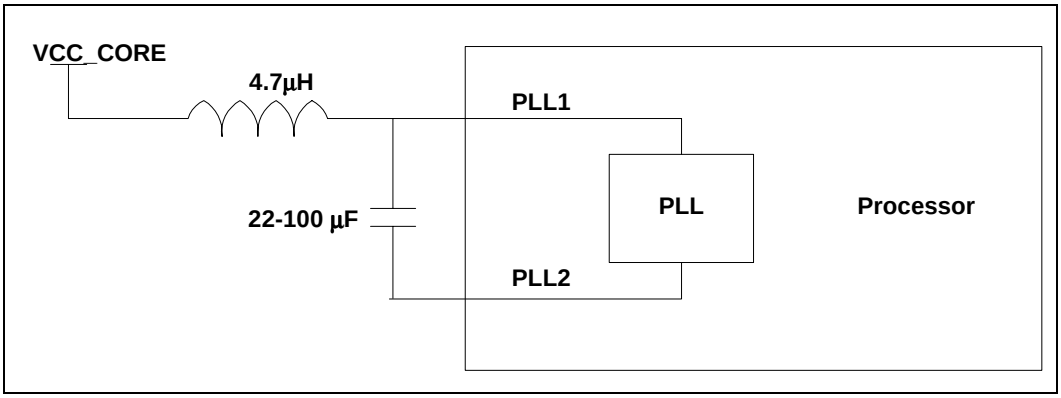
5.5.2 Processor PLL Filter Recommendations

It is highly critical that phase lock loop power delivery to the processor meets Intel's requirements. A low pass filter is required for power delivery to pins PLL1 and PLL2. This serves as an isolated, decoupled power source for the internal PLL.

5.5.2.1 Topology

PGA370 processors have internal phase lock look (PLL) clock generators, which are analog and require a quiet power supply to minimize jitter. PLL1 should have a 4.7-µH inductor connected in series to Vcc_{CORE}, and PLL2 should be connected through a capacitor (22- to 100-µF) to PLL1. See Figure 5-7.

Figure 5-7. Processor PLL Filter



Other routing requirements:

- The capacitor (C) should be close to the PLL1 and PLL2 pins, < 0.1Ω per route.
- The PLL2 route should be parallel and next to PLL1 route (minimize loop area).
- The inductor (L) should be close to C; any routing resistance should be inserted between Vcc_{CORE} and L.

5.5.2.2 Filter Specification

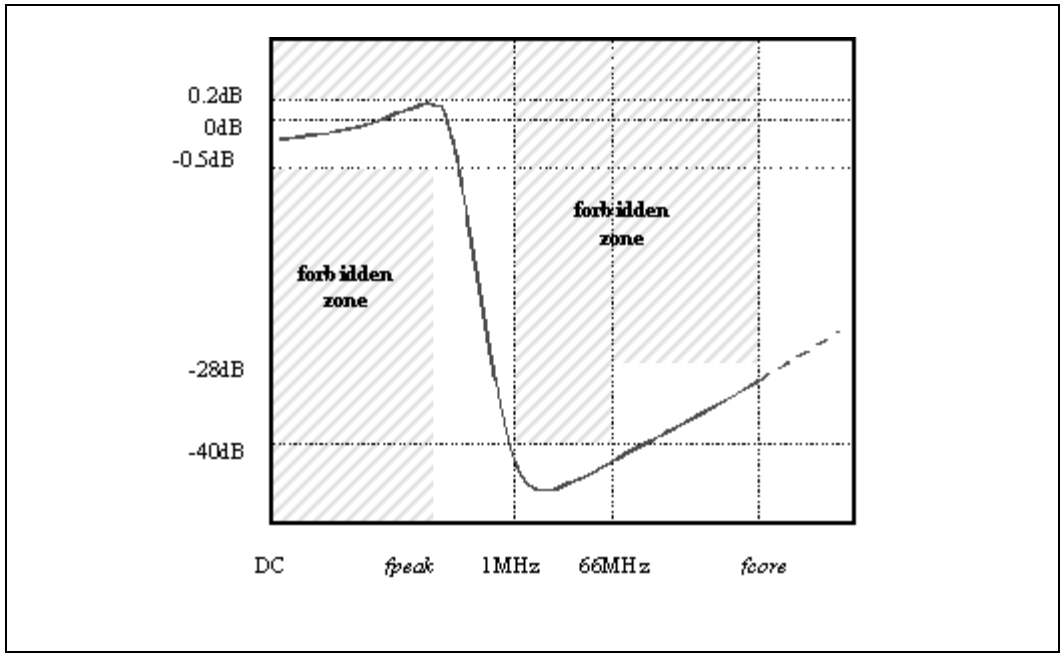
The function of the filter is to protect the PLL from external noise through low-pass attenuation.

The low-pass specification, with input at Vcc_{CORE} and output measured across the capacitor, is as follows:

- < 0.2dB gain in pass band
- < 0.5dB attenuation in pass band (see DC drop in next set of requirements)
- > 34dB attenuation from 1MHz to 66MHz
- > 28dB attenuation from 66MHz to core frequency

The filter specification is graphically shown in Figure 5-8.

Figure 5-8. PLL Power Low Pass Filter Response



Other requirements:

- Use shielded type inductor to minimize magnetic pickup
- Filter should support DC current > 30mA
- DC voltage drop from VCC to PLL1 should be < 60mV, which in practice implies series R < 2Ω; also means pass band (from DC to 1Hz) attenuation < 0.5dB for VCC = 1.1V, and < 0.35dB for VCC = 1.5V.

This page intentionally left blank

Thermals 6

The Intel® Pentium® III Processor with 512KB L2 Cache requires a robust thermal solution for proper operation. To provide detail descriptions and example solutions for effective thermal management, a separate document has been created. Please see the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet* and *Intel® Pentium® III Processor in the FC-PGA2 Package Thermal Design Guidelines* for more information.

6.1 THERMTRIP# Requirements

In the event the processor drives the THERMTRIP# signal active during valid operation, both the Vcc and Vtt supplies to the processor must be powered off to prevent thermal runaway of the processor. Valid operation refers to the operating conditions where the THERMTRIP# signal is guaranteed valid. The time required from THERMTRIP# assertion to Vcc rail at 1/2 nominal is 5 seconds and THERMTRIP# asserted to Vtt rail at 1/2 nominal is 5 seconds.

Table 6-1. THERMTRIP# Timing Requirements

Power Rail	Power Target	Time Required for Power Drop
Vcc	1/2 Nominal Vcc	5.0 seconds
Vtt	1/2 Nominal Vtt	5.0 seconds

6.2 THERMTRIP# Erratum

Intel has identified an issue with THERMTRIP# which may incorrectly assert during de-assertion of RESET# at nominal operating temperatures in Intel® Pentium® III Processors with 512KB L2 Cache (CPUID 06B1h). The assertion of THERMTRIP# will cause the processor to shut down internally and stop execution. This issue can lead to intermittent system power-on boot failures.

To prevent the risk of power-on boot failures a platform workaround is required. The system must provide a rising edge on the TCK signal during the power-on sequence that meets all of the following requirements:

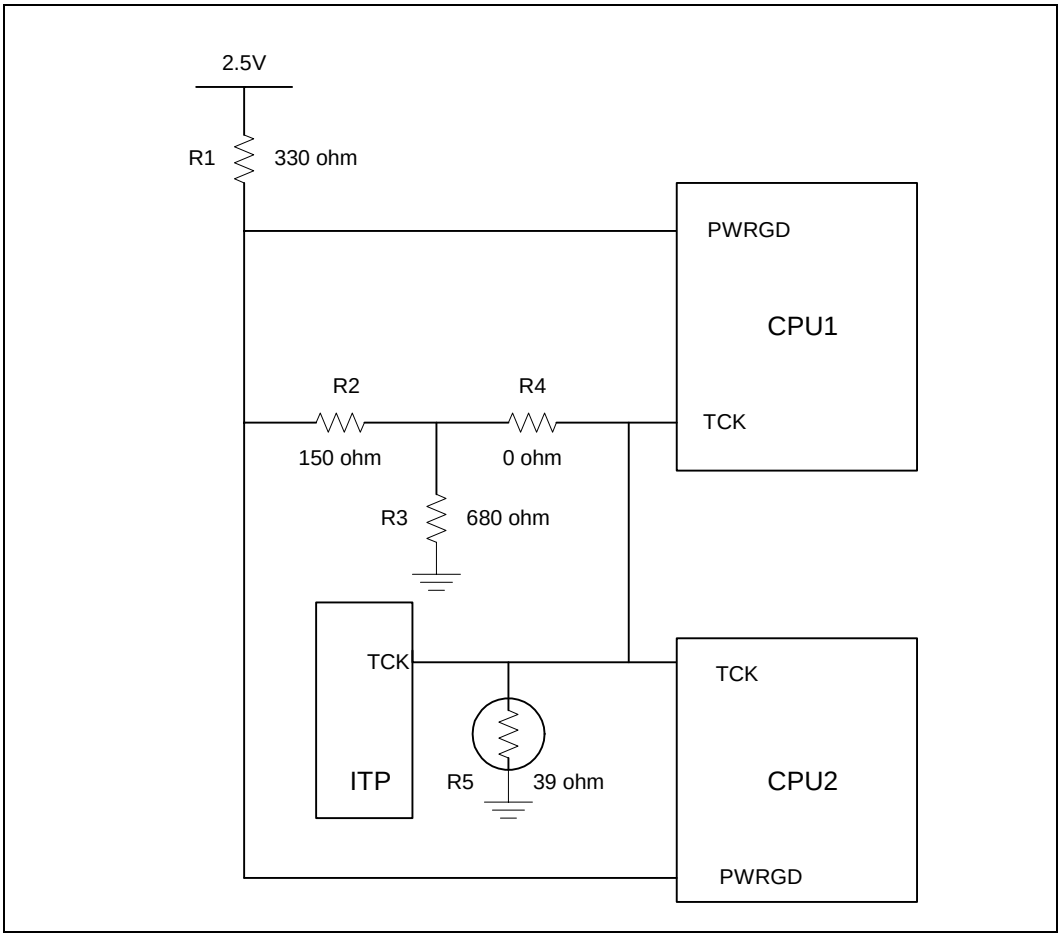
- Edge occurs after Vcc_{CORE} is valid and stable
- Edge occurs before or at the de-assertion of RESET#
- Edge occurs after all Vref input signals are at valid voltage levels
- TCK input meets the Vih_{min} and Vih_{max} requirements of the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet.*

Specific workaround implementations may be platform specific. The following example has been tested as an acceptable workaround implementation.

The example workaround circuit, shown in Figure 6-1, requires circuit modifications for ITP tools to function correctly. These modifications must remove the workaround circuitry from the platform and may cause systems to fail to boot. Issuing the ITP 'Reset Target' command on failing systems will reset the system while providing a sufficient rising edge on the TCK pin to ensure system boot.

The example workaround circuit shown does not support production motherboard test methodologies that require the use of the processor JTAG/TAP port. Alternative workaround solutions must be found if such test capability is required.

Figure 6-1. Example Dual Processor THERMTRIP# Workaround Circuit



NOTES:
1. For Production Boards: Depopulate R5
2. To use ITP: Install R5, Depopulate R4
3. Assumes the inputs to the CPU_PWRGD are open collector signals that are Wire-ANDed together

The example workaround circuit assumes that the PWRGD inputs into the processors are open collector. Tying the PWRGD inputs together in a Wired-AND fashion allows each processor to receive PWRGD at the same time but at the latter of the 2 separate PWRGD assertions. If separation of the PWRGD inputs to each processor is required, extra circuitry will be required.

Please consult the *Pentium® III Processor Specification Update* for additional information on this issue.

Processor Migration Considerations 7

7.1 Overview

This section describes the required changes to AGTL+ only processor platforms in order to convert them to AGTL compatible processor platforms. The information in this section should be used in conjunction with specifications presented in the latest version of the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet* and the *Pentium® III Processor for the PGA370 Socket Datasheet*, as well as information provided in other design guides such as the *VRM 8.5 DC-DC Converter Design Guidelines*. Design decisions should always be based on information contained in the latest *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet*.

For reliable Intel® Pentium® III Processor with 512KB L2 Cache operation, the designer must ensure that the requirements in this guideline are fully satisfied.

7.2 Implement VRM 8.5

The Intel® Pentium® III Processor with 512KB L2 Cache requires a VRM 8.5 compliant VRM for its power supply. Compliance with the following subsections is required for proper processor operation. This new VRM specification contains several features needed to meet the Intel® Pentium® III Processor with 512KB L2 Cache's operating requirements.

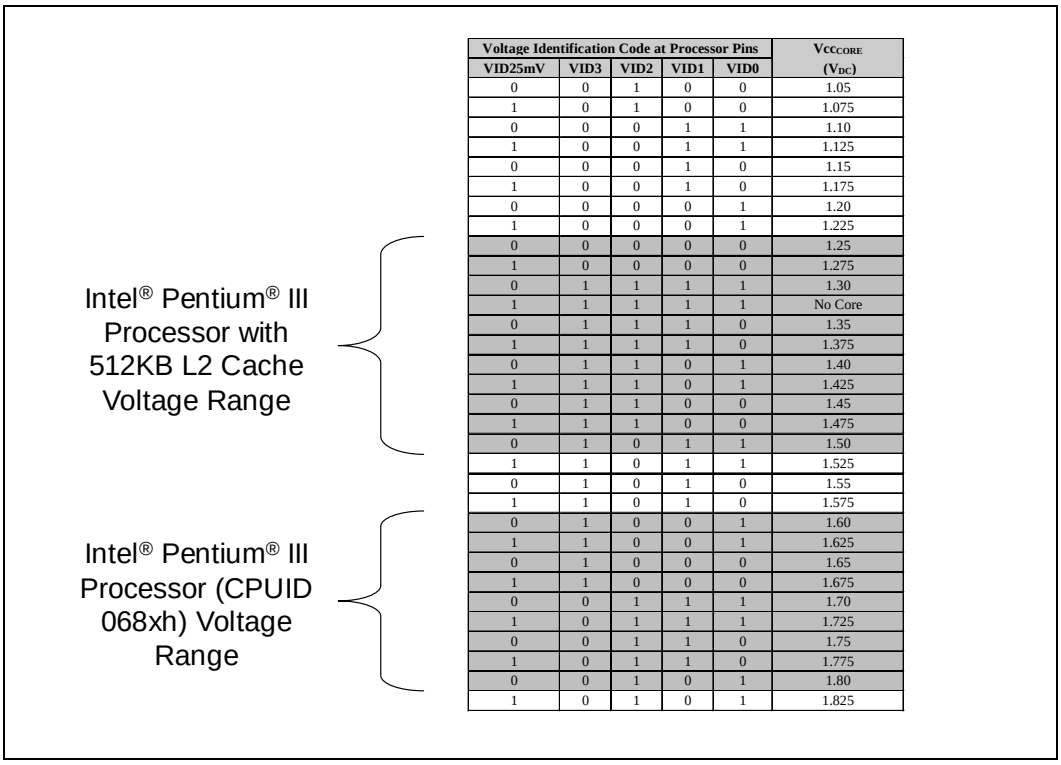
- Higher currents
- Smaller voltage increments. VID25MV pin added to enable 25 mV step
- Active voltage positioning (load line transient specs)
- VTT_PWRGD timer. Supports new BSEL and VID implementation. Asserted 1 ms after VTT is stable
- New connector and keepouts
- New voltage ranges

The specification for the new VRM design can be found in *VRM 8.5 DC-DC Converter Design Guideline*, which is available from Intel.

7.2.1 VRM 8.5 Voltage Range

Figure 7-1 shows the operational voltage ranges for AGTL compatible processors.

Figure 7-1. Voltage Range Comparison



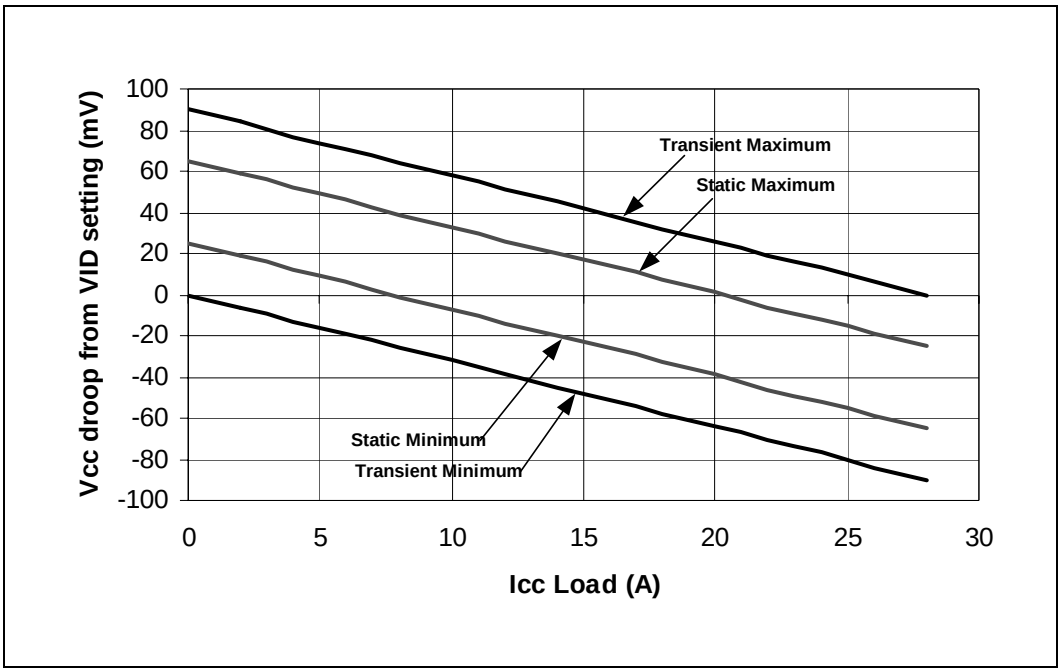
Voltage Identification Code at Processor Pins					Vcc_{CORE} (V_{DC})
VID25mV	VID3	VID2	VID1	VID0	
0	0	1	0	0	1.05
1	0	1	0	0	1.075
0	0	0	1	1	1.10
1	0	0	1	1	1.125
0	0	0	1	0	1.15
1	0	0	1	0	1.175
0	0	0	0	1	1.20
1	0	0	0	1	1.225
0	0	0	0	0	1.25
1	0	0	0	0	1.275
0	1	1	1	1	1.30
1	1	1	1	1	No Core
0	1	1	1	0	1.35
1	1	1	1	0	1.375
0	1	1	0	1	1.40
1	1	1	0	1	1.425
0	1	1	0	0	1.45
1	1	1	0	0	1.475
0	1	0	1	1	1.50
1	1	0	1	1	1.525
0	1	0	1	0	1.55
1	1	0	1	0	1.575
0	1	0	0	1	1.60
1	1	0	0	1	1.625
0	1	0	0	0	1.65
1	1	0	0	0	1.675
0	0	1	1	1	1.70
1	0	1	1	1	1.725
0	0	1	1	0	1.75
1	0	1	1	0	1.775
0	0	1	0	1	1.80
1	0	1	0	1	1.825

7.2.2 Active Voltage Positioning

The new VRM design now includes active voltage positioning. Active voltage positioning allows the VRM to improve handling of load transients. This is accomplished by adjusting the output voltage of the VRM as a function of the load current so the voltage is optimally positioned for system transients. In addition, the better system transients response allows for fewer output capacitors, which reduces the VR footprint and reduces cost. Finally, this new design should reduce the number of design changes as frequencies increase.

In order for a platform to support AGTL compatible processors, it must meet the new VRM guidelines outlined in the *VRM 8.5 DC-DC Converter Design Guidelines*. In particular, the voltage regulator must be able to respond to the transient and static loads specified in Figure 7-2.

Figure 7-2. Active Voltage Positioning Operating Parameters



7.2.3 VRM 8.5 Modules

The *VRM 8.5 DC-DC Converter Design Guidelines* introduces a new connector for the VRM module. This new module design has more input and output voltage pins to handle higher current demands. It also provides better electrical characteristics.

The module keepout area has also changed in the new design. Volumetrically, the module is smaller than the VRM 8.4 module design. The new connector is now longer, but results in a smaller overall board area.

Please refer to the *VRM 8.5 DC-DC Converter Design Guidelines* from Intel for more information.

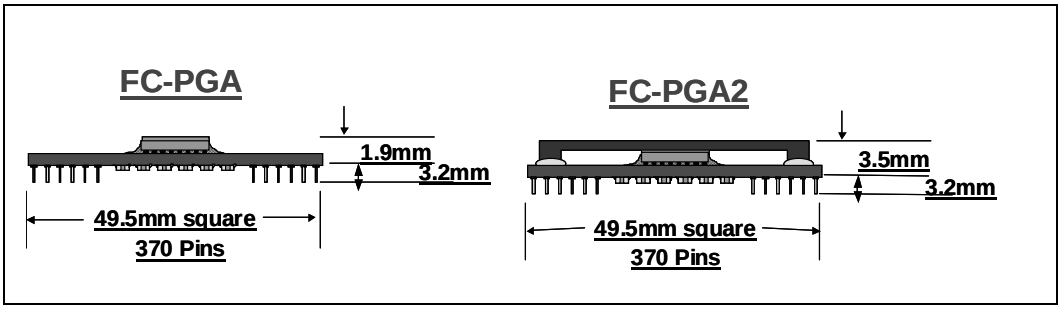
7.3 Package Changes (FC-PGA2)

The Intel® Pentium® III Processor with 512KB L2 Cache introduces a new packaging technology termed the FC-PGA2. The FC-PGA2 package leverages the previous FC-PGA package technology used on previous PGA370 socket processors. The FC-PGA2 package adds an Integrated Heat Spreader (IHS) to improve heat conduction from the processor die. The new package prevents the need for exotic thermal solutions in higher power density processors. The Intel® Pentium® III Processor with 512KB L2 Cache can be cooled using the existing Intel® Pentium® III Processor (CPUID 068xh) thermal solutions.

Figure 7-3 shows the changes to the package mechanicals between the FC-PGA and FC-PGA2 designs. Because of the additional height of the Integrated Heat Spreader (IHS), it may be necessary to accommodate an overall taller cooling solution. In addition, on the FC-PGA2, the heatsink is attached

further from the socket, so larger heatsink clips may be needed. Please refer to the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet* for more detailed information about the FC-PGA2 mechanical design.

Figure 7-3. Package Comparisons



7.4 Pinout Changes

The Intel® Pentium® III Processor with 512KB L2 Cache uses the same PGA370 socket that AGTL+ only processors use. No changes to this socket should be needed to create an Intel® Pentium® III Processor with 512KB L2 Cache platform.

However, several of the pin definitions for the Intel® Pentium® III Processor with 512KB L2 Cache have changed from their AGTL+ only processor definitions. A summary of these changes are provided in Table 7-1. The platform must implement the pinout changes shown below to be compatible with the Intel® Pentium® III Processor with 512KB L2 Cache.

Table 7-1. Pin Differences List

Pin	Intel® Pentium® III Processor with 512KB L2 Cache Platform	AGTL+ Only Processor Platform
AL1	RSVD	VSS
AF36	DETECT	GND
AG1	VTT	EDGCTRL
AM2	KEY	RSVD
AN3	DYN_OE	VSS
AJ3	RESET#2	VSS
X4	VSS	RESET2#
AK4	VTT_PWRGD	VSS
AK22	$V_{CMOSREF}$	VREF7
Y33	BCLK#/CLKREF[1]	CLKREF
N37	NCHCTRL	RSVD
X34	VTT	VCC_{CORE}
AK36	VID25MV	VSS
AD36	VTT	$VCC_{1.5}$
AB36	VTT	VCC_{CMOS}

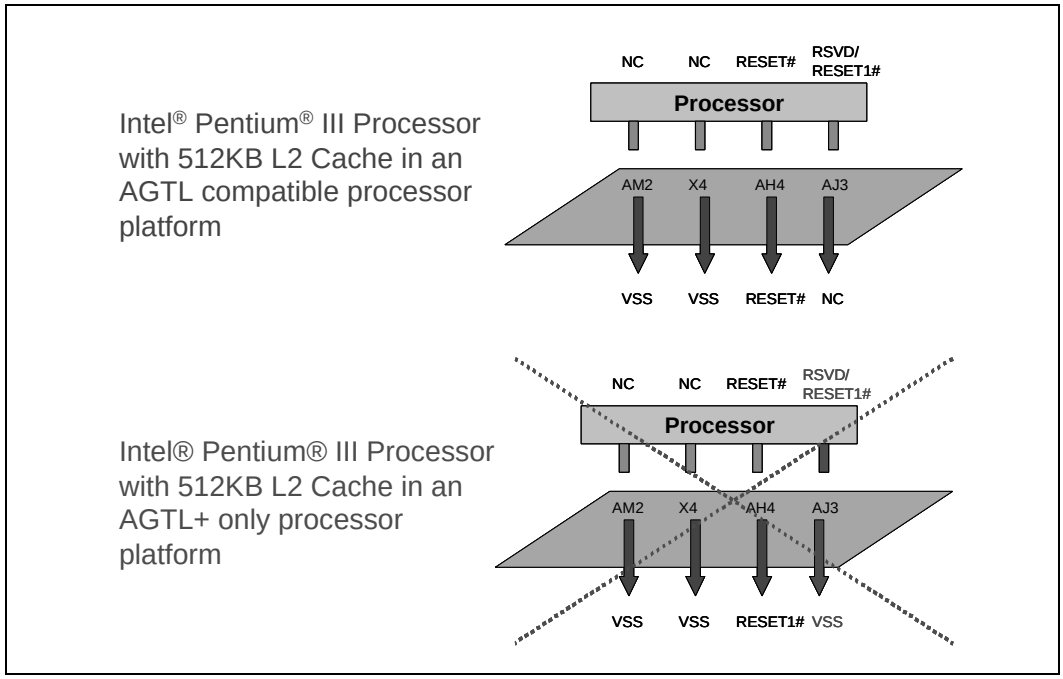
Table 7-1. Pin Differences List

Pin	Intel® Pentium® III Processor with 512KB L2 Cache Platform	AGTL+ Only Processor Platform
Z36	RSVD	$VCC_{2.5}$
E21	RSVD	$V_{CORE}DET$
G37	VTT	RSVD

NOTE:
1. For a single-ended clock source, this pin is treated as CLKREF and requires an external reference circuit. For a differential clock source, this pin is the complimentary clock input to BCLK.

The reset signals in the new pin definitions provide an electrical keying feature for socket PGA370 processors. This feature is used to prevent operation of socket PGA370 processors in incompatible platforms. If the Intel® Pentium® III Processor with 512KB L2 Cache is placed in an AGTL+ only processor platform, it will be held in reset. An AGTL+ only processor will be held in reset if it is placed in an Intel® Pentium® III Processor with 512KB L2 Cache platform. The Intel® Pentium® III Processor (CPUID 068xh) with AGTL Capability works in both platforms and is keyed accordingly. Figure 7-4 shows how this feature works for an Intel® Pentium® III Processor with 512KB L2 Cache in an AGTL+ only processor platform and in an Intel® Pentium® III Processor with 512KB L2 Cache ready platform.

Figure 7-4. Electrical Keying Mechanism



7.5 Dual Processor Specific Pin Recommendations

7.5.1 DETECT (AF36)

The DETECT pin in dual processor Intel® Pentium® III Processor with 512KB L2 Cache designs is not used. This pin is used by uniprocessor, Universal Motherboard designs to detect what processor is installed in the socket (AGTL+ only or AGTL compatible processor). Intel recommends leaving the DETECT pin unconnected or connecting it to ground in dual processor designs.

7.5.2 RESET2 (AJ3)

The RESET2 pin is used to hold an Intel® Pentium® III Processor with 512KB L2 Cache in reset if it is placed in an incompatible platform. Intel recommends this pin be left as a no connect on Intel® Pentium® III Processor with 512KB L2 Cache dual processor system designs.

7.5.3 KEY (AM2)

The KEY pin is part of the electrical keying feature of an Intel® Pentium® III Processor with 512KB L2 Cache compatible system. It is used to prevent incompatible AGTL+ only processors from functioning in the system. An AGTL+ only processor placed in the system will be held in reset by this pin. Intel recommends the KEY pin be connected to ground in Intel® Pentium® III Processor with 512KB L2 Cache dual processor platforms to allow this electronic key feature to work correctly.

7.6 AGTL Bus Transition

The Intel® Pentium® III Processor with 512KB L2 Cache introduces a new signaling voltage level of 1.25 volts. This new signalling level is termed AGTL. Because of the different signaling levels, the AGTL and the older AGTL+ signaling are incompatible. Table 7-2 summarizes the signaling aspects of the two schemes and how they relate to the processors of interest.

Table 7-2. Signalling Parameter Comparisons

	AGTL+ Only Processors	Intel® Pentium® III Processor (CPUID 068xh) with AGTL Capability	Intel® Pentium® III Processor with 512KB L2 Cache
Signalling Level	1.5V Only	1.25 or 1.5 V, Auto-detect	1.25V Only
GTL Reference	1.0V	0.833V or 1.0V, Auto-detect	0.833V

Because of the different signaling levels, an Intel® Pentium® III Processor with 512KB L2 Cache will not operate in an AGTL+ only processor platform. An AGTL+ only processor, similarly, will not operate in an AGTL Intel® Pentium® III Processor with 512KB L2 Cache platform. The Intel® Pentium® III Processor (CPUID 068xh) with AGTL Capability has auto-detecting I/O buffers that are compatible with both AGTL and AGTL+.

The termination resistors for the Intel® Pentium® III Processor with 512KB L2 Cache AGTL signaling are integrated into the processor package. This is similar to AGTL+ only processor implementation. The Rtt reference resistor is to be set to 56 ohms in a uni-processor platform and 68 ohms in a dual processor platform. This is different than the previous AGTL+ only processor platforms that have a range of allowable Rtt values.

For dual processor platforms with only one processor populated, a terminator must be plugged into the empty socket to maintain the correct termination of the host bus. The specifications for this terminator are contained the *Intel® Pentium® III Processor with 512KB L2 Cache Bus Terminator Design Guide*. The AGTL+ only processor platform terminator will not work in an Intel® Pentium® III Processor with 512KB L2 Cache platform because of the pin differences. Please consult the Intel Developer Website for vendor information.

7.7 Host Bus Layout Changes

The host bust routing recommendations may be different in an Intel® Pentium® III Processor with 512KB L2 Cache dual processor system than previous socket 370 dual processor designs. Intel recommends using the routing guidelines presented in this document for Intel® Pentium® III Processor with 512KB L2 Cache dual processor systems. Intel also recommends careful simulation of the host bus to verify a design's timing parameters.

The IBIS models for the Intel® Pentium® III Processor with 512KB L2 Cache and Intel® Pentium® III Processor (CPUID 068xh) with AGTL Capability are available from the Intel Developer Website. Please contact chipset vendors for buffer models for their products.

7.8 Single Ended Clocking Support

The Intel® Pentium® III Processor with 512KB L2 Cache supports both 1.0V differential and 2.5V single-ended (SE) clocking. The processor will auto-detect the clocking method in use by monitoring the Y33 (BLCK#) pin for activity at reset. The clocking specifications for differential and SE clocking can be found in the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet*. The specifications for SE clocking in the Intel® Pentium® III Processor with 512KB L2 Cache platform are more constrained than the previous AGTL+ only processor platform. This tighter timing specification is to allow SE clocking to maintain frequency parity with differential clocking. The processor clocking circuitry of any legacy platform that is being updated for Intel® Pentium® III Processor with 512KB L2 Cache support should be closely examined to ensure it meets the tighter timing specification.

Intel expects only minor modifications to existing high quality clock drivers to meet the new timing specification. Please contact your chipset vendor for clock vendor information.

7.9 VID & BSEL Signals

The Intel® Pentium® III Processor with 512KB L2 Cache introduces a new implementation of the VID and BSEL signals. The VID and BSEL signals are now volatile and are only valid after the qualifying signal, DYN_OE is active. The logic that sets these signals to the correct value is powered by VTT, so they will be unstable when power is first applied. Therefore, the VID and BSEL signals should only be sampled after DYN_OE is active, indicating that these outputs are now in a valid state.

7.9.1 Power On Sequence

The power on sequence for the Intel® Pentium® III Processor with 512KB L2 Cache has changed as compared to AGTL+ only processors. The Intel® Pentium® III Processor with 512KB L2 Cache now receives VTT_PWRGD as part of the sequence to indicate that the voltage regulator can latch the processor's operating voltage and begin to drive Vcc_{CORE}. Please refer to the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet* for more information on the required power up sequence.

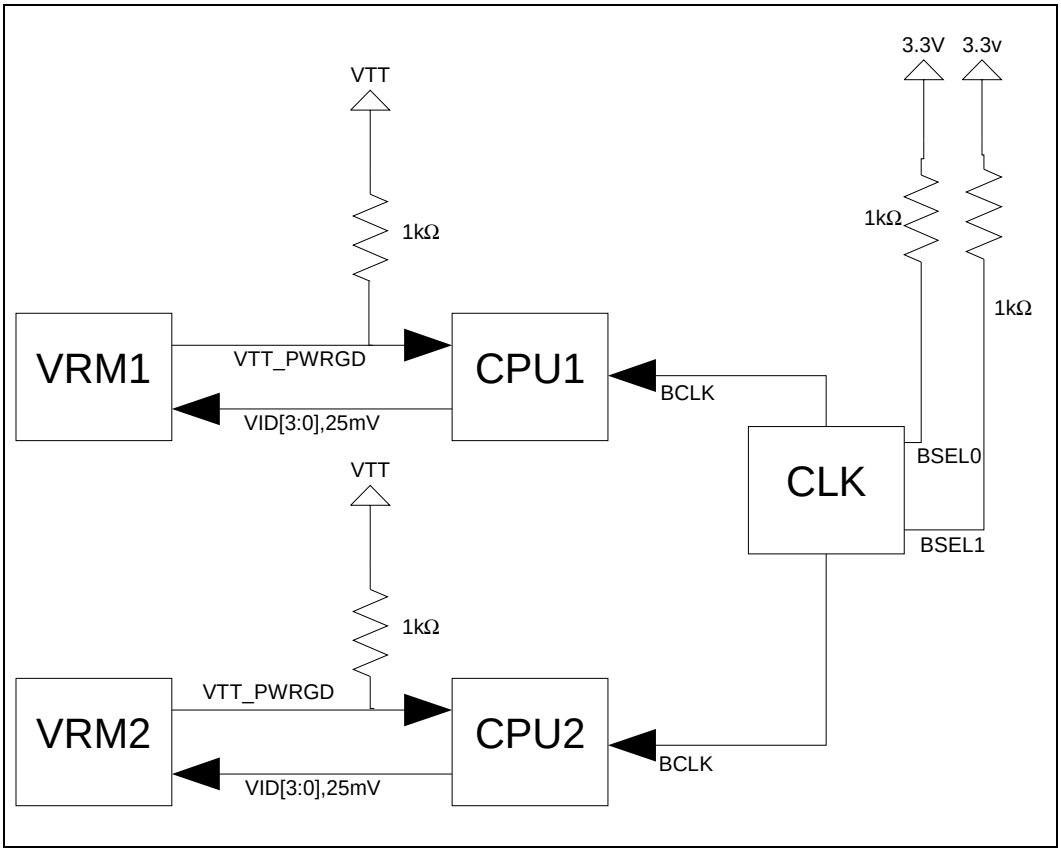
7.9.2 Signalling Changes

On the Intel® Pentium® III Processor with 512KB L2 Cache, the VID and BSEL signals are true open drain CMOS outputs and are no longer shorts or opens to VSS. Because of this, these signals now need to be pulled-up to 3.3V through 1KΩ resistors.

7.9.3 Legacy Clock Driver Support

In legacy systems being converted to Intel® Pentium® III Processor with 512KB L2 Cache based systems and in single-ended clocking systems, the clock driver may not support the new VTT-PWRGD signal. In this case, it is necessary to modify the standard power sequencing circuit mentioned in the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet*. Figure 7-5 shows a summary of modifications needed.

Figure 7-5. SE Clocking Implementation



The first modification that must be made is to strap the clocking and chipset circuitry to operate at 133 MHz. This is done by pulling up the BSEL pins on these devices to 3.3V. The clock generator and chipset will now always operate at 133 MHz and will no longer depend on the processor to drive the host bus frequency to the BSEL pins at power. Please note, however, that 133 MHz capable processors are all that can be used in the system once this modification is made.

The VTT_PWRGD routing must also be modified to allow for legacy clock driver support. Even though the host bus clocking is being strapped to a set value, the processors still require VTT_PWRGD to do VID determination. The VTT_PWRGD signal from the selected VR should be routed to the VTT_PWRGD input on both processor sockets. By routing the VTT_PWRGD signal this way, the signal will be available to both processor sockets if only one contains a processor.

Dynamic BSEL selection could be used in a legacy or single-ended clock driver system. A complex circuit to delay power delivery to the clock drivers and chipsets is needed to allow for dynamic BSEL operation. Intel will not be pursuing such a design recommendation.

7.10 PICCLK Voltage Change

The voltage level for the PICCLK signal has changed to 2.0 volts. This change may require adjustments to the PICCLK generator or external circuitry added to current designs so they provide the correct voltage ranges.

7.11 ITP Changes

The Intel® Pentium® III Processor with 512KB L2 Cache uses different signaling levels than AGTL+ only processors. Because of this, the In-Target Probe (ITP) interposer used for AGTL+ only processors is not compatible with the Intel® Pentium® III Processor with 512KB L2 Cache platform. A new interposer and software are available for the Intel® Pentium® III Processor with 512KB L2 Cache platform. Please consult your ITP vendor for details.

7.12 Logic Analyzer Interface

The Intel® Pentium® III Processor with 512KB L2 Cache uses the AGTL signalling scheme. Since the voltage swings and thresholds are different in AGTL than AGTL+ only processor platforms, a new logic analyzer interface is required. Please contact your logic analyzer vendor for a compatible logic analyzer interface.

This page intentionally left blank

System Design Checklist 8

8.1 Introduction

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an Intel® Pentium® III Processor with 512KB L2 Cache system design. This is not a complete list and does not guarantee that a design will function properly. Besides the items in the following text, refer to the most recent version of the design guide for more detailed instructions on designing a motherboard.

8.2 Design Checklist Summary

The following tables contain design considerations for the various portions of a design. Each table describes one portion and is titled accordingly.

8.3 Host Interface AGTL Bus and AGTL Signals

It is strongly recommended that AGTL signals be routed on signal layers next to the ground layer. It is important to provide effective signal return paths with low inductance.

Table 8-1. AGTL Signals (Sheet 1 of 2)

CPU Pin	Pin Connection
A[35:3]#	Connect to chipset and second CPU.
ADS#	Connect to chipset and second CPU.
AERR#	Connect to chipset and second CPU. Pull up to V_{TT} through a 150W resistor at chipset. See Wired-OR section for details.
AP[1:0]#	Connect to chipset and second CPU.
BERR#	Connect to chipset and second CPU. Pull up to V_{TT} through a 150W resistor at chipset. See Wired-OR section for details
BINIT#	Connect to chipset and second CPU. Pull up to V_{TT} through a 150W resistor at chipset. See Wired-OR section for details
BNR#	Connect to chipset and second CPU. Pull up to V_{TT} through a 150W resistor at chipset. See Wired-OR section for details
BP[3:2]#	Leave as N/C.
BPM[1:0]	Leave as N/C.
BPRI#	Connect to chipset and second CPU.
BR0#	Connect BR0# from CPU0 to BR1# of CPU1. Connect BREQ0# of CPU0 to BR0# of chipset.
BR1#	Connect BR1# from CPU0 to BR0# of CPU1.
D[63:0]#	Connect to chipset and second CPU.
DBSY#	Connect to chipset and second CPU.

Table 8-1. AGTL Signals (Sheet 2 of 2)

CPU Pin	Pin Connection
DEFER#	Connect to chipset and second CPU.
DEP[7:0]#	Connect to chipset and second CPU.
DRDY#	Connect to chipset and second CPU.
HIT#	Connect to chipset and second CPU. Pull up to V_{TT} through a 150Ω resistor at chipset. See Wired-OR section for details
HITM#	Connect to chipset and second CPU. Pull up to V_{TT} through a 150Ω resistor at chipset. See Wired-OR section for details
LOCK#	Connect to chipset and second CPU.
REQ[4:0]#	Connect to chipset and second CPU.
RESET#	86 Ω pull-up to V_{TT} tied to 22 Ω series resistor to a 10 pF cap to ground, connect to chipset and second CPU. Connect to ITP pin 2 (RESET#) with 240 Ω series resistor and 68Ω pull-up to V_{TT}.
RESET2#	Not Connected
RP#	Connect to chipset and second CPU.
RS[2:0]#	Connect to chipset and second CPU.
RSP#	Connect to chipset and second CPU.
TRDY#	Connect to chipset and second CPU.

8.4 CMOS (Non-AGTL) Signals

It is recommended to route CMOS signal traces on one signal layer, and not next to AGTL traces. Try to avoid long traces to eliminate speed path issues, especially for APIC clock and APID data signals.

Table 8-2. CMOS Signals (Sheet 1 of 2)

CPU Pin	Pin Connection
A20M#	Connect to second CPU and pull up through ~330 Ω to VccCMOS. May also need to be connected to chipset or compatibility logic. For boards supporting preproduction processors, this pin must be connected to frequency selection circuitry.
FERR#	Connect to second CPU and pull up through ~150 Ω to VccCMOS. May need to connect to chipset or server management logic.
FLUSH#	Connect to second CPU and pull up through ~150 Ω to VccCMOS
IERR#	Pull up through ~150 Ω to VccCMOS if connected to external logic. Leave unconnected otherwise.
IGNNE#	Connect to second CPU and pull up through ~330 Ω to VccCMOS. May also need to be connected to chipset or compatibility logic. For boards supporting preproduction processors, this pin must be connected to frequency selection circuitry.
INIT#	Connect to second CPU and pull up through ~330 Ω to VccCMOS. May also need to be connected to chipset or compatibility logic.
LINT0/INTR	Connect to interrupt control logic and second CPU and pull up through ~330 Ω to VccCMOS. For boards supporting preproduction processors, this pin must be connected to frequency selection circuitry.

Table 8-2. CMOS Signals (Sheet 2 of 2)

CPU Pin	Pin Connection
LINT1/NMI	Connect to interrupt control logic and second CPU and pull up through ~330 Ω to VccCMOS. For boards supporting preproduction processors, this pin must be connected to frequency selection circuitry.
PICD[1:0]	Connect to second CPU and pull up through ~150 Ω to VccCMOS. May also need to be connect to interrupt control logic.
PWRGOOD	Connect to second CPUs and pull up through 150-330 Ω to 1.8 V. output from the PWRGOOD logic.
SLP#	Connect to second CPU and pull up through ~330 Ω to $Vcc_{CMOS1.5}$. May also need to be connected to chipset or compatibility logic.
SMI#	Connect to second CPU and pull up through ~330 Ω to $Vcc_{CMOS1.5}$. May also need to be connected to chipset or compatibility logic.
STPCLK#	Connect to second CPU and pull up through ~330 Ω to $Vcc_{CMOS1.5}$. May also need to be connected to chipset or compatibility logic.
THERMTRIP#	See Chapter 6 for more information.

8.5 TAP/ITP Checklist for 370-Pin Socket Processors

There are several mechanical, electrical, and functional constraints on the debug port which must be followed, please see the *Intel® Pentium® III Processor with 512KB L2 Cache Datasheet*, along with Chapter 3 of this document for details.

Table 8-3. TAP/ITP Signals

CPU Pin	Pin Connection
PRDY#	Pull-up resistor that matches GTL characteristic impedance to VTT, 240 Ω series resistor to ITP.
PREQ#	200-300 Ω pull-up to VccCMOS and connect to ITP.
TCK	39 Ω pull-down to Gnd, and connect to ITP.
TDO	150 Ω pull-up to VccCMOS and connect to ITP.
TDI	200-300 Ω pull-up to VccCMOS and connect to ITP. Connect TDI from CPU0 to TDO on CPU1.
TMS	39 Ω pull-up to VccCMOS and connect to ITP.
TRST#	500-680 Ω pull-down to Gnd and connect to ITP.

8.6 Miscellaneous Checklist for 370-Pin Socket Processors

Host bus clocks are critical. Signal integrity and timing of these signals should be carefully evaluated and simulated. It is strongly recommended that system bus clocks be routed on signal layers next to the ground layer and do not traverse multiple signal layers. Please see Chapter 4 for details.

Table 8-4. Clock Signals

CPU Pin	Pin Connection
BCLK BCLK#/CLKREF	For single ended clocking connect BCLK to clock generator through 22 - 33 Ω series resistor (OEM must simulate based on driver characteristics). Connect BCLK# to a filtered 1.25 V supply.To reduce pin-to-pin skew, tie host clock outputs together at the clock driver then route to both processors and chipset. For differential clocking signals must be length matched from the receivers to a resistive network, and from the network to the receiver. The resistive network consists of a 33.2 Ω 1% series resistor on each line, and a 475 Ω resistor between them. Lastly both lines are pulled down with a 63.4 Ω 1% resistor to GND. See Chapter 4 for more details.
PICCLK	Must be connected from the clock generator to the PICCLK pin on the CPUs. Voltage divider circuitry should yield 2.0 V (OEM must simulate based on driver characteristics).

Table 8-5. Miscellaneous Signals

CPU Pin	Pin Connection
BSEL0	For single ended clocking connect to clock generator **ONLY**. Pull up to 3.3 V with a 1 KΩ resistor. NC on processor 0 and 1. For differential clocking connect BSEL0 on CPU0 to BSEL0 on CPU1, pull up to 3.3 V with a 1 KΩ resistor, connect to clock generator
BSEL1	For single ended clocking connect to clock generator **ONLY**. Pull up to 3.3 V with a 1 KΩ resistor. NC on processor 0 and 1. For differential clocking connect BSEL1 on CPU0 to BSEL1 on CPU1, pull up to 3.3 V with a 1 KΩ resistor, connect to clock generator.
CPUPRES#	Tie to GND, leave it N/C, or could be connected to powergood logic to gate system from powering on if no processor is present.
DETECT	Leave unconnected or connect to Vss
KEY	Connect to Vss.
NCHCTRL	Pull up through 14 Ω to V_{TT}.
THERMDN	Thermal diode cathode. Connect to thermal sensor device.
THERMDP	Thermal diode anode. Connect to thermal sensor device.
RTTCTRL	68 Ω 1% pull-down to GND.

Table 8-5. Miscellaneous Signals

CPU Pin	Pin Connection
SLEWCTRL	110 Ω 1% pull-down to GND.
VID[3:0]	Connect to on-board VR or VRM. For on-board VR, a 1 KΩ pull-up to 3.3V is required. Some of these solutions have internal pull-ups. Optional override (jumpers, ASIC, etc) could be used. May also connect to system monitoring device.
VID25	Connect to on-board VR or VRM. 25mV should connect to VID5 or VID25mV. For on-board VR, a 1 KΩ pull-up to 3.3V is required. Some of these solutions have internal pull-ups. Optional override (jumpers, ASIC, etc) could be used. May also connect to system monitoring device.

Table 8-6. Power Signals

CPU Pin	Pin Connection
DYN_OE	Connected to V_{TT} through a 1 KΩ pullup resistor
PLL1, PLL2	Low pass filter on VCC_{CORE} provided on MB. Typically a 4.7 µH inductor in series with VCC_{CORE} is connected to PLL1 then through a series 22-100µF capacitor to PLL2.
$Vcc_{CMOS1.5}$	Connected to the Vcc1.5 power supply. Must have some high and low frequency decoupling.
$Vcc_{CMOS2.5}$	Connected to 2.5 V voltage source. Should have some high and low frequency decoupling.
$Vcc_{CMOS1.8}$	Connected to 1.8V voltage source. Should have some high and low frequency decoupling.
VCC_{CORE}	Connect to core voltage regulator. Provide low frequency decoupling. Guidelines: 16 4.7µF in 1206 package placed inside PGA370 socket cavity on primary side of board.
VREF[7:0]	Connect to Vref voltage divider made up of 75 Ω 1% and 150 Ω 1% resistors connected to V_{TT}. Processor VREF must be separate from Chipset VREF. Guidelines: Three each (minimum) 0.1 µF in 0603 package placed within 500 mils of VREF pins.
VCMOS_REF	Connect to 1.0 V voltage divider derived from VccCMOS.
VTT_ PWRGD	Connected to V_{TT} through a 1 KΩ pullup resistor, and connect to VTT_PWRGD circuitry.
VTT	Connect AG1, AK16, AL13, AL21, AN11, AN15, G35, G37, AD36, AB36, X34, AA33, AA35, AN21, E23, S33, S37, U35, U37, AH20 to 1.25 V regulator. Provide high and low frequency decoupling. Guidelines: 20 0.1 µF in 0603 package placed within 200 mils of each PGA 370 socket; place as many as possible inside socket cavity.
Reserved	The following pins must be left as no-connects: AK30, AL1, E21, F10, L33, N33, N35, Q33, Q35, Q37, R2, W35, X2, Y1, Z36.

This page intentionally left blank