Intel® Pentium® III Processor with 512KB L2 Cache Dual Processor Platform

Design Guide Update

December 2001

Document Number: 298647-001

Contents

Revision History

Revision	Draft/Changes	Date
-001	Initial Release	December 2001

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® Pentium® III Processor with 512KB L2 Cache Dual Processor Platform Design Guide	249658-001

Nomenclature

General Design Considerations includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® Pentium® III processor with 512KB L2 cache.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Shaded: This item is either new or modified from the previous version of the document.

Number.	GENERAL DESIGN CONSIDERATIONS
	There are no General Design Considerations changes in this Design Guide Update revision.

Number	DOCUMENTATION CHANGES
1	Changed: Design Guide Introduction, Section 1; Modified
2	Changed: State of the Data, Section 1.4; Modified
3	Changed: General Topology and Layout Requirements, Section 3.2; Changed and Expanded
4	Changed: System Design Checklist Table 8-6.Power Signals; Modified

This page is intentionally left blank.

General Design Considerations

There are no General Design Considerations changes in this Design Guide Update revision.

This page is intentionally left blank.

Documentation Changes

1. Changed: Design Guide Introduction, Section 1; Modified

The first sentence of the first paragraph has been changed to read:

> This design guide documents Intel's design recommendations for dual-processor systems based on the Intel® Pentium® III Processor with 512K L2 Cache processor and the Intel® Pentium® III Processor (CPUID 068xh) with AGTL signaling capability for use with either the Micron* Copperhead chipset, or the Serverworks* HE-SL chipset.

2. Changed: State of the Data, Section 1.4; Modified

Add the following sentence to the end of the paragraph:

> The recommendations for the Micron* Copperhead chipset are based on pre-silicon simulations.

3. Changed: General Topology and Layout Requirements, Section 3.2; Changed and Expanded

The first sentence of the paragraph following Figure 3-1 has been changed to the following:

> Table 3-5 and Table 3-5a contain the length specifications for the segments of the T-topology.

The following table has been added after Table 3-5:

Table 3-5a. Trace Lengths for T Topology (Micron Chipset)

Segment	Min Length (inches)	Max Length (inches)
L0	3.25	3.75
L1	3.25	3.75
L2	1.75	2.5

The following table has been added after Table 3-7:

Table 3-7a. Trace Lengths for Terminator-less T Topology (Micron chipset)

Segment	Min Length (inches)	Max Length (inches)
L0	3.25	3.75
L1	3.25	3.75
L2	1.75	2.5
L3	0.0	1.0

4. Changed: System Design Checklist Table 8-6.Power Signals

The following checklist item is changed in Table 8-6.Power Signals:

VCMOS_REF	Connect to 1.0V voltage divider derived from VccCMOS. Voltage divider is made up of 75Ω 1% and 150Ω 1% resistors.