



***Pentium[®] II Processor –
Low-Power Module at 266 MHz
66-MHz SDRAM DIMM
Routing Guidelines***

Application Note

June 1999



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1.0 Introduction

The purpose of this application note is to define the routing guidelines for 66-MHz SDRAM DIMM memory systems in Pentium® II Processor – Low-Power Module/Intel 440BX AGPset systems. The routing guidelines are specified in pre-layout simulation results only. Post-layout simulations and post-silicon signal integrity analysis are not available to correlate with the pre-layout simulation results. Therefore, when following these guidelines, it is recommended that the developer simulate these signals for proper signal integrity, flight time and cross talk.

1.1 Key Terms

The Pentium® II Processor – Low-Power Module is identical to the Intel® Pentium II Processor Mobile Module Connector 2 (MMC-2). A complete description of this module is located in the *Intel® Pentium® II Processor – Low-Power Module* datasheet (order number 273256).

Intel 440BX AGPset refers to both the 82443BX Host Bridge/Controller and the 82371EB PCI ISA IDE Xcelerator. A complete description of this chipset is located in the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet (order number 290633).

SDRAM DIMM refers to synchronous DRAM dual in-line memory modules.

1.2 Related Documents

These documents are available for download from Intel’s World Wide Web site at <http://www.intel.com>.

Table 1. Related Intel Documents

| Document Title | Order Number |
|---|---|
| <i>Intel® Pentium® II Processor – Low-Power Module</i> datasheet | 273256 |
| <i>Mobile Pentium® II Processor Specification Update</i> | 243887 |
| <i>Intel® 440BX AGPset: 82443BX Host Bridge/Controller</i> datasheet | 290633 |
| <i>82443BX Host Bridge/Controller Electrical and Thermal Specification</i> datasheet addendum | 273218 |
| <i>Intel® 440BX AGPset: 82443BX Host Bridge/Controller Specification Update</i> | 290639 |
| <i>4-Clock 66 MHz 72-Bit ECC Unbuffered SDRAM DIMM Specification, Rev. 1.0</i> | Contact your Field Sales Representative |

1.3 66 MHz SDRAM DIMM System Considerations

The 66-MHz SDRAM DIMM system differs from a 66-MHz SO-DIMM system; there are a few fundamental differences that must be understood when designing a system to support 66-MHz SDRAM DIMM operation. Refer to Table 2 for a list of these differences.

Table 2. SDRAM DIMM and SO-DIMM Differences

| | 66-MHz SDRAM DIMM | 66-MHz SO-DIMM |
|------------------------|------------------------|-----------------------|
| Routing Length | 2 – 9 in. [†] | 1.2 – 3.94 in. |
| Clocking | 4 Clocks | 2 Clock |
| Board Impedance | 70 Ω \pm 15% | 60 Ω \pm 15% |

[†] Depending on the signal traces, routing lengths can vary. Refer to the *4-Clock 66 MHz 72-Bit ECC Unbuffered SDRAM DIMM Specification* for more information.

2.0 66-MHz SDRAM DIMM Memory Guidelines

This section lists guidelines to be followed when routing the signal traces for the board design. The order in which signals are routed first and last will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing all of the high speed bus signals first. Either order can be used, as long as the guidelines listed here are followed. Even when these guidelines are followed, it is still highly recommended that the developer simulate these signals for proper signal integrity, flight time and cross talk.

2.1 66-MHz SDRAM DIMM Interface Overview

The 82443BX Host Bridge/Controller integrates a main memory DRAM controller that supports a 72-bit SDRAM array for 66-MHz environments. The DRAM controller interface is fully configurable through a set of control registers. A complete description of these registers is provided in the *Intel[®] 440BX AGPset: 82443BX Host Bridge/Controller* datasheet (order number 290633).

2.1.1 SDRAM Interface Signals

The following section explains the connectivity between the Low-Power Module and the 66-MHz SDRAM DIMMs. A list of the signal names that are used in the 66-MHz SDRAM DIMM interface is provided in Table 3.

Note: MAB[13,10] are not inverted. These address bits are used to define various SDRAM commands.

2.2 66-MHz SDRAM DIMM Layout Guidelines

Table 3. SDRAM Connectivity

| 82443BX Pins/Connection | DIMM Pins | Pin Function |
|------------------------------------|--|-------------------------------|
| CKBF buffer outputs DCLK[x:y] | CK[3:0] (4 DCLKs per DIMM) | Clock |
| CKE[3:0] | CKE[1:0] | Clock Enable |
| CSA#[3:0] | S#[1:0] (2 CS per DIMM) S#[3:2] (2 CS per DIMM) | Chip Select |
| GND | A13 | Address |
| MAB10, MAB#[9:0] | A[10:0] | Address |
| MAB#11 | BA0 | Address |
| MAB#12 | BA1, A12 | Address |
| MAB13 | A11 | Address |
| MD[63:0] | DQ[63:0] | Data |
| MECC[7:0] | CB[7:0] | Error Checking and Correction |
| Strap for SMBus Individual Address | SA[2:0] | SMBus Address |
| SMBDATA | SDA | SMBus Data |
| SMBCLK | SCL | SMBus Clock |
| SCASA# | CAS# | SDRAM Column Address Select |
| SRASA# | RAS# | SDRAM Row Address Select |
| WEA# | WE0# | Write Enable |

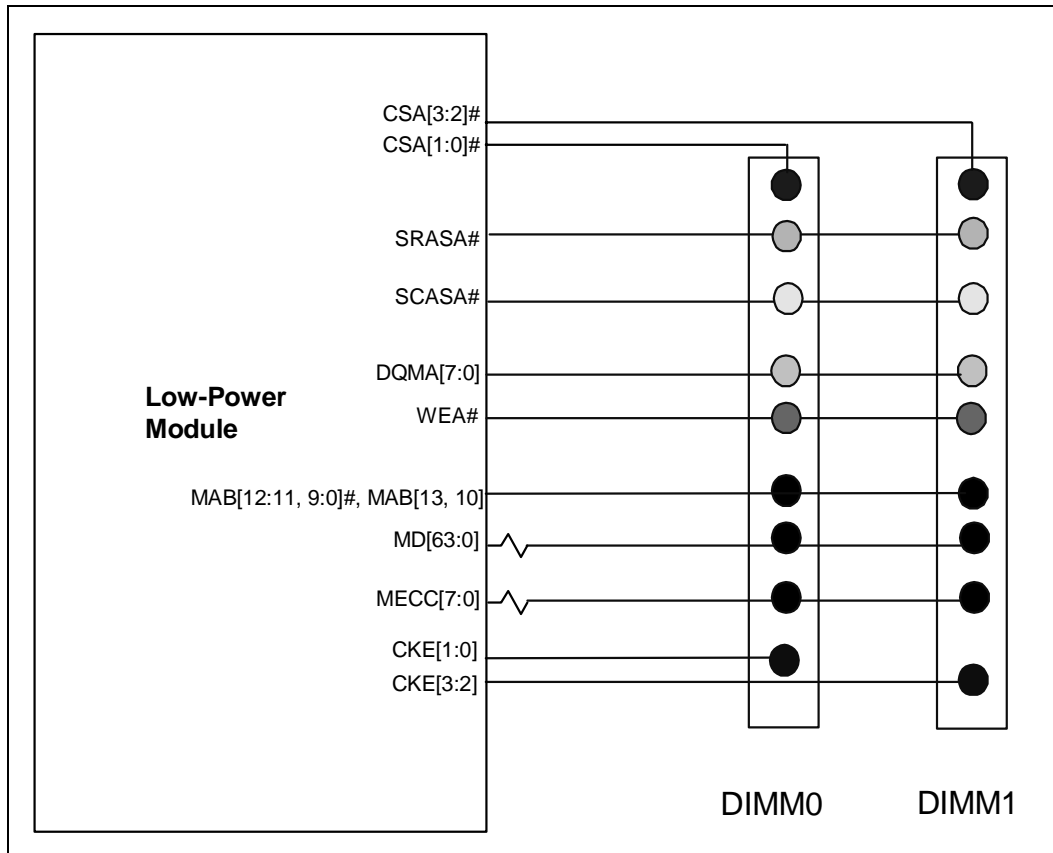
NOTES:

1. Some of the pin ranges above are dependent on which DIMM is being reviewed; “x” and “y” indicate signal copies.
2. The memory data bit traces may be byte-swapped to simplify board routing and minimize trace lengths. This should also be done for the data bits within the byte channel.
3. Board impedance should be $55 \Omega \pm 10\%$.
4. All resistors should be maximum 5% tolerance.
5. Populate the furthest DIMM first to avoid stub reflections.
6. See the *SDRAM Serial Presence Detect Data Structure* Specification for information on EEPROM register contents (<http://developer.intel.com/design/chipsets/memory/spdsd12a.htm>).

2.2.1 DIMM Connection - SDRAM

Figure 1 shows the DIMM connections on the system electronics. The guidelines described in this document are based on the assumption that 2-DIMM slots are present on the system electronics.

Figure 1. SDRAM - 2 DIMMs



2.2.2 Trace Lengths for 2 DIMM Design

The following section illustrates signal topology and provides the minimum and maximum trace lengths to the DIMM connector pads for each signal group in a 2-DIMM design.

2.2.2.1 Data - MD[63:0], MECC[7:0]

Figure 2. MD[63:0], MECC[7:0] Topology

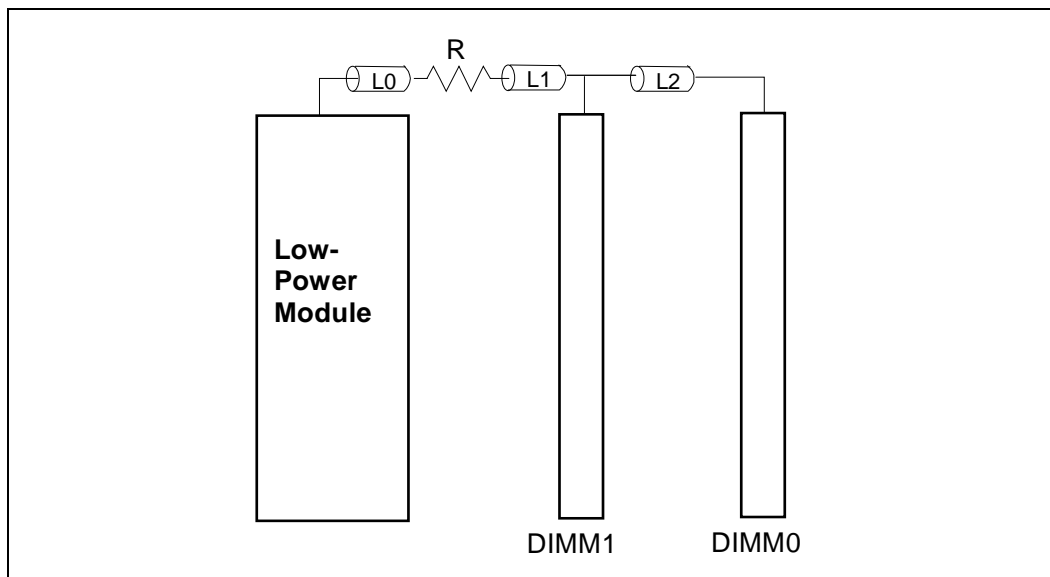


Table 4. Trace lengths MD[63:0], MECC[7:0]

| Section | Minimum | Maximum |
|----------|---------|----------------------|
| L0 | n/a | 1.0 in. |
| L2 | n/a | 1.0 in. |
| L0+L1+L2 | 1.0 in. | 8.0 in. |
| Series R | n/a | 18 Ω \pm 5% |

Figure 3. DQMA[7:0] Topology

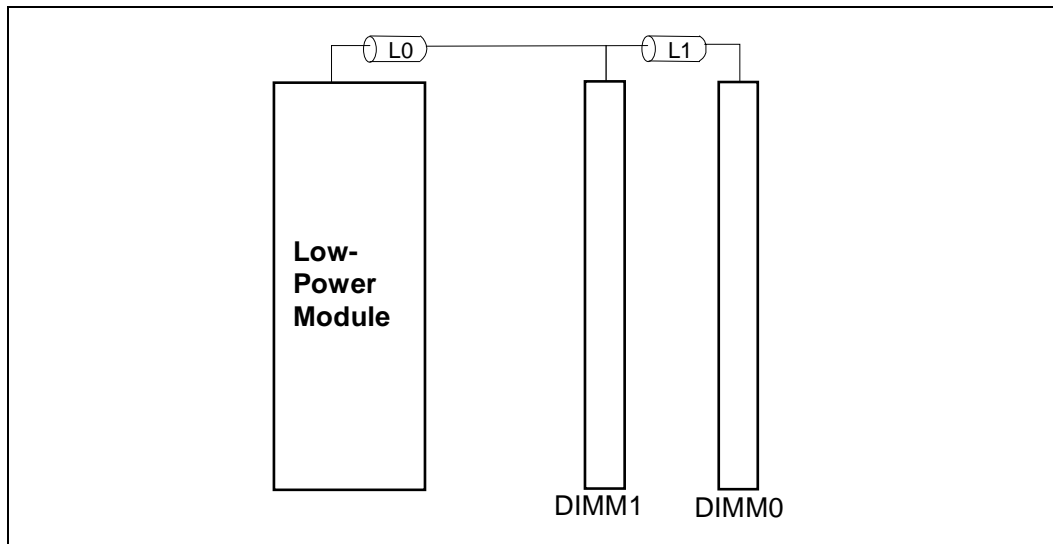


Table 5. Trace Lengths for DQMA[7:0]

| Section | Minimum | Maximum |
|---------|---------|---------|
| L0 | 1.0 in. | n/a |
| L1 | n/a | 1.0 in. |
| L0 + L1 | 1.0 in. | 8 in. |

2.2.2.2 Chip Select - CSA[3:0]#

Figure 4. CSA[3:0]# Topology

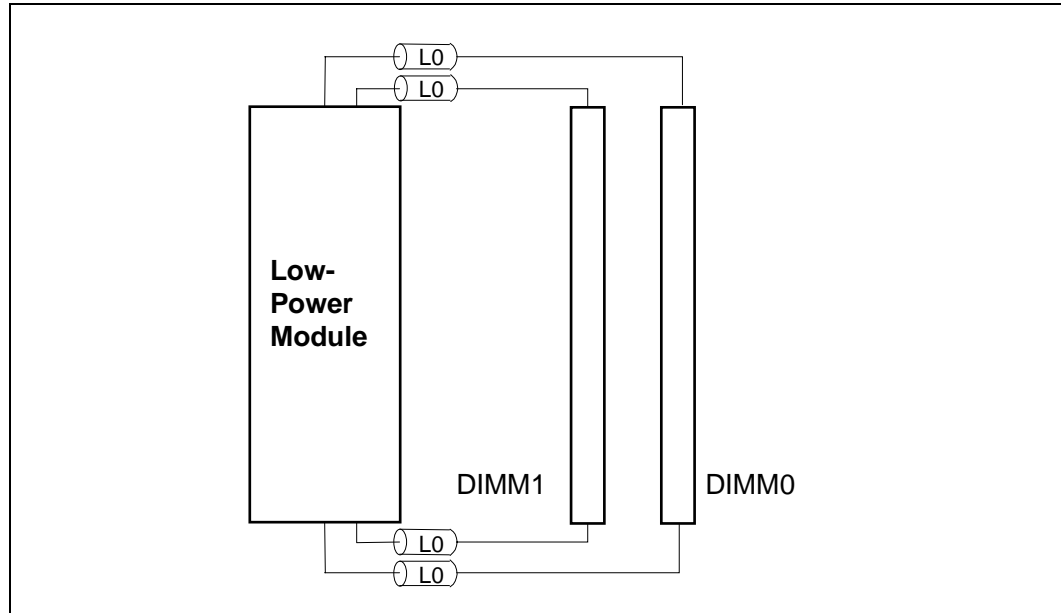


Table 6. Trace Lengths for CSA[3:0]#

| Section | Minimum | Maximum |
|---------|---------|---------|
| L0 | 1 in. | 5 in. |

2.2.2.3 Clock Enable - CKE[3:0]

Figure 5. CKE[3:0] Topology

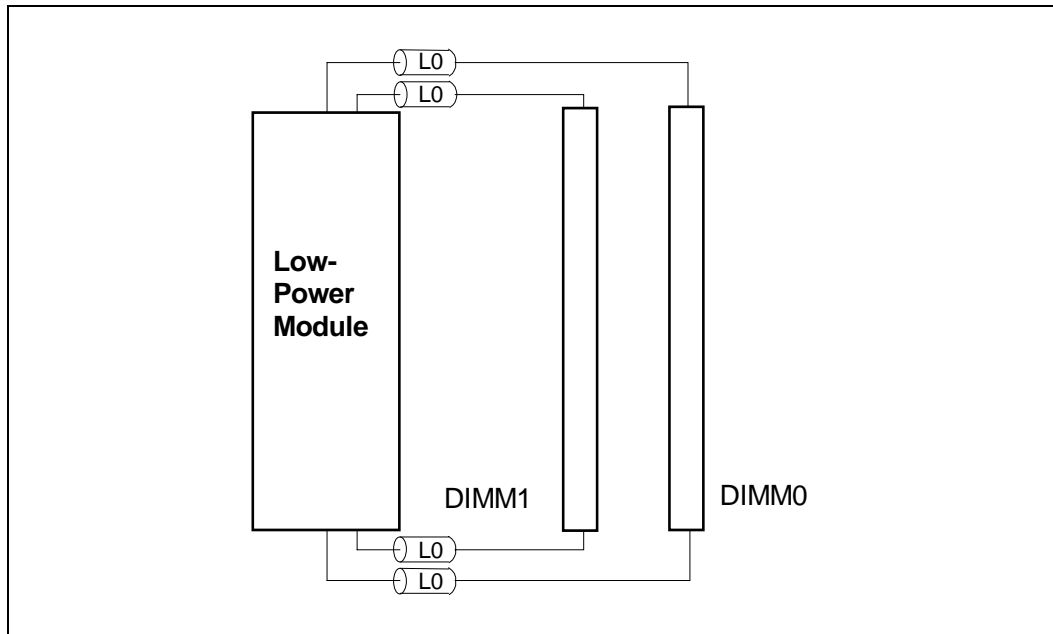


Table 7. Trace lengths for CKE[3:0]

| Section | Minimum | Maximum |
|---------|---------|---------|
| L0 | 1 in. | 5 in. |

2.2.2.4 Command - MAB[13:0]x, WEA#, SRASA#, SCASA#

Figure 6. MAB[13:0]x, WEA#, SRASA#, SCASA# Topology

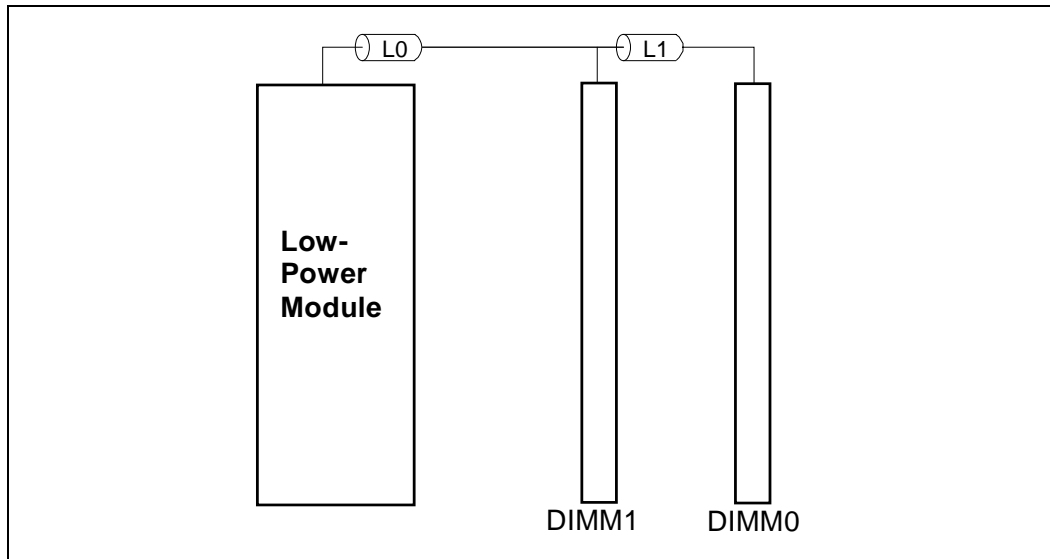


Table 8. Trace Lengths for MAB[13:0]x, WEA#, SRASA#, SCASA#

| Section | Minimum | Maximum |
|---------|---------|---------|
| L0 | 1.0 in. | n/a |
| L1 | n/a | 1.0 in. |
| L0 + L1 | 1.0 in. | 8 in. |

3.0 SDRAM Clock Guidelines

This section defines the clock timing, lengths and series termination for SDRAM-related clocks.

3.1 Timing Guidelines

Figure 7 and Table 9 show a simplified SDRAM clock layout for the timing specifications.

Note: Even when following the SDRAM clock layout guidelines, it is highly recommended that the developer ensure that the maximum and minimum SDRAM clock skews are within the timing specifications.

Figure 7. SDRAM Clock Timing Specification

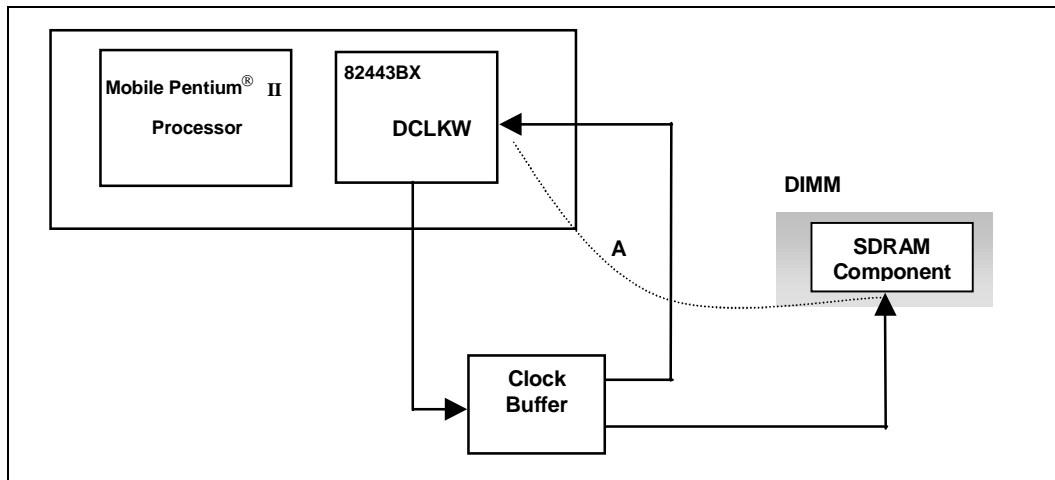


Table 9. Timing Specifications for Maximum and Minimum SDRAM Clock Skews

| Symbol | Description | Ck100-M Pin-to-Pin | Boards | Total |
|--------|-----------------------------|-------------------------------|-------------------------------|-------------------------------|
| A | DCLKWR to SDRAM (SCLK) skew | 250 ps (max) -250 ps (min) | 400 ps (max) -400 ps (min) | 650 ps (max) -650 ps (min) |

3.2 Clock Layout Guidelines

The following guidelines are required for proper clock layout:

- Series matching resistors are required.
 - Place as near to the driver pin as possible, less than 1inch.
- Route all clocks on internal layers to provide better trace delay consistency and EMI containment.
- Set board impedance at $55 \Omega \pm 10\%$.
- Minimize the usage of vias in clock signals.
- Set the width to spacing ratio of all clocks to 1:2.

Figure 8. Clocking Layout Diagram - 66 MHz

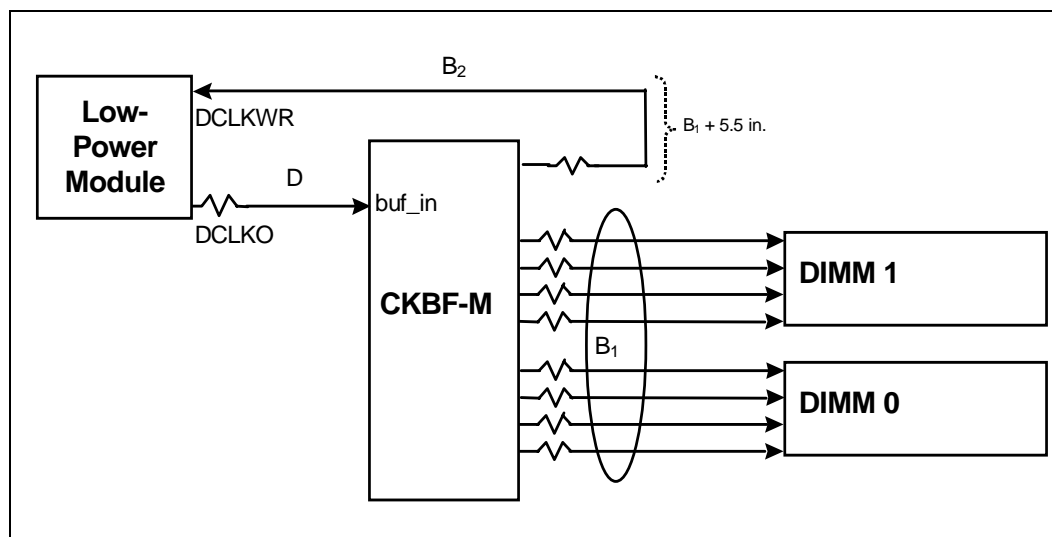


Table 10. Trace Lengths for SDRAM Clocks and DCLK

| Variable | Trace Impedance | Trace Length | Minimum | Maximum | Resistor |
|----------------|----------------------|--------------|---------|---------|---------------------|
| D | $55 \Omega \pm 10\%$ | n/a | 0 in. | 4.0 in. | $18 \Omega \pm 5\%$ |
| B ₁ | $55 \Omega \pm 10\%$ | B | 0 in. | 3.0 in. | $8 \Omega \pm 5\%$ |
| B ₂ | $55 \Omega \pm 10\%$ | B + 5.5 in. | 5.5 in. | 8.5 in. | $20 \Omega \pm 5\%$ |

