Pentium® III Processor – Low-Power Module

Datasheet

Product Features

- Mobile Pentium® III processor at 500 MHz
- On-die, primary 16-Kbyte Instruction cache and 16-Kbyte Write Back Data cache
- On-die, 256-Kbyte L2 cache
  - — Eight-way set associative
  - — Runs at the speed of the processor core
- Fully compatible with previous Intel mobile microprocessors
  - — Binary compatible with all applications
  - — Support for MMX™ technology
- Supports streaming SIMD
- Power management features that provide low-power dissipation
  - — Quick Start mode
  - — Deep Sleep mode
- Integrated math co-processor
- Integrated active thermal feedback (ATF) system
- Programmable trip point interrupt or poll mode for temperature reading
- Intel 82443BX Host Bridge/Controller
  - — DRAM controller supports 3.3-V SDRAM at 100 MHz
  - — Supports PCI CLKRUN# protocol
  - — SDRAM clock enable support and self-refresh of SDRAM during Suspend mode
  - — PCI bus control 3.3 V only, *PCI Specification Revision 2.1* compliant
- Supports a single AGP 66-MHz, 3.3-V device
- Thermal transfer plate (TTP) for heat dissipation
- Above 80% peak efficiency
- Integrated VR solution

Order Number: 273299-001
January 2000

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Revision History

Date	Revision	Updates
January 2000	001	Initial Release

1.0 Introduction

This document provides the technical specifications for integrating the Pentium® III Processor – Low-Power Module into the latest applied computing systems for today's embedded market.

Building around this design gives the system manufacturer these advantages:

- Avoids complexities associated with designing high-speed processor core logic boards.
- Provides an upgrade path from previous Intel Low-Power Modules using a standard interface.

1.1 References

Refer to the following documents for additional information relating to the Pentium III Processor – Low-Power Module.

Table 1. Related Documents

Document Title	Order Number or URL
Mobile Pentium® III Processor in BGA2 and Micro-PGA2 Packages at 400 MHz, 450 MHz, and 500 MHz datasheet	245302
Mobile Pentium® III Processor Specification Update	245306
Intel® 440BX AGPSet: 82443BX Host Bridge/Controller datasheet	290633
Intel® 440BX AGPset 82443BX Host Bridge/Controller Specification Update	290639
82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) datasheet	290562
82371EB PCI-to-ISA/IDE Xcelerator (PIIX4E) Specification Update	290635
CK97 Clock Synthesizer Design Guidelines	243867
Intel Pentium® III Processor - Low-Power Module Design Guide	273319
Low-Power Module Memory Bus Simulation Methodology	273316
PLow-Power Module SDRAM DIMM Routing Guidelines	273317
Mobile Pentium® II Processor and Pentium II Processor Mobile Module Thermal Sensor Interface Specifications	243724
66/100 MHz PC SDRAM Unbuffered SO-DIMM Specification Rev 1.0	http://www.intel.com/design/chipsets/memory/sdram.htm

2.0 Architecture Overview

The module contains a mobile Pentium III processor core that runs at 500 MHz with a 100-MHz processor system bus (PSB) speed.

The Intel® 440BX AGPset provides immediate system-level support and includes the PIIX4E PCI/ISA bridge and the Intel 82443BX Host Bridge/Controller. The PIIX4E provides extensive power management capabilities and supports the 82443BX Host Bridge/Controller. The system electronics should include a PIIX4E device to connect to the Low-Power Module.

Key features of the Intel 82443BX Host Bridge/Controller include: the DRAM controller supporting SDRAM at 3.3 V with a burst read at x-1-1-1; a PCI CLKRUN# signal to request the PIIX4E to regulate the PCI clock on the PCI bus; the 82443BX clock enables Self-Refresh mode of SDRAM during Suspend mode and is compatible with SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM) modes of power management; and E_SMRAM mode supports write-back cacheable SMRAM up to 1 Mbyte.

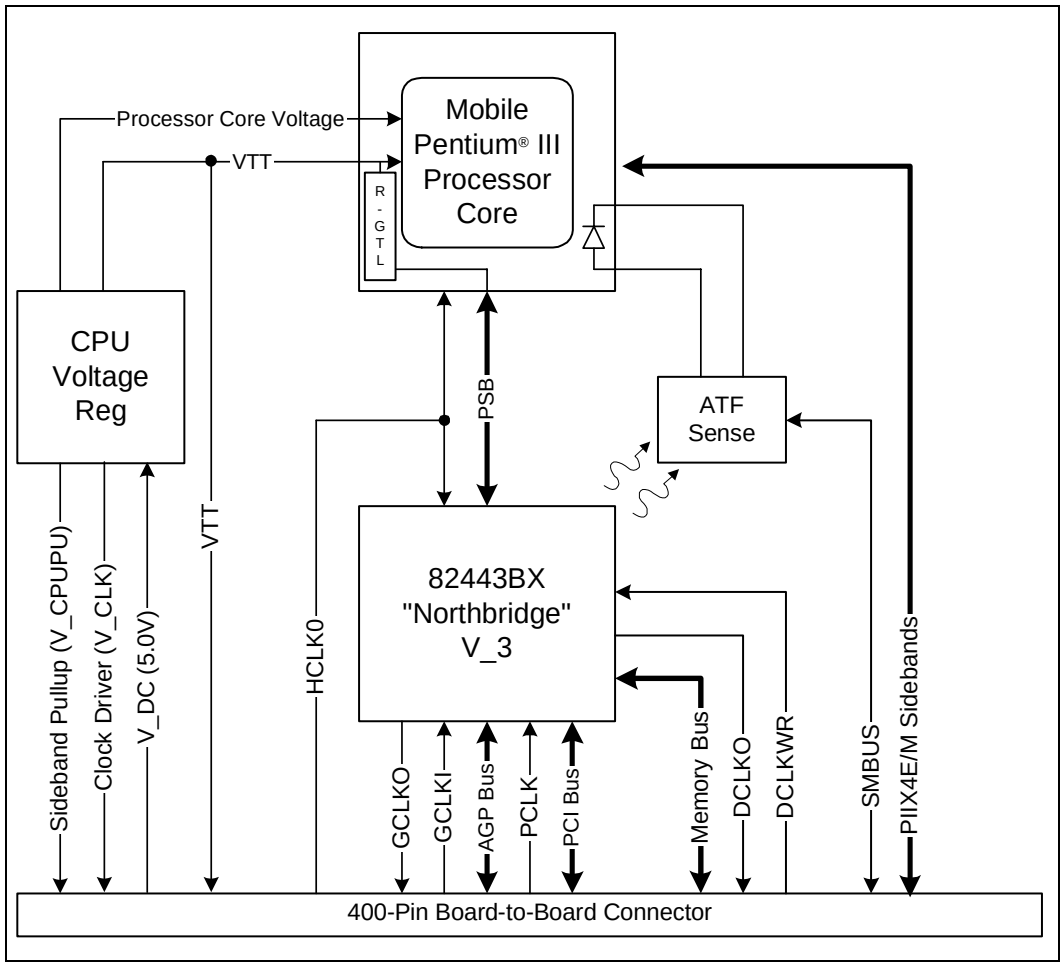
A thermal transfer plate on the mobile Pentium III processor and the 82443BX Host Bridge/Controller provides heat dissipation and thermal attach points for the manufacturer's thermal solution.

An on-board voltage regulator converts the system DC voltage to the processor's core and I/O voltage. Isolating the processor voltage requirements allows the system manufacturer to incorporate different processor variants into a single applied computing system that supports an input voltage of 5.0 V DC. The integrated module voltage regulator enables an above 80% peak efficiency and de-couples the processor voltage requirements from the system.

Also incorporated is active thermal feedback (ATF) sensing, compliant to the *ACPI Specification Rev 1.0*. An integrated system management bus (SMBus) compliant thermal sensor supports the internal and external temperature sensing with programmable trip points.

Figure 1 illustrates the block diagram of the Pentium III Processor – Low-Power Module.

Figure 1. Pentium® III Processor – Low-Power Module Block Diagram



3.0 Signal Information

This section provides information on the signal groups for the Pentium III Processor Low-Power Module.

3.1 Signal Definitions

Table 2 provides a list of signals by category and the corresponding number of signals in each category. For proper signal termination, see the *Low-Power Module Design Guide* (order number 273319).

Table 2. Connector Signal Summary

Signal Group	Number of Pins
Memory	109
AGP	60
PCI	58
Processor/PIIX4E Sideband	8
Power Management	7
Clocks	9
Voltage: V_DC	20
Voltage: V_3S	9
Voltage: V_3	16
Voltage: V_5	3
Voltage: VCCAGP	4
Voltage: V_CPUPU	1
Voltage: V_CLK	1
ITP/JTAG	9
Module ID	4
Ground	45
Reserved	37
Total	400

3.1.1 Signal List

The following notations are used to denote signal type:

I	Input pin
O	Output pin
O D	Open-drain output pin requiring a pullup resistor
I D	Open-drain input pin requiring a pullup resistor
I/O D	Input/Open-drain output pin requiring a pullup resistor
I/O	Bi-directional input/output pin

The signal description also includes the type of buffer used for a particular signal:

GTL+	Open-drain GTL+ interface signal
PCI	PCI bus interface signals
AGP	AGP bus interface signals
CMOS	The CMOS signals are 1.5 V, 2.5 V, or 3.3 V, depending on their functional group.

3.1.2 Memory Signal Description

Table 3 provides descriptions of the memory interface signals.

Table 3. Memory Signal Descriptions

Name	Type	Voltage	Description
MECC[7:0]	I/O CMOS	V_3	**Memory ECC Data:** These signals carry Memory ECC data during access to DRAM. ECC is implemented but not tested on the Pentium III Processor – Low-Power Module. ECC is not supported on the Low-Power Modules.
CSA[5:0]#	O CMOS	V_3	**Chip Select (SDRAM):** These pins activate the SDRAMs. SDRAM accepts any command when its CS# pin is active low.
DQMA[7:0]	O CMOS	V_3	**Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during a read cycle and as a byte mask during a write cycle.
MAB[9:0]# MAB[10] MAB[12:11]# MAB[13]	O CMOS	V_3	**Memory Address (SDRAM):** This is the row and column address for DRAM. The 82443BX Host Bridge/Controller has two identical sets of address lines (MAA and MAB#). The Low-Power Module supports only the MAB set of address lines. For additional addressing features, please refer to the *Intel 440BX AGPSet: 82443BX Host Bridge/Controller Datasheet (Order number: 290633).*
MWEA#	O CMOS	V_3	**Memory Write Enable (SDRAM):** MWEA# should be used as the write enable for the memory data bus.
SRASA#	O CMOS	V_3	**SDRAM Row Address Strobe (SDRAM):** When active low, this signal latches Row Address on the positive edge of the clock. This signal also allows Row access and pre-charge.
SCASA#	O CMOS	V_3	**SDRAM Column Address Strobe (SDRAM):** When active low, this signal latches Column Address on the positive edge of the clock and also allows Column access.
CKE[5:0]	O CMOS	V_3	**SDRAM Clock Enable (SDRAM):** SDRAM clock enable pin. When these signals are deasserted, SDRAM enters the power-down mode. Each row is individually controlled by its own clock enable.
MD[63:0]	O CMOS	V_3	**Memory Data:** These signals are connected to the DRAM data bus. They are not terminated on the Low-Power Module.

3.1.3 AGP Signals

Table 4 provides descriptions of the AGP interface signals.

Table 4. AGP Signal Descriptions (Sheet 1 of 2)

Name	Type	Voltage	Description
GAD[31:0]	I/O AGP	V_3	**AGP Address/Data**: These signals are the standard AGP address and data lines. This bus functions in the same way as the PCI AD[31:0] bus. The address is driven with FRAME# assertion, and data is driven or received in following clocks.
GC/BE[3:0]#	I/O AGP	V_3	**AGP Command/Byte Enable:** This bus carries the command information during AGP cycles when PIPE# is used. During an AGP write, this bus contains byte enable information. The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on the subsequent clocks.
GFRAME#	I/O AGP	V_3	**AGP Frame:** This signal is not used during AGP transactions. GFRAME# remains deasserted by an internal pullup resistor. Assertion of this signal indicates the address phase of a PCI transfer and negation indicates that the cycle initiator desires one more data transfer.
GDEVSEL#	I/O AGP	V_3	**AGP Device Select**: This signal provides the same function as PCI DEVSEL#. GDEVSEL# is not used during AGP transactions. The 82443BX Host Bridge/Controller drives this signal when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
GIRDY#	I/O AGP	V_3	**AGP Initiator Ready**: This signal indicates that the AGP compliant target is ready to provide all write data for the current transaction. The signal is asserted when the initiator is ready for a data transfer.
GTRDY#	I/O AGP	V_3	**AGP Target Ready**: This signal indicates that the AGP compliant master is ready to provide all write data for the current transaction. The signal is asserted when the target is ready for a data transfer.
GSTOP#	I/O AGP	V_3	**AGP Stop:** This signal has the same function as PCI STOP#. This signal is not used during AGP transactions. Asserted by the target to request the master to stop the current transaction.
GREQ#	I AGP	V_3	**AGP Request:** AGP master requests for AGP.
GGNT#	O AGP	V_3	**AGP Grant:** The same function as on PCI. Additional information is provided on the ST[2:0] bus. For example: PCI Grant: Permission is given to the master to use PCI.
GPAR	I/O AGP	V_3	**AGP Parity**: A single parity bit is provided over GAD[31:0] and GC/BE[3:0]. This signal is not used during AGP transactions.
PIPE#	I AGP	V_3	**Pipelined Request:** The current master asserts this signal to indicate that a full width address will be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted.
SBA[7:0]	I AGP	V_3	**Sideband Address**: This bus provides an additional conduit to pass address and commands to the 82443BX Host Bridge/Controller from the AGP master.
RBF#	I AGP	V_3	**Read Buffer Full**: This signal indicates when the master is ready to accept previously requested, low-priority read data.

Table 4. AGP Signal Descriptions (Sheet 2 of 2)

Name	Type	Voltage	Description
ST[2:0]	O AGP	V_3	**Status Bus:** This bus provides information from the arbiter to an AGP Master on what it may do. These bits only have meaning when GGNT is asserted.
ADSTB[B:A]	I/O AGP	V_3	**AD Bus Strobes**: These signals provide timing for double-clocked data on the GAD bus. The agent providing data drives these signals. These signals are identical copies of each other.
SBSTB	I AGP	V_3	**Sideband Strobe**: This signal provides timing for a sideband bus. The SBA[7:0] (AGP master) drives the sideband strobe.

3.1.4 PCI Signals

Table 5 provides descriptions of the PCI signals.

Table 5. PCI Signal Descriptions (Sheet 1 of 2)

Name	Type	Voltage	Description
AD[31:0]	I/O PCI	V_3	**Address/Data:** These are the standard PCI address and data lines. The address is driven with FRAME# assertion, and data is driven or received in the following clocks.
C/BE[3:0]	I/O PCI	V_3	**Command/Byte Enable:** The command is driven with FRAME# assertion, and byte enables corresponding to supplied or requested data are driven on the following clocks.
FRAME#	I/O PCI	V_3	**Frame:** Assertion of this signal indicates the address phase of a PCI transfer. Negation of this signal indicates that the cycle initiator desires one more data transfer.
DEVSEL#	I/O PCI	V_3	**Device Select:** The 82443BX Host Bridge/Controller drives this signal when a PCI initiator is attempting to access DRAM. DEVSEL# is asserted at medium decode time.
IRDY#	I/O PCI	V_3	**Initiator Ready:** This signal is asserted when the initiator is ready for a data transfer.
TRDY#	I/O PCI	V_3	**Target Ready:** This signal is asserted when the target is ready for a data transfer.
STOP#	I/O PCI	V_3	**Stop:** This signal is asserted by the target to request the master to stop the current transaction.
PLOCK#	I/O PCI	V_3	**Lock:** This signal indicates an exclusive bus operation and may require multiple transactions to complete. When LOCK# is asserted, nonexclusive transactions may proceed. The 82443BX supports lock for CPU initiated cycles only. PCI initiated locked cycles are not supported.
REQ[4:0]#	I PCI	V_3	**PCI Request:** PCI master requests the PCI bus.
GNT[4:0]#	O PCI	V_3	**PCI Grant:** Permission is given to the master to use the PCI.

Table 5. PCI Signal Descriptions (Sheet 2 of 2)

Name	Type	Voltage	Description
PHOLD#	I PCI	V_3	**PCI Hold:** This signal comes from the expansion bridge and is the bridge request for the PCI. The 82443BX Host Bridge/Controller drains the DRAM write buffers, drains the processor-to-PCI posting buffers, and acquires the host bus before granting the request via PHLDA#. This ensures that GAT timing is met for ISA masters. The PHOLD# protocol has been modified to include support for passive release.
PHLDA#	O PCI	V_3	**PCI Hold Acknowledge:** This signal is driven by the 82443BX Host Bridge/Controller to grant PCI to the expansion bridge. The PHLDA# protocol has been modified to include support for passive release.
PAR	I/O PCI	V_3	**Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0]#.
SERR#	I/O PCI	V_3	**System Error:** The 82443BX asserts this signal to indicate an error condition. For further information, refer to the *Intel 440BX AGPSet: 82443BX Host Bridge/Controller* datasheet *(Order Number: 290633)*.
CLKRUN#	I/O D PCI	V_3	**Clock Run:** This is an open-drain output and input. The 82443BX Host Bridge/Controller requests the central resource, PIIX4E, to start or maintain the PCI clock by asserting CLKRUN#. The 82443BX Host Bridge/Controller three-states CLKRUN# upon deassertion of Reset (since CLK is running upon deassertion of Reset).
PCI_RST#	I CMOS	V_3	**Reset:** When asserted, this signal asynchronously resets the 82443BX Host Bridge/Controller. The PCI signals also three-state, compliant with *PCI Revision 2.1 Specifications*.

3.1.5 Processor and PIIX4E Sideband Signals

Table 6 provides descriptions of the processor and PIIX4E sideband signals.

Table 6. Processor and PIIX4E Sideband Signal Descriptions (Sheet 1 of 2)

Name	Type	Voltage	Description
FERR#	O D CMOS	V_CPUPU	**Numeric Coprocessor Error:** This pin functions as an FERR# signal supporting coprocessor errors. This signal is tied to the coprocessor error signal on the processor and is pulled active low by the processor to the PIIX4E.
IGNNE#	I D CMOS	V_CPUPU	**Ignore Error:** This open-drain signal is connected to the Ignore Error pin on the processor and is driven by the PIIX4E.
INIT#	I D CMOS	V_CPUPU	**Initialization:** INIT# is asserted by the PIIX4E to the processor for system initialization. This signal is an open-drain.
INTR	I D CMOS	V_CPUPU	**Processor Interrupt:** INTR is driven by the PIIX4E to signal the processor that an interrupt request is pending and needs to be serviced. This signal is an open-drain.
NMI	I D CMOS	V_CPUPU	**Non-Maskable Interrupt:** NMI is used to force a non-maskable interrupt to the processor. The PIIX4E ISA bridge generates an NMI when either SERR# or IOCHK# is asserted, depending on how the NMI Status and Control Register is programmed. This signal is an open-drain.

NOTE: See Table 9 for V_CPUPU definition.

Table 6. Processor and PIIX4E Sideband Signal Descriptions (Sheet 2 of 2)

Name	Type	Voltage	Description
A20M#	I D CMOS	V_CPUPU	**Address Bit 20 Mask:** When enabled, this open-drain signal causes the processor to emulate the address wraparound at 1 Mbyte, which occurs on the Intel® 8086 processor.
SMI#	I D CMOS	V_CPUPU	**System Management Interrupt:** SMI# is an active-low synchronous output from the PIIX4E that is asserted in response to one of many enabled hardware or software events. The SMI# open-drain signal can be an asynchronous input to the processor. However, in this chipset, SMI# is synchronous to PCLK.
STPCLK#	I D CMOS	V_CPUPU	**Stop Clock:** STPCLK# is an active-low, synchronous open-drain output from the PIIX4E that is asserted in response to one of many hardware or software events. STPCLK# connects directly to the processor and is synchronous to PCICLK. When the processor samples STPCLK# asserted, it responds by entering a low-power state (Quick Start). The processor exits this mode only when this signal is deasserted.

NOTE: See Table 9 for V_CPUPU definition.

3.1.6 Power Management Signals

Table 7 provides descriptions of the power management signals. The SM_CLK and SM_DATA signals refer to the two-wire serial SMBus interface. Although this interface is currently used solely for the digital thermal sensor, the SMBus contains reserved serial addresses for future use.

Table 7. Power Management Signal Descriptions

Name	Type	Voltage	Description
SUS_STAT1#	I CMOS	V_3ALWAYS†	**Suspend Status:** This signal connects to the SUS_STAT1# output of PIIX4E. SUS_STAT1# provides information on host clock status and is asserted during all suspend states.
VR_ON	I CMOS	V_3	**VR_ON:** Voltage regulator ON. This 3.3-V (5.0-V tolerant) signal controls the operation of the voltage regulator. VR_ON should be generated as a function of the PIIX4E SUSB# signal, which is used for controlling the “Suspend State B” voltage planes. This signal should be driven by a digital signal with a rise/fall time of less than or equal to 1 µs. ($V_{IL, min}$ =0.4 V, $V_{IH, min}$ =3.0 V.)
VR_PWRGD	O	V_3	**VR_PWRGD:** This signal is driven high by the Low-Power Module to indicate that the voltage regulator is stable. The signal is pulled low using a 100-KΩ resistor when inactive. It can be used in some combination to generate the system PWRGOOD signal.
BXPWROK	I CMOS	V_3	**Power OK to BX:** This signal must go active at least 1 ms after the V_3 power rail is stable and 1 ms prior to deassertion of PCIRST#.
SM_CLK	I/O D CMOS	V_3	**Serial Clock:** This clock signal is used on the SMBus interface to the digital thermal sensor.
SM_DATA	I/O D CMOS	V_3	**Serial Data:** Open-drain data signal on the SMBus interface to the digital thermal sensor.
ATF_INT#	O D CMOS	V_3	**ATF Interrupt:** This signal is an open-drain output signal of the digital thermal sensor.

† V_3ALWAYS is a 3.3-V supply and is generated whenever V_DC is available and supplied to the PIIX4E resume well.

3.1.7 Clock Signals

Table 8 provides descriptions of the clock signals.

Table 8. Clock Signal Descriptions

Name	Type	Voltage	Description
PCLK	I PCI	V_3	**PCI Clock In:** PCLK, an input to the Low-Power Module, is one of the system's PCI clocks. This clock is used by all of the 82443BX Host Bridge/Controller logic in the PCI clock domain. This clock is stopped when the PIIX4E PCI_STP# signal is asserted and/or during all suspend states.
HCLK0	I CMOS	V_CLK	**Host Clock In:** This clock is an input to the Low-Power Module from the CK100-M/CK100-SM clock source. The processor and the 82443BX Host Bridge/Controller use HCLK0. This clock is stopped when the PIIX4E CPU_STP# signal is asserted and/or during all suspend states.
HCLK1	I CMOS	V_CLK	**Host Clock In:** This clock is an input to the Low-Power Module from the CK100-M/CK100-SM clock source. This signal is not implemented on the Low-Power Modules.
DCLK0	O CMOS	V_3	**SDRAM Clock Out:** A 100-MHz SDRAM clock reference generated internally by the 82443BX Host Bridge/Controller onboard PLL. It feeds an external buffer that produces multiple copies for the SO-DIMMs.
DCLKRD	I CMOS	V_3	**SDRAM Read Clock:** A feedback reference from the SDRAM clock buffer. The 82443BX Host Bridge/Controller uses this clock when reading data from the SDRAM array. **This signal is not implemented on the Low-Power Modules.**
DCLKWR	I CMOS	V_3	**SDRAM Write Clock:** A feedback reference from the SDRAM clock buffer. The 82443BX Host Bridge/Controller uses this clock when writing data to the SDRAM array.
GCLKIN	I CMOS	V_3	**AGP Clock In:** The GCLKIN input is a feedback reference from the GCLKO signal.
GCLKO	O CMOS	V_3	**AGP Clock Out:** This signal is generated by the 82443BX Host Bridge/Controller onboard PLL from the HCLK0 host clock reference. The frequency of GCLKO is 66 MHz. The GCLKO output is used to feed both the PLL reference input pins on the 82443BX Host Bridge/Controller and the AGP device. The board layout must maintain complete symmetry on loading and trace geometry to minimize AGP clock skew.
FQS	O CMOS	V_3S	**Frequency Select:** This output indicates the desired host clock frequency for the Low-Power Module.

3.1.8 Voltage Signals

Table 9 provides descriptions of the voltage signals.

Table 9. Voltage Descriptions

Name	Type	Number of pins	Description
V_DC	I	20	DC Input: 5.0 V. See note below.
V_3S	I	9	**SUSB# Controlled 3.3 V:** A power managed 3.3-V supply, and an output of the voltage regulator on the system electronics. This rail is off during STR, STD, and Soff. [1]
V_5	I	3	**SUSC# Controlled 5.0 V:** A power managed 5.0-V supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.[1,2]
V_3	I	16	**SUSC# Controlled 3.3 V:** A power managed 3.3-V supply. An output of the voltage regulator on the system electronics. This rail is off during STD and Soff.[1]
VCCAGP	I	4	**AGP I/O Voltage**: This voltage rail is not implemented on the Low-Power Module and is defined for upgrade purposes only. Intel recommends that this voltage rail be connected to V_3 on the system electronics.
V_CPUPU	O	1	**Processor I/O Ring:** The Low-Power Module drives this signal to power the processor interface signals, such as the PIIX4E open-drain pullups for the processor and PIIX4E sideband signals. V_CPUPU is tied to 1.5 V.
V_CLK	O	1	**Processor Clock Rail:** The Low-Power Module drives V_CLK to power the CK100-M VDDCPU rail.

NOTES:
1. Refer to the *82371AB PCI-to-ISA/IDE Xcelerator (PIIX4)* datasheet (Order Number 290562) for additional information on suspend modes.
2. If you are connecting V_DC and V_5 in the system electronics, see “V_DC and V_5 Decoupling” on page 38.

3.1.9 ITP and JTAG Pins

Table 10 provides descriptions of the ITP and JTAG signals, which the system manufacturer can use to implement a JTAG chain and an ITP port if desired.

Table 10. ITP and JTAG Pin Descriptions

Name	Type	Voltage	Description
TDO	O D	V_CPUPU	**JTAG Test Data Out:** A serial output port. TAP instructions and data are shifted out of the processor from this port.
TDI	I	V_{TT}	**JTAG Test Data In:** A serial input port. TAP instructions and data are shifted into the processor from this port.
TMS	I	V_{TT}	**JTAG Test Mode Select:** Controls the TAP controller change sequence.
TCLK	I	V_{TT}	**JTAG Test Clock:** A testability clock for clocking the JTAG boundary scan sequence.
TRST#	I	V_{TT}	**JTAG Test Reset:** TRST# asynchronously resets the TAP controller in the processor.
FS_PREQ#	I	V_{TT}	**Debug Mode Request:** This signal is driven by the ITP and makes a request to enter the debug mode.
FS_PRDY#	O	V_{TT}	**Debug Mode Ready:** FS_PRDY# is driven by the processor and informs the ITP that the processor is in the debug mode.
FS_RESET#	O	V_{TT}	**Processor Reset:** The processor reset status to the ITP.
V_{TT}	O	V_{TT}	**GTL+ Termination Voltage:** Used by the POWERON pin on the ITP debug port to determine when target system is on. POWERON is pulled up using a 1-KΩ resistor to V_{TT}. Other ITP signals may use this power rail for pullup.

NOTE: FS_RESET# and FS_PRDY# are pulled up to V_{TT} inside the mobile Pentium® III processor core.

3.1.10 Miscellaneous Pins

Table 11 provides descriptions of the miscellaneous signal pins.

Table 11. Miscellaneous Pin Descriptions

Name	Type	Number	Description
Module ID[3:0]	O CMOS	4	**Module Revision ID**: These pins track the revision level of the Low-Power Module. A 100-KΩ pullup resistor to V_3S must be placed on the system electronics for these signals. See “Labeling Information” on page 55 for more detail.
Ground	I	45	Ground
Reserved	RSVD	33	Unallocated Reserved pins. All Reserved pins must not be connected.

3.2 Connector Pin Assignments

Table 12 lists the signals for each pin of the connector to the system electronics. Refer to “Pin and Pad Assignments” on page 22 for the pin assignments.

Table 12. Connector Pin Assignment – Rows A-E (Sheet 1 of 2)

Pin Number	Row A	Row B	Row C	Row D	Row E
1	SBA5	ADSTBB	GND	GAD31	SBA7
2	GAD25	GAD24	SBA6	SBA4	SBA0
3	GAD30	GAD29	GAD26	GAD27	GND
4	GND	VCCAGP	GAD4	GAD6	GDA8
5	RBF#	GAD1	GAD3	GAD5	GC/BE0#
6	BXPWROK	RESERVED	GAD2	ADSTBA	GND
7	MD0	MD1	V_3	CLKRUN#	GAD7
8	MD2	MD33	GND	MD32	MD34
9	MD36	MD4	MD3	MD35	MD34
10	MD7	MD38	MD37	MD6	MD5
11	MD41	MD42	MD40	MD39	MD8
12	MD43	MD11	GND	MD10	MD9
13	MD14	MD45	MD44	MD13	MD12
14	MECC4	MECC0	ND15	ND47	ND46
15	SCASA#	MWEA#	MECC5	RESERVED	GND
16	GND	MID1	DQMA0	DQMA1	RESERVED
17	V_3	DQMA4	MID0	DQMA5	CSA#
18	CSA1#	CSA2#	CSA4#	CSA3#	GND
19	SRASA#	CSA5#	MAB0#	MAB1#	RESERVED
20	RESERVED	RESERVED	MAB2#	RESERVED	MAB3#
21	RESERVED	MAB4#	GND	RESERVED	MAB6#
22	RESERVED	RESERVED	MAB5#	RESERVED	MAB7#
23	MAB8#	RESERVED	RESERVED	MSB9#	MAB10
24	RESERVED	MAB11#	MAB12#	RESERVED	DCLK0
25	MAB13	V_3	GND	CKE0	DCLKRD
26	CKE1	MID2	CKE3	CE4	GND
27	CKE5	CKE2	MID3	RESERVED#	RESERVED#
28	RESERVED	RESERVED#	DQMA2	DCLKWR	GND
29	GND	V_{TT}	RESERVED	FS_PREQ#	DQMA3
30	FS_RESET#	V_3	MD26	GND	MD25
31	FS_PRDY#	GND	MD58	MD57	MD60
32	RESERVED#	SMCLK	TDO	TCLK	FERR#
33	RESERVED	SMDAT	TDI	TMS	IGNNE#

Table 12. Connector Pin Assignment – Rows A-E (Sheet 2 of 2)

Pin Number	Row A	Row B	Row C	Row D	Row E
34	RESERVED	FQS	RESERVED	TRST#	ATF_INT#
35	RESERVED	V_5	V_3S	V_3S	V_3S
36	V_CPUPU	V_5	V_3S	V_3S	V_3S
37	V_CLK	V_5	V_3S	V_3S	V_3S
38	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
39	V_DC	V_DC	V_DC	V_DC	V_DC
40	V_DC	V_DC	V_DC	V_DC	V_DC

Table 13. Connector Pin Assignment – Rows F-K (Sheet 1 of 2)

Pin Number	Row F	Row G	Row H	Row J	Row K
1	GREQ#	GND	PIP#	SBA3	GND
2	ST0	ST1	SBA1	SBSTB	GCLKI
3	GGNT#	ST2	SBA2	GND	CGLK0
4	GAD13	GSTOP#	GAD16	GAD20	GAD23
5	GAD12	GPAR	GAD18	GAD17	GC/BE3#
6	GAD10	GAD15	GFRAME#	GND	GAD22
7	GAD11	GC/BE1#	GTRDY#	GC/BE2#	GAD21
8	GAD9	GAD14	GDEVESEL#	GIRDY#	GAD19
9	GND	VCCAGP	GND	VCCAGP	GAD28
10	AD0	AD4	AD2	AD3	AD1
11	GND	C/BE0#	AD6	GND	AD5
12	VCCAGP	AD10	AD7	AD8	AD9
13	MECC1	AD13	GND	AD12	AD11
14	SERR#	PAR	AD15	C/BE1#	AD14
15	AD16	TRDY#	STOP#	DEVSEL#	PLOCK#
16	AD19	GND	AD17	GND	AD18
17	AD23	AD30	AD24	C/BE2#	AD21
18	AD27	AD22	C/BE3#	AD26	PCLK
19	PCI_RST#	GND	AD20	AD28	GND
20	RESERVED	PHOLD#	AD31	AD29	AD25
21	IRDY#	FRAME#	GND	REQ1#	REQ0#
22	GND	GNT2#	REQ2#	REQ3#	GNT3#
23	GNT1#	GNT4#	GNT0#	REQ4#	GND
24	GND	PHLDA#	GND	V_3	MD59
25	DQMA6	MECC7	MD50	MD51	MD54
26	MECC2	MD48	MD18	MD52	MD24

Table 13. Connector Pin Assignment – Rows F-K (Sheet 2 of 2)

27	DQMA7	MD16	MD19	GND	MD23
28	MECC6	MD17	MD21	MD53	MD55
29	MECC3	MD49	MD20	MD22	MD56
30	MD27	MD28	GND	MD62	MD63
31	GND	MD29	MD61	MD30	MD31
32	DMI#	INTR	VR_ON	GND	GND
33	NMI	SUS_STAT1#	VR_PWRGD	GND	HCLK0
34	A20M#	STPCLK#	INIT#	GND	GND
35	V_3	V_3	V_3	GND	HCLK1
36	V_3	V_3	V_3	GND	GND
37	V_3	V_3	V_3	V_3	V_3
38	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
39	V_DC	V_DC	V_DC	V_DC	V_DC
40	V_DC	V_DC	V_DC	V_DC	V_DC

3.3 Pin and Pad Assignments

The 400-pin connector has a 1.27-mm pitch and a BGA-style surface mount. Refer to "Height Restrictions" on page 50 for size information. Figure 2 shows the 400-pin connector pad assignments.

Figure 2. 400-Pin Connector Pad Footprint

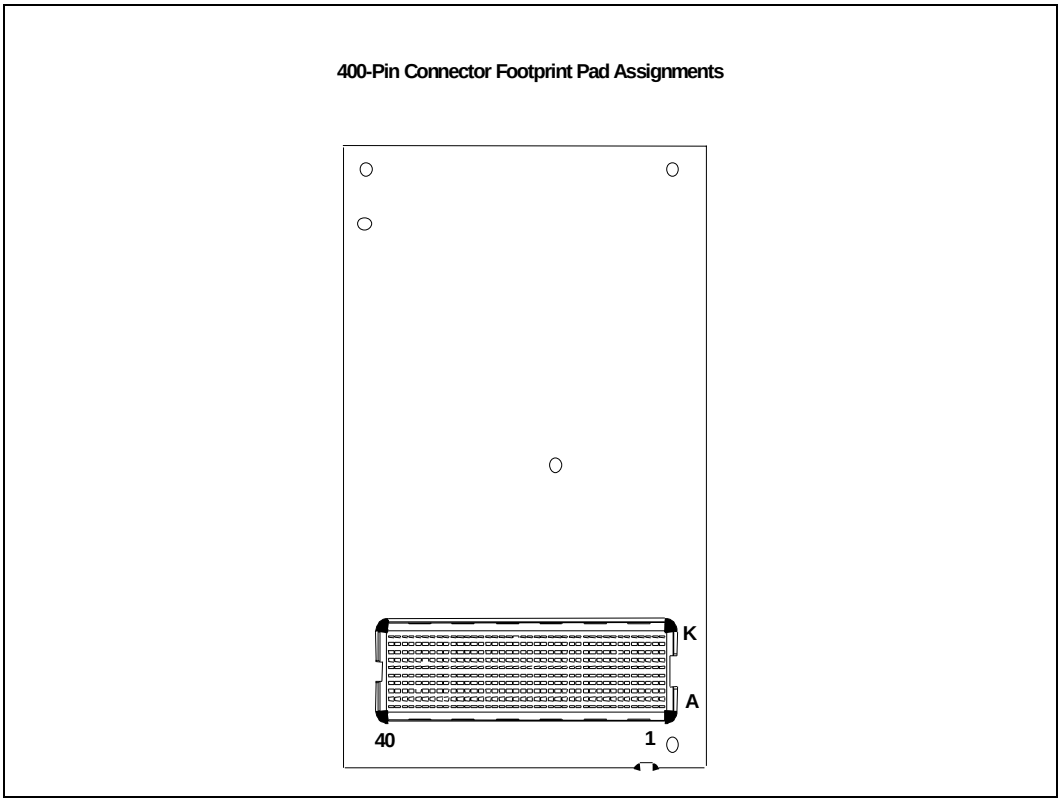


Table 14 summarizes some of the key connector specifications.

Table 14. Connector Specifications

Parameter	Condition	Specification
Material	Contact	Copper Alloy
	Housing	Thermo-Plastic Molded Compound: LCP
Electrical	Current	0.5 A
	Voltage	50 VAC
	Insulation Resistance	100 mΩ
	Termination Resistance	20-mΩ maximum at 20-mV open circuit with 10 mA
	Capacitance	5 pF maximum per contact
Mechanical	Mating Cycles	50 Cycles
	Connector Mating Force	50 lbs (22.7 kg) maximum
	Contact Unmating Force	30 lbs (13.6 kg) maximum

4.0 Functional Description

4.1 Pentium® III Processor Low-Power Module

The Pentium III Processor Low-Power Module runs at 500 MHz with a 100-MHz processor system bus (PSB).

4.2 L2 Cache

The on-die L2 cache is 256 Kbyte, eight-way set associative, and runs at the speed of the processor core.

4.3 The 82443BX Host Bridge/Controller

Intel's 82443BX Host Bridge/Controller is a highly integrated device that combines the bus controller, the DRAM controller, and the PCI bus controller into one component. The 82443BX Host Bridge/Controller has multiple power management features designed for applied computing systems such as:

- CLKRUN#, a feature that enables controlling of the PCI clock on or off
- The 82443BX Host Bridge/Controller suspend modes, which include Suspend-To-RAM (STR), Suspend-To-Disk (STD), and Power-On-Suspend (POS)
- System Management RAM (SMRAM) power management modes, which include Compatible SMRAM (C_SMRAM) and Extended SMRAM (E_SMRAM). C_SMRAM is the traditional SMRAM feature implemented in all Intel PCI chipsets. E_SMRAM is a new feature that supports write-back cacheable SMRAM space up to 1 Mbyte. To minimize power consumption while the system is idle, the internal 82443BX Host Bridge/Controller clock is turned off (gated off) when there is no processor and PCI activity. This is accomplished by setting the G_CLK enable bit in the 82443BX power management register through the system BIOS.

4.3.1 Memory Organization

The memory interface of the 82443BX Host Bridge/Controller is available at the connector. This allows for the following:

- One set of memory control signals, sufficient to support up to three SO-DIMM sockets and six banks of SDRAM at 100 MHz
- One CKE signal for each bank

Memory features *not* supported by the 82443BX Host Bridge/Controller in this product are:

- Eight banks of memory
- 256-Mbit memory devices
- Second set of memory address lines (MAA[13:0])
- Extended Data Out (EDO) DRAM
- 66-MHz memory bus

The clocking architecture supports the use of SDRAM. Due to the tight timing requirements of the 100-MHz SDRAM clocks, the clocking mode for SDRAM memory configurations allows all host and SDRAM clocks to be generated from the same clocking architecture on the system electronics. For complete details about memory device support, organization, size, and addressing when using SDRAM memory and trace length guidelines, refer to the *Low-Power Module SDRAM DIMM Routing Guidelines* (order number 273317).

4.3.2 Reset Strap Options

Several strap options on the memory address bus define the behavior of the Low-Power Module after reset. Other straps are allowed to override the default settings. Table 15 shows the various straps and their implementation.

Table 15. Configuration Straps for the 82443BX Host Bridge/Controller

Signal	Function	Module Default Setting	Optional Override on System Electronics
MAB[12]#	Host Frequency Select	Strapped high on the module for 100 MHz	None
MAB[11]#	In Order Queue Depth	No strap, maximum queue depth is set at 8	None
MAB[10]#	Quick Start Select	Strapped high on the module for Quick Start mode	None
MAB[9]#	AGP Disable	No strap (AGP is enabled)	Strap high to disable AGP
MAB[7]#	MM Configuration	No strap (Standard mode)	None
MAB[6]#	Host Bus Buffer Mode Select	Strapped high on the module for mobile PSB buffers	None

4.3.3 PCI Interface

The PCI interface of the 82443BX Host Bridge/Controller is available at the connector. The 82443BX Host Bridge/Controller supports the PCI Clockrun protocol for PCI bus power management. In this protocol, PCI devices assert the CLKRUN# open-drain signal when they require the use of the PCI interface.

The 82443BX Host Bridge/Controller is responsible for arbitrating the PCI bus. The 82443BX Host Bridge/Controller can support up to five PCI bus masters. There are five PCI Request/Grant pairs (REQ[4:0]# and GNT[4:0]#) available on the connector to the system electronics.

The PCI interface on the connector is 3.3 V only. PCI devices that are 5.0 V are not supported.

The 82443BX Host Bridge/Controller is compliant with the *PCI 2.1 Specification*, which improves the worst case PCI bus access latency from earlier PCI specifications. The 82443BX Host Bridge/Controller supports only Mechanism #1 for accessing PCI configuration space. This implies that signals AD[31:11] are available for PCI IDSEL signals. However, since the 82443BX Host Bridge/Controller is always device #0, AD11 is never asserted during PCI configuration cycles as an IDSEL. The 82443BX reserves AD12 for the AGPbus. AD13 is the first available address line usable as an IDSEL. Intel recommends that AD18 be used by the PIIX4E.

4.3.4 AGP Interface

The 82443BX Host Bridge/Controller is compliant with the *AGP Interface Specification Revision 1.0*, which supports an asynchronous AGP interface coupling to the 82443BX core frequency. The AGP interface can achieve real data throughput in excess of 500 Mbytes per second using an AGP 2X graphics device. Actual bandwidth may vary depending on specific hardware and software implementations.

4.4 Power Management

4.4.1 Clock Control Architecture

The Low-Power Module's clock control architecture is optimal for applied computing designs. The clock control architecture consists of seven different clock states: Normal, Stop Grant, Auto Halt, Quick Start, HALT/Grant Snoop, Sleep, and Deep Sleep. The Auto Halt state provides a low-power clock state that can be controlled through the software execution of the HLT instruction. The Quick Start state provides a very low-power, low-exit latency clock state that can be used for hardware controlled "idle" states. The Deep Sleep state provides an extremely low-power state that can be used for Power-On-Suspend states, which is an alternative to shutting off the processor's power. The exit latency of the Deep Sleep state has been reduced to 30 µs. The Stop Grant and Sleep states are not available on the Low-Power Module as these states are intended for desktop or server systems. The Stop Grant state and the Quick Start clock state are mutually exclusive. For example, a strapping option on signal A15# chooses which state is entered when the STPCLK# signal is asserted. Strapping the A15# signal to ground at Reset enables the Quick Start state. Otherwise, asserting the STPCLK# signal puts the processor into the Stop Grant state.

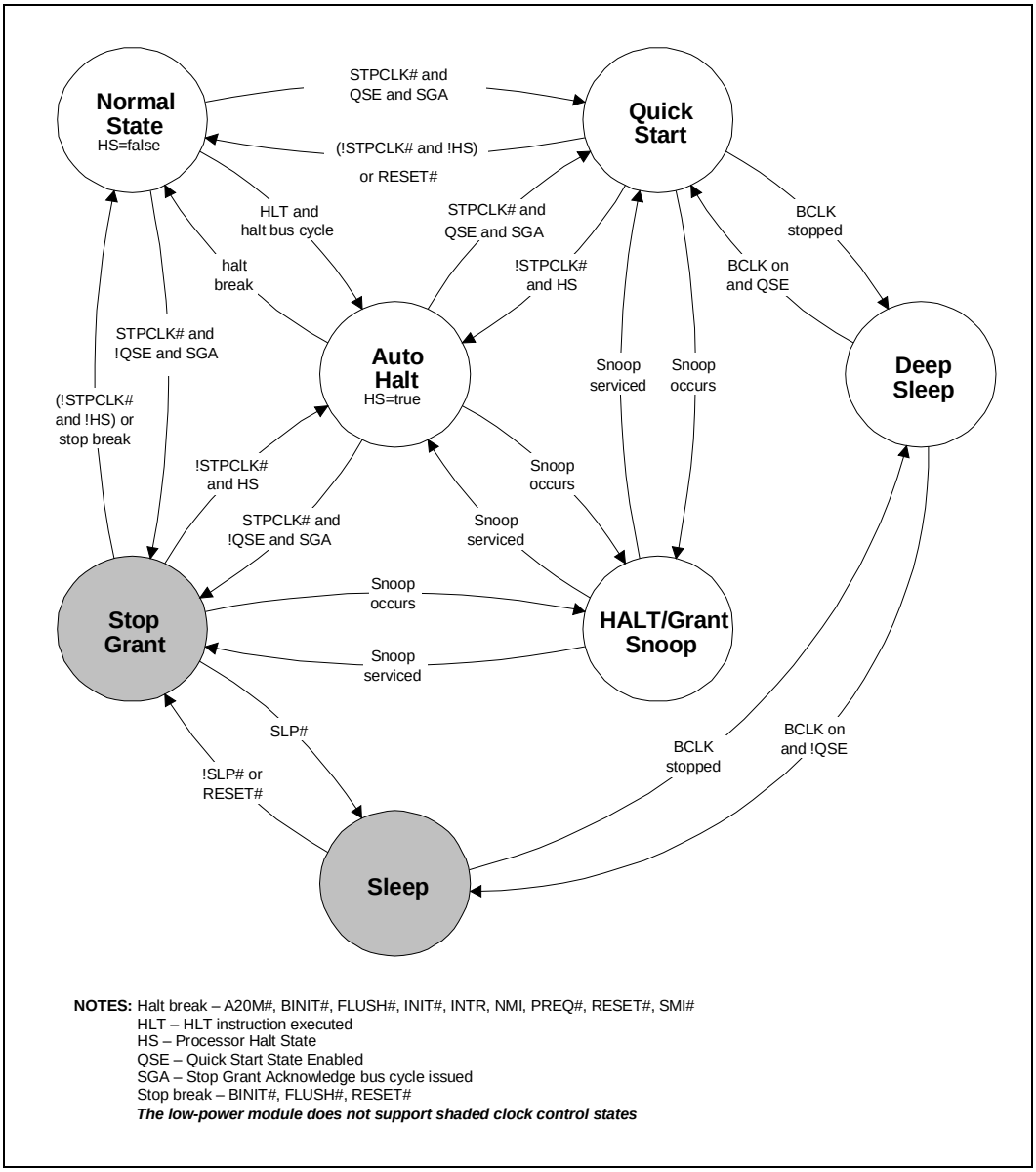
Table 16 provides information on the clock control states and Figure 3 illustrates the clock control architecture. Performing state transitions not shown in Figure 3 is neither recommended nor supported.

Table 16. Clock State Characteristics

Clock State	Exit Latency	Processor Power	Snooping	System Uses
Normal		Varies	Yes	Normal program execution
Auto Halt	Approximately 10 bus clocks	1.2 W	Yes	Software controlled entry-idle mode
Stop Grant†	10 bus clocks	1.2 W	Yes	Hardware controlled entry/exit mobile throttling
Quick Start	Through Snoop, to HALT/Grant Snoop state: immediate Through STPCLK#, to Normal state: 10 bus clocks	500 mW	Yes	Hardware controlled entry/exit mobile throttling
HALT/Grant Snoop	A few bus clocks after the end of snoop activity	Not specified	Yes	Supports snooping in the low-power states
Sleep†	To Stop Grant state 10 bus clocks	500 mW	No	Hardware controlled entry/exit mobile throttling
Deep Sleep	30 µs	150 mW	No	Hardware controlled entry/exit mobile throttling

† Intel Low-Power Modules do not support this clock control state.

Figure 3. Clock Control States



NOTES: Halt break – A20M#, BINIT#, FLUSH#, INIT#, INTR, NMI, PREQ#, RESET#, SMI#
HLT – HLT instruction executed
HS – Processor Halt State
QSE – Quick Start State Enabled
SGA – Stop Grant Acknowledge bus cycle issued
Stop break – BINIT#, FLUSH#, RESET#
The low-power module does not support shaded clock control states

4.4.1.1 Normal State

The Normal state is the normal operating mode where the processor's core clock is running, and the processor is actively executing instructions.

4.4.1.2 Auto Halt State

This is a low-power mode entered by the processor through the execution of the HLT instruction. The power level of this mode is similar to the Stop Grant state. A transition to the Normal state is made by a halt break event (one of the following signals going active: NMI, INTR, BINIT#, INIT#, RESET#, FLUSH#, or SMI#).

Asserting the STPCLK# signal while in the Auto Halt state causes the processor to transition to the Stop Grant state or the Quick Start state, where a Stop Grant Acknowledge bus cycle is issued. Deasserting STPCLK# causes the processor to return to the Auto Halt state without issuing a new Halt bus cycle.

The SMI# (System Management Interrupt) is recognized in the Auto Halt state. The return from the SMI handler can be to either the Normal state or the Auto Halt state. See the *Intel® Architecture Software Developer's Manual, Volume III: System Programming Guide* (order number 243192) for more information. No Halt bus cycle is issued when returning to the Auto Halt state from the System Management mode (SMM).

The FLUSH# signal is serviced in the Auto Halt state. After flushing the on-chip caches, the processor returns to the Auto Halt state without issuing a Halt bus cycle. Transitions in the A20M# and PREQ# signals are recognized while in the Auto Halt state.

4.4.1.3 Stop Grant State

The Low-Power Module does not support the Stop Grant state.

In desktop systems, the processor enters Stop Grant mode with the assertion of the STPCLK# signal when it is configured for the Stop Grant state (via the A15# strapping option). The processor still can respond to snoop requests and latch interrupts. Latched interrupts are serviced when the processor returns to the Normal state. Only one occurrence of each interrupt event is latched. A transition back to the Normal state can be made by the deassertion of the STPCLK# signal or the occurrence of a stop break event (a BINIT#, FLUSH#, or RESET# assertion).

The processor returns to the Stop Grant state after the completion of a BINIT# bus initialization unless STPCLK# has been deasserted. RESET# assertion causes the processor to immediately initialize itself. However, the processor stays in the Stop Grant state after initialization until STPCLK# is deasserted. If the FLUSH# signal is asserted, the processor flushes the on-chip caches and returns to the Stop Grant state. A transition to the Sleep state can be made by the assertion of the SLP# signal.

While in the Stop Grant state, assertions of SMI#, INIT#, INTR, and NMI (or LINT[1:0]) are latched by the processor. These latched events are not serviced until the processor returns to the Normal state. Only one of each event is recognized upon return to the Normal state.

4.4.1.4 Quick Start State

The processor enters this mode with the assertion of the STPCLK# signal when the processor is configured for the Quick Start state (via the A15# strapping option). In the Quick Start state, the processor is only capable of acting on snoop transactions generated by the PSB priority device. Because of its snooping behavior, Quick Start can only be used in single processor configurations.

A transition to the Deep Sleep state can be made by stopping the clock input to the processor. A transition back to the Normal state (from the Quick Start state) is made only if the STPCLK# signal is deasserted.

While in this state, the processor is limited in its ability to respond to input. It is incapable of latching any interrupts, servicing snoop transactions from symmetric bus masters, or responding to FLUSH# and BINIT# assertions. In the Quick Start state, the processor does not respond properly to any input signal other than STPCLK#, RESET#, or BPRI#. If any other input signal changes, then the behavior of the processor will be unpredictable. No serial interrupt messages may begin or be in progress while the processor is in the Quick Start state.

RESET# assertion causes the processor to immediately initialize itself, but the processor stays in the Quick Start state after initialization until STPCLK# is deasserted.

4.4.1.5 HALT/Grant Snoop State1234

The processor responds to snoop transactions on the PSB while in the Auto Halt, Stop Grant, or Quick Start state. When a snoop transaction is presented on the system bus, the processor enters the HALT/Grant Snoop state. The processor remains in this state until the snoop has been serviced and the PSB is quiet. After the snoop has been serviced, the processor returns to its previous state. If the HALT/Grant Snoop state is entered from the Quick Start state, then the input signal restrictions of the Quick Start state still apply in the HALT/Grant Snoop state (except for those signal transitions that are required to perform the snoop).

4.4.1.6 Sleep State

The Low-Power Module does not support the Sleep state.

In desktop systems, the Sleep state is a very low-power state in which the processor maintains its context and the phase locked loop (PLL) maintains phase lock. The Sleep state can only be entered from the Stop Grant state. After entering the Stop Grant state, the SLP# signal can be asserted, causing the processor to enter the Sleep state. The SLP# signal is not recognized in the Normal state or the Auto Halt state.

The processor can be reset by the RESET# signal while in the Sleep state. If RESET# is driven active while the processor is in the Sleep state, then SLP# and STPCLK# must immediately be driven inactive to ensure that the processor correctly initializes itself.

Input signals (other than RESET#) may not change while the processor is in or is transitioning into or out of the Sleep state. Input signal changes at these times cause unpredictable behavior. Thus, the processor is incapable of snooping or latching any events in the Sleep state.

While in the Sleep state the processor can enter its lowest power state, the Deep Sleep state. Removing the processor's input clock puts the processor in the Deep Sleep state. PICCLK may be removed in the Sleep state.

4.4.1.7 Deep Sleep State

The Deep Sleep state is the lowest power mode that the processor can enter while maintaining its context. The processor enters the Deep Sleep state by stopping the BCLK input to the processor while the processor is in the Sleep state or the Quick Start state. For proper operation, the BCLK input should be stopped in the low state.

The processor returns to the Sleep state or the Quick Start state from the Deep Sleep state when the BCLK input is restarted. Due to the PLL lock latency, there is a 30-µs delay after the clocks have started before this state transition happens. PICCLK may be removed in the Deep Sleep state. PICCLK should be designed to turn on when BCLK turns on while transitioning out of the Deep Sleep state.

The input signal restrictions for the Deep Sleep state are the same as for the Sleep state, except that RESET# assertion results in unpredictable behavior.

5.0 Electrical Specifications

The following section provides the electrical requirements for the Pentium III Processor – Low-Power Module.

5.1 DC Requirements

Table 17 provides the DC power supply design criteria.

Table 17. DC Requirements

Symbol	Parameter	Min	Nom	Max	Unit	Notes
V_DC Signal Parameters						
V_{DC}	DC Input Voltage	4.75	5.0	5.25	V	
I_{DC}	DC Input Current	0.1	3.0	3.8	A	
I_{DC_RMS}	RMS Ripple Current			7.5	A	
I_{DC_Surge}	Maximum Surge Current for V_DC			20.0	A	1
V_5 Signal Parameters						
V_5	Power Managed 5.0-V Supply	4.75	5.0	5.25	V	
I_5	Power Managed 5.0-V Current, Operating	20.0	50.0	100.0	mA	
I_{5_Surge}	Maximum Surge Current for V_5			1.5	A	1
V_3 Signal Parameters						
V_3	Power Managed 3.3-V Supply	3.135	3.3	3.465	V	
I_3	Power Managed 3.3-V Current	0.8	1.2	3.0	A	
I_{3_Surge}	Maximum Surge Current for V_3			4.0	A	
V_CPUPU Signal Parameters						
V_{CPUPU}	Processor I/O Ring Voltage	1.375	1.5	1.625	V	
I_{CPUPU}	Processor I/O Ring Current	0.0	10.0	20.0	mA	
V_CLK Signal Parameters						
V_{CLK}	Processor Clock Rail Voltage	2.375	2.5	2.625	V	
I_{CLK}	Processor Clock Rail Current	24.0	35.0	80.0	mA	2

NOTES:
1. A 20-µS duration.
2. These values are system dependent.

5.2 AC Requirements

Table 18 shows the BCLK AC requirements.

Table 18. AC Specifications at the Processor Core Pins

T#[1]	Parameter[2,3]	Min	Nom	Max	Unit	Note
	System Bus Frequency		100		MHz	Note
	BCLK Period		10		ns	Note 4
	BCLK Period Stability			±250	ps	Notes 5, 6, 7
T3	BCLK High Time	2.85			ns	At > 1.7 V, Note
T4	BCLK Low Time	2.55			ns	At < 0.7 V, Note
T5	BCLK Rise Time	0.175		0.875	ns	Note 7 0.9 V ~ 1.6 V
T6	BCLK Fall Time	0.175		0.875	ns	Note 7 1.6 V ~ 0.9 V

NOTES:
1. Figure 4 on page 32 illustrates these intervals.
2. All AC timings for the GTL+ signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All GTL+ signal timings (address bus, data bus, etc.) are referenced at 1.00 V at the processor core pins.
3. All AC timings for the CMOS signals are referenced to the BCLK rising edge at 1.25 V at the processor core pin. All CMOS signal timings (compatibility signals, etc.) are referenced at 1.25 V at the processor core pins.
4. The internal core clock frequency is derived from the PSB clock. The PSB clock to core clock ratio is determined during initialization and is predetermined by the Low-Power Module. The BCLK period allows a +0.5-ns tolerance for clock driver variation.
5. Measured on the rising edge of adjacent BCLKs at 1.25 V. The jitter present must be accounted for as a component of BCLK skew between devices.
6. The clock driver's closed loop jitter bandwidth must be set low to allow any PLL-based device to track the jitter created by the clock driver. The -20 dB attenuation point, as measured into a 10-pF to a 2-pF load, should be less than 500 kHz. This specification may be ensured by design characterization and/or measured with a spectrum analyzer. See the *CK97 Clock Synthesizer Design Guidelines* for further details.
7. Not 100% tested. Specified by design characterization as a clock driver requirement.

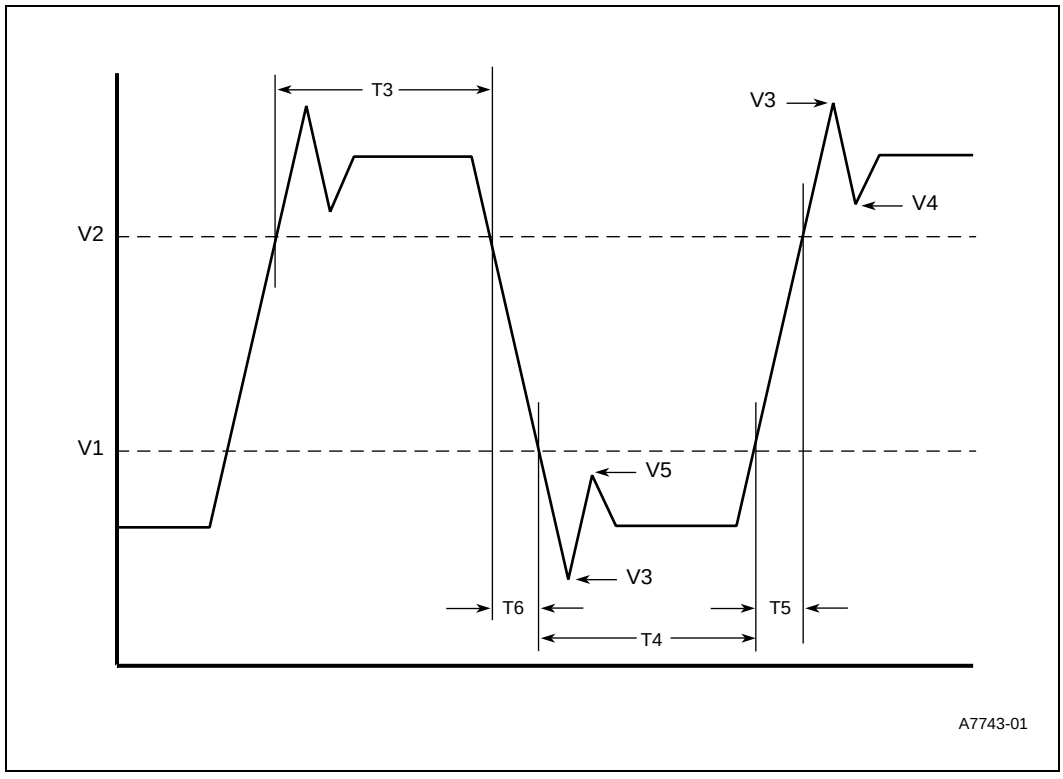
Table 19 describes the signal quality specifications at the processor core for the PSB clock (BCLK) signal. Figure 4 describes the signal quality waveforms for the PSB clock at the processor core pins.

Table 19. BCLK Signal Quality Specifications at the Processor Core

V#	Parameter	Min	Max	Unit	Notes
V1	V_{IL_BCLK}		0.7	V	Note 1
V2	V_{IH_BCLK}	1.7		V	Note 1
V3	V_{IN} Absolute Voltage Range	-0.7	3.5	V	Undershoot, Overshoot, Note 2
V4	Rising Edge Ringback	1.7		V	Absolute Value, Note 4
V5	Falling Edge Ringback		0.7	V	Absolute Value, Note 4
	BCLK rising/falling slew rate	0.8	4.0	V/ns	Note 4

NOTES:
1. On the rising edge of BCLK, there must be a minimum overshoot to 2.0 V. The clock must rise monotonically between V_{IL_BCLK} and 2.0 V and fall monotonically between V_{IH_BCLK} and V_{IL_BCLK}.
2. BCLK must rise/fall monotonically between V_{IL_BCLK} and V_{IH_BCLK}.
3. All specifications in this table apply only when BCLK is running. BCLK may not be above $V_{IH\_BCLK,max}$ or below $V_{IL\_BCLK,MIN}$ for more than 50% of the clock cycle.
4. The rising and falling edge ringback voltage specified is the minimum (rising) or maximum (falling) absolute voltage that the BCLK signal can dip back to after passing the V_{IH_BCLK} (rising) or V_{IL_BCLK} (falling) voltage limits.

Figure 4. BCLK Waveform at the Processor Core Pins



5.3 Processor Core Voltage Regulation

The DC voltage regulator (DC/DC converter) is designed to support the core voltage and I/O ring voltage for current and future Intel mobile processors. The DC voltage regulator provides the appropriate mobile Pentium III processor core voltage, the GTL+ bus termination voltage, the processor sideband signal pull-up voltage, and the clock driver buffer voltage. Of these voltages, only the processor sideband pullup voltage (V_CPUPU) and the clock driver buffer voltage (V_CLK) are delivered to the system electronics.

The Low-Power Module supports input DC voltage of 5.0 V from the system battery or power supply.

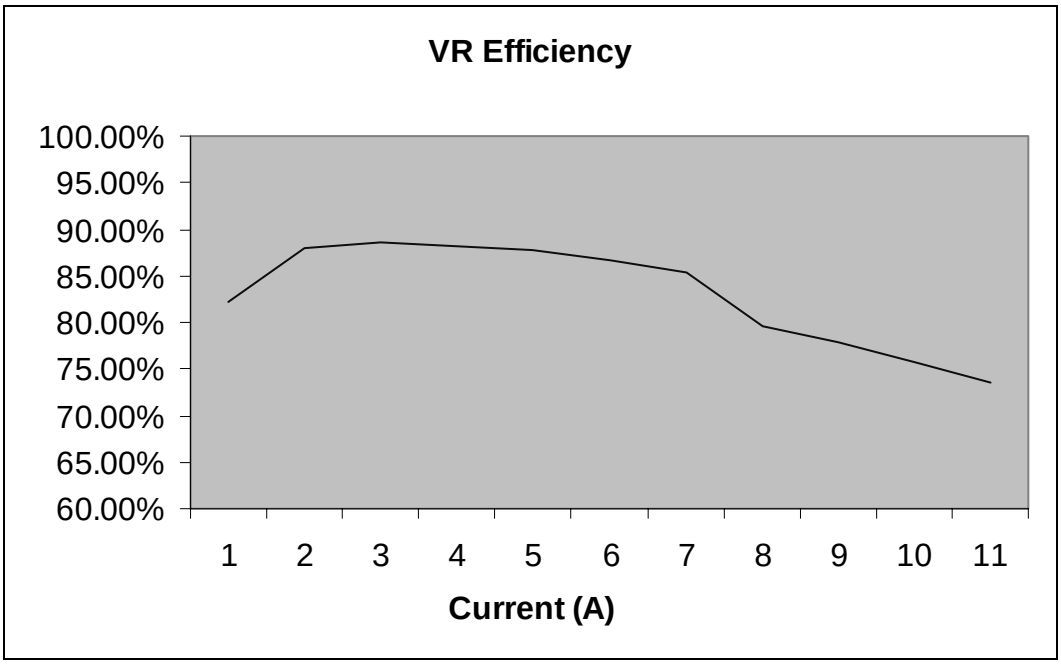
5.3.1 Voltage Regulator Efficiency

There are three voltage regulators (VR) on the Low-Power Module. These voltage regulators generate the processor core voltage and the processor I/O ring voltage. The core voltage regulator provides the required current from the V_DC supply, and its relative efficiencies are shown in Table 20 and Figure 5. The V_CLK and V_{TT} voltage regulators tap the V_3 plane.

Table 20. V_CORE Power Conversion Efficiency

V_CORE = 1.6 V	
I_{CORE} (A)	Efficiency at V_DC = 5.0 V
1	82.15%
2	88.04%
3	88.55%
4	88.14%
5	87.67%
6	86.59%
7	85.47%
8	79.67%
9	77.87%
10	75.71%
11	73.55%

Figure 5. V_CORE Efficiency Chart



5.3.2 Voltage Regulator Control

The VR_ON pin on the 400-pin connector allows a 3.3-V signal to control the voltage regulator. The system manufacturer can use this signal to turn the voltage regulator on or off. VR_ON should be controlled as a function of the same signal (SUSB#) used to control the system's switched 5.0-V and 3.3-V power planes. The PIIX4E defines Suspend B as the Power Management state in which power is physically removed from the processor and the voltage regulator. In this state, the SUSB# pin on the PIIX4E controls these power planes. The Low-Power Module provides the VR_PWRGD signal, which indicates that the voltage regulator power is operating at a stable voltage level. The system manufacturer should use this signal on the system electronics to control power inputs and to gate PWROK to the PIIX4E South Bridge. Table 21 provides the detailed definitions and sequences of the voltage signals.

Table 21. Voltage Signal Definitions (Sheet 1 of 2)

Signal	Source	Definitions
V_DC	System Electronics	V_DC is required to be 5.0 V DC and is driven by the system electronics' power supply. V_DC powers the Low-Power Module DC-to-DC converter for the processor core and I/O voltages. The Low-Power Module cannot be inserted or removed while V_DC is powered on.
V_5	System Electronics	V_5 is supplied by the system electronics for the voltage regulator.
V_3	System Electronics	V_3 is supplied by the system electronics for the 82443BX and powers the Low-Power Module's linear regulators for generating the V_CLK and V_CPUPU voltage rails. It stays on during suspend.
V_3S	System Electronics	V_3S is supplied by the system electronics and is shut off during suspend.

Table 21. Voltage Signal Definitions (Sheet 2 of 2)

Signal	Source	Definitions
VR_ON	System Electronics	VR_ON is a 3.3-V signal that enables the voltage regulator circuit. When driven active high the voltage regulator circuit is activated. The signal driving VR_ON should be a digital signal with a rise/fall time of less than or equal to 1 µs. ($V_{IL, max}$ =0.4 V, $V_{IH, min}$ =3.0 V.)
V_CORE	Low-Power Module	A result of VR_ON being asserted, V_CORE is an output of the DC-DC regulator on the Low-Power Module and is driven to the core voltage of the processor.
VR_PWRGD	Low-Power Module	Upon sampling the voltage level of V_CORE (minus tolerances for ripple), VR_PWRGD is driven active high. When asserting VR_ON, VR_PWRGD is guaranteed to be stable after 6 ms. If VR_PWRGD is not sampled active within 1 second of the assertion of VR_ON, then the system electronics should deassert VR_ON. After V_CORE is stabilized, VR_PWRGD asserts to logic high. This signal must not be pulled up by the system electronics. VR_PWRGD should be “logically ANDed” with V_3S to generate the PIIX4E input signal, PWROK. The system electronics should monitor VR_PWRGD to verify that it is asserted high prior to the active high assertion of PIIX4E PWROK.
V_CPUPU	Low-Power Module	V_CPUPU is 1.5 V. The system electronics uses this voltage to power the PIIX4E-to-processor interface circuitry.
V_CLK	Low-Power Module	V_CLK is 2.5 V. The system electronics uses this voltage to power the HCLK[1:0] drivers for the processor clock.

The following list includes additional specifications and clarifications of the power sequence timing and Figure 6 provides an illustration.

- The VR_ON signal may only be asserted to a logical high by a digital signal *after* V_DC ≥ 4.75 V, V_5 ≥ 4.5 V, and V_3 ≥ 3.0 V.
- The Rise Time and Fall Time of VR_ON must be less than or equal to 1 µs.
- VR_ON has its V_{IL} (max) = +0.4 V and V_{IH} (min) = +3.0 V.
- The VR_PWRGD is asserted to logic high (3.3 V) after V_CORE is stabilized and V_DC reaches 5.0 V. This signal should not and cannot be pulled up by the system electronics.
- In the power-on process, Intel recommends raising the higher voltage power plane first (V_DC), followed by the lower power planes (V_5, V_3), and finally assert VR_ON after above voltage levels are met on all rails. The power-off process should be the reverse process; for example, VR_ON gets deasserted, followed by the lower power planes, and finally the higher power planes.
- VR_ON must monotonically rise through its V_{IL} to V_{IH} and fall through its V_{IH} to V_{IL} points. The sign or slope cannot change between V_{IL} and V_{IH} in rising and V_{IH} and V_{IL} in falling.
- VR_ON must provide an instantaneous in-rush current to the Low-Power Module with the following values as listed in Table 22.

Table 22. VR_ON In-Rush Current

	Instantaneous	DC Operating
Maximum	41.0 mA	0.1 µA
Typical	0.2 mA	0.0 µA

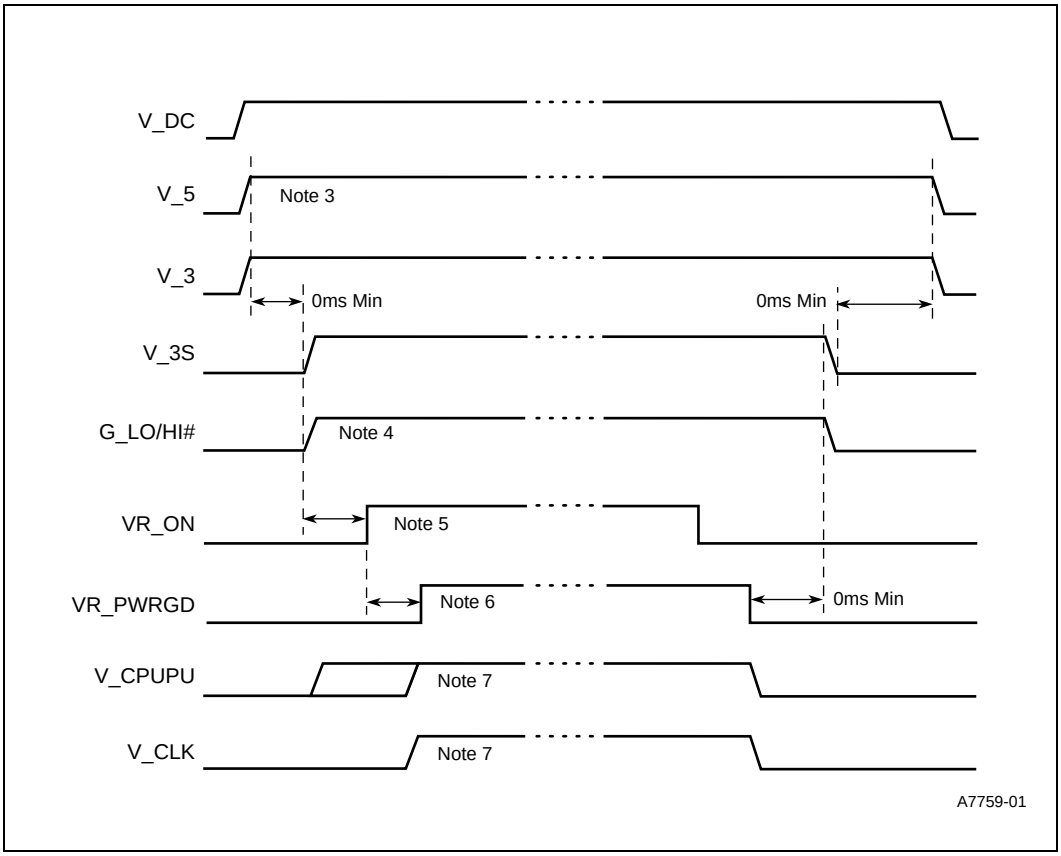
- VR_ON Valid-Low Time: This specifies how long VR_ON must be low for a valid off before VR_ON can be turned on again. In going from a valid on to off and then back on, the

following conditions must be met to prevent damage to the customer system or the Low-Power Module:

— VR_ON must be low for 1 ms

— The original voltage level requirements for turn-on must be met before assertion of VR_ON (i.e., V_DC ≥ 4.75 V, V_5 ≥ 4.5 V, and V_3 ≥ 3.0 V).

Figure 6. Power Sequence Timing



NOTES:
1. PWROK on the I/O board should be active on when VR_PWRGD is active and V_3S is good.
2. CPU_RST from the I/O board should be active for a minimum of 6 ms after PWROK is active and PLL_STP# and CPU_STP# are inactive. Note that PLL_STP# is an AND condition of RSMRST# and SUSB# on the PIIX4E.
3. This is the 5-V power supplied to the Low Power Module. This should be the first 5.0-V plane to power up. Stays on during suspend.
4. G_LO/HI# must be high at the rising edge of VR_ON. If it is not, the BIOS must assert this signal very early in core execution.
5. V_DC ≥ 4.75 V , V_5 ≥ 4.5 V, V_3S ≥ 3.0 V.
6. When asserting VR_ON, VR_PWRGD is guaranteed to be stable after 6 ms.
7. V_CPUPU and V_CLK are generated on the module.

5.3.3 Power Planes: Bulk Capacitance Requirements

The placement of sufficient bulk capacitance on the system electronics board is critical to the operation of the Pentium III Processor – Low-Power Module. Intel has provided the maximum possible bulk capacitance on the module. However, in order to achieve proper filtering and in-rush current protection, it is imperative that additional filtering be provided on the system electronics board. Table 23 details the bulk capacitance requirements for the system electronics.

Note: Observe the voltage rating requirement for the capacitors on each respective voltage rail.

Table 23. Capacitance Requirement per Power Plane

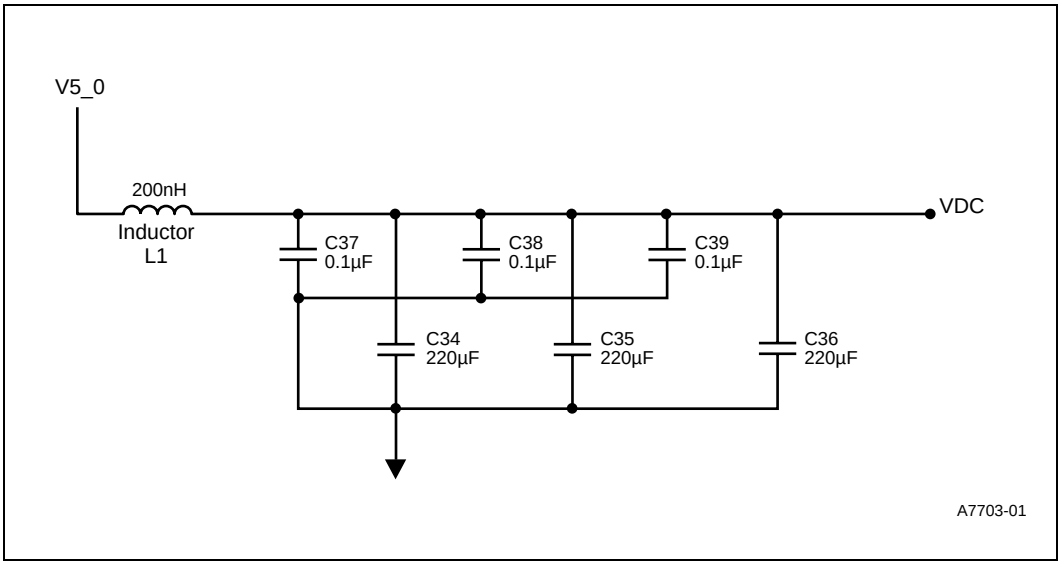
Power Plane	Bulk Capacitance Requirements			High Frequency Capacitance Requirements
	Total Capacitance[4]	ESR[3]	Ripple Current	
V_DC	100 µF	20 mΩ	3 A ~ 5 A	0.1 µF, 0.01 µF[1]
V_5	100 µF	100 mΩ	1 A	0.1 µF, 0.01 µF[1]
V_3	470 µF	100 mΩ	1 A	0.1 µF, 0.01 µF[1]
V_3S	100 µF	100 mΩ		0.1 µF, 0.01 µF[1]
VCC_AGP	22 µF	100 mΩ	1 A	0.1 µF, 0.01 µF[1]
V_CPUPU	2.2 µF			8200 pF[1]
V_CLK	10 µF			8200 pF[2]

NOTES:
1. These capacitances should be located near the connector.
2. V_CLK filtering should be located next to the system clock synthesizer.
3. In order to reduce ESR, Intel recommends the use of multiple bulk capacitors rather than a single large capacitor.
4. Intel strongly recommends that customers pay close attention to capacitor design considerations. Specifically, the “Capacitance vs. Temperature De-rating Curve,” “Capacitance vs. Applied DC Voltage De-rating Curve,” and the “Capacitance vs. Frequency De-rating Curve.” Some capacitor dielectrics are particularly susceptible to these conditions; for example Y5V ceramic capacitors.

5.3.3.1 V_DC and V_5 Decoupling

If V_DC and V_5 are tied together, ensure that decoupling guidelines are strictly followed to avoid noise from the V_DC rail coupling to the V_5 rail. Noise could trigger the undervoltage lockout circuits on the module. The example circuit shown in Figure 7 adheres to the decoupling guidelines.

Figure 7. V_DC to V_5 Decoupling Circuit Example



Exact component values are system dependant. Intel recommends that specific component values be determined through full simulation and parasitic modeling.

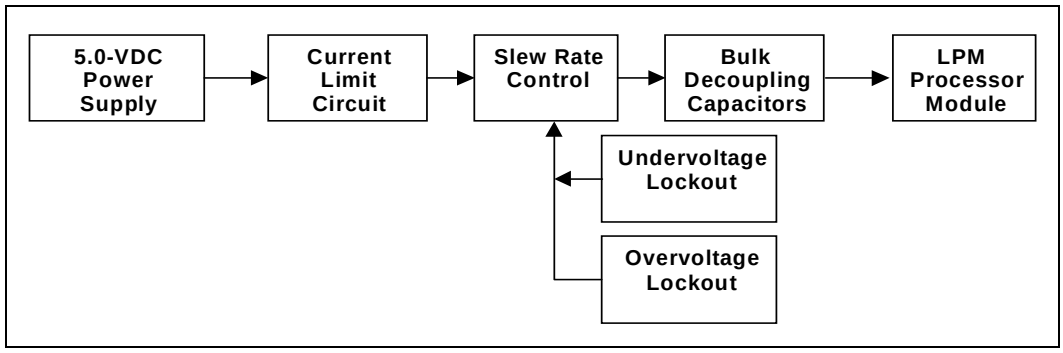
5.3.4 Surge Current Guidelines

5.3.4.1 DC Power System Protection

The recommended DC Power System Protection consists of six elements:

- A DC power supply that is capable of delivering 5.0 V, ± 5%, to the Low-Power Module
- An overcurrent protection circuit that provides a means to limit the maximum current available to the system
- A slew-rate control circuit that provides a controlled voltage slew rate at turn-on providing protection for components sensitive to fast voltage rise times
- An undervoltage lockout circuit that protects against potentially damaging high currents that can be encountered when the DC power supply voltage is too low
- An overvoltage lockout circuit that provides protection from potentially damaging high DC power supply voltages
- Bulk decoupling capacitors that provide filtering and a reservoir of energy that can provide a faster transient response than the power supply

Figure 8. V_DC Power System Protection Block Diagram



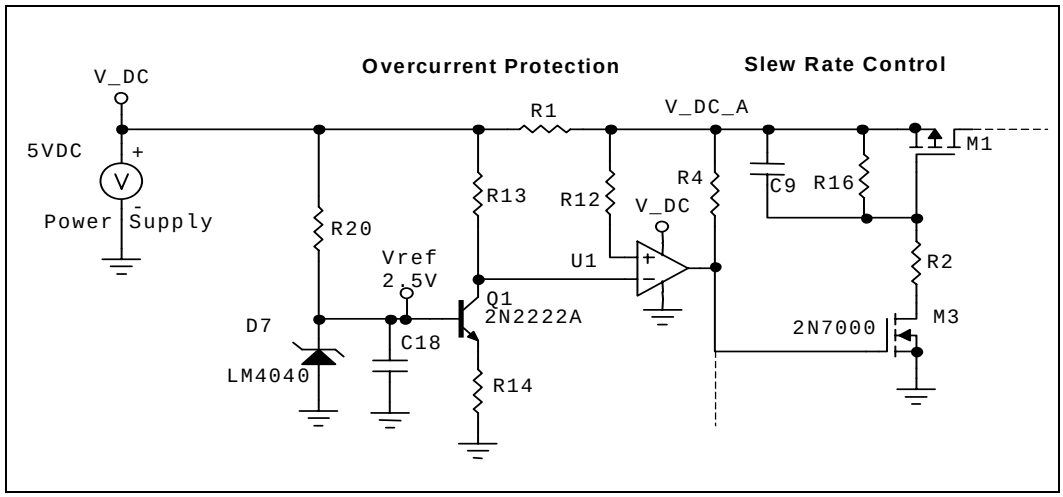
5.3.4.2 The 5.0-V DC Power Supply

The 5.0-V power supply must be able to deliver 5.0 V, ± 5% to the Low-Power Module, measured at the Low-Power Module.

5.3.4.3 Overcurrent Protection

The overcurrent protection circuit provides a way to limit current drawn by the module. Under normal operating conditions, I_DC should not be expected to exceed 3.8 A. To allow for component variations and margining issues, a reasonable I_DC current limit is 6 A. Figure 9 shows an example of an overcurrent protection circuit.

Figure 9. Overcurrent Protection Circuit Example



The following is provided as an example only. Customers should determine their specific requirements and calculate component values accordingly.

- Let I_DC(limit)= 6 A
- Let β(Q1)= 100
- Let R1= 5 mΩ = 0.005 Ω
- Let R12 = 100 Ω
- Let R13 = 100 Ω
- Let V(R14) ≈ 1.8 V
- Let I(R20) ≈ 100 µA

When power is initially applied to the circuit, C18 charges up to 2.5 V through R20. This slowly rising voltage is applied to the base of the current source, Q1. The voltage on R14 is approximately 2.5 V minus the base-emitter drop of about 0.7 V (at 25° C): $V_{(R14)} \approx 1.8$ V. Q1 is a 2N2222A with a moderate β of about 100. Therefore, the current through R13 is approximately equal to the current through R14.

The charging of C18 provides a small increment of delay since U1 does not allow R4 to pull up the gate of M3 until Q1 has pulled the non-inverting input of U1 down slightly.

The voltage developed across R1 is a function of the load.

Equation 1. $V(R1) = I\_DC \cdot R1$

If the maximum I_DC expected is 3 A, it may be reasonable to set the I_DC current limit at 6 A. If the current sense resistor, R1 is selected to be 5 mΩ (0.005 Ω), the maximum voltage developed across this resistor would be:

Equation 2. $I\_DC_{(limit)} \cdot R_{sense} = 6A \cdot 5E - 3 = 30$ mV

The offset voltage applied to the inverting input of the comparator, U1, should then be 30 mV. If R13 is selected to be 100 Ω, the current can then be calculated:

Equation 3. $I_{offset} = 30$ mV / 100 Ω = 3 00 µA

Note: For a successful design, the system designer should also take into consideration the input offset of the comparator. The general rule suggests that the design offset should be at least ten times greater than the device offsets.

The value of R14 can now be calculated:

Equation 4. R14 = 1.8V / 300 µA = 6 KΩ

(The nearest standard 1% value is 6.04 KΩ)

In reference to R20, the LM4040-2.5 has a very wide operating current range from 60 µA to 15 mA. In order to provide the current source base drive, the following is needed:

Equation 5. $I_{base} \approx I_c / \beta = 300$ µA / 100 = 3 µA

If 100 µA is selected for $I_{(R20)}$, this would be adequate for the reference and current source base drive. Since both of these currents must be satisfied at the low-power supply margin, a V_DC of 4.75 V is assumed.

Equation 6. R20 = (V_DC - V_{ref}) / $I_{(R20)}$ = (4.75 - 2.50) / 100 µA = 22.5 KΩ)

(To allow for component tolerances, 20 KΩ might be a good choice.)

5.3.4.4 Slew-rate Control

The slew-rate control regulates the rate that the power supply voltage is applied to the system:

- Let the threshold voltage of M1, V_t = -1.0 V
- Let M1 $V_{GS(sat)}$ = -2.4 V, also denoted as V_{sat}
- Let R16 = 100 KΩ
- Let t_delay = 500 µs
- Let C_{total} = The sum or the Bulk Caps. + the sum of the Module Caps. = 5 * 22 µF + 2 X 4.7 µF = 119.4 µF

M1 is a low RDS(on) p-channel MOSFET such as the Siliconix Si4435DY*. When the power supply voltage is applied and increased to a value that exceeds the Lockout value, (4.75 V is used in this example), the undervoltage lockout circuit allows R4 to pull up the gate of M3 to start a turn-on sequence. M3 pulls its drain toward ground, forcing current to flow through R2. M1 does not start to source any current until after t_delay, with t_delay defined as the following:

Equation 7. $t\_delay = -R2 \cdot C9 \cdot \ln [1 - V_t / (V\_DC - V_G)]$

Equation 8. $V_{GS} = [R16 / (R16 + R2)] \cdot V\_DC$

The published minimum threshold of the Si4435DY is a V_{GS} of -1.0V; i.e. C9 must charge to 1.0 V before M1 starts to turn on. The delay, t_delay, is the time required to charge C9 to 1.0 V.

Assuming a negligible voltage drop across M3, when M3 is ON, the voltage on the Gate of M1, V_G, with respect to ground, is the voltage developed across R2: $VG \equiv V_{(R2)}$. If a minimum steady-state bias on M1 is desired to be -4.5 V, this will be the voltage dropped across R16. At the low end of the V_DC margin, 4.75 V:

Equation 9. $V_G = V\_DC + V_{GS}$ = 4.75 V - 4.65 V = 0.1 V (with respect to ground)

Equation 10. $R2 = V_G \cdot R16 / (V\_DC - V_G)$, R2 = 5.556 KΩ

(The nearest standard 1% value is 5.62 KΩ. The example continues with R2 = 5.62 KΩ.)

Rearranging Equation 7 to solve for C9 yields:

Equation 11. $C9 = -t\_delay / [R2 \cdot \ln(1 - V_t / (V\_DC - V_G))]$

Now a value for C9 can be calculated.

Equation 12. C9 = 0.354 µF

(A close standard value of 0.33 µF yields a t_delay of 466 µs.)

The ramp-up time, t_ramp, is defined as:

Equation 13. $t\_ramp = -R2 \cdot C9 \cdot \ln(1 - V_{SAT}/V_{GS}) - t\_delay$

If M1 has a VGS(sat) of -2.4 V:

Equation 14. t_ramp = 948.8 µs

The maximum current during the power-up ramp is:

Equation 15. $I_{max} = C_{total}$ (d/dt v) ≈ C_{total} · V_DC/t_ramp

If the total Capacitance, Ctotal on the V_DC bus, is 119.4 µF, then see the equation below.

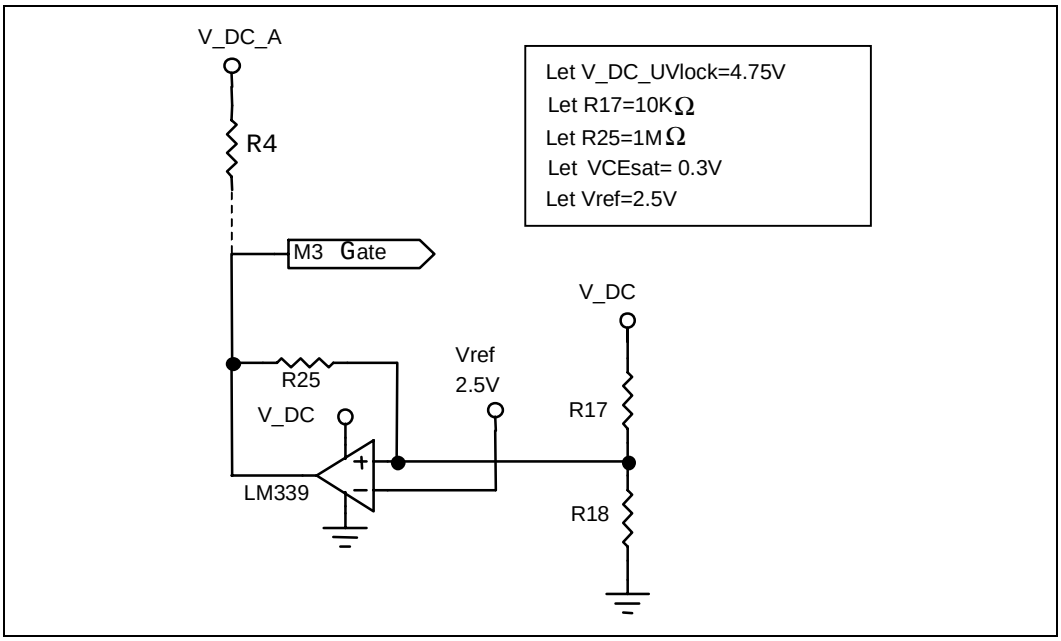
Equation 16. I_{max} = 598 µA

Summary: From the values assumed and calculated, t_delay = 466 µs, t_ramp = 949 µs, and I_{max} = 598 µA.

5.3.4.5 Undervoltage Lockout: Circuit Description, V_DC_UVlock(out)

The circuit in Figure 10 shows the undervoltage lockout portion of the V_DC Supply circuit. This circuit protects and locks out the applied voltage to the module to prevent an accidental turn-on at low V_DC supply voltages. A low voltage applied to the module could result in destructive current levels.

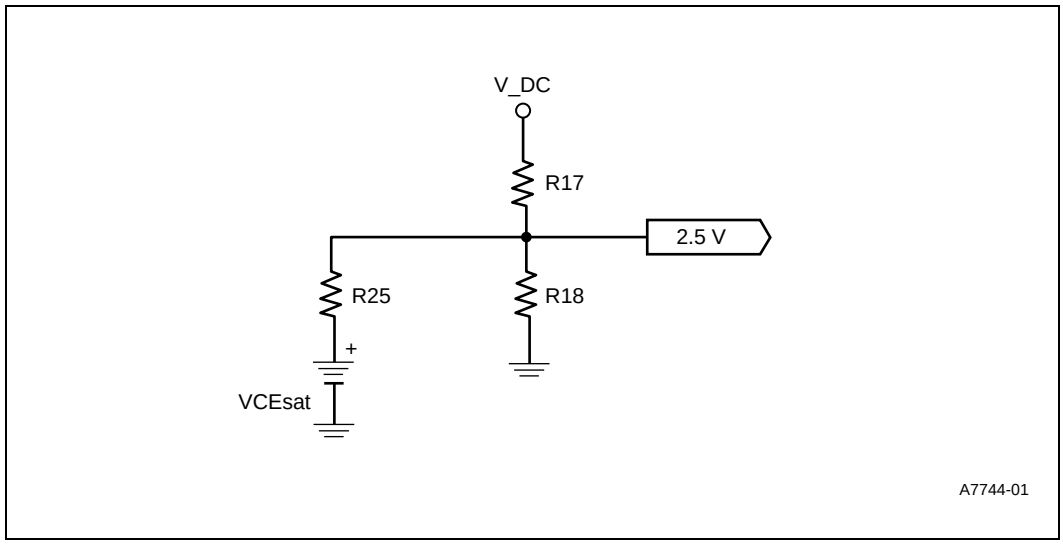
Figure 10. Undervoltage Lockout Circuit Example



The output of the LM339 comparator is an open-collector. It is low when the applied voltage at V_DC is less than 4.75 volts. This holds the gate of M3 low, which does not allow the slew-rate controller to turn-on. The 2.5-V reference, V_{ref}, voltage is derived from D7 in Figure 9. When non-inverting input of the comparator exceeds V_{ref}, 2.5 V, the comparator trips and allows its output to go to a High-Z state. The Gate of M3 can then be pulled up by R4 starting the controlled power-up slew.

The following model is used to calculate the undervoltage lockout trip point.

Figure 11. Undervoltage Lockout Model



VCEsat is the saturation voltage of the comparator output transistor.

The comparator trip-point voltage can be calculated with the following equation:

Equation 17. $V\_DC\_UVlock = V_{ref} + [V_{ref} / R18 + (V_{ref} - VCEsat) / R25] \cdot R17$

If power to the module is to be held off until V_DC exceeds 4.75 V, Equation 17 can be rearranged to solve for R18.

Equation 18. $R18 = V_{ref} \cdot R17 \cdot R25 / [R25 \cdot (V\_DC\_UVlock - V_{ref}) - (R17 \cdot (V_{ref} - VCEsat)]$

A value for R18 can be determined by plugging these values into Equation 18.

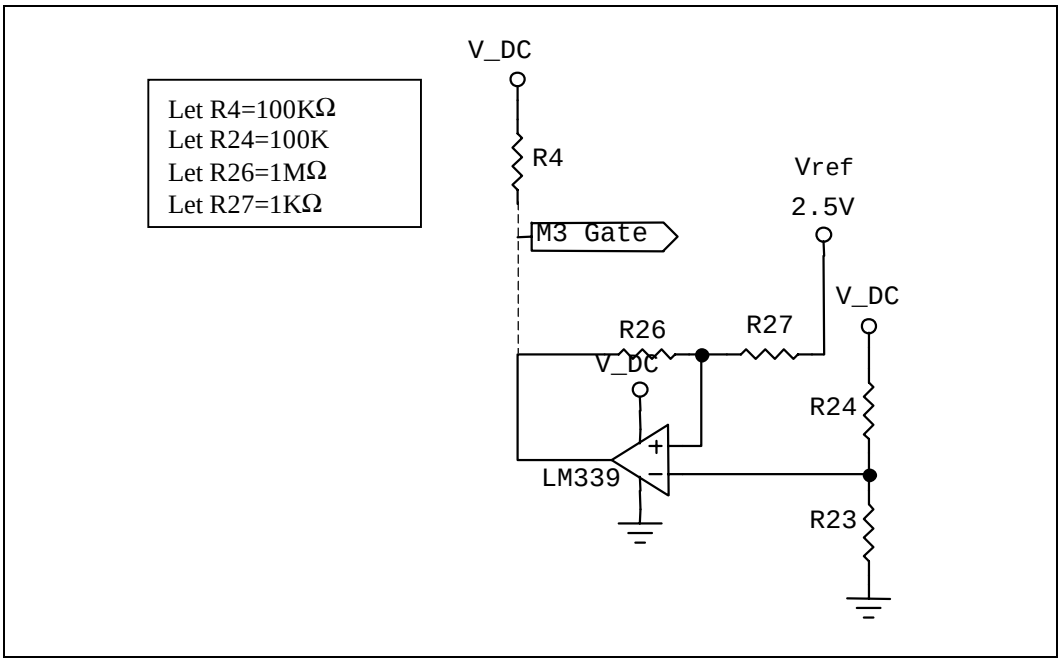
R18 = 11 KΩ

(11 KΩ is a standard 1% resistor value.)

5.3.4.6 Overvoltage Lockout: Circuit Description

The Low-Power Module operates with a maximum input voltage of 5.25 V. This circuit can be set to lock out the input voltage if it exceeds the desired input.

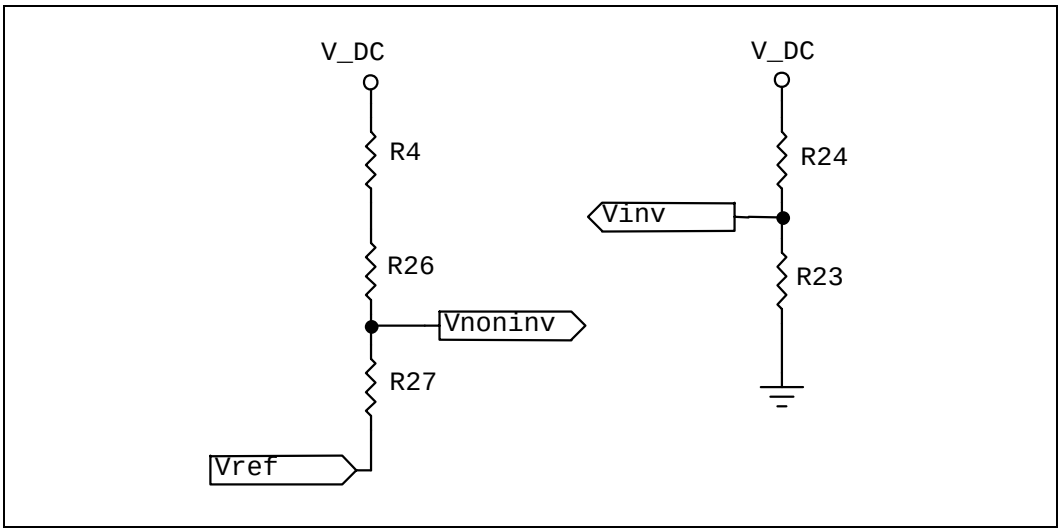
Figure 12. Overvoltage Lockout Circuit Example



The LM339 comparator is an open-collector output and is pulled low when the applied voltage at V_DC is too high, thus disabling the slew-rate circuit.

The model below is used for component calculations.

Figure 13. Overvoltage Lockout Model



Assume that the desired V_DC overvoltage lockout is 6.0 V. Using Equation 19, the input to the non-inverting input of the OV lockout comparator can be calculated.

The lockout trip voltage can be calculated with the following equations:

Equation 19. $V_{noninv} = V_{ref} + [R27 \cdot (V\_DC\_OVlock - V_{ref}) / (R4 + R26 + R27)]$

Equation 20. $V_{noninv} = 2.503\ V$

Equation 21. $V_{inv} = V\_DC\_OVlock \cdot R23 / (R23 + R24)$

The output of the 0 V lockout comparator becomes active and pulls down when the inverting input becomes greater than the 2.503 V input on the non-inverting input. Equation 21 can be rearranged to solve for R23.

Equation 22. $R23 = R24 \cdot V_{inv} / (V\_DC\_OVlock - V_{inv})$

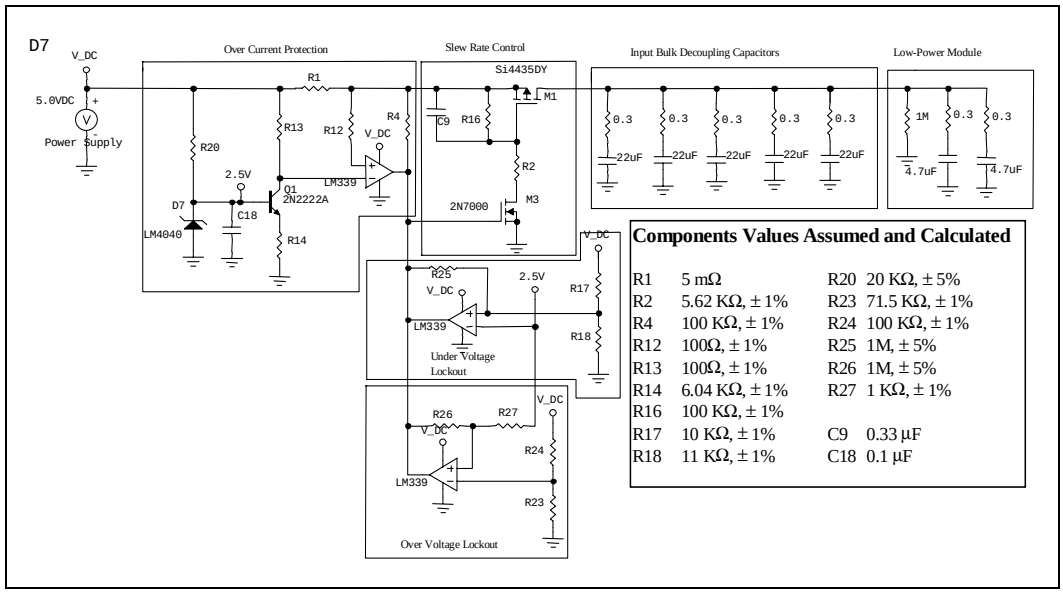
The OV lockout comparator trip point is defined by $V_{inv} = V_{noninv} = 2.503\ V$. Equation 22 provides a solution for R23.

Equation 23. $R23 = 71.576\ K\Omega$

(The nearest standard 1% value is 71.5 KΩ)

If V_DC exceeds 6.0 V, the voltage on the OV lockout comparator inverting input will exceed 2.503 V. This will cause the comparator to trip, pulling its output low and disabling the power skew control circuit which, in turn, will disconnect V_DC from the Low-Power Module.

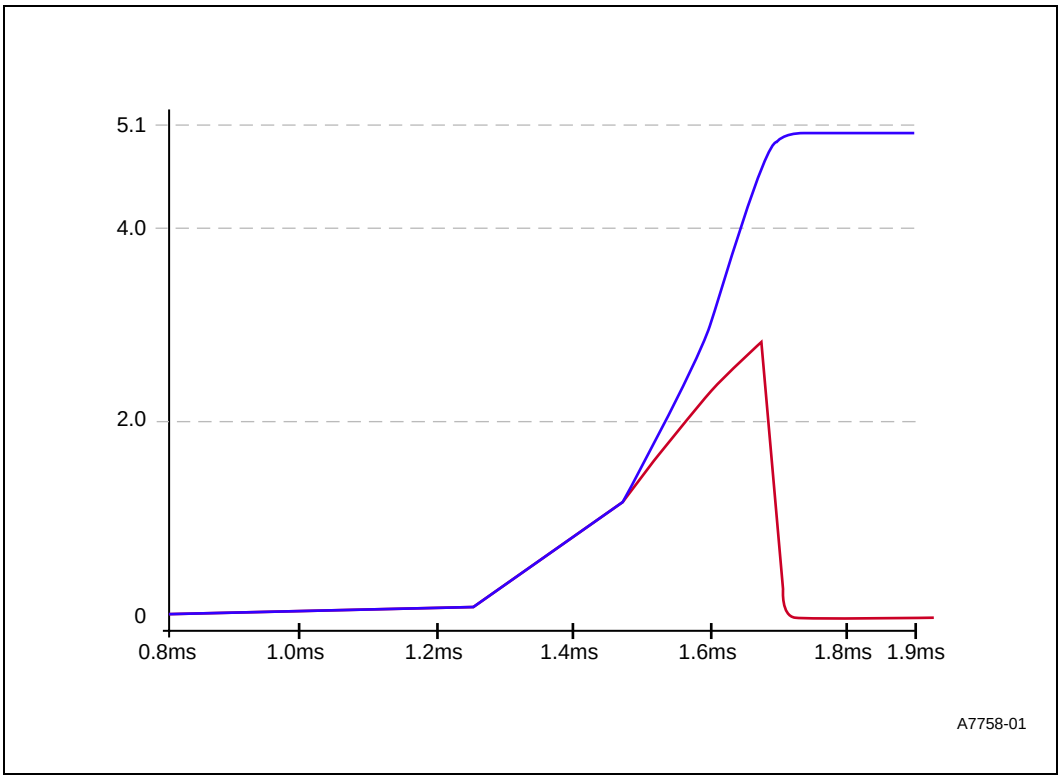
Figure 14. Recommended Power Supply Protection Circuit for the System Electronics



Components Values Assumed and Calculated

R1	5 mΩ	R20	20 KΩ, ± 5%
R2	5.62 KΩ, ± 1%	R23	71.5 KΩ, ± 1%
R4	100 KΩ, ± 1%	R24	100 KΩ, ± 1%
R12	100Ω, ± 1%	R25	1M, ± 5%
R13	100Ω, ± 1%	R26	1M, ± 5%
R14	6.04 KΩ, ± 1%	R27	1 KΩ, ± 1%
R16	100 KΩ, ± 1%		
R17	10 KΩ, ± 1%	C9	0.33 µF
R18	11 KΩ, ± 1%	C18	0.1 µF

Figure 15. Simulation of V_DC Voltage Skew



5.4 Active Thermal Feedback

Table 24 identifies the address allocated for the SMBus thermal sensor used on the Low-Power Module.

Table 24. Thermal Sensor SMBus Address

Function	Fixed Address AD Bits (6:4)	Selectable Address AD Bits (3:0)
Thermal Sensor	011	1110
Reserved	010	1010
Reserved	010	1011

NOTE: The thermal sensor used is compliant with SMBus addressing.

5.5 Thermal Sensor Configuration Register

The configuration register of the thermal sensor controls the operating mode (Auto Conversion or Standby) of the device. Since the processor temperature varies dynamically during normal operation, the Auto Conversion mode should be used exclusively to monitor the processor temperature. Table 25 shows the format of the configuration register. If the RUN/STOP bit is low, then the thermal sensor enters Auto-Conversion mode. If the RUN/STOP bit is set high, then the thermal sensor immediately stops converting and enters the Standby mode. The thermal sensor still performs temperature conversions in Standby mode when it receives a one-shot command. However, the result of a one-shot command during Auto Conversion mode is not guaranteed. Intel does not recommend using the one-shot command to monitor temperature when the processor is active; only Auto Conversion mode should be used. Contact your Intel representative for further information.

Table 25. Thermal Sensor Configuration Register

Bit	Name	Reset State	Function
7 MSB	MASK	0	Masks SMBALERT# when high
6	RUN/STOP	0	Standby mode control bit. If it is low, then the device enters Auto Convert mode. If it is high, then the device immediately stops converting and enters Standby mode where the one-shot command can be performed.
5-0	Reserved	0	Reserved for future use

NOTE: All reserved bits should be written as “0” and read as “don’t care” for programming purposes.

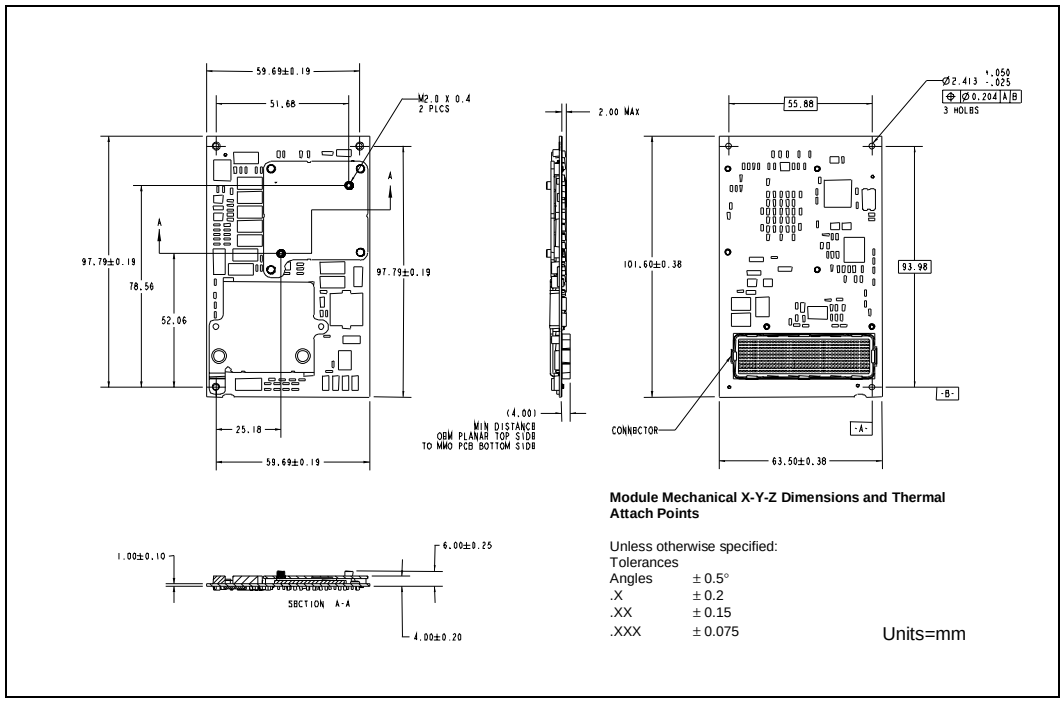
6.0 Mechanical Specification

This section provides the physical dimensions for the Pentium III Processor – Low-Power Module.

6.1 Module Dimensions

Figure 16 shows the board dimensions and the connector orientation.

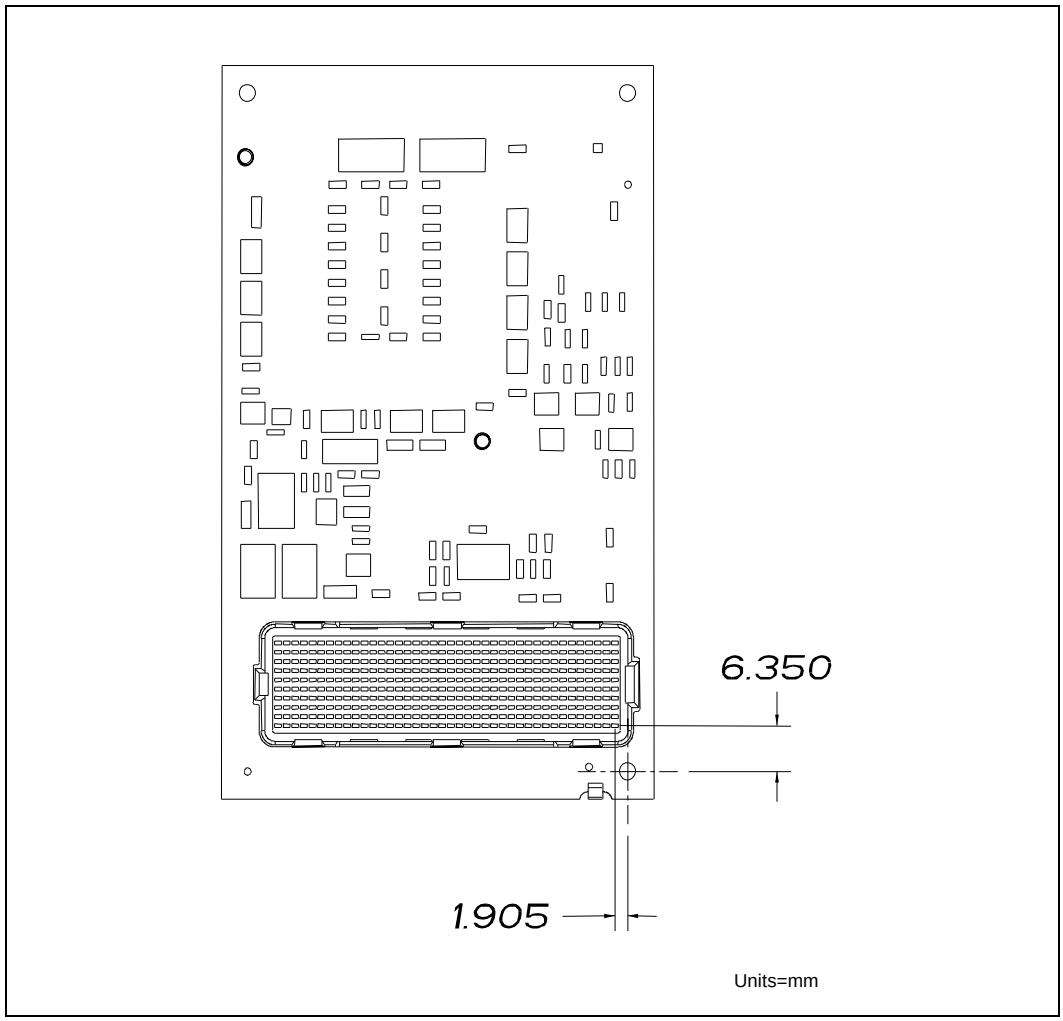
Figure 16. Board Dimensions



6.1.1 Pin 1 Location on the Connector

Figure 17 shows the location of Pin 1 of the 400-pin connector.

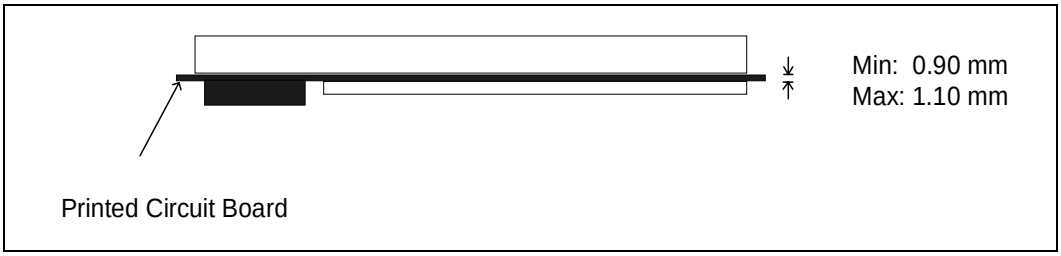
Figure 17. Board Dimensions and Connector Orientation



6.1.2 Printed Circuit Board

Figure 18 shows the minimum and maximum thickness of the Low Power Module printed circuit board (PCB). The range of PCB thickness allows for different PCB technologies to be used with Intel Low-Power Modules.

Figure 18. Low Power Module Printed Circuit Board Thickness

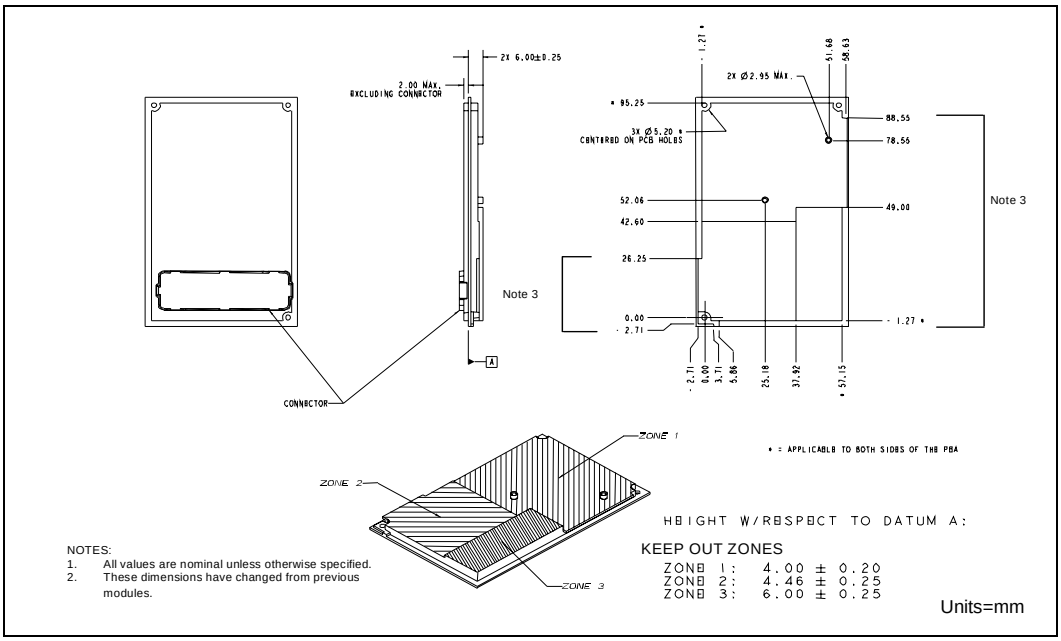


6.1.3 Height Restrictions

Figure 19 shows the height restrictions of the Low-Power Module. The keep-out zone is also illustrated.

Three mating connectors are available in heights of approximately 4 mm, 6 mm, and 8 mm. The three sizes provide flexibility in choosing the system electronics components between the two boards.

Figure 19. Keep-out Zone



6.2 Thermal Transfer Plate

The thermal transfer plate (TTP) provides heat dissipation on the mobile Pentium III processor and the 82443BX. The TTP may vary on previous generations of Intel Low-Power Modules. The TTP provides the thermal attach point, where a system manufacturer can transfer heat through the system using a heat pipe, a heat spreader plate, or other thermal solutions. Attachment dimensions for the thermal interface block to the TTP are provided in Figure 20 and Figure 21. The system manufacturer should use the exact dimensions for maximum contact area to the TTP while ensuring that no warpage of the TTP occurs. If warpage occurs, the thermal resistance of the module could be adversely affected.

When attaching a mating block to the TTP, a thermal elastomer or thermal grease should be used as an interface material. This material reduces the thermal resistance. The customer thermal interface block should be secured to the CPU TTP with M2 screws using a maximum torque of 1.5 Kg*cm to 2.0 Kg*cm (equivalent to 0.147 N*m to 0.197 N*m). The thread length of the 2.00-mm screws should be 2.25-mm gaugeable thread (2.25-mm minimum to 2.80-mm maximum). The TTP thermal resistance between the processor core to the top center of the TTP does not exceed 1° C per watt.

Figure 20. 82443BX Thermal Transfer Plate

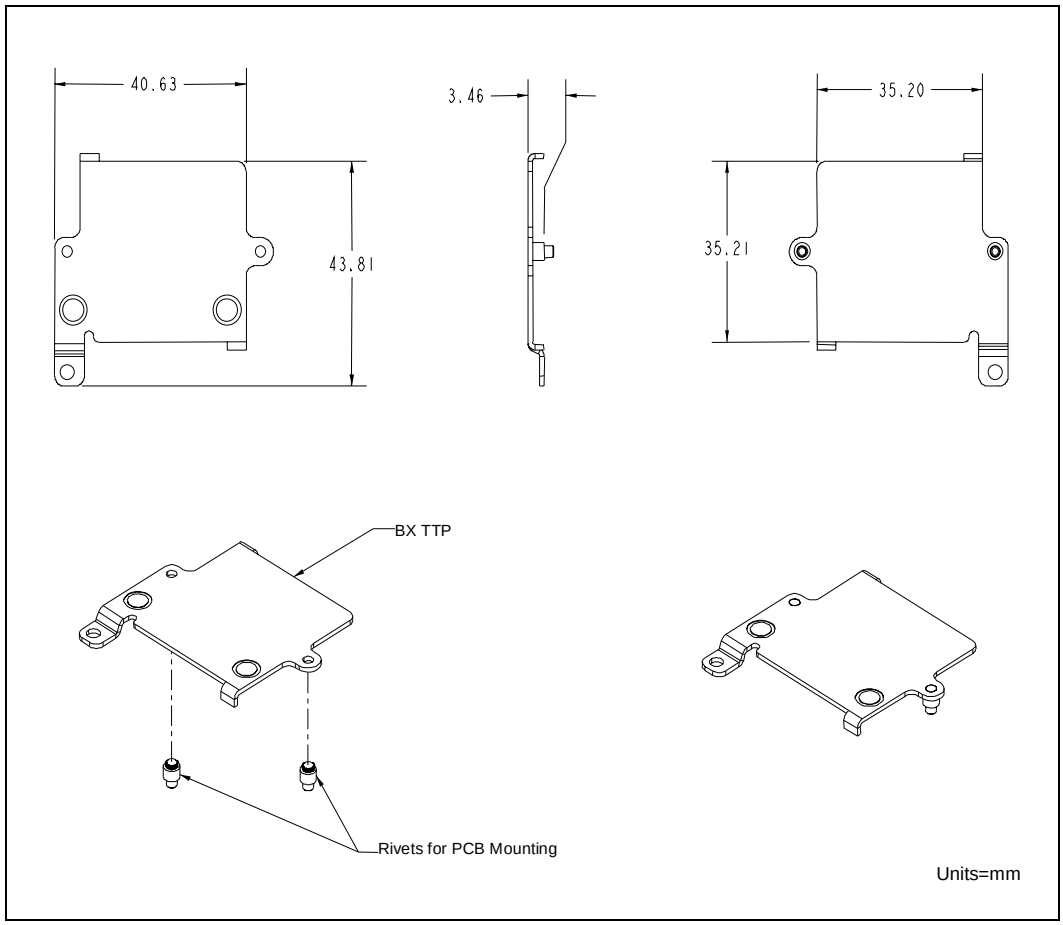
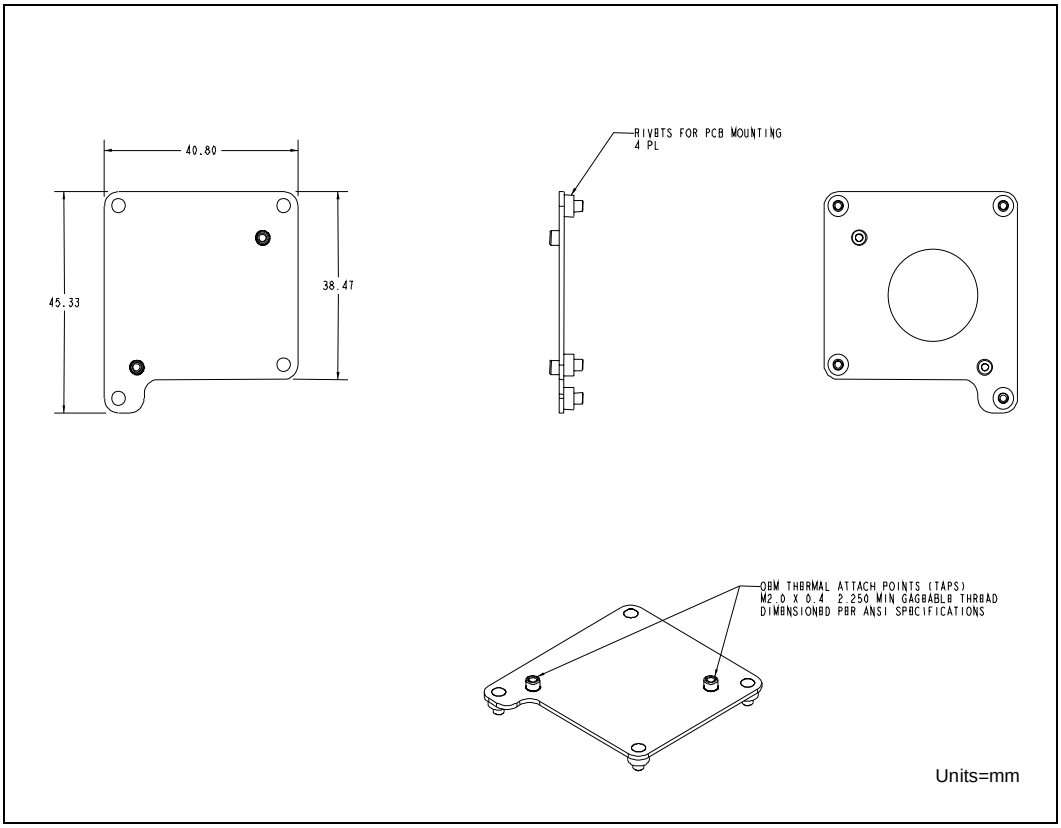


Figure 21. CPU Thermal Transfer Plate



6.3 Physical Support

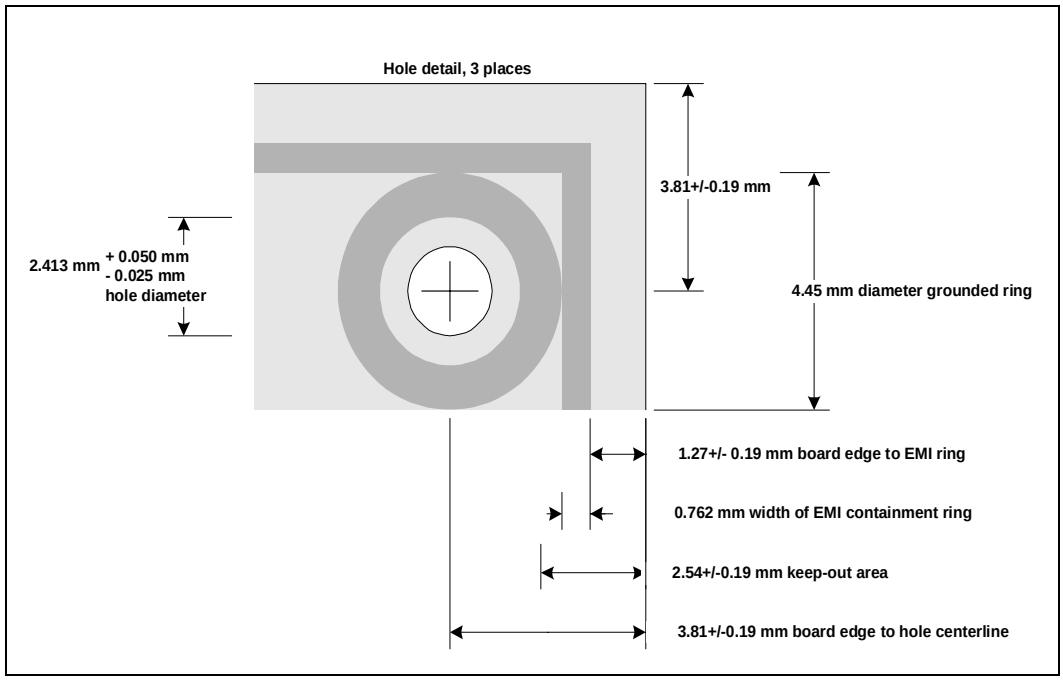
6.3.1 Mounting Requirements

Three mounting holes are available for securing the Low-Power Module to the system base or the system electronics. See Figure 16 for mounting hole locations. These hole locations and board edge clearances remain fixed for all Intel Low-Power Modules. All three mounting holes should be used to ensure long term mechanical reliability and EMI integrity of the system.

The board edge clearance includes a 0.762-mm (0.030 inches) wide EMI containment ring around the perimeter of the module. This ring is on each layer of the module PCB and is grounded. On the surface of the module, the metal is exposed for EMI shielding purposes. The hole patterns also have a plated surrounding ring to use a metal standoff for EMI shielding purposes. Standoffs should be used to provide support for the installed module. However, the warpage of the baseboard can vary and should be calculated into the final dimensions of the standoffs used.

Figure 22 shows the standoff support hole patterns, the board edge clearance, and the dimensions of the EMI containment ring. No components are placed on the board in the keep-out area.

Figure 22. Standoff Holes, Board Edge Clearance, and EMI Containment Ring



6.3.2 Weight

The Pentium III Processor – Low-Power Module weight is approximately 58 grams.

7.0 Thermal Specification

7.1 Thermal Design Power

Table 26 provides the typical thermal design power (TDP) specification. The typical TDP is the typical power dissipation under normal operating conditions at nominal V_CORE (CPU power supply) while executing the worst case power instruction mix. This includes the power dissipated by all of the relevant components. During all operating environments, the processor junction temperature (T_j) must be within the specified range of 0° C to 100° C.

The power handling capability of the system thermal solution may be reduced to less than the recommended typical TDP shown in Table 26 with the implementation of firmware/software control or "throttling" that reduces the CPU power consumption and dissipation.

For more information, see the *Pentium® III Processor Low-Power Module Thermal Design Guide* (order number 273300).

Table 26. Thermal Design Power Specification

Symbol	Parameter	Typical 500 MHz	Notes
TDP_{Module}	Module Thermal Design Power	15.0 W	Module = core + 82443BX + voltage regulator, Notes 1, 2

NOTES:
1. The processor temperature, T_j, must be within the specified range of 0° C to 100° C.
2. TDP_{Module} is a thermal solution design reference point for customer thermal solution readiness for total module power.

8.0 Labeling Information

Intel Low-Power Modules are tracked in two ways. The first is by the product tracking code (PTC). Intel uses the PTC label to determine the assembly level of the Low-Power Module. Figure 23 shows where the PTC can be found on the Low-Power Module. The PTC contains 13 characters and provides the following information.

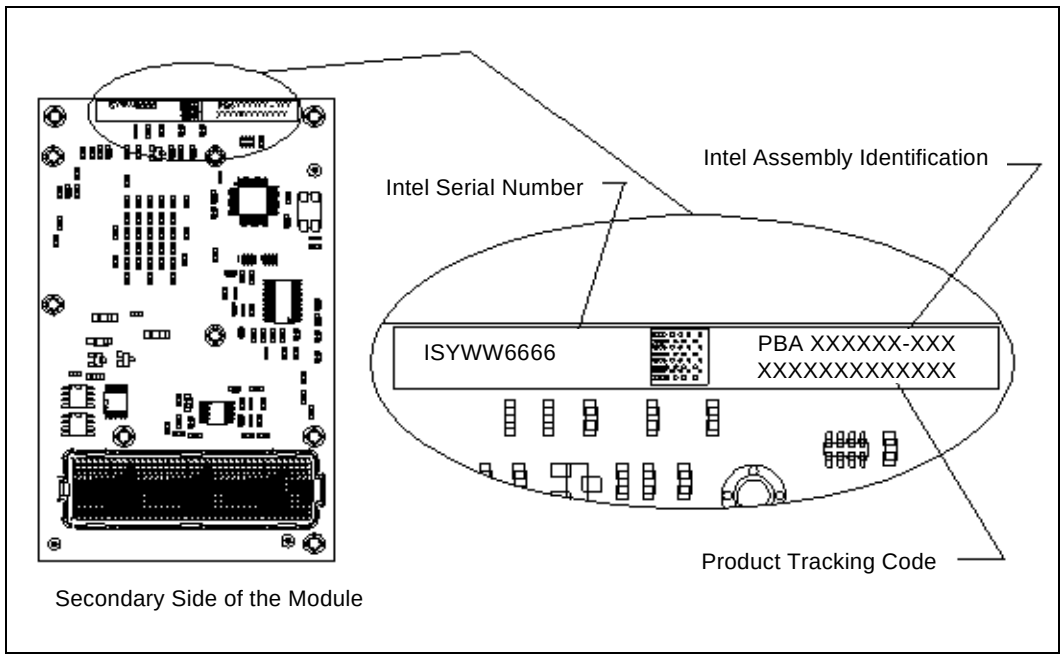
Example: EM500L00102ES

Definition:

EM	Embedded Module
500	Speed identity
L	Low-Power Module
001	Initial release
02	256-Kbyte cache size
ES	Engineering sample

Note: The last two letters of the PTC depend on the design revision. For example, QS is used for qualification sample, and PS is used for production sample.

Figure 23. Product Tracking Code



The second tracking method uses a customer-generated software utility. Four strapping resistors located on the module determine its production level. If connected and terminated properly, up to 16 module revision levels can be determined. A customer-generated software utility can then read these ID bits with CPU IDs and stepping IDs to provide a complete module manufacturing revision level. For more information, contact your Intel representative.

9.0 Environmental Standards

The environmental standards are defined in Table 27.

Table 27. Environmental Standards

Parameter	Condition	Specification
Temperature Cycle	Non-operating Operating	-40° C to 85° C 0° C to 55° C
Humidity	Unbiased	85% relative humidity at 55° C
Voltage	V_5 V_3	5.0 V ± 5% 3.3 V ± 5%
Shock	Non-operating Unpackaged Packaged Packaged	Half Sine, 2 G, 11 msec Trapezoidal, 50 G, 11 msec Inclined impact at 5.7 ft/s Half Sine, 2 ms at 36 inches simulated free fall
Vibration	Unpackaged Packaged Packaged	5 Hz to 500 Hz, 2.2-gRMS random 10 Hz to 500 Hz, 1.0 gRMS 11,800 impacts 2 Hz to 5 Hz (low frequency)
ESD Damage	Human Body Model	Non-powered test of the module only for non-catastrophic failure. The Low-Power Module is tested at 2 KV and then inserted in a system for functional test.