Low-Power Module Memory Bus Simulation Methodology

Application Note

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Application Note

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1.0 Introduction

This application note describes a simulation methodology for interfacing memory signals from the Low-Power Module to the 100-MHz Unbuffered SDRAM Dual In-Line Memory Modules (SDRAM DIMM). The models used to drive the simulation tool are based on the I/O Buffer Industry Standard (IBIS).

Note: The simulation methodology in this application note is based on 100 MHz SDRAM DIMM designs; however, the same methodology applies to 66 MHz SDRAM DIMM designs.

1.1 Key Terms

The Low-Power Module is designed for applied computing market segments. A complete description of the available modules is located in the *Intel® Pentium® II Processor with On-Die Cache – Low-Power Module* datasheet (order number 273257), *Intel® Pentium® II Processor – Low-Power Module* datasheet (order number 273256), and the *Intel® Pentium® III Processor – Low-Power Module* datasheet (order number 273299).

Intel 440BX AGPset refers to both the 82443BX Host Bridge/Controller and the 82371EB PCI ISA IDE Xcelerator. A complete description of this chipset is located in both the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet (order number 290633) and the *82371AB PCI-TO-ISA/IDE Xcelerator (PIIX4)* datasheet (order number 290562).

SDRAM DIMM refers to synchronous DRAM dual in-line memory modules.

SE Board refers to the system electronics board.

1.2 Related Documents

You can download these documents from Intel's World Wide Web site at http://www.intel.com.

Table 1. Related Intel Documents

Document	Order Number (URL)
Intel® Pentium® III Processor – Low-Power Module datasheet	273299
Mobile Pentium® III Processor Specification Update	245306
Intel® Pentium® II Processor – Low-Power Module datasheet	273256
Intel® Pentium® II Processor with On-Die Cache – Low-Power Module datasheet	273257
Mobile Pentium® II Processor Specification Update	243887
82371AB PCI-TO-ISA/IDE Xcelerator (PIIX4) datasheet	290562
82371EB PCI ISA IDE Xcelerator (PIIX4E) Specification Update	290635
Intel® 440BX AGPset: 82443BX Host Bridge/Controller datasheet	290633
82443BX Host Bridge/Controller Electrical and Thermal Timing Specification datasheet addendum	273218
Intel® 440BX AGPset: 82443BX Host Bridge/Controller Specification Update	290639
66/100 MHz PC SDRAM Unbuffered SO-DIMM Specification Rev 1.0	http://www.intel.com/design/chipsets/memory/sdram.htm

2.0 Simulation Prerequisites

The following information is needed to simulate the Low-Power Module memory bus:

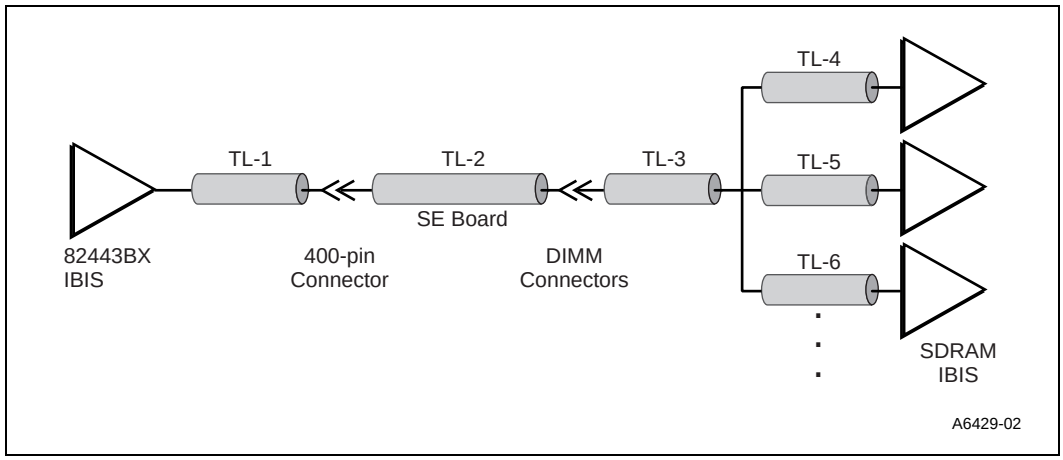
- Low Power Module I/O Buffer Model Specification (contact your Intel Field Sales Representative)
  - — Module interconnect specifications
  - — Connector parameters
- *82443BX Electrical and Thermal Timing Specifications* datasheet addendum, Rev 1.0 (order number: 273218)
  - — 82443BX AC and DC Specifications
- *PC SDRAM Unbuffered DIMM Specification*, Rev 1.0 (http://www.intel.com/design/chipsets/memory/sdram.htm)
  - — DIMM board layout
  - — SDRAM AC and DC specifications
- I/O Buffer Models
  - — 82443BX IBIS model, Rev 1.2 (contact your Intel Field Sales Representative). The 82443BX IBIS model is used for the Intel® 440BX AGPset chipset.
  - — SDRAM component IBIS models. The unbuffered SDRAM IBIS models are available in x8 and x16 configurations from various memory manufacturers.

3.0 Simulation Block Diagram

Figure 1 shows the simulation block diagram for the Low-Power Module/DIMM memory interface. The Low-Power Module Buffer Model describes the interconnect characteristics between the Low-Power Module 400-pin connector, and the 82443BX Host Bridge/Controller.

As shown in Figure 1, the Low-Power Module I/O Buffer Model Specification is used to model the net (TL-1) and the 400-pin connector model. The *PC SDRAM Unbuffered DIMM* specification, which describes the interconnect characteristics of the SDRAM DIMM, is used to model the nets (TL-3, TL-4, TL-5, TL-6) of the DIMMs. Based on all the corners of simulations, as described in Section 5.0, the interconnect on the system electronics (SE) board (TL-2) can be specified to meet the setup/hold requirements for both the SDRAM and 82443BX Host Bridge/Controller.

Figure 1. Simulation Model Components



4.0 Details of the Electrical Interconnect Models

This section provides detailed information on the electrical interconnect models used for the simulation. Table 2 lists the assumed characteristics for the Low-Power Module, the system electronics board, and the DIMM interface, for fast, slow, and worst-case signal quality models.

Table 2. Fast, Slow, and Worst-Case Signal Quality Corner Interconnect Models

Component	Parameter	Min	Typical	Max	Units
Low-Power Module	Impedance (Z_0)	47	55	63	Ω
	Dielectric (E_r)	4.1	4.4	4.8	
	Trace Propagation Delay (t_{pd})	138	162	186	ps/in
SE Board	Impedance (Z_0)	47	55	63	Ω
	Dielectric (E_r)	4.1	4.4	4.8	
	Trace Propagation Delay (t_{pd})	138	162	186	ps/in
DIMM	Impedance (Z_0)	60	70	80	Ω
	Dielectric (E_r)	4.2	4.4	4.8	
	Trace Propagation Delay (t_{pd})	133	158	183	ps/in

Figure 2, shows the *Pi*-element network model used for the 400-pin module connector.

Figure 2. 400-pin Connector Package Model

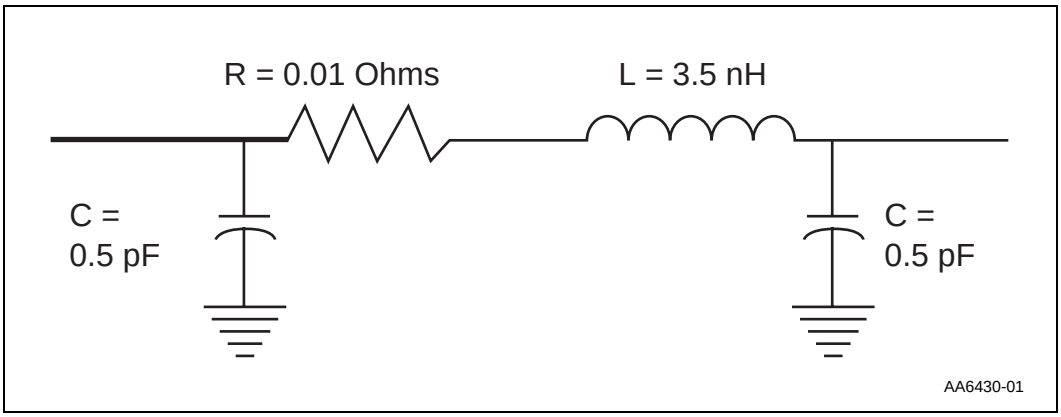
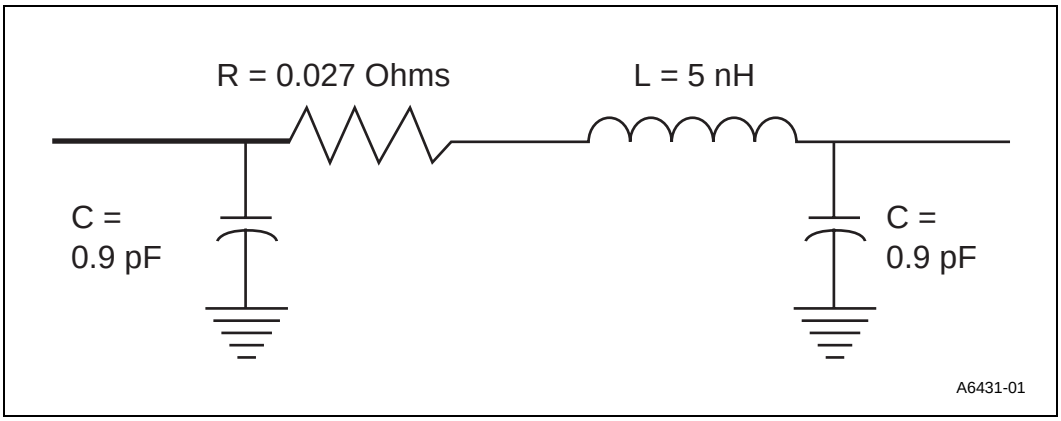


Figure 3 shows the *Pi*-element network model used for the DIMM connector.

Figure 3. DIMM Connector Package Model



5.0 Simulation Conditions

The DIMM topology routing for each signal is defined in the *PC SDRAM Unbuffered DIMM* specification. Figure 4 shows the two-DIMM system connection and the possible receiver pin loads for each memory signal. For example, a fully populated x8 with ECC arrangement for a two-DIMM system yields the heaviest receiving pin load (2 x 18 = 36 loads) on the SRAS_A#, SCAS_A#, WE_A#, and MAB# signals, as shown in Table 3. Since the Low-Power Module is also designed to support a one-DIMM system, a x16 arrangement DIMM yields the lightest pin load (four loads) on the same signals.

The heaviest and lightest receiving pin loads for each Low-Power Module memory signal is used for slow (setup) and fast (hold) corner simulations, respectively.

The DIMMs used for this simulation are x8, x8 with ECC, and x16 DIMM arrangements.

Figure 4. DIMM Connection

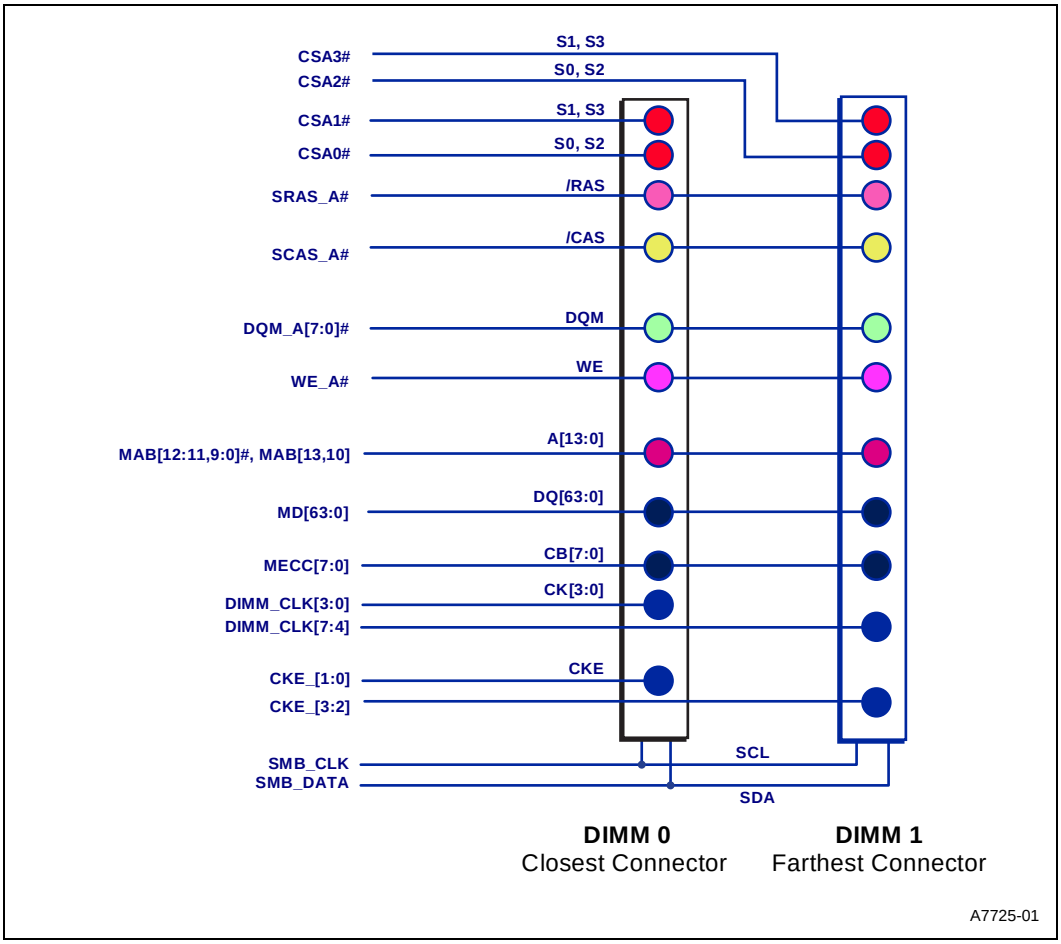


Table 3. Low-Power Module Memory Interface Pin Loading

SDRAM Signals	Number of Populated DIMM Sockets on SE Board†	Number of Pin Loads		
		DIMM x8	DIMM x8 with ECC	DIMM x16
SRAS_A#	1 min, 2 max	8 min, 16 max	9 min, 18 max	4 min, 8 max
SCAS_A#	1 min, 2 max	8 min, 16 max	9 min, 18 max	4 min, 8 max
WE_A#	1 min, 2 max	8 min, 16 max	9 min, 18 max	4 min, 8 max
MAB[x:x]#	1 min, 2 max	8 min, 16 max	9 min, 18 max	4 min, 8 max
CKE[x:x]	1	8	9	4
CSA[x:x]#	1	8	9	4
MD[x:x], MECC[x:x]	1 min, 2 max	1 min, 2 max	1 min, 2 max	1 min, 2 max
DQM_A[x:x]#	1 min, 2 max	1 min, 2 max	1 min, 2 max	1 min, 2 max

† Assumes a two-DIMM socket system.

Table 4 lists the Low-Power Module/DIMM condition used in the simulation. Each driver/receiver pair of the memory signal with the heaviest/lightest pin load is simulated with these conditions. The first four entries of the table are used for slow corner (setup) simulations in conjunction with heaviest receiver pin loads of the driver/receiver signal pair. The last four entries of the table are used for fast corner (hold) and signal quality simulations in conjunction with the lightest receiver pin loads of the driver/receiver signal pair.

Table 4. Simulation Conditions

Driver	Receiver	Low-Power Module/SE Board Trace Velocity (ns/in)	DIMM Trace Velocity (ns/in)	Low-Power Module/SE Board Impedance (Ohms)	DIMM Impedance (Ohms)
Slow	Slow	0.186	0.183	63	80
Slow	Slow	0.186	0.183	63	60
Slow	Slow	0.186	0.183	47	80
Slow	Slow	0.186	0.183	47	60
Fast	Fast	0.138	0.133	63	80
Fast	Fast	0.138	0.133	63	60
Fast	Fast	0.138	0.133	47	80
Fast	Fast	0.138	0.133	47	60

In general, a simulation tool assumes a no-loss transmission line in the pre-layout simulation. Also, each signal is simulated as a single net. No crosstalk is taken into account.

After the system electronics board is designed to meet the memory interface trace length requirement, a crosstalk simulation can be run with adjacent parallel lines. The stackup and trace width are varied to run a fast and slow corner simulation. However, this document only describes the methodology for pre-layout simulations.

6.0 Flight Time and Signal Quality Definitions

6.1 Flight Time Simulation

Flight time (T_{FLIGHT}) is the time difference between a signal crossing V_{REF} at the input pin of the SDRAM device and the output pin of the driver crossing V_{REF} where it drives a test load (shown in Figure 5). For Low-Power Module memory interface simulations, V_{REF} and the test load are specified to be 1.4 V and a 0 pF load respectively. These values can be found in the *82443BX Host Bridge/Controller Electrical and Thermal Timing Specification Datasheet Addendum* (order number 273218).

As shown in Figure 5, the T_{FLIGHT} equation is:

$$T_{FLIGHT} = T_{FLIGHT\_SYSTEM} - T_{REF}$$

Figure 5. Determining Flight Time

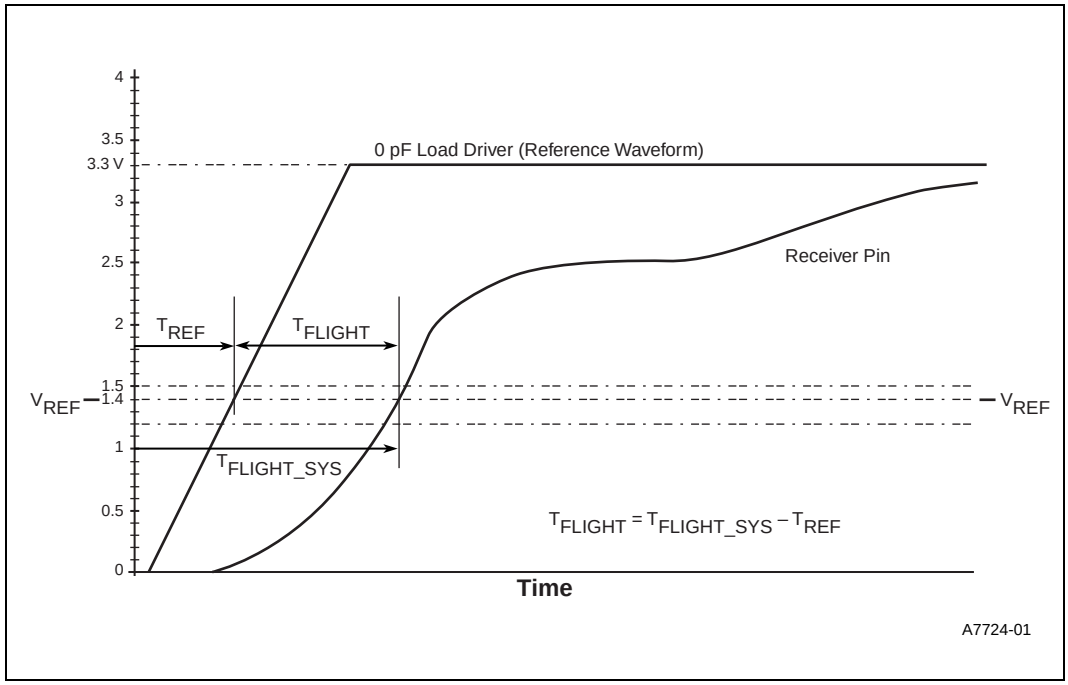


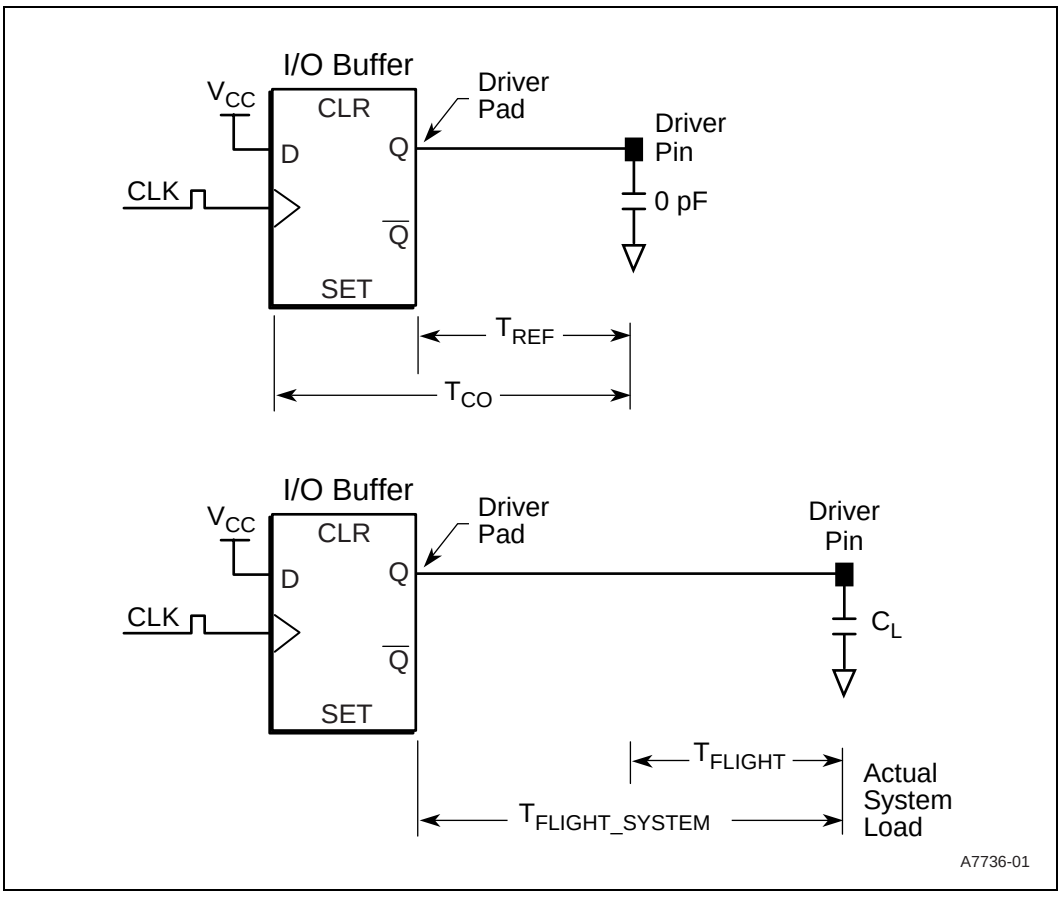
Figure 6 shows the different configurations for T_{CO} testing and flight time simulation. The flip-flop represents the logic input and driver stage of a typical Low-Power Module memory interface I/O buffer. T_{CO} (time from clock to output receiver switches) timings are specified at the driver pin output. T_{FLIGHT_SYSTEM} is usually reported by a simulation tool as the time from the driver pad starting its transition to the time when the receiver's input pin sees a valid data input. Since both timing numbers (T_{CO} and T_{FLIGHT_SYSTEM}) will include propagation time from the pad to the pin, it is necessary to subtract this time (T_{REF}) from the reported flight time to avoid double counting. T_{REF} is defined as the time that it takes for the driver output pin to reach the measurement voltage, V_{REF} (1.4 V), starting from the beginning of the driver transition at the pad. T_{REF} must be generated using the same test load (0 pF) for T_{CO}. Intel provides this timing value in the 440BX AGPset I/O buffer models.

In this manner, the following valid delay equation is satisfied:

Valid Delay = $T_{CO} + T_{FLIGHT} = T_{CO} + T_{FLIGHT\_SYS} - T_{REF}$
$= T_{CO\_MEASURED} + T_{FLIGHT\_MEASURED}$

The valid delay equation is the total time from when the driver sees a valid clock pulse to the time when the receiver sees a valid data input.

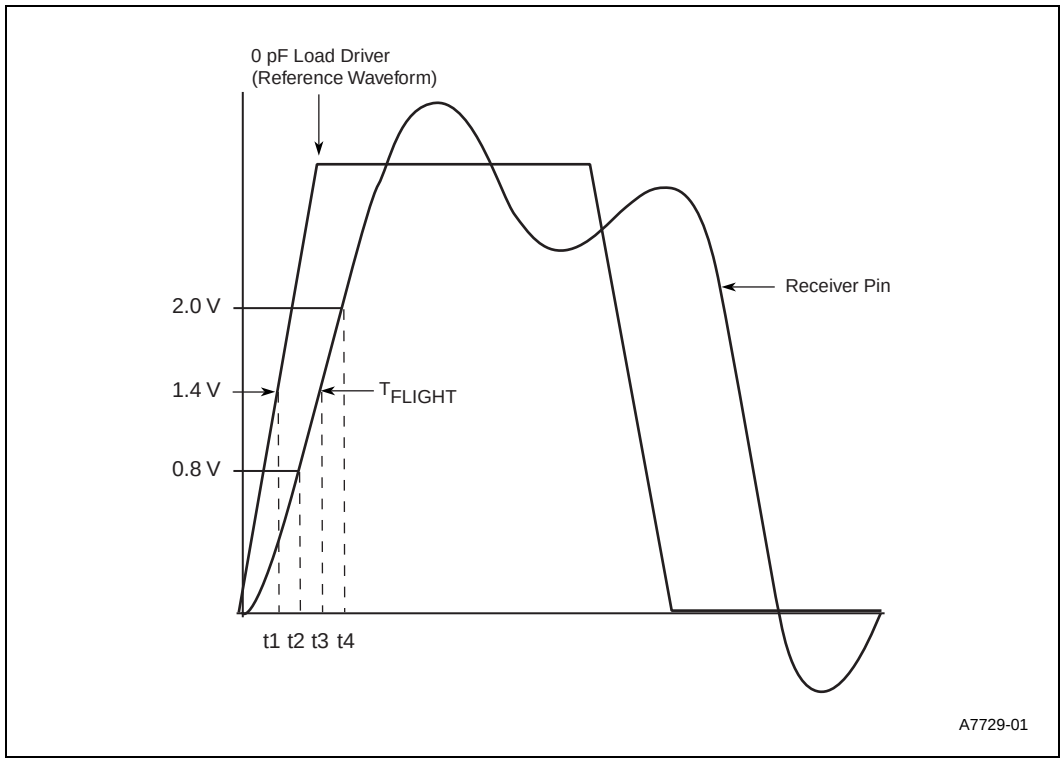
Figure 6. Test Load vs. Actual System Load



6.2 Flight Time Determination for Setup Time

The maximum flight time measurement is used to determine the setup time of a memory signal. Both the rising and falling edges should be considered. Figure 7 shows the determination of maximum flight time for the rising edge of a memory signal.

Figure 7. Flight Time (Rising Edge)



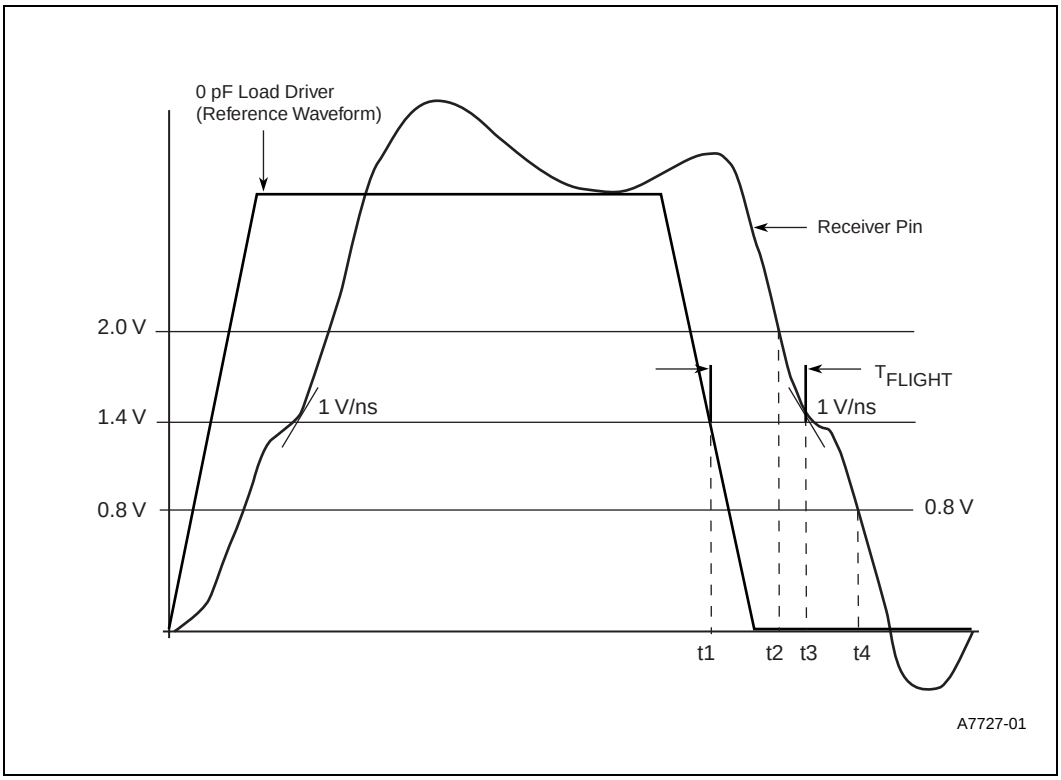
The flight time of the rising edge is measured between the driver and receiver at 1.4 V (T1 and T3) since the threshold switching voltage of the SDRAM is at this voltage.

However, when the edge rate (20% – 80% measurement) of the flight time is less than 1 V/ns, then the flight time is measured between the driver at 1.4 V (T1) and the receiver at 2.0 V (V_{ih}, T4), and derating it by subtracting 600 ps as recommended by Intel.

The maximum flight time is the greater of the two measurements.

Figure 8 shows the determination of flight time for the falling edge of a signal.

Figure 8. Flight Time (Falling Edge)



The flight time of the falling edge is determined between the driver and receiver at 1.4 V (T1 and T3).

However, when the edge rate of the flight time is less than 1 V/ns, then the flight time is determined between the driver at 1.4 V (T1) and the receiver at 0.8 V (V_{il}, T4), and derating it by subtracting 600 ps as recommended by Intel.

The maximum flight time is the greater of the two measurements.

6.2.1 Hold Time (Rising Edge)

The minimum flight time measurement is used to determine the hold time of a memory signal.

The flight time of the rising edge is determined between the driver and receiver at 1.4 V (T1 and T3) as shown in Figure 5.

However, when the edge rate of the flight time is less than 1 V/ns, then the flight time is determined between the driver at 1.4 V (T1) and receiver at 0.8 V (V_{il}, T2), and derating it by adding 600 ps as recommended by Intel.

The minimum flight time is the lesser of the two measurements.

Repeat the above process for the falling edge with the exception that the flight time is measured between 1.4 V (T1) and 2.0 V (T2) as shown in Figure 7.

6.3 Signal Quality

Signal quality is simulated using the fast corner models because the fast edge rates will induce the worst case overshoot and ringback. Overshoot is that part of the signal that transitions above V_{CC} or below V_{SS} when measured at the receiver pin. Ringback is measured as that part of the signal that crosses V_{CC} in the negative direction to its lowest part (for low to high transitions) and that part of the signal that crosses V_{SS} in the positive direction to its highest part (for high-to-low transitions). Settling time is measured at V_{CC} minus 10% at the point the signal last crosses that voltage for low-to-high transitions. For high-to-low transitions, settling time is measured at the last crossing of V_{SS} plus 10% of V_{CC}.

Figure 9. Low Power Module Interface Overshoot/Undershoot, Settling Limit, and Ringback

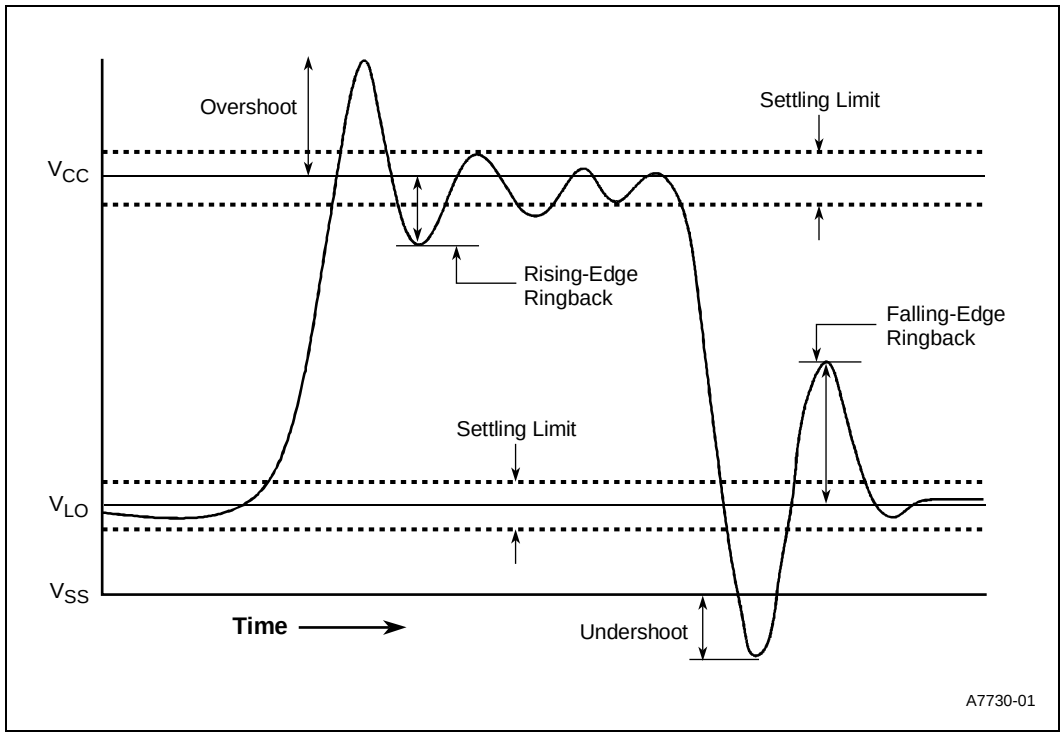


Table 5 outlines the signal quality criteria that are used to define constraints on overshoot and undershoot. In the case of the *PC SDRAM Unbuffered DIMM* specification, the maximum instantaneous overshoot/undershoot is ±1.5 V, and the inputs may overshoot beyond maximum V_{CC} (V_{CC} + 5%) or undershoot below V_{SS} for 5 ns on the SDRAM inputs. For Low-Power Module/440BX memory interface signal quality conditions, the maximum instantaneous overshoot/undershoot is ±1.6 V, and the inputs may overshoot beyond maximum V_{CC} (V_{CC} + 5%) or undershoot below V_{SS} by 0.8 for 7.0 ns on the inputs.

Table 5. Signal Quality Criteria

Driver	Receiver	Overshoot	Undershoot	Rise Time (min)	Fall Time (min)
CLK Driver	SDRAM	≤ 1.5 V for ≤ 5 ns	≤ 1.5 V for ≤ 5 ns	1 V/ns	1 V/ns
440BX	SDRAM	≤ 1.5 V for ≤ 5 ns	≤ 1.5 V for ≤ 5 ns	1 V/ns	1 V/ns
CLK Driver	440BX	≤ 1.6 V for ≤ 7 ns	≤ 1.6 V for ≤ 7 ns	1 V/ns	1 V/ns
SDRAM	440BX	≤ 1.6 V for ≤ 7 ns	≤ 1.6 V for ≤ 7 ns	1 V/ns	1 V/ns

When there is a signal quality issue on a memory signal where the ringback crosses the threshold regions (*i.e.*, V_{ih}, V_{il}), then the maximum and minimum flight time has to be re-measured. In this case, the flight time of a signal has to be measured at the last crossing of 2.0 V (T3) for the rising edge and at the last crossing of 0.8 V (T6) for the falling edge. Figure 10 shows how to measure the flight time when there is ringing.

Figure 10. Flight Time Measurement (With Ringing)