AP-384

APPLICATION NOTE

Designing with the 28F016XD

BRIAN DIPERT
SENIOR TECHNICAL MARKETING ENGINEER

SUJAN KAMRAN
TECHNICAL MARKETING ENGINEER

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1.0 INTRODUCTION

This application note discusses comparisons between the 28F016XD and DRAM memories. It also offers recommendations for determining compatibility between the 28F016XD and DRAM controllers, and provides suggestions for designing DRAM controllers with the 28F016XD in mind. The 28F016XD, an Intel 16-Mbit flash memory component, retains full software backwards-compatibility with the 28F008SA and adds the following features:

- Multiplexed address/address interface with RAS# and CAS# control inputs
- SmartVoltage technology
- 3.3V or 5.0V V_{CC} operation

The 28F016XD leverages the existing DRAM controller in system designs and thereby minimizes the glue logic required to interface to flash memory. It is a 16-Mbit device, organized as 1 Mbyte x 16. The 28F016XD has ten row addresses and ten column addresses, multiplexed on inputs A_0–A_9.

The 28F016XD is fully nonvolatile, giving it significant power and performance advantages over the traditional disk-plus-DRAM alternative. The 28F016XD does not lose data when power is removed from the device. By permanently storing and executing programs from the 28F016XD, the inherently slow disk drive-to-DRAM load delay is eliminated. The 28F016XD also does not require refresh cycles (although the 28F016XD will properly ignore any refresh cycles that are issued to it).

2.0 28F016XD COMPARISONS TO DRAM

The following sections discuss specific areas of comparison between the 28F016XD and 16-Mbit (1M x 16) DRAMs in 60 ns and 70 ns speed bins. Please reference the 28F016XD datasheet for a full description of the 28F016XD.

2.1 Voltage and Current Specifications

One obvious difference between the 28F016XD and DRAMs is that flash memory specifications reference a V_{PP} voltage, used with data write and erase operations. All V_{PP}-related voltage and current specifications are unique to the 28F016XD. Note that the 28F016XD offers the option to connect V_{PP} either to 12.0V ± 5% or to 5.0V ± 10% (which may also be the V_{CC} operating voltage). The 28F016XD includes V_{CC} current specifications during data write, erase and erase suspend operations. These operations are unique to flash memory; therefore, these specifications are not found in DRAM datasheets.

The 28F016XD specifies a V_{LKO} (lockout) voltage. This specification relates to circuitry within the flash memory that protects it from unwanted data alteration. The V_{LKO} specification is not found in DRAM datasheets. The 28F016XD also provides the deep power-down mode, not available on DRAMs. 28F016XD read, standby (CMOS), RAS#-only refresh and CAS#-before-RAS# refresh currents are all lower than those seen with DRAMs.

A comparison between the 28F016XD and representative 16-Mbit DRAMs (valid at the time this application note was written) is shown in Table 1.

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Table 1. 28F016XD Read, Standby and Refresh Currents Compared to 60 ns–70 ns 16-Mbit DRAM

Parameter	DRAM (3.3V)	28F016XD (3.3V)	DRAM (5.0V)	28F016XD (5.0V)
V_{CC} Read Current	90–150 mA	70 mA	90–160 mA	120 mA
V_{CC} Fast Page Mode Read Current	80 mA	60 mA	70–140 mA	110 mA
V_{CC} Standby Current (CMOS Inputs)	400 µA	130 µA	300 µA	130 µA
V_{CC} Standby Current (TTL Inputs)	2 mA	4 mA	2 mA	4 mA
V_{CC} CAS#-before-RAS# Refresh Current	90–160 mA	55 mA	90–150 mA	65 mA
V_{CC} RAS#-Only Refresh Current	90–150 mA	70 mA	90–160 mA	120 mA
V_{CC} Standby Current (Self Refresh Mode)	5 mA	55 mA	5 mA	65 mA

Tables 2 and 3 show added and revised (as compared to 16-Mbit DRAM) 28F016XD DC specifications.

Table 2. 28F016XD Added/Revised DC Characteristics

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°

Sym	Parameter	Min	Typ	Max	Unit	Test Condition
$I_{CC}1$	V_{CC} Word Read Current		50	70	mA	$V_{CC} = V_{CC}$ Max RAS#, CAS# = V_{IL} RAS#, CAS#, Addr. Cycling @ t_{RC} = min I_{OUT} = 0 mA Inputs = TTL or CMOS Single Row and Column Address Valid throughout Cycle
$I_{CC}2$	V_{CC} Standby Current		1	4	mA	$V_{CC} = V_{CC}$ Max RAS#, CAS#, RP# = V_{IH} WP#, 3/5# = V_{IL} or V_{IH}
$I_{CC}3$	V_{CC} RAS#-Only Refresh Current		50	70	mA	$V_{CC} = V_{CC}$ Max CAS# = V_{IH} RAS# = V_{IL} RAS#, Addr. Cycling @ t_{RC} = min Inputs = TTL or CMOS Single Row Address Valid throughout Cycle

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Table 2. 28F016XD Added/Revised DC Characteristics (Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°

Sym	Parameter	Min	Typ	Max	Unit	Test Condition
$I_{CC}4$	V_{CC} Fast Page Mode Word Read Current		40	60	mA	V_{CC} = V_{CC} Max RAS#, CAS# = V_{IL} CAS#, Addr. Cycling @ t_{PC} = min I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH} Single Column Address Valid throughout Cycle
$I_{CC}5$	V_{CC} Standby Current		70	130	µA	V_{CC} = V_{CC} Max RAS# CAS# RP# = V_{CC} ± 0.2V WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
$I_{CC}6$	V_{CC} CAS#-before-RAS# Refresh Current		40	55	mA	V_{CC} = V_{CC} Max CAS#, RAS# = V_{IL} CAS#, RAS#, Addr. Cycling @ t_{RC} = min Inputs = TTL or CMOS Address Static throughout Cycle
$I_{CC}7$	V_{CC} Standby Current (Self Refresh Mode)		40	55	mA	V_{CC} = V_{CC} Max RAS#, CAS# = V_{IL} I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH} Address Static throughout Cycle
I_{CCD}	V_{CC} Deep Power-Down Current		2	5	µA	RP# = GND ± 0.2V
I_{CCW}	V_{CC} Word Write Current		8	12	mA	V_{PP} = 12.0V ± 5% Word Write in Progress
			8	17	mA	V_{PP} = 5.0V ± 10% Word Write in Progress
I_{CCE}	V_{CC} Block Erase Current		6	12	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
			9	17	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current		1	4	mA	RAS#, CAS# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby/Read Current		± 1	± 10	µA	$V_{PP} \leq V_{CC}$
			30	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current		0.2	5	µA	RP# = GND ± 0.2V

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Table 2. 28F016XD Added/Revised DC Characteristics (Continued)

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°

Sym	Parameter	Min	Typ	Max	Unit	Test Condition
I_{PPW}	V_{PP} Word Write Current		10	15	mA	V_{PP} = 12.0V ± 5% Word Write in Progress
			15	25	mA	V_{PP} = 5.0V ± 10% Word Write in Progress
I_{PPE}	V_{PP} Block Erase Current		4	10	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
			14	20	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current		30	50	µA	Block Erase Suspended
V_{PPLK}	V_{PP} Erase/Write Lock Voltage	0.0		1.5	V	
$V_{PPH}1$	V_{PP} during Write/Erase Operations	4.5	5.0	5.5	V	
$V_{PPH}2$	V_{PP} during Write/Erase Operations	11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage	2.0			V	

Table 3. 28F016XD Added/Revised DC Characteristics

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to +70°C

Sym	Parameter	Min	Typ	Max	Unit	Test Condition
$I_{CC}1$	V_{CC} Word Read Current		90	120	mA	V_{CC} = V_{CC} Max RAS#, CAS# = V_{IL} RAS#, CAS#, Addr. Cycling @ t_{RC} = min I_{OUT} = 0 mA Inputs = TTL or CMOS Single Row and Column Address Valid throughout Cycle
$I_{CC}2$	V_{CC} Standby Current		2	4	mA	V_{CC} = V_{CC} Max RAS#, CAS#, RP# = V_{IH} WP#, 3/5# = V_{IL} or V_{IH}
$I_{CC}3$	V_{CC} RAS#-Only Refresh Current		90	120	mA	V_{CC} = V_{CC} Max CAS# = V_{IH} RAS# = V_{IL} RAS#, Addr. Cycling @ t_{RC} = min Inputs = TTL or CMOS Single Row Address Valid throughout Cycle

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Table 3. 28F016XD Added/Revised DC Characteristics (Continued)

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to +70°C

Sym	Parameter	Min	Typ	Max	Unit	Test Condition
$I_{CC}4$	V_{CC} Fast Page Mode Word Read Current		80	110	mA	$V_{CC} = V_{CC}$ Max RAS#, CAS# = V_{IL} CAS#, Addr. Cycling @ t_{PC} = min I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH} Single Column Address Valid throughout Cycle
$I_{CC}5$	V_{CC} Standby Current		70	130	µA	$V_{CC} = V_{CC}$ Max RAS#, CAS#, RP# = V_{CC} ± 0.2V WP#, 3/5# = V_{CC} ± 0.2V or GND ± 0.2V
$I_{CC}6$	V_{CC} CAS#-before-RAS# Refresh Current		50	65	mA	$V_{CC} = V_{CC}$ Max CAS#, RAS# = V_{IL} CAS#, RAS#, Addr. Cycling @ t_{RC} = min Inputs = TTL or CMOS Address Static throughout Cycle
$I_{CC}7$	V_{CC} Standby Current (Self Refresh Mode)		50	65	mA	$V_{CC} = V_{CC}$ Max RAS#, CAS# = V_{IL} I_{OUT} = 0 mA Inputs = V_{IL} or V_{IH} Address Static throughout Cycle
I_{CCD}	V_{CC} Deep Power-Down Current		2	5	µA	RP# = GND ± 0.2V
I_{CCW}	V_{CC} Word Write Current		25	35	mA	V_{PP} = 12.0V ± 5% Word Write in Progress
			25	40	mA	V_{PP} = 5.0V ± 10% Word Write in Progress
I_{CCE}	V_{CC} Block Erase Current		18	25	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
			20	30	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current		2	4	mA	RAS#, CAS# = V_{IH} Block Erase Suspended
I_{PPS}	V_{PP} Standby/Read Current		± 1	± 10	µA	$V_{PP} \leq V_{CC}$
			30	200	µA	$V_{PP} > V_{CC}$
I_{PPD}	V_{PP} Deep Power-Down Current		0.2	5	µA	RP# = GND ± 0.2V

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Table 3. 28F016XD Added/Revised DC Characteristics (Continued)

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to +70°C

Sym	Parameter	Min	Typ	Max	Unit	Test Condition
I_{PPW}	V_{PP} Word Write Current		7	12	mA	V_{PP} = 12.0V ± 5% Word Write in Progress
			17	22	mA	V_{PP} = 5.0V ± 10% Word Write in Progress
I_{PPE}	V_{PP} Block Erase Current		5	10	mA	V_{PP} = 12.0V ± 5% Block Erase in Progress
			16	20	mA	V_{PP} = 5.0V ± 10% Block Erase in Progress
I_{PPES}	V_{PP} Erase Suspend Current		30	50	µA	Block Erase Suspended
V_{PPLK}	V_{PP} Erase/Write Lock Voltage	0.0		1.5	V	
$V_{PPH}1$	V_{PP} during Write/Erase Operations	4.5	5.0	5.5	V	
$V_{PPH}2$	V_{PP} during Write/Erase Operations	11.4	12.0	12.6	V	
V_{LKO}	V_{CC} Erase/Write Lock Voltage	2.0			V	

2.2 Timing Specifications

28F016XD timing specifications are divided into the following categories in the datasheet:

- Common Parameters
- Read Cycle
- Write Cycle
- Read-Modify-Write Cycle
- Fast Page Mode Cycle (including fast page mode read-modify-write)
- Refresh Cycle (including refresh period)
- Miscellaneous

Many 28F016XD specifications match or improve on those of 60 ns and 70 ns DRAMs. Programming additional DRAM controller wait-states will accommodate most slower 28F016XD specs.

In some cases, specifications that have identical values for both reads and writes to DRAM (such as RAS# and CAS# pulse widths and hold times), have been differentiated (separate specs for read and write) on the 28F016XD. This differentiation both accurately reflects 28F016XD functionality and improves the DRAM controller interface to 28F016XD, in some cases.

Common Parameters

Table 4 compares 28F016XD common parameters to DRAM, with incompatible specifications shaded for emphasis. Areas where the 28F016XD improves upon DRAM specifications are outlined in bold. Notice that the 28F016XD's RAS# precharge time specification is much shorter than that for DRAM, while the 28F016XD's CAS# precharge time specification is slightly longer. Also, the 28F016XD's row address hold time after RAS#, column address hold time after CAS# and CAS#-to-RAS# precharge time are slightly longer than those for DRAM.

Table 4. 28F016XD Common Parameters Compared to 60 ns–70 ns 16-Mbit DRAM

Sym	Description	DRAM (3.3V)	28F016XD (3.3V)	DRAM (5.0V)	28F016XD (5.0V)
t_{RP}	RAS# Precharge Time (min)	40 ns	10 ns	40-50 ns	10 ns
t_{CP}	CAS# Precharge Time (min)	10 ns	15 ns	10 ns	15 ns
t_{ASR}	Row Address Set-Up Time (min)	0 ns	0 ns	0 ns	0 ns
t_{RAH}	Row Address Hold Time (min)	10 ns	15 ns	10 ns	15 ns
t_{ASC}	Column Address Set-Up Time (min)	0 ns	0 ns	0 ns	0 ns
t_{CAH}	Column Address Hold Time (min)	10–15 ns	20 ns	10–15 ns	20 ns
t_{CRP}	CAS# to RAS# Precharge Time (min)	5 ns	10 ns	5 ns	10 ns
t_{DZO}	OE# Delay Time from Data-In (min)	0 ns	0 ns	0 ns	0 ns
t_{DZC}	CAS# Delay Time from Data-In (min)	0 ns	0 ns	0 ns	0 ns

Read Cycle Specifications

28F016XD read cycle specification incompatibilities compared to DRAM can be summarized in the following three points:

- The 28F016XD's access time from column address is longer than that for DRAM
- The 28F016XD's access time from OE# and CAS# active is longer than that for DRAM
- The 28F016XD's data tri-state delay from OE#, RAS# or CAS# inactive is longer than that for DRAM

Table 5 compares 28F016XD read cycle specifications to DRAM, with incompatible specifications shaded for emphasis. Areas where the 28F016XD improves upon DRAM specifications are outlined in bold.

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Table 5. 28F016XD Read Cycle Specifications Compared to 60 ns–70 ns 16-Mbit DRAM

Sym	Description	DRAM (3.3V)	28F016XD (3.3V)	DRAM (5.0V)	28F016XD (5.0V)
$t_{RC(R)}$	Random Read Cycle Time (min)	110 ns	105 ns	110–130 ns	95 ns
$t_{RAS(R)}$	RAS# Pulse Width (Reads) (min)	70 ns	95 ns	60–70 ns	85 ns
$t_{CAS(R)}$	CAS# Pulse Width (Reads) (min)	15 ns	40 ns	15–20 ns	35 ns
$t_{RCD(R)}$	RAS# to CAS# Delay Time (Reads) (min)	15–20 ns	15 ns	15–20 ns	15 ns
$t_{RSH(R)}$	RAS# Hold Time (Reads) (min)	15 ns	30 ns	15–20 ns	30 ns
$t_{CSH(R)}$	CAS# Hold Time (Reads) (min)	70 ns	95 ns	60–70 ns	85 ns
t_{RAC}	Access Time from RAS# (max)	70 ns	95 ns	60–70 ns	85 ns
t_{CAC}	Access Time from CAS# (max)	15 ns	40 ns	15–20 ns	35 ns
t_{AA}	Access Time from Column Address (max)	30 ns	75 ns	30–35 ns	65 ns
t_{OEA}	OE# Access Time (max)	13–15 ns	40 ns	15–20 ns	35 ns
t_{RCS}	Read Command Set-Up Time (min)	0 ns	5 ns	0 ns	5 ns
t_{RCH}	Read Command Hold Time Referenced to CAS# (min)	0 ns	0 ns	0 ns	0 ns
t_{RRH}	Read Command Hold Time Referenced to RAS# (min)	0 ns	0 ns	0 ns	0 ns
t_{RAL}	Column Address to RAS# Lead Time (min)	75 ns	15 ns	30–35 ns	15 ns
t_{CAL}	Column Address to CAS# Lead Time (min)	30 ns	75 ns	30–35 ns	65 ns
t_{CLZ}	CAS# to Output in Low-Z (min)	0 ns	0 ns	0 ns	0 ns
t_{OH}	Output Data Hold Time (min)	0 ns	0 ns	0 ns	0 ns
t_{OHO}	Output Data Hold Time from OE# (min)	0 ns	0 ns	0 ns	0 ns
t_{OFF}	Output Buffer Turn-Off Delay (max)	13–15 ns	30 ns	15 ns	30 ns
t_{OEZ}	Output Buffer Turn-Off Delay Time from OE# (max)	13–15 ns	30 ns	15–20 ns	30 ns
t_{CDD}	CAS# to Data in Delay Time (min)	13–15 ns	30 ns	15–20 ns	30 ns

Write Cycle Specifications

Most 28F016XD write cycle specification incompatibilities compared to DRAM can be summarized by the fact that the 28F016XD CAS# active pulse width during writes is longer than the DRAM requirement. The 28F016XD's data hold time and WE# hold time from CAS# are also longer than that specified for 3.3V DRAM. Table 6 compares 28F016XD write cycle specifications to DRAM, with incompatible specifications shaded for emphasis. Areas where the 28F016XD improves upon DRAM specifications are outlined in bold.

Read-Modify-Write Cycle Specifications

28F016XD read-modify-write cycle specification incompatibilities compared to DRAM are caused by a combination of the read and write cycle incompatibilities described earlier. Read-modify-cycles are commonly used to "flip bits" in DRAM data tables and video memory. Given the flash memory usage model (read mostly, alter data infrequently), read-modify-write cycles to the 28F016XD will not occur in most applications.

Table 7 compares 28F016XD read-modify-write cycle specifications to DRAM, with incompatible specifications shaded for emphasis.

Table 6. 28F016XD Write Cycle Specifications Compared to 60 ns–70 ns 16-Mbit DRAM

Sym	Description	DRAM (3.3V)	28F016XD (3.3V)	DRAM (5.0V)	28F016XD (5.0V)
$t_{RC(W)}$	Random Write Cycle Time (min)	110 ns	90 ns	110–130 ns	75 ns
$t_{RAS(W)}$	RAS# Pulse Width (Writes) (min)	70 ns	80 ns	60–70 ns	65 ns
$t_{CAS(W)}$	CAS# Pulse Width (Writes) (min)	15 ns	65 ns	15–20 ns	50 ns
$t_{RCD(W)}$	RAS# to CAS# Delay Time (Writes) (min)	15 ns	15 ns	15 ns	15 ns
$t_{RSH(W)}$	RAS# Hold Time (Writes) (min)	15 ns	65 ns	15–20 ns	50 ns
$t_{CSH(W)}$	CAS# Hold Time (Writes) (min)	70 ns	80 ns	60–70 ns	65 ns
t_{WCS}	Write Command Set-Up Time (min)	0 ns	0 ns	0 ns	0 ns
t_{WCH}	Write Command Hold Time (min)	8–10 ns	15 ns	10–15 ns	15 ns
t_{WCR}	Write Command Hold Time Referenced to RAS# (min)	30–55 ns	30 ns	45 ns	30 ns
t_{WP}	Write Command Pulse Width (min)	15 ns	15 ns	15 ns	15 ns
t_{RWL}	Write Command to RAS# Lead Time (min)	15–20 ns	65 ns	15–20 ns	50 ns
t_{CWL}	Write Command to CAS# Lead Time (min)	15 ns	65 ns	15–20 ns	50 ns
t_{DS}	Data-In Set-Up Time (min)	0 ns	0 ns	0 ns	0 ns
t_{DH}	Data-In Hold Time (min)	10 ns	15 ns	10–15 ns	15 ns

Table 7. 28F016XD Read-Modify-Write Cycle Specifications Compared to 60 ns–70 ns 16-Mbit

Sym	Description	DRAM (3.3V)	28F016XD (3.3V)	DRAM (5.0V)	28F016XD (5.0V)
t_{RWC}	Read-Modify-Write Cycle Time	155–160 ns	200 ns	150–185 ns	175 ns
t_{CWD}	CAS# to WE# Delay Time	38–40 ns	70 ns	35–50 ns	65 ns
t_{AWD}	Column Address to WE# Delay Time	53–55 ns	105 ns	50–65 ns	100 ns
t_{OEH}	OE# Command Hold Time	0–15 ns	15 ns	15–20 ns	15 ns

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Fast Page Mode Cycle Specifications

28F016XD fast page mode cycle specification incompatibilities compared to DRAM have the same root causes as the read and write cycle incompatibilities described earlier. Fast page mode read-modify-write cycles to the 28F016XD will not occur in the majority of applications.

Table 8 compares 28F016XD fast page mode cycle specifications to DRAM, with incompatible specifications shaded for emphasis. Areas where the 28F016XD improves upon DRAM specifications are outlined in bold.

Refresh Cycle Specifications

Flash memory does not require refresh to retain stored data contents. However, by interfacing to a DRAM controller, it may automatically receive the same refresh cycles that DRAM receives. The 28F016XD supports all common refresh cycles; CAS#-before-RAS#, RAS#-only, hidden and self-refresh. In these modes, it will either drive or float the data bus just as a DRAM would. Refresh cycles have no other effect on 28F016XD stored data.

Table 9 compares 28F016XD refresh cycle specifications to DRAM, with incompatible specifications shaded for emphasis. Areas where the 28F016XD improves upon DRAM specifications are outlined in bold.

Table 8. 28F016XD Fast Page Mode Cycle Specifications Compared to 60 ns–70 ns 16-Mbit DRAM

Sym	Description	DRAM (3.3V)	28F016XD (3.3V)	DRAM (5.0V)	28F016XD (5.0V)
$t_{PC(R)}$	Fast Page Mode Cycle Time (Reads) (min)	35–45 ns	75 ns	35–45 ns	65 ns
$t_{PC(W)}$	Fast Page Mode Cycle Time (Writes) (min)	35–45 ns	80 ns	35–45 ns	65 ns
$t_{RASP(R)}$	RAS# Pulse Width (Reads) (min)	60–70 ns	95 ns	60 ns	85 ns
$t_{RASP(W)}$	RAS# Pulse Width (Writes) (min)	60–70 ns	80 ns	60 ns	65 ns
t_{CPA}	Access Time from CAS# Precharge (max)	35–40 ns	85 ns	35–40 ns	70 ns
t_{CPW}	WE# Delay Time from CAS# Precharge (min)	10 ns	0 ns	10 ns	0 ns
$t_{CPRH(R)}$	RAS# Hold Time from CAS# Precharge (reads) (min)	35 ns	75 ns	35–45 ns	65 ns
$t_{CPRH(W)}$	RAS# Hold Time from CAS# Precharge (writes) (min)	35 ns	80 ns	35–45 ns	65 ns
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time (min)	85 ns	170 ns	85–100 ns	145 ns

Table 9. 28F016XD Refresh Cycle Specifications Compared to 60 ns–70 ns 16-Mbit DRAM

Sym	Description	DRAM (3.3V)	28F016XD (3.3V)	DRAM (5.0V)	28F016XD (5.0V)
t_{CSR}	CAS# Set-Up Time (CAS#-before-RAS# Refresh) (min)	5 ns	10 ns	10 ns	10 ns
t_{CHR}	CAS# Hold Time (CAS#-before-RAS# Refresh) (min)	10–15 ns	10 ns	10–20 ns	10 ns
t_{WRP}	WE# Set-Up Time (CAS#-before-RAS# Refresh) (min)	10 ns	10 ns	10 ns	10 ns
t_{WRH}	WE# Hold Time (CAS#-before-RAS# Refresh) (min)	15 ns	10 ns	10–15 ns	10 ns
t_{RPC}	RAS# Precharge to CAS# Hold Time (min)	5 ns	10 ns	0–10 ns	10 ns
t_{RASS}	RAS# Pulse Width (Self-Refresh Mode) (min)	100 µs	0 ns	100 µs	0 ns
t_{RPS}	RAS# Precharge Time (Self-Refresh Mode) (min)	40 ns	10 ns	40–50 ns	10 ns
t_{CPN}	CAS# Precharge Time (Self-Refresh Mode) (min)	10 ns	10 ns	10 ns	10 ns
t_{CHS}	CAS# Hold Time (Self-Refresh Mode) (min)	600 ns	0 ns	600 ns	0 ns
t_{REF}	Refresh Period (max)	16 ms	∞	16 ms	∞

Miscellaneous Specifications

The 28F016XD documentation contains timing specifications not found in DRAM datasheets. These timings relate to the 28F016XD's additional control inputs/outputs and voltages (3/5#, WP#, RP#, RY/BY#, V_{PP}) as well as minimum data write and erase durations. Tables 10 and 11 show these additional specifications, at 3.3V V_{CC} and 5.0V V_{CC} respectively.

Table 10. 28F016XD Added/Revised AC Timings

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Versions	28F016XD - 95		
Parameter	**Min**	**Max**	**Unit**
RP# High to RAS# Going Low	480		ns
RP# Set-Up to WE# Going Low	480		ns
V_{PP} Set-Up to CAS# High at End of Write Cycle	100		ns
CAS# High to RY/BY# Going Low		100	ns
RP# Hold from Valid Status Register Data and RY/BY# High	0		ns
V_{PP} Hold from Valid Status Register Data and RY/BY# High	0		ns
RP# Low to 3/5# High (t_{PLYH})	0		µs
3/5# High to RP# High (t_{YHPH})	2		µs
RP# Low to V_{CC} at 3.0V (min) or 3.6V (max) (t_{PL3V})	0		µs

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Table 10. 28F016XD Added/Revised AC Timings (Continued)

V_{CC} = 3.3V ± 0.3V, V_{PP} = 5.0V ± 0.5V, T_A = 0°C to +70°C

Sym	Parameter	Min	Typ	Max	Units
$t_{WHRH}1$	Word Write Time	TBD	35	TBD	µs
$t_{WHRH}3$	Block Write Time	TBD	1.2	TBD	sec
	Block Erase Time	TBD	1.4	TBD	sec
	Erase Suspend Latency Time to Read	1.0	12	75	µs

V_{CC} = 3.3V ± 0.3V, V_{PP} = 12.0V ± 0.6V, T_A = 0°C to +70°C

Sym	Parameter	Min	Typ	Max	Units
$t_{WHRH}1$	Word Write Time	5	9	TBD	µs
$t_{WHRH}3$	Block Write Time	TBD	0.3	1.0	sec
	Block Erase Time	0.3	0.8	10	sec
	Erase Suspend Latency Time to Read	1.0	9	55	µs

Table 11. 28F016XD Added/Revised AC Timings

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to +70°C

Versions	28F016XD - 85		
Parameter	**Min**	**Max**	**Unit**
RP# High to RAS# Going Low	300		ns
RP# Set-Up to WE# Going Low	300		ns
V_{PP} Set-Up to CAS# High at End of Write Cycle	100		ns
CAS# High to RY/BY# Going Low		100	ns
RP# Hold from Valid Status Register Data and RY/BY# High	0		ns
V_{PP} Hold from Valid Status Register Data and RY/BY# High	0		ns
RP# Low to 3/5# Low (t_{PLYL})	0		µs
3/5# Low to RP# High (t_{YLPH})	2		µs
RP# Low to V_{CC} at 4.5V (min) (t_{PL5V})	0		µs

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Table 11. 28F016XD Added/Revised AC Timings (Continued)

V_{CC} = 5.0V ± 0.5V, V_{PP} = 5.0V ± 0.5V, T_A = 0°C to +70°C

Sym	Parameter	Min	Typ	Max	Units
$t_{WHRH}1$	Word Write Time	TBD	25	TBD	µs
$t_{WHRH}3$	Block Write Time	TBD	0.85	TBD	sec
	Block Erase Time	TBD	1.0	TBD	sec
	Erase Suspend Latency Time to Read	1.0	9	55	µs

V_{CC} = 5.0V ± 0.5V, V_{PP} = 12.0V ± 0.6V, T_A = 0°C to +70°C

Sym	Parameter	Min	Typ	Max	Units
$t_{WHRH}1$	Word Write Time	4.5	6	TBD	µs
$t_{WHRH}3$	Block Write Time	TBD	0.2	1.0	sec
	Block Erase Time	0.3	0.6	10	sec
	Erase Suspend Latency Time to Read	1.0	7	40	µs

2.3 Package and Pinout

Although the 28F016XD includes all necessary inputs and outputs for interfacing to DRAM controllers, its pinout and package do not match those of DRAMs but instead evolve from other 16-Mbit Intel flash memories. The 28F016XD uses a 56-lead TSOP package, with pinout shown in Figure 1 and package dimensions shown in Figure 2.

Comparable 1M x 16 (16-Mbit) DRAMs use two packages, a 42-lead SOJ and 44-lead TSOP. Examples of these DRAM pinouts are shown in Figures 3 and 4.

Table 12 summarizes pinout comparisons between the 28F016XD in 56-lead TSOP and various DRAM package options.

If compatibility between the 28F016XD and DRAM "footprints" is desired, 28F016XD flash memories can be placed on DRAM-compatible SIMMs. Please see the Additional Information section of this application note for documentation that covers this topic in more detail.

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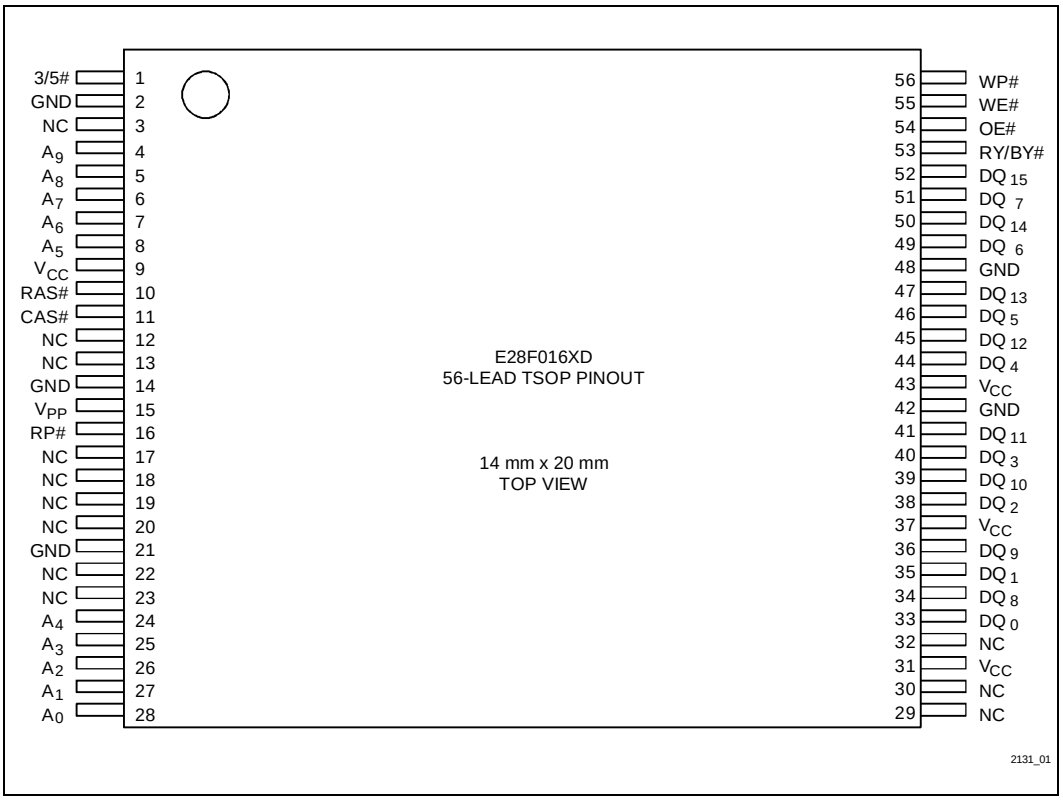

Figure 1. 28F016XD 56-Lead TSOP Type I Pinout Configuration

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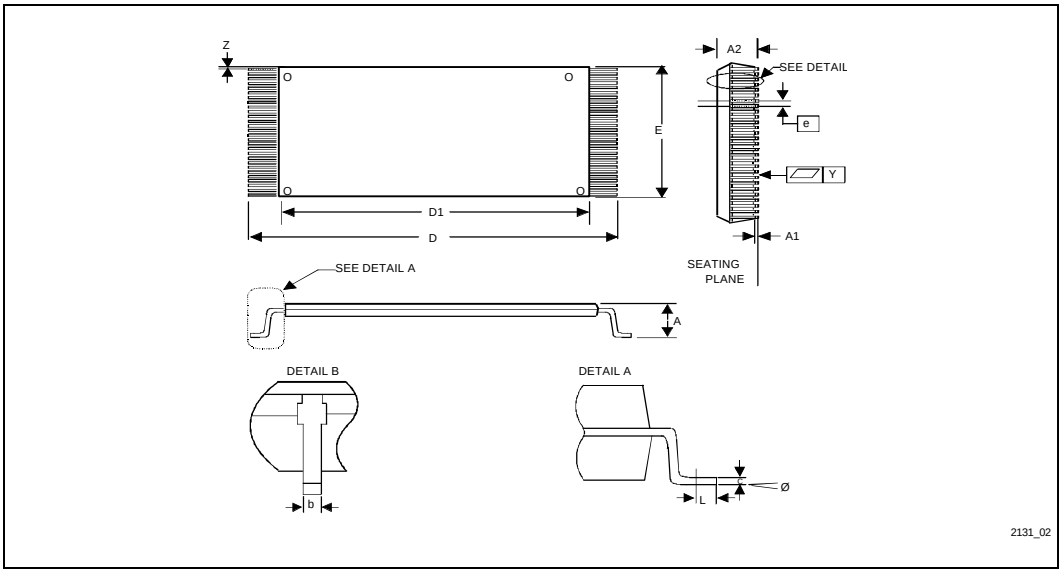

Figure 2. 28F016XD 56-Lead TSOP Type I Package Dimensions

Family: Thin Small Out-Line Package				
Symbol	**Millimeters**			
	Minimum	**Nominal**	**Maximum**	**Notes**
A			1.20	
A_1	0.050			
A_2	0.965	0.995	1.025	
b	0.100	0.150	0.200	
c	0.115	0.125	0.135	
D_1	18.20	18.40	18.60	
E	13.80	14.00	14.20	
e		0.50		
D	19.80	20.00	20.20	
L	0.500	0.600	0.700	
N		56		
∅	0°	3°	5°	
Y			0.100	
Z	0.150	0.250	0.350	

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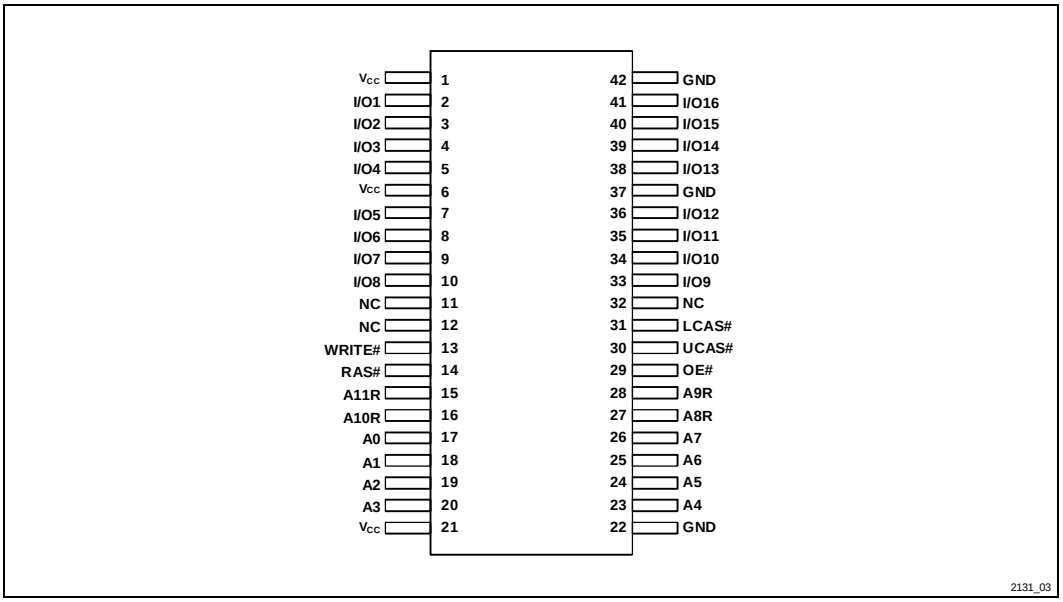

Figure 3. 16-Mbit DRAM 42-Lead SOJ Pinout Configuration

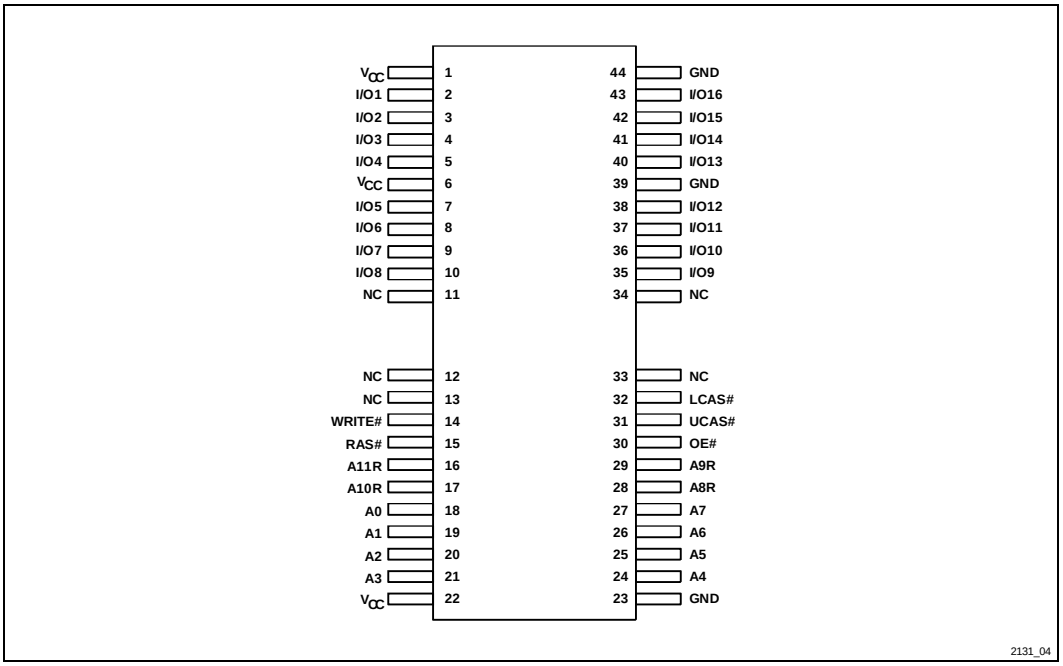

Figure 4. 16-Mbit DRAM 44-Lead TSOP Pinout Configuration

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Table 12. 28F016XD Pinout Compared to 16-Mbit DRAM

Pin Name	42-Lead SOJ DRAM Pin Number	44-Lead TSOP DRAM Pin Number	56-Lead TSOP 28F016XD Pin Number
V_{CC}	1, 6, 21	1, 6, 22	9,31,37,43
V_{PP}	—	—	15
GND	22, 37, 42	23, 39, 44	2, 14, 21, 42, 48
DQ_0	2	2	33
DQ_1	3	3	35
DQ_2	4	4	38
DQ_3	5	5	40
DQ_4	7	7	44
DQ_5	8	8	46
DQ_6	9	9	49
DQ_7	10	10	51
DQ_8	33	35	34
DQ_9	34	36	36
DQ_{10}	35	37	39
DQ_{11}	36	38	41
DQ_{12}	38	40	45
DQ_{13}	39	41	47
DQ_{14}	40	42	50
DQ_{15}	41	43	52
A_0	17	18	28
A_1	18	19	27
A_2	19	20	26
A_3	20	21	25
A_4	23	24	24
A_5	24	25	8
A_6	25	26	7
A_7	26	27	6
A_8	27	28	5
A_9	28	29	4
WE#	13	14	55

ADVANCE INFORMATION

Table 12. 28F016XD Pinout Compared to 16-Mbit DRAM (Continued)

Pin Name	42-Lead SOJ DRAM Pin Number	44-Lead TSOP DRAM Pin Number	56-Lead TSOP 28F016XD Pin Number
OE#	29	30	54
RAS#	14	15	10
CAS#	—	—	11
CASL#	31	32	—
CASH#	30	31	—
RP#	—	—	16
RY/BY#	—	—	53
WP#	—	—	55
3/5#	—	—	1
NC	11, 12, 15, 16, 32	11, 12, 13, 33, 34	3, 12, 13, 17, 18, 19, 20, 22, 23, 29, 30, 32

2.4 Capacitance

28F016XD input/output capacitance specifications compared to 16-Mbit DRAMs are shown in Table 13.

3.0 28F016XD INTERFACING TO DRAM CONTROLLERS

Section 2.0 identified areas of compatibility and incompatibility between the 28F016XD and DRAMs. This section, on the other hand, discusses how to determine the 28F016XD's ability to interface with an already-designed DRAM controller. Section 3.0 is divided into three topics:

- Configurable Specification Interfacing
- Non-Configurable Specification Interfacing
- Additional 28F016XD Interface Hardware

Figure 5 shows an example interface between the 28F016XD and system CPU via a standard DRAM controller. This interface diagram will be used in the example calculations to follow. The DRAM controller provides no RD# output, so the 28F016XD's OE# input is grounded. CAS# low in conjunction with active WR# is decoded as a write, overriding OE#. Parity is disabled within the DRAM controller (at least for the banks in which the 28F016XD resides).

Note that data buffering is done by the DRAM controller itself. In designs that do not provide this capability or in very high chip count arrays, transceivers can be used to minimize CPU local bus or DRAM bus loading by the DRAM/28F016XD memory subsystem. When determining the need for isolation transceivers, keep in mind that the 28F016XD input and output capacitance are higher than those for comparable DRAM (as explained in Section 2.4).

Table 13. 28F016XD Capacitance Specifications Compared to 16-Mbit DRAM

Symbol	Description	DRAM (3.3V)	28F016XD (3.3V)	DRAM (5.0V)	28F016XD (5.0V)
C_{IN}	Capacitance Looking into an Address Pin	5 pF	8 pF	5-6 pF	8 pF
C_{CTRL}	Capacitance Looking into a Control Pin	7 pF	8 pF	7 pF	8 pF
C_{OUT}	Capacitance Looking into an Output Pin	7 pF	12 pF	7-10 pF	12 pF

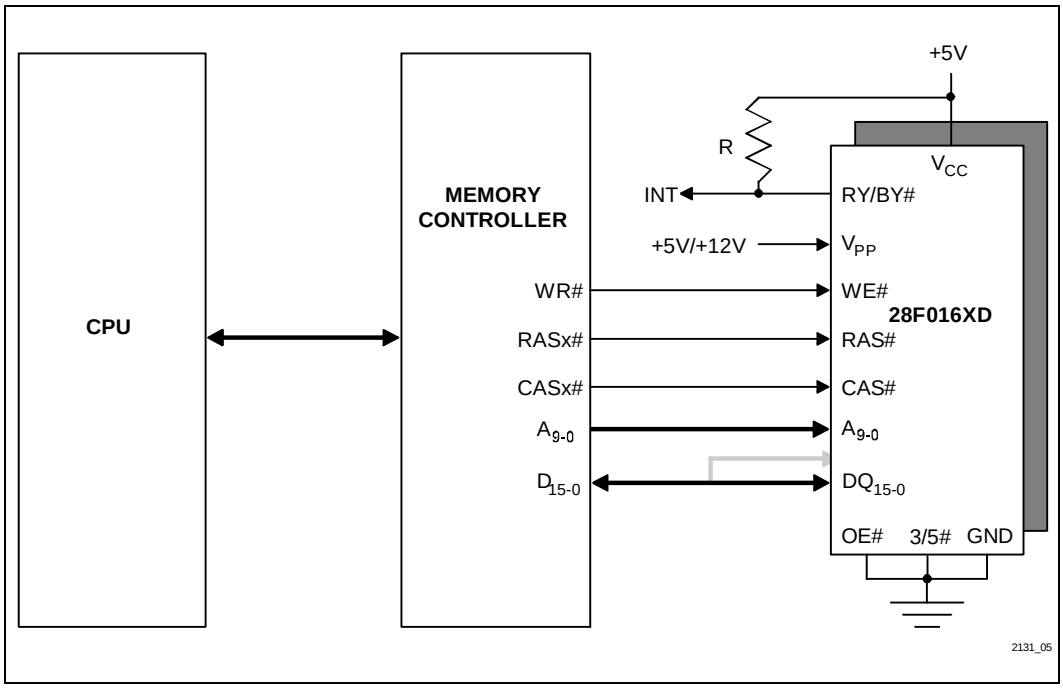

Figure 5. Example DRAM Controller Interface to the 28F016XD

Please reference Figures 6 and 7 for example DRAM controller waveforms, which will also be used in calculations to follow. These diagrams show timings for a 1x-clock driven (i.e., 25 or 33 MHz) system. For a 2x-clock driven (i.e., 50 or 66 MHz) DRAM controller waveform, the main difference is in the clock period shown; CLK is halved within the DRAM controller to generate its signals. The X-Y-Y-Y format shows how many 1x or 2x clock cycles are used for the first data access (including RAS# transitions) and subsequent accesses (toggling CAS# in fast page mode).

The examples assume that both minimum and maximum delays after CLK edges are provided for RAS#, CAS# and addresses. If minimum delays are not given in DRAM controller documentation, contact the vendor for more information. Alternatively, a 0 ns delay can be assumed, although this may impact interface to the 28F016XD.

X-Y-Y-Y wait-state formats are often shown in conjunction with a clock frequency (i.e., 4-2-2-2 at 33 MHz) in DRAM controller datasheets. This does not mean that this wait-state setting is unique to the CLK shown; wait-state settings are frequency-independent from the DRAM controller point of view. The wait-state format/clock frequency combination simply indicates a standard DRAM speed bin setting (i.e., 60 or 70 ns DRAM). For DRAM controllers with minimal flexibility in wait-state configuration, the 28F016XD may still be interface-compatible, albeit at a slower frequency.

The following sections will make the assumptions listed below:

- The DRAM controller will not generate read-modify-write cycles to the 28F016XD.
- Only areas in which 28F016XD specifications exceed those for DRAM will be discussed. Compatibility is assumed when 28F016XD specifications match or improve upon DRAM specifications.
- Signal transition times (rise and fall) will not be included in example calculations.

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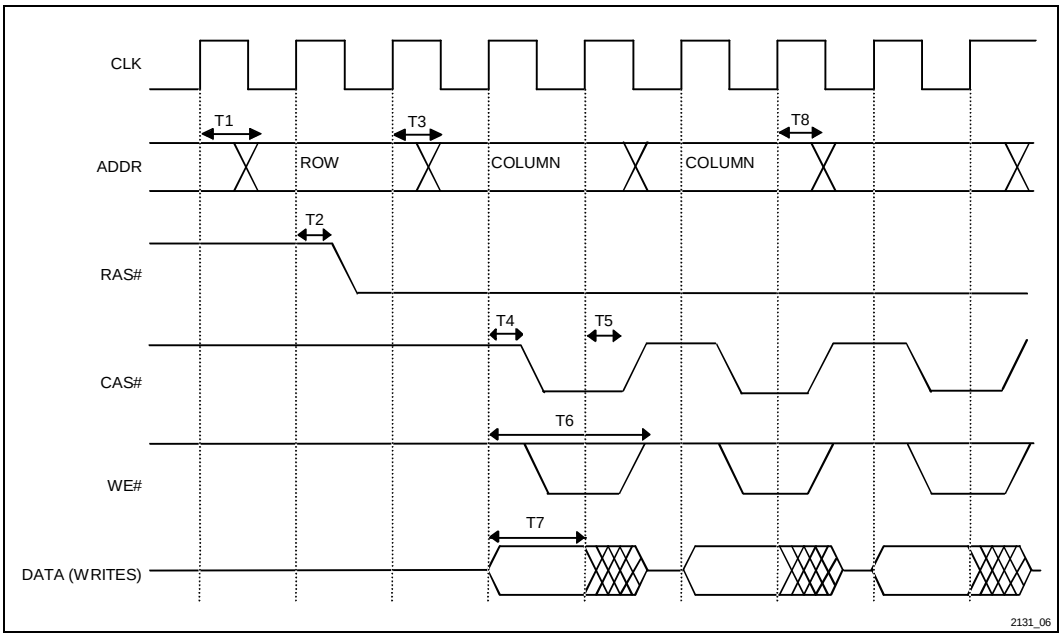

Figure 6. 4-2-2-2 Fast Page Mode DRAM Controller Sequence

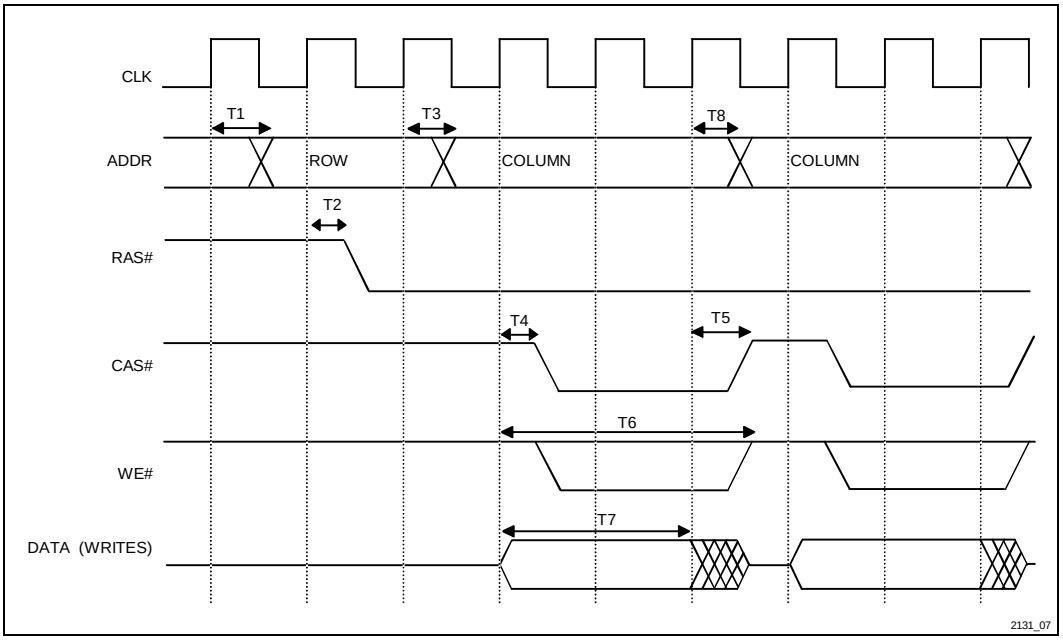

Figure 7. 5-3-3-3 Fast Page Mode DRAM Controller Sequence

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3.1 Configurable Specification Interfacing

Many 28F016XD specification incompatibilities (with respect to DRAM) can be resolved by programming the DRAM controller for additional wait-states. Most DRAM controllers have a programmable CAS# low time (and some can be programmed with different settings for reads and writes). Additionally, some DRAM controllers also allow the RAS#-to-CAS# delay to be programmed. Both of these settings automatically extend the RAS# low time.

Focus on the following specifications when determining proper DRAM controller configuration for the 28F016XD. With the exception of specifications discussed in Section 3.2, all other specification incompatibilities between the 28F016XD and DRAM will be satisfied if these four requirements are met:

t_{CAC}

This specification gives the timing delay from CAS# active to valid data during memory reads. When calculating the required t_{CAC} setting needed to interface the 28F016XD to the system CPU, include not only the raw memory access time but also the propagation delay of the DRAM controller buffers or transceiver logic, and the data set-up time to CLK of the CPU.

The example shows that at 33 MHz, a 5-3-3-3 DRAM controller setting will accommodate the 28F016XD t_{CAC} access time, buffer/transceiver propagation delay and CPU set-up time requirements.

Example:
t_4 = 5 ns (max)
t_{CLK} = 30 ns (33 MHz CLK)
t_{PROP} = 8 ns (max)
t_{SETUP} = 2 ns (min)
t_{CAC} (required) = (t_{CLK} - t_4) - t_{PROP} - t_{SETUP} + (wait-states)

DRAM Controller t_{CAC} Requirement (4-2-2-2)	DRAM Controller t_{CAC} Requirement (5-3-3-3)	28F016XD t_{CAC} Specification (5.0V V_{CC})	28F016XD t_{CAC} Specification (3.3V V_{CC})
15 ns	45 ns	35 ns	40 ns

t_{AA}

This specification gives the timing delay from column address stable to valid data during memory reads. The 28F016XD is an enhanced fast page mode memory; a read access begins when column address is stable versus waiting to begin until CAS# transitions low. DRAM controllers that can provide a stable address in advance of CAS#'s active transition will interface to the 28F016XD with minimal additional wait-states.

The example shows that at 33 MHz, a 5-3-3-3 DRAM controller setting will accommodate the 28F016XD t_{AA} access time, buffer/transceiver propagation delay and CPU set-up time requirements.

Example:
t_3 = 5 ns (max)
t_{CLK} = 30 ns (33 MHz CLK)
t_{PROP} = 8 ns (max)
t_{SETUP} = 2 ns (min)
t_{AA} (required) = (t_{CLK} + t_{CLK} - t_3) - t_{PROP} - t_{SETUP} + (wait-states)

DRAM Controller t_{AA} Requirement (4-2-2-2)	DRAM Controller t_{AA} Requirement (5-3-3-3)	28F016XD t_{AA} Specification (5.0V V_{CC})	28F016XD t_{AA} Specification (3.3V V_{CC})
45 ns	75 ns	65 ns	75 ns

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t_{RAC}

This specification gives the timing delay from RAS# active to valid data during memory reads.

The example shows that at 33 MHz, a 5-3-3-3 DRAM controller setting will accommodate the 28F016XD t_{RAC} access time, buffer/transceiver propagation delay and CPU set-up time requirements.

Example:
t_2 = 5 ns (max)
t_{CLK} = 30 ns (33 MHz CLK)
t_{PROP} = 8 ns (max)
t_{SETUP} = 2 ns (min)
t_{RAC} (required) = (t_{CLK} + t_{CLK} + t_{CLK} - t_2) - t_{PROP} - t_{SETUP} + (wait-)

DRAM Controller t_{RAC} Requirement (4-2-2-2)	DRAM Controller t_{RAC} Requirement (5-3-3-3)	28F016XD t_{RAC} Specification (5.0V V_{CC})	28F016XD t_{RAC} Specification (3.3V V_{CC})
75 ns	105 ns	85 ns	95 ns

$t_{CAS(W)}$

This specification defines the minimum CAS#-active time required to successfully write a command to the 28F016XD.

The example shows that at 33 MHz, a 5-3-3-3 DRAM controller setting will accommodate the 28F016XD $t_{CAS(W)}$ time at 5.0V V_{CC}, but that a 6-4-4-4 setting or lower CLK frequency will be required at 3.3V V_{CC}.

Example:
t_4 = 5 ns (max)
t_5 = 2 ns (min)
t_{CLK} = 30 ns (33 MHz CLK)
$t_{CAS(W)}$ (required) = (t_{CLK} + t_5 - t_4) + (wait-states)

DRAM Controller $t_{CAS(W)}$ Requirement (4-2-2-2)	DRAM Controller $t_{CAS(W)}$ Requirement (5-3-3-3)	28F016XD $t_{CAS(W)}$ Specification (5.0V V_{CC})	28F016XD $t_{CAS(W)}$ Specification (3.3V V_{CC})
27 ns	57 ns	50 ns	65 ns

3.2 Non-Configurable Specification Interfacing

Some 28F016XD specification incompatibilities (with respect to DRAM) cannot be resolved by configuring DRAM controller wait-states. Determining DRAM controller compatibility with these specifications is crucial for ensuring the ability to interface to the 28F016XD.

Focus on the following non-configurable specifications when determining proper DRAM controller configuration for 28F016XD. In combination with the configurable specifications discussed in Section 3.1, all other specification incompatibilities between the 28F016XD and DRAM will be satisfied if these requirements are met:

t_{CAH}

This specification describes the minimum column address hold after CAS# active transitions.

In this example, the 28F016XD successfully interfaces to the DRAM controller.

Example:
t_4 = 5 ns (max)
t_8 = 2 ns (min)
t_{CLK} = 30 ns (33 MHz CLK)
t_{CAH} (required) = $t_{CLK} + t_8 - t_4$

DRAM Controller t_{CAH} Requirement	28F016XD t_{CAH} Specification (5.0V V_{CC})	28F016XD t_{CAH} Specification (3.3V V_{CC})
27 ns	20 ns	20 ns

t_{CP}

This specification describes the minimum CAS#-high (inactive) time requirement between consecutive accesses to the 28F016XD.

In this example, the 28F016XD successfully interfaces to the DRAM controller.

Example:
t_4 = 2 ns (min)
t_5 = 5 ns (max)
t_{CLK} = 30 ns (33 MHz CLK)
t_{CP} (required) = $t_{CLK} + t_4 - t_5$

DRAM Controller t_{CP} Requirement	28F016XD t_{CP} Specification (5.0V V_{CC})	28F016XD t_{CP} Specification (3.3V V_{CC})
27 ns	15 ns	15 ns

t_{CRP}

This specification describes the minimum CAS#-high (inactive) to RAS#-low (active) precharge time requirement between consecutive accesses to the 28F016XD.

In this example, the 28F016XD successfully interfaces to the DRAM controller.

Example:
t_2 = 2 ns (min)
t_5 = 5 ns (max)
t_{CLK} = 30 ns (33 MHz CLK)
t_{CRP} (required) = $t_{CLK} + t_2 - t_5$

DRAM Controller t_{CRP} Requirement	28F016XD t_{CRP} Specification (5.0V V_{CC})	28F016XD t_{CRP} Specification (3.3V V_{CC})
27 ns	10 ns	10 ns

t_{RAH}

This specification describes the minimum row address hold after RAS# active transitions.

In this example, the 28F016XD successfully interfaces to the DRAM controller.

Example:
t_2 = 5 ns (max)
t_3 = 2 ns (min)
t_{CLK} = 30 ns (33 MHz CLK)
t_{RAH} (required) = t_{CLK} + t_3 - t_2

DRAM Controller t_{RAH} Requirement	28F016XD t_{RAH} Specification (5.0V V_{CC})	28F016XD t_{RAH} Specification (3.3V V_{CC})
27 ns	15 ns	15 ns

t_{WCH}

This specification defines the minimum WE# hold time after CAS# active transitions. The vast majority of DRAM controllers will hold WE# active throughout the CAS#-low interval, automatically satisfying t_{WCH}. For those that do not, the example below shows how to calculate the timing relationship between CAS# and WE#. When determining specification t_6, ensure that it is being specified from the same CLK edge as t_4, or add appropriate t_{CLK} periods to adjust t_6 appropriately.

In this example, the 28F016XD successfully interfaces to the DRAM controller.

Example:
t_4 = 5 ns (max)
t_6 = 20 ns (min)
t_{CLK} = 30 ns (33 MHz CLK)
t_{WCH} (required) = t_6 - t_4

DRAM Controller t_{WCH} Requirement	28F016XD t_{WCH} Specification (5.0V V_{CC})	28F016XD t_{WCH} Specification (3.3V V_{CC})
15 ns	15 ns	15 ns

t_{DH}

This specification defines the minimum data hold time after CAS# active transitions. The example below shows how to calculate the timing relationship between CAS# and WE#. When determining specification t_7, ensure that it is being specified from the same CLK edge as t_4, or add appropriate t_{CLK} periods to adjust t_7 appropriately.

In this example, the 28F016XD successfully interfaces to the DRAM controller.

Example:
t_4 = 5 ns (max)
t_7 = 20 ns (min)
t_{CLK} = 30 ns (33 MHz CLK)
t_{DH} (required) = t_7 - t_4

DRAM Controller t_{DH} Requirement	28F016XD t_{DH} Specification (5.0V V_{CC})	28F016XD t_{DH} Specification (3.3V V_{CC})
15 ns	15 ns	15 ns

t_{RCS}

This specification describes the minimum WE# inactive setup time to CAS# for reads.

Most DRAM controllers available today include a RD# output and support early write cycles. In these cases, WE# is transitioned inactive within a write, as soon as CAS# is activated “low,” or at the conclusion of a write. This guarantees that WE# will be inactive “high” in advance of subsequent reads.

t_{OFF}, t_{OEZ} and t_{CDD}

t_{OFF} specifies the maximum delay from CAS# inactive until the 28F016XD outputs transition to high-Z. t_{OEZ} is similar, and specifies delay from OE# inactive. t_{CDD} specifies the minimum delay from CAS# inactive until the DRAM controller can drive the data bus (for writes to memory). These specifications are closely related to each other.

The simplest method of ensuring that system designs accommodate these specifications is to insert a software delay between a read from the 28F016XD and a write to memory in the same bank. This gives the 28F016XD adequate time to disable its outputs and avoids data bus contention. Alternatively, transceivers (with faster output float times) can be placed between 28F016XD data outputs and the DRAM controller data bus.

ADVANCE INFORMATION

3.3 Additional Circuitry Required to Interface to the 28F016XD

A properly-designed system requires minimal circuitry beyond the DRAM controller to interface to the 28F016XD. The following sections discuss this circuitry, much of which is optional.

V_{PP} Generation

As discussed in Section 2.1, the 28F016XD requires a V_{PP} voltage for Data Write and Erase operations. Valid V_{PP} voltage ranges are 5.0V ± 10% ($V_{PPH}1$) and 12.0V ± 5% ($V_{PPH}2$). In a 5.0V system design, the V_{PP} voltage can be supplied by the same power supply that provides V_{CC} and switched for write protection purposes. Alternatively, Figure 8 shows an example circuit that generates 12.0V from a 5.0V or 3.3V input.

See the Additional Information section of this document for information on AP-357, which covers the topic of 12.0V generation in greater detail.

RP# Input

RP# (Reset/Power-Down) has several functions:

- Resets internal automation
- Transitions the 28F016XD to deep power-down mode
- Provides write protection during system power transitions

Circuitry like that shown in Figure 9 should be used to control RP#. Application Note AP-374 covers the topic of flash memory write protection in great detail; see the Additional Information section of this document. GPIO general purpose input/output (for power management) and system RESET# control are optional depending on application.

WP# Input

WP# allows selective lock of blocks within the 28F016XD to prevent unwanted data alteration. If this functionality is desired, it can be implemented via GPIO control. Otherwise, WP# can be disabled by connecting it to V_{CC}.

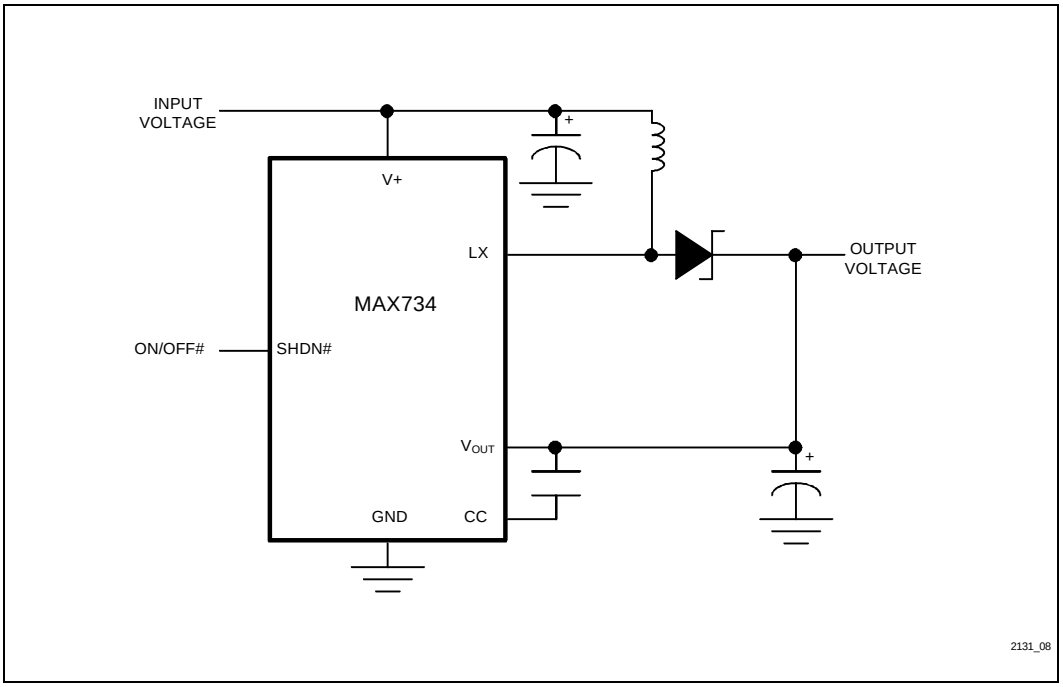

Figure 8. 12.0V Converter with Integrated Switch

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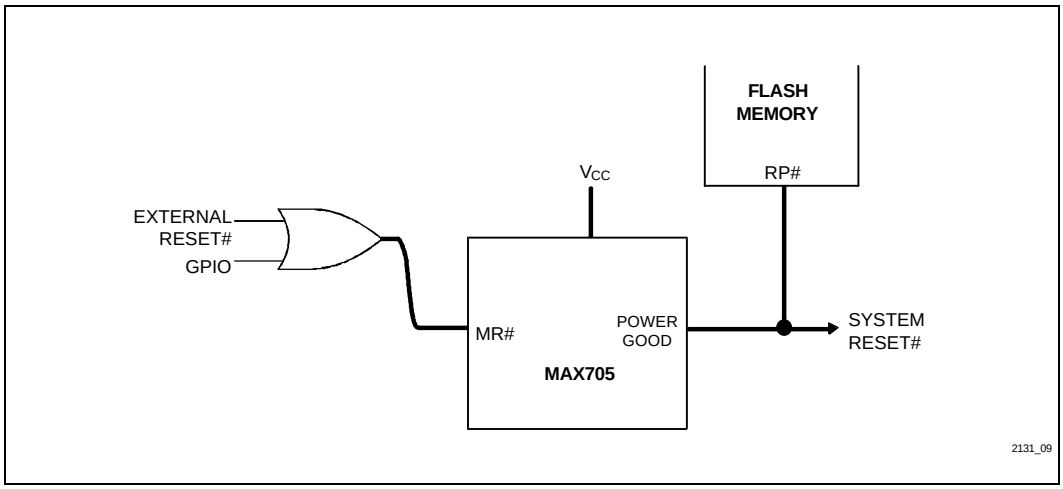

Figure 9. RP# Control for the 28F016XD

RY/BY# Output

RY/BY# provides hardware indication of the status of internal 28F016XD automation, and can be connected to a system interrupt input if desired. Alternatively, the 28F016XD Status Registers provide identical information and can be read by system software to determine completion of Data Write and/or Erase.

Parity

The 28F016XD, unlike some DRAMs, does not provide parity information. If parity is required for the DRAM subsystem and the DRAM controller provides only global parity enable/disable (or requires parity), external circuitry such as a PAL or dedicated logic chip can supply parity bits during 28F016XD reads. See Figure 10 for an example.

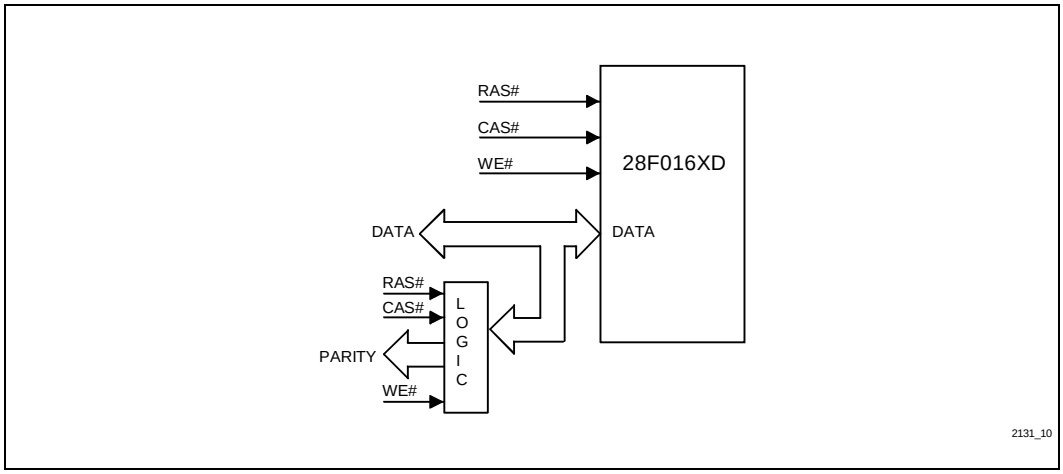

Figure 10. External Parity Generation

ADVANCE INFORMATION

4.0 DESIGNING 28F016XD COMPATIBILITY AND OPTIMIZATION INTO DRAM CONTROLLERS

Timing Analysis

Section 2.2 discussed areas of timing incompatibility between the 28F016XD and 16-Mbit DRAMs. DRAM controllers should provide a range of wait-state configurations to ensure that they operate with the 28F016XD at all required CLK frequencies. Additionally, the non-configurable specifications of Section 3.2 should be closely reviewed. Finally, for reads, DRAM controllers that provide the column address in advance of CAS# will interface to the 28F016XD with a minimum of additional wait-states.

Per-Bank Parity and Wait-State Control

The 28F016XD is not subject to the same alpha particle "soft errors" that affect DRAM, so it does not provide parity data bits. If parity checking is desired for the DRAM subsystem, per-bank parity control allows the 28F016XD and DRAM to be placed in separate controller banks. Parity can be enabled for those banks containing DRAM and disabled for banks containing the 28F016XD.

Section 2.2 also revealed that read and write timings for the 28F016XD are slower than those for DRAM at high CLK frequencies. Per-bank wait-state control allows the 28F016XD and DRAM to be placed in separate banks and individually configured to optimize performance of each.

Fast RAS# Precharge

The 28F016XD does not require precharge between accesses when RAS# is toggled. Therefore, its t_{RP} (RAS# precharge time) specification is much shorter than that required for DRAM (10 ns for the 28F016XD vs. 40–50 ns for DRAM). A DRAM controller with configurable RAS# precharge delay can exploit this 28F016XD advantage.

Refresh Disable

The 28F016XD also does not require refresh to retain stored data contents. Per-bank refresh enable/disable or refresh enable/disable on an address range basis will eliminate unnecessary cycles to the 28F016XD, optimizing performance and lowering power consumption.

5.0 CONCLUSION

This application note has discussed comparisons between the 28F016XD and DRAM, compatibility between the 28F016XD and DRAM controllers, and optimization of new DRAM controllers for the 28F016XD. Consult reference documentation for a more complete understanding of compatibility and device capabilities. Please contact your local Intel or distribution sales office for more information on Intel's flash memory products.

6.0 ADDITIONAL INFORMATION

6.1 References

Order Number	Document/Tool
290533	28F016XD DRAM-Interface Flash Memory Datasheet
297372	"16-Mbit Flash Product Family User's Manual"
292092	AP-357 "Power Supply Solutions for Flash Memory"
292123	AP-374 "Flash Memory Write Protection Techniques"
292163	AP-610 "Flash Memory In-System Code and Data Update Techniques"
292168	AP-614 "Adapting DRAM Based Designs for the 28F016XD"
292152	AB-58 "28F016XD-Based SIMM Designs"
292165	AB-62 "Compiling Optimized Code for Flash Memories"
297508	FLASHBuilder Utility
Contact Intel/Distribution Sales Office	28F016XD Benchmark Utility
Contact Intel/Distribution Sales Office	28F016XD iBIS Models
Contact Intel/Distribution Sales Office	28F016XD VHDL Models
Contact Intel/Distribution Sales Office	28F016XD Timing Designer Library Files
Contact Intel/Distribution Sales Office	28F016XD Orcad and ViewLogic Schematic Symbols

ADVANCE INFORMATION

6.2 Revision History

Number	Description
001	Original Version
002	Increased I_{PPS} (V_{PP} Read Current) for $V_{PP} > V_{CC}$ to 200 µA at V_{CC} = 3.3/5.0V Corrected "RP# High to RAS# Going Low" to be a "Min" specification at V_{CC} = 3.3/5.0V, in Tables 10 and 11 Removed "Page Buffer Word Write Time" and "Full Chip Erase Time" specifications from Tables 10 and 11 Increased Typical "Word/Block Write Times" (t_{WHR1}/t_{WHR3}) for V_{PP} = 5.0V Tables 10 and 11 t_{WHR1} from 24.0 µs to 35.0 µs and t_{WHR3} from 0.8 sec to 1.2 sec at V_{CC} = 3.3V t_{WHR1} from 10.6 µs to 25.0 µs and t_{WHR3} from 0.6 sec to 0.85 sec at V_{CC} = 5.0V Added "Erase Suspend Latency Time to Read" specification to Tables 10 and 11 Minor cosmetic changes throughout document
003	Corrected Introduction to indicate "3.3V or 5V V_{CC} Operation" Added 3/5# pin to: Test Conditions of $I_{CC}2/I_{CC}5$ Specifications, Miscellaneous Specifications section, Pinout Configuration (Figure 1), Pinout Comparison (Table 12) and DRAM Controller Interface Example (Figure 5). Modified test conditions for I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} in Tables 2 and 3 to include "Address Valid/Static throughout Cycle." Modified Tables 10 and 11 to include 3/5# pin: Removed V_{CC} at 3.0V/4.5V (min) to RP# high specifications; Added t_{PLYL}/t_{PLYH}, t_{YLPH}/t_{YHPH} and t_{PL5V}/t_{PL3V} specifications. Changed "WE# High to RY/BY# Going Low" specification name to "CAS# High to RY/BY# Going Low" in Tables 10 and 11. Corrected TSOP Mechanical Specification A1 from 0.50 mm to 0.050 mm Corrected WP# in Pinout Comparison (Table 12) to be pin 56 on 28F016XD device Removed pin 1 on 28F016XD from NC in Pinout Comparison (Table 12) Corrected t_{OEX} references in Section 3.2 to t_{OEZ} Updated Additional Information Section Minor cosmetic changes throughout document

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