AP-623

APPLICATION NOTE

Multi-Site Layout Planning with Intel's Boot Block Flash Memory

December 1996

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APPENDIX A: Additional Information

REVISION HISTORY

Number	Description
-001	Original version
-002	Added previously omitted PDIP layouts; made textual corrections
-003	Added 1/2M bulk (32-L PLCC) to Boot Block (40-L TSOP) layouts Added 1M Boot Block (32-L PDIP) to 2M Boot Block (40-L PDIP) layout Added 2M Boot Block (40-L PDIP) to 2/4/8M Boot Block (40-L TSOP) layout Added 2/4M Boot Block (48-L TSOP) to 2/4M Boot Block (56-L TSOP) layout Added AMD 29Fx00 flash (48-L TSOP) to Intel 2/4/8M Boot Block (48-L TSOP) Added Sharp LH28Fx00 flash (56-L TSOP) to Intel 2/4/8M Boot Block (48-L TSOP)

1.0 INTRODUCTION

Flash memory has become an integral part of today's design environment. It spans a gamut of applications, from industrial products to household items. Flash memory can be found in point-of-sale terminals and barcode scanners; closer to home, flash memory is an important part of many cellular phones as well as personal computers. With so many uses, it is no wonder flash memory comes in so many different flavors and sizes.

With so many choices available on the market today, design engineers are placed in the precarious position of having to choose the best technological fit for their application while maintaining enough flexibility to permit real-time changes to accommodate market requirements. For example, the pinout and package offerings from one manufacturer may not necessarily be compatible with those of another.

This application note provides a means for designers to build in flexibility without sacrificing technology or exposing themselves to undue risk. This application note focuses on compatible layouts between Intel's Boot Block products (for upgrading from one density or package to another) as well as layouts that support multiple vendors flash memory offerings. This is not meant to be an exhaustive list by any means; rather it is intended as an illustration of how careful planning during the design stages of a product can provide additional flexibility at critical junctures when changes are required. All the layouts cited in this document are available on Intel's bulletin board system (BBS) and World Wide Web page.

2.0 INTEL'S BOOT BLOCK FLASH MEMORY

Due to the vast array of uses flash memory encompasses, it is difficult to cover the entire scope of flexible layout strategies for all available flash memory. Instead, this application note focuses on a subset of this large group: Boot Block flash memory. Boot Block flash memory is an asymmetrically-blocked architecture (see Figure 1) that ranges in density from 1- Mbit (128K x 8) to 8-Mbit (1024K x 8 or 512K x 16). The individually-lockable boot block, which can be thought of as a ROM, is intended for storage of critical code segments. The two parameter blocks may be used to store code or data segments previously placed in E^2 devices. The main block(s) are available for mass storage of code and/or data. The tri-function capability of Boot Block flash memory is a large part of its appeal. It is widely used in PC applications to safeguard the BIOS, the basic input/output system without which the PC will not function.

3.0 BOOT BLOCK PACKAGE AND PINOUT OPTIONS

As mentioned earlier, flash memory products come in many flavors and sizes. Boot Block flash is no exception. Intel's Boot Block flash memory is available in x8 only or x8/x16 configurations. The 1-Mbit Boot Block flash memory is available in a 32-pin J-leaded chip carrier (PLCC), a 32-pin plastic dual in-line package (PDIP), and a 32-lead thin small outline package (TSOP). The 1-Mbit density is only available in x8 configuration, regardless of package.

SmartVoltage and Smart 5 flash memory products range in density from 2M to 8M. They are offered in 40-lead, 48-lead and 56-lead TSOP or 44-lead plastic small outline package (PSOP, sometimes referred to as SOP).

The 40-lead TSOP package is x8 only. The 48-lead and 56-lead TSOP devices are x8/x16 configurable, as is the 44-lead PSOP package. Bus width selection is controlled via the BYTE# pin (Figure 2). In both the 40-lead and 48-lead TSOP packages, all densities are pin-for-pin compatible. The 2-Mbit and 4-Mbit densities in the PSOP package are pin compatible; however this package did not have sufficient pins to support the 8M density without sacrificing a feature. As a result, the 8-Mbit device (PSOP package only) does not support boot block locking at 5V (no WP# pin). Boot block locking at 12V is still available.

Intel has added a BIOS-optimized 2-Mbit flash memory device, the 28F002BC, to its product portfolio. The 28F002BC is an 80 ns (or 120 ns), top boot, x8 flash device. It is available in 40-lead TSOP, 40-lead PDIP and 44-lead PSOP. The 40-lead TSOP and 44-lead PSOP are compatible with SmartVoltage and Smart 5 products. The 40-lead PDIP is a unique pinout.

It is clearly apparent the choice of package has a direct correlation to the flexibility of a design. Previously, PLCC and PDIP packages dominated the market. As probers, steppers, and handlers advanced in capability, new packages were developed to enable smaller form factors. Additionally, space requirements grew more stringent, making it necessary to combine the features of several devices into one package, thereby decreasing board space requirements.

Today, a TSOP package is one of the smallest form factors available. It has a 0.500 mm (20 Mils) lead pitch and maximum height of 1.2 mm (47 Mils). The 40-lead package has a nominal width of 10.0 mm (394 Mils) and length, including leads, of 20.0 mm (787 Mils). A PSOP package, in comparison, has 1.27 mm (50 Mils) lead pitch, which is the same as a PLCC package. The maximum height of a PSOP is 2.95 mm (116 Mils); the package dimensions are 16.0 mm (630 Mils) by 28.3 mm (1,110 Mils). Bear in mind the numbers provided above are package dimensions. When laying out a board that will accommodate differing packages, landpad measurements must be used. Landpad dimensions are slightly larger than package dimensions to accommodate offsets in package placement.

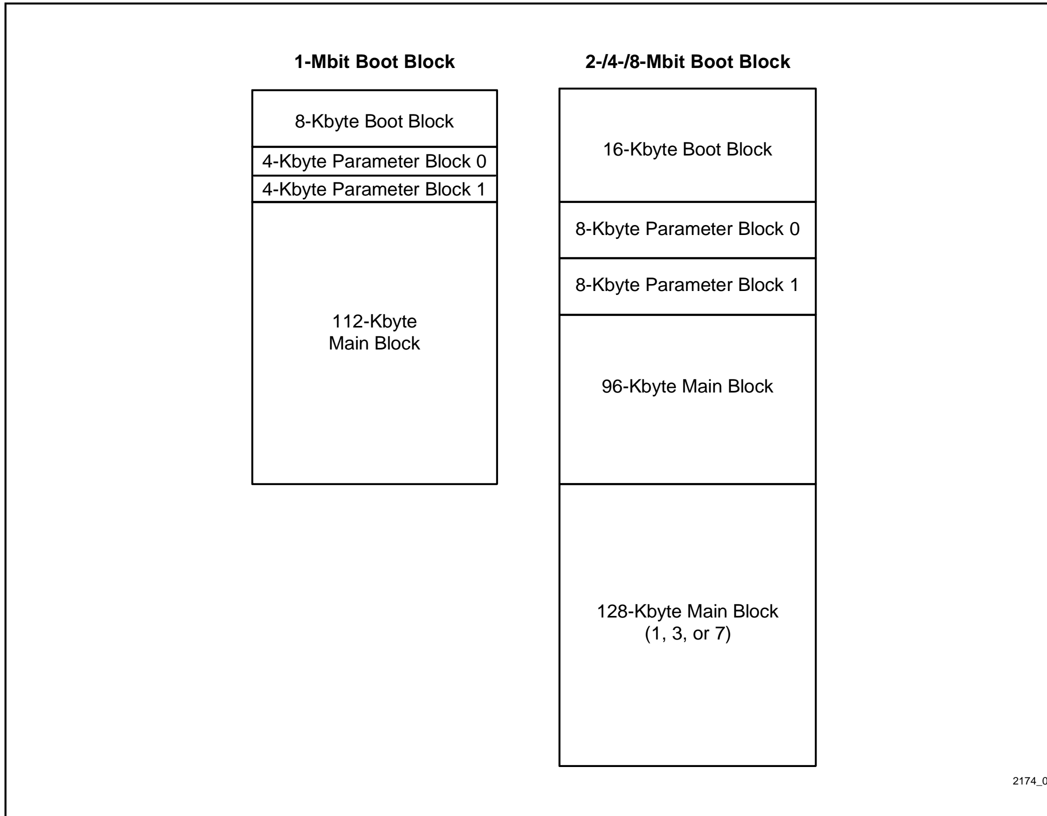


Figure 1. Intel Boot Block Flash Memory Architecture

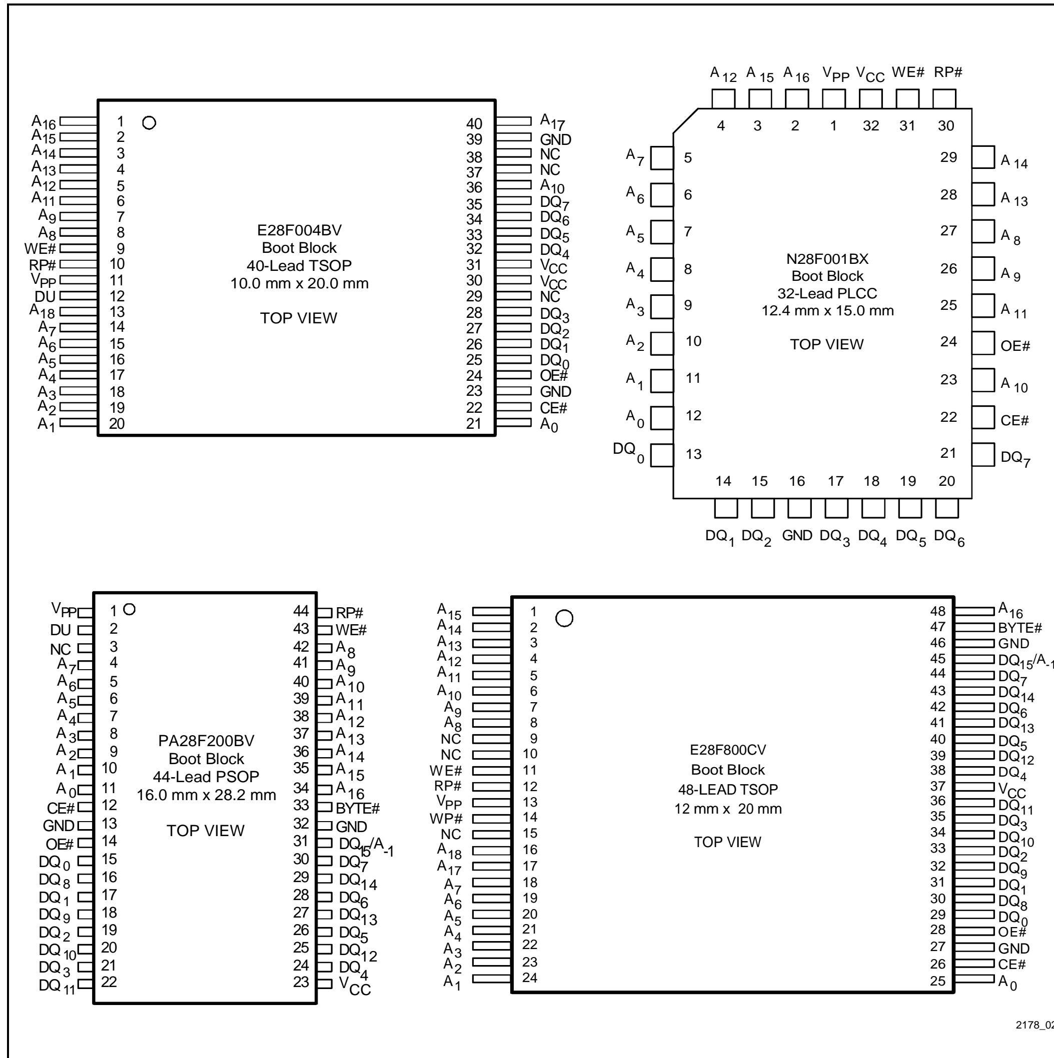


Figure 2. Example Boot Block Packages and Pinouts

Table 1. PCB Layout Descriptions

Case	Section
1. Intel 1-/2-Mb Bulk Flash (32L PLCC) to Intel 2-/4-/8-Mb Boot Block (40L TSOP) File: BKN32E40.EXE	4.1.1
2. Intel 1-Mb Boot Block (32L PLCC) to Intel 2-/4-Mb Boot Block (44L PSOP) File: BXN32P44.EXE	4.2.1
3. Intel 1-Mb Boot Block (32L PLCC) to Intel 2-/4-/8-Mb Boot Block (40L TSOP) File: BXN32E40.EXE	4.2.2
4. Intel 1-Mb Boot Block (32L TSOP) to Intel 2-/4-/8-Mb Boot Block (40L TSOP) File: BXE32E40.EXE	4.2.3
5. Intel 1-Mb Boot Block (32L PDIP) to Intel 2-/4-/8-Mb Boot Block (44L PSOP) File: BXD32P44.EXE	4.2.4
6. Intel 1-Mb Boot Block (32L PDIP) to Intel 2-/4-/8-Mb Boot Block (40L TSOP) File: BXD32E40.EXE	4.2.5
7. Intel 1-Mb Boot Block (32L PDIP) to Intel 2-Mb Boot Block (40L PDIP) File: BCD32D40.EXE	4.2.6
8. Intel 2-Mb Boot Block (40L TSOP) to Intel 2-Mb Boot Block (40L PDIP) File: BCE40D40.EXE	4.2.7
9. Intel 2-Mb Boot Block (56TSOP) to Intel 2-/4-/8-Mb Boot Block (48L TSOP) File: BVE48E56.EXE	4.2.8
10. AMD 29F040 Symmetrically-Blocked (32L PLCC) to Intel 4-/8-Mb Boot Block (44L PSOP) File: AMN32P44.EXE	4.3.1
11. AMD 29F040 Symmetrically-Blocked (32L PLCC) to Intel 4-/8-Mb Boot Block (40L TSOP) File: AMN32E40.EXE	4.3.2
12. AMD 29F040 Symmetrically-Blocked (32L TSOP) to Intel 4-/8-Mb Boot Block (40L TSOP) File: AME32E40.EXE	4.3.3
13. AMD 29Fx00 Symmetrically-Blocked (48L TSOP) to Intel 2-/4-/8- Boot Block (40L TSOP)File: AME48E48.EXE	4.3.4
14. Atmel 29C040 Symmetrically-Blocked (40L TSOP) to Intel 4-/8-Mb Boot Block (40L TSOP) File: ATE402E40.EXE	4.3.5
15. Sharp LH28Fx00 Flash Memory (56L TSOP) to Intel 2-/4- Boot Block (48L TSOP)	4.3.6

4.0 BOOT BLOCK PCB LAYOUTS

The layouts contained in this document were generated using Intel's small form factor design rules. All layouts presented in this application note assume a four-layer stack: signal-power-ground-signal. The section pertaining to board design considerations looks at other possible layer stacks and their advantages and disadvantages. Since power and ground pins are generally connected to their respective planes, V_{CC} and GND pins have been left unconnected. High voltage inputs (e.g., 12V V_{PP}) are also unconnected. The traces for these inputs are usually isolated from standard traces (to reduce crosstalk); they also tend to be shorter and wider (to limit transmission line effects) than standard signal traces. Layouts for compatibility between Intel devices include RP# where appropriate; for competitive layouts, RP# remains unconnected. Standard design practice is to connect RP# to the RESET input of the non-Intel device. Lastly, higher density address pins are connected where appropriate.

Layouts were designed using the PADS Work* PCB layout package, available from PADS Software, Inc. The Gerber outputs generated are industry-standard and can be used on any PCB layout tool that accepts the Gerber

input format. Postscript files are also available; these can be printed on any postscript printer (in the event a layout tool is not readily accessible). All layout files are posted on Intel's WWW home page, http://www.intel.com/design/flcomp. Table 1 provides a complete list of Boot Block layouts referenced in this application note.

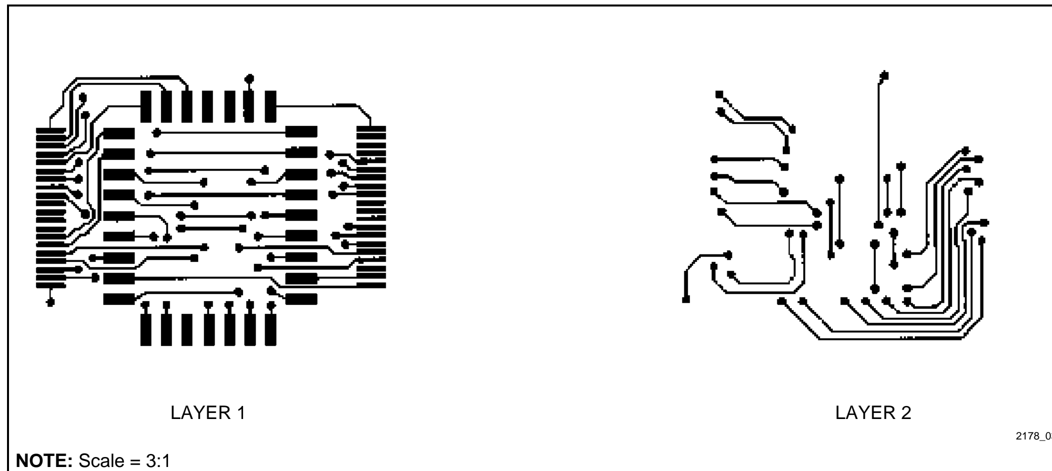
4.1 Intel 1-/2-Mbit Bulk Flash to 2-/4-/8-Mbit Boot Block

There are some applications that use the 1-/2-Mb bulk flash memory. These designs may want to migrate to higher functionality Boot Block device. Other changes must be considered when making a transition of this kind, including software, device identifier and additional functionality. The bulk flash layout below provides flexibility between 1-/2-Mb bulk and 2-/4-/8-Mb Smart 5 or SmartVoltage densities. Address A_{18}–A_{19} are not connected and should be routed if used within a specific design.

4.1.1 32-LEAD PLCC TO 40-LEAD TSOP

The layout in Figure 3 shows a 32-lead PLCC (1-/2-Mb bulk) to a 40-lead TSOP (2-/4-/8-Mb Boot Block) memory. The PLCC has 50 Mil (thousandth of an inch) leads whereas the TSOP has 20 Mil lead pitch. The parameters used to derive this layout are as follows:

Feature	Dimension
Total Layout Area (PLCC to TSOP)	0.645" sq. (416.15 mm^2)
X,Y	0.919 " x 0.702" (23.34 mm x 17.83 mm)
Via Size	0.025" (0.635 mm)
Trace Width	0.006" (0.152 mm)
Trace-to-Trace Clearance	0.006" (0.152 mm)
Trace-to-Pad Clearance	0.006" (0.152 mm)
Pad-to-Pad Clearance	0.006" (0.152 mm)



NOTE: Scale = 3:1

Figure 3. 1-/2-Mbit Bulk Flash (32-Lead PLCC) to 2-/4-/8-Mbit Boot Block (40-Lead TSOP)

4.2 Intel 1-Mbit Boot Block to 2-/4-/8-Mbit Boot Block

Most BIOS applications today utilize the 1-Mb Boot Block flash memory device. BIOS engineers have been compressing code in order to fit the growing system BIOS requirements within the allotted 128 Kbyte available memory space. The emergence of Plug and Play and Universal Serial Bus has pushed BIOS code beyond 1-Mb. The layouts in this section provide flexibility from 1-Mb to 8-Mb densities.

4.2.1 32-LEAD PLCC TO 44-LEAD PSOP

The layout in Figure 4 shows a 32-lead PLCC (1-Mb flash) to a 44-lead PSOP (2-/4-Mb flash) memory. Both the PLCC and the PSOP have 50 Mil lead pitch, making them more rugged and easier to handle manually. As the layout shows, the PLCC can be placed entirely within the PSOP, thus minimizing the space consumption. Connecting address line 18 on the PSOP package (pin 2) provides an upgrade path from 1 Mbit to 8 Mbit. However, this replaces the WP# function (8 Mbit only) previously connected to that pin, eliminating 5V boot block locking or unlocking. This function can still be achieved by applying 12V to RP#.

The parameters used to derive this layout are given in the following table:

Feature	Dimension
Total Layout Area (PLCC to PSOP)	0.800” sq. (515.50 mm^2)
X,Y	0.730 “ x 1.096” (18.53 mm x 27.82 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.008” (0.203 mm)

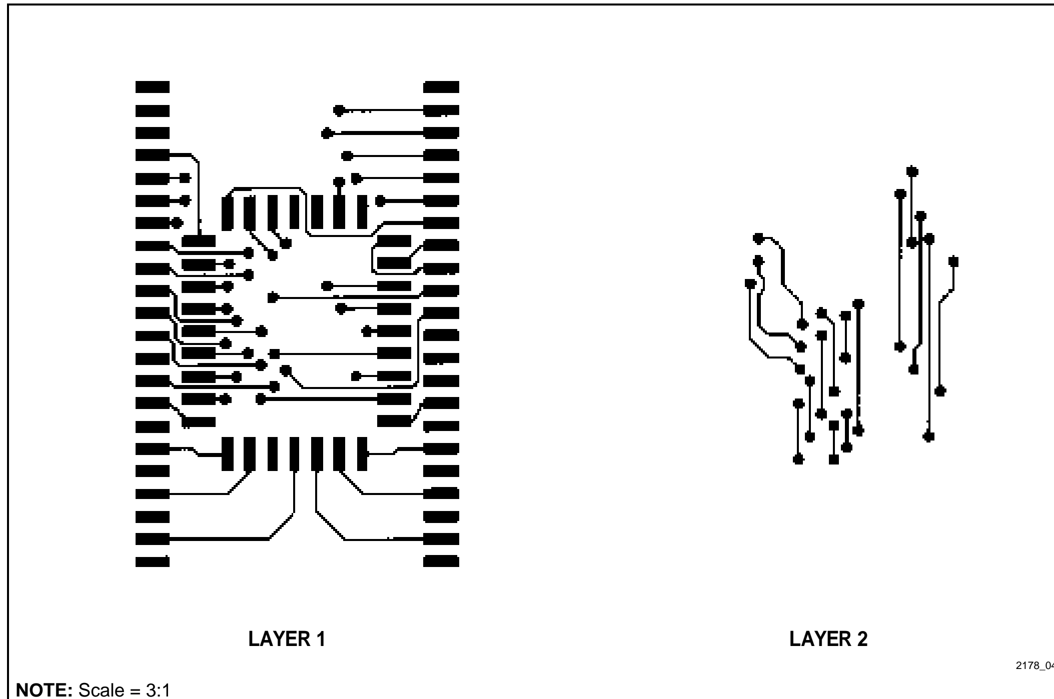


Figure 4. 1-Mbit Boot Block (32-Lead PLCC) to 2-/4-/8-Mbit Boot Block (44-Lead PSOP)

4.2.2 32-LEAD PLCC TO 40-LEAD TSOP

The TSOP package is the best choice for space-constrained designs. Its 20 Mil lead pitch and 47 Mil height makes TSOP ideal for designs with limited board space. As shown in Figure 5, the PLCC/TSOP dual footprint takes up almost no additional board space. This same layout can be used to upgrade from 1-Mbit Boot Block up to an 8-Mbit Boot Block.

Feature	Dimension
Total Layout Area (PLCC to TSOP)	0.558” sq. (359.29 mm^2)
X,Y	0.844 “ x 0.660” (21.45 mm x 16.75 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)

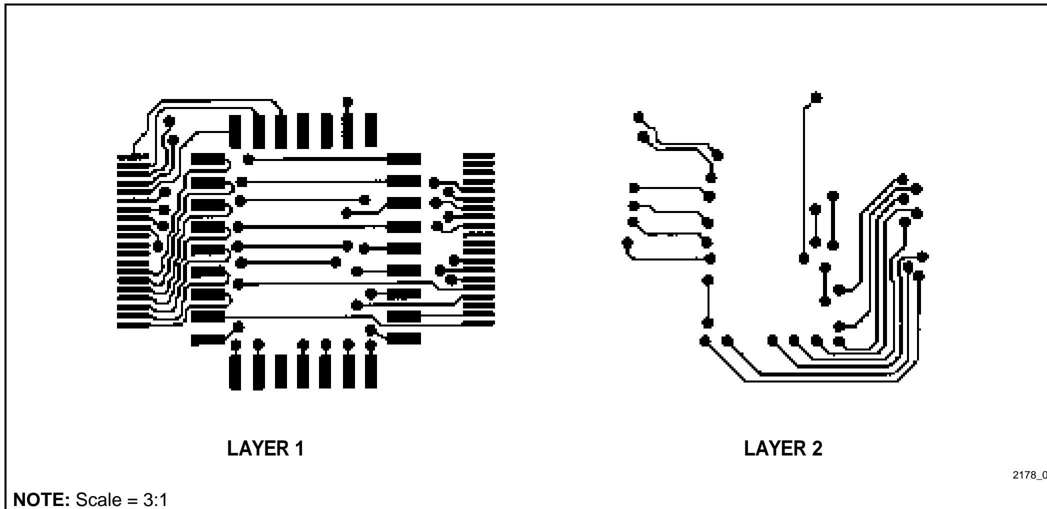


Figure 5. 1-Mbit Boot Block (32-Lead PLCC) to 2-/4-/8-Mbit Boot Block (40-Lead TSOP)

4.2.3 32-LEAD TSOP TO 40-LEAD TSOP

For designs using the 1-Mb Boot Block in the 32-lead TSOP package, the upgrade path of choice is to the 40-lead TSOP 2-/4-/8-Mbit flash memory. With a slight shift in the placement, as illustrated in Figure 6, a minimal footprint can be obtained that enables both devices to be interchanged on any given board. This kind of flexibility protects your design during constrained times and also allows multiple sources at your discretion.

Feature	Dimension
Total Layout Area (PLCC to PSOP)	0.800” sq. (277.46 mm^2)
X,Y	1.053 “ x 0.409” (26.73 mm x 10.38 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)

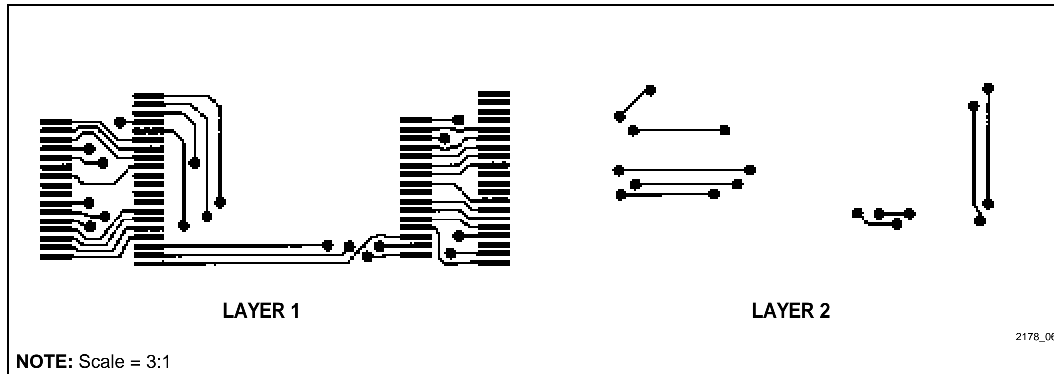


Figure 6. 1-Mbit Boot Block (32-Lead TSOP) to 2-/4-/8-Mbit Boot Block (40-Lead TSOP)

4.2.4 32-LEAD PDIP TO 44-LEAD PSOP

Customers using the PDIP package are typically less space-constrained. Although this package is durable, especially during manual handling, it is relatively large compared to other packages. Newer designs are migrating from through-hole to surface mount packages. Figure 7 depicts a layout from PDIP to PSOP. The footprint shown is applicable for upgrading from 1-Mbit to 8-Mbit Boot Block.

Feature	Dimension
Total Layout Area (PDIP to PSOP)	1.480” sq. (954.64 mm^2)
X,Y	0.933 “ x 1.586” (23.70 mm x 40.28 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)

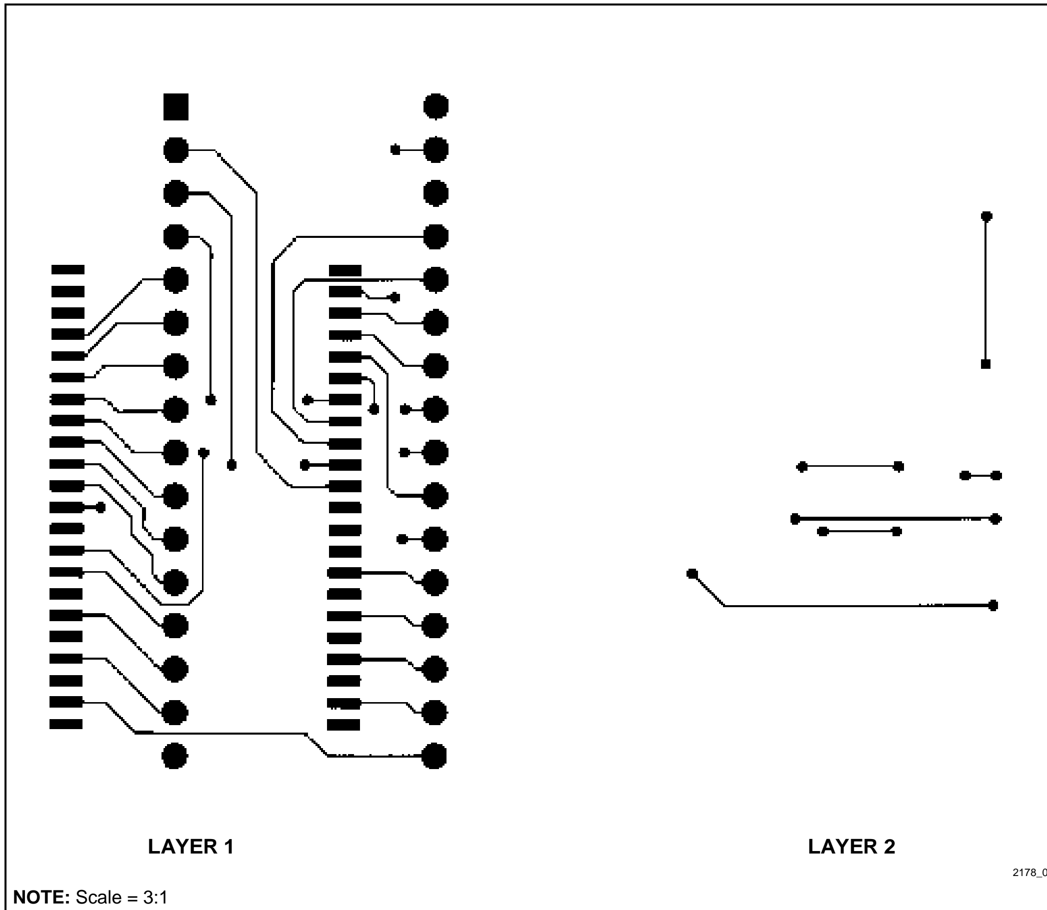
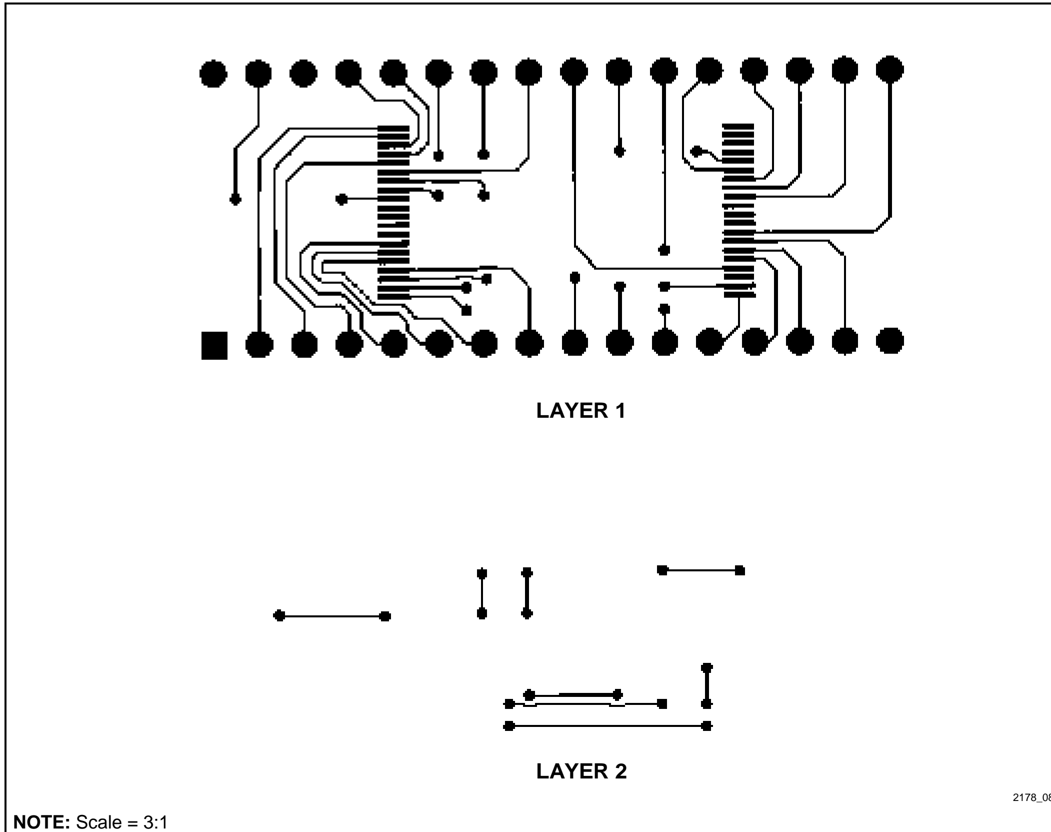


Figure 7. 1-Mbit Boot Block (32-Lead PDIP) to 2-Mbit Boot Block (44-Lead PSOP)

4.2.5 32-LEAD PDIP TO 40-LEAD TSOP

The layout for converting a PDIP to a TSOP is shown in Figure 8. Notice the tremendous space savings accomplished with this shift in package. This layout supports upgrading from a 1-Mbit boot block to a 2-Mb, 4-Mb, or 8-Mb Boot Block flash memory.

Feature	Dimension
Total Layout Area (PDIP to TSOP)	1.063” sq. (689.60 mm^2)
X,Y	1.572 “ x 0.676” (39.93 mm x 17.17 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)



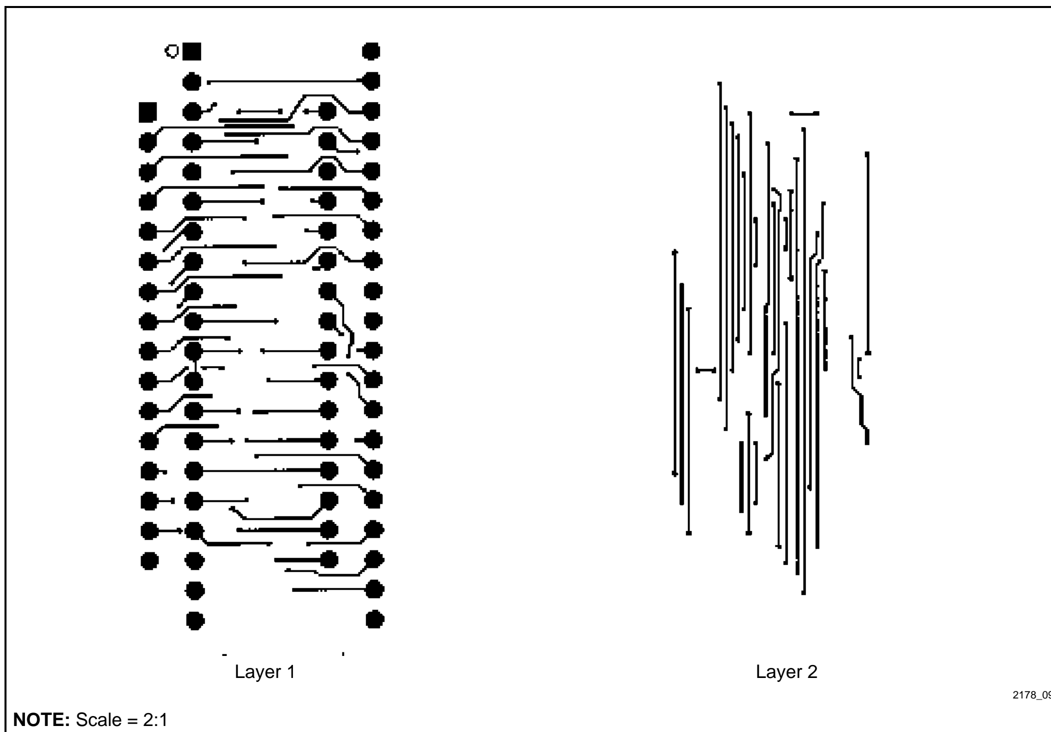
NOTE: Scale = 3:1

Figure 8. 1-Mbit Boot Block (32-Lead PDIP) to 2-Mbit Boot Block (40-Lead TSOP)

4.2.6 32-LEAD PDIP TO 40-LEAD PDIP

For designs that currently use a 32-lead PDIP flash memory and do not require surface mount packaging, the BIOS-optimized 2-Mb flash, in the 40-lead PDIP package, is an excellent alternative. The layout in Figure 9 shows one example of how to migrate from the 32-lead PDIP to the 40-lead PDIP. This layout supports upgrading from a 1-Mbit Boot Block to a 2-Mb 28F002BC Boot Block flash memory.

Feature	Dimension
Total Layout Area (PDIP to PDIP)	1.878” sq. (1,211.43 mm^2)
X,Y	0.932 “ x 2.015” (23.67 mm x 51.18 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.009” (0.229 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)



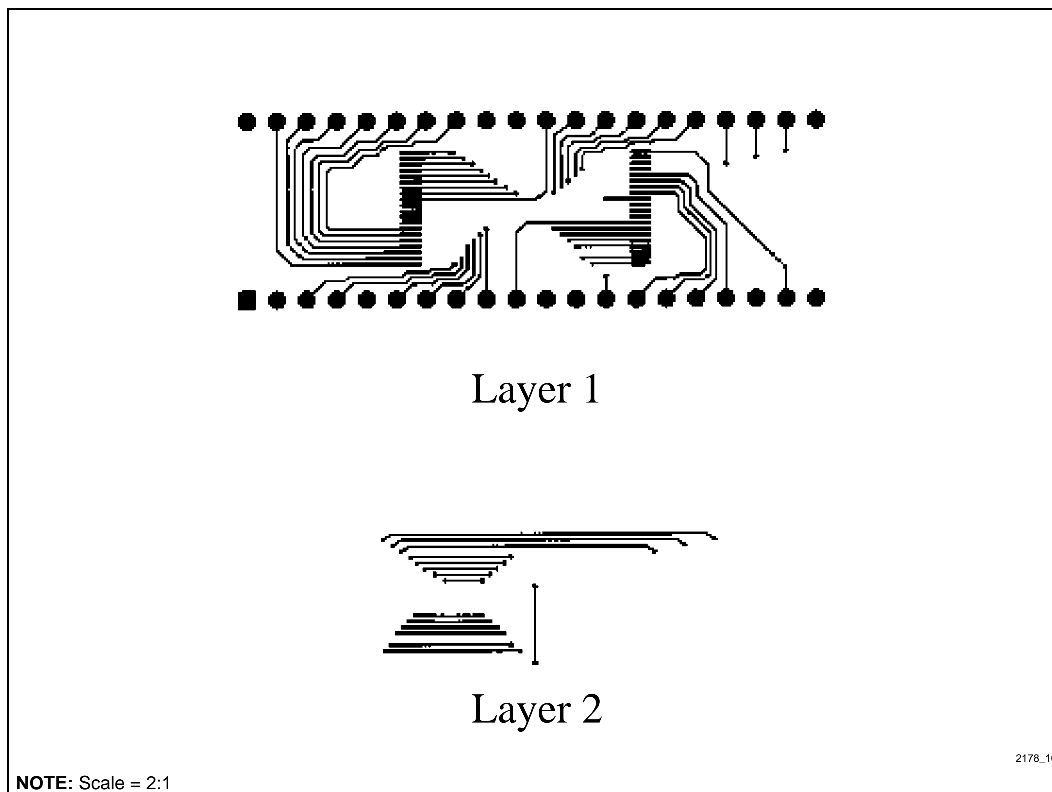
NOTE: Scale = 2:1

Figure 9. 1-Mbit Boot Block (32-Lead PDIP) to 2-Mbit Boot Block (40-Lead PDIP)

4.2.7 40-LEAD PDIP TO 40-LEAD TSOP

The cyclic nature of the memory industry virtually necessitates a multi-source strategy. The layout in Figure 10 is an example of how to design a board for both surface mount and through-hole package flexibility. This layout supports the 2-Mbit Boot Block (40-lead PDIP) and 2-/4-/8-Mbit Boot Block (40-lead TSOP).

Feature	Dimension
Total Layout Area (PDIP to PDIP)	1.339" sq. (863.77 mm^2)
X,Y	2.004 " x 0.668" (50.90 mm x 16.97 mm)
Via Size	0.025" (0.635 mm)
Trace Width	0.009" (0.229 mm)
Trace-to-Trace Clearance	0.006" (0.152 mm)
Trace-to-Pad Clearance	0.006" (0.152 mm)
Pad-to-Pad Clearance	0.006" (0.152 mm)



NOTE: Scale = 2:1

Figure 10. 2-Mb Boot Block (40-Lead PDIP) to 2-/4-/8-Mb Boot Block (40-Lead TSOP)

4.2.8 48-LEAD TSOP TO 56-LEAD TSOP

Smart 5 and SmartVoltage flash devices are available in both 48-lead and 56-lead TSOP. For maximum flexibility, boards may be laid out to support both package types. Figure 11 shows an example compact layout for a board that supports both 48-lead and 56-lead TSOP. This layout is applicable for 2-/4-/8-Mb Smart 5 and SmartVoltage flash products.

Feature	Dimension
Total Layout Area (PDIP to PDIP)	0.551” sq. (355.39 mm^2)
X,Y	0.951 “ x 0.579” (24.16 mm x 14.71 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.006” (0.152 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)

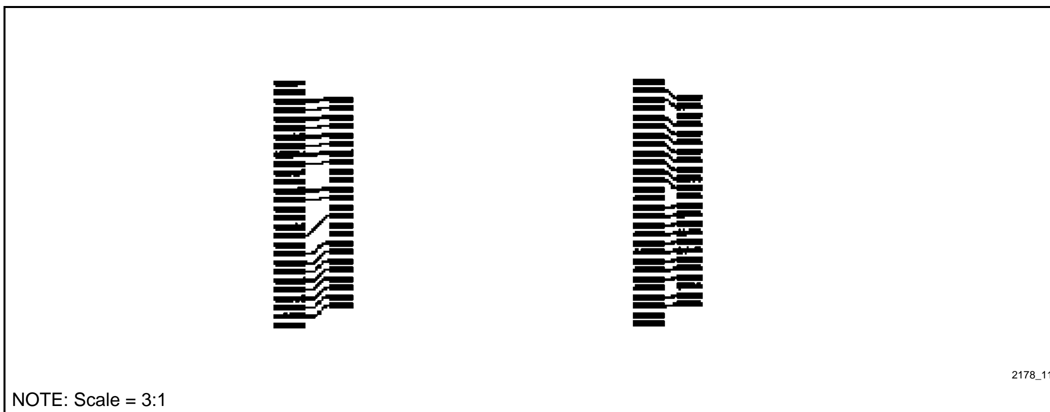


Figure 11. 2-/4-/8-Mbit Boot Block (48-Lead TSOP) to 2/-4-/8-Mbit Boot Block (56-Lead TSOP)

4.3 Other Flash Memories to Intel Boot Block Flash Memory

The really unique aspect of multi-site layouts is the ability to support multiple vendors on the same board. By placing dual footprints on a board, a design can be made to support, say, both an Intel 4-Mb flash device and an AMD 4-Mb flash device. There may be some software changes required, but the flexibility realized outweighs the potential software inconvenience. Additionally, software changes tend to be less costly than complete board redesign for new package types.

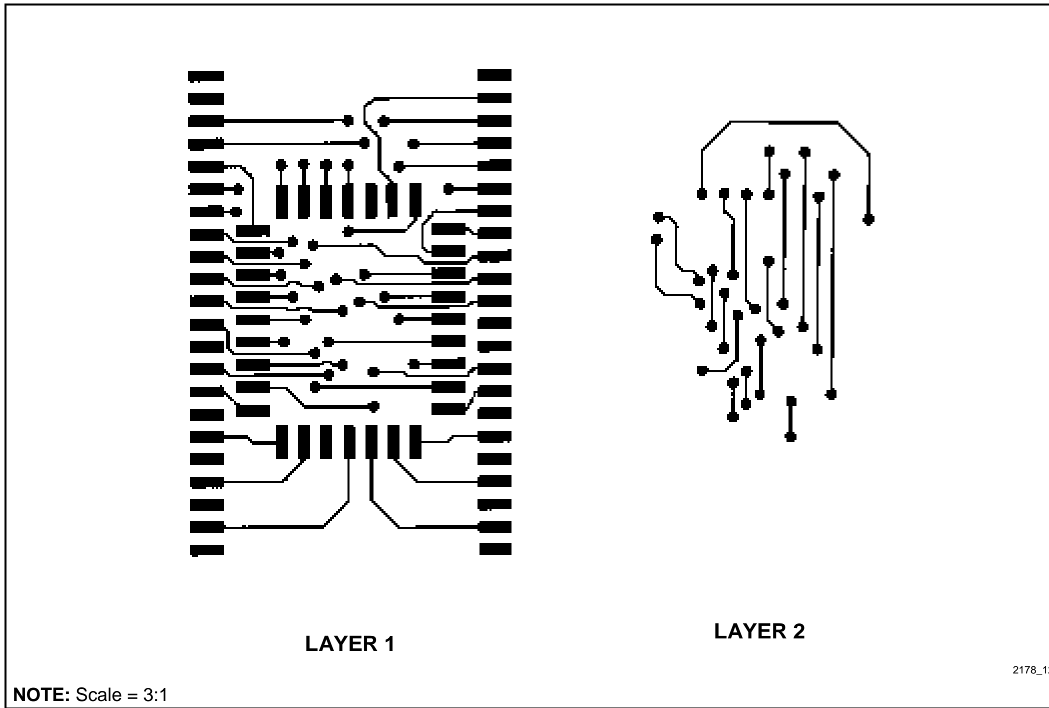
As market changes take place, customer needs will drive peaks and valleys on the supply and demand curve. During surplus supply situations, multi-site layouts may not be of much benefit, but their value during constrained supply times cannot be disputed. With dual footprints on a board, a design can utilize multiple vendor products, thus making it more adaptable to the changing times yet to come.

4.3.1 AMD 4-MBIT SYMMETRICALLY-BLOCKED FLASH TO INTEL BOOT BLOCK FLASH

AMD's 4-Mb sector erase flash memory contains eight, equal-sized 64-KB blocks. For designs that use this device, software emulation techniques will allow the same design to use both the Intel 4-Mb Boot Block flash memory and AMD's 4-Mb Sector Erase flash memory. The actual algorithms that accomplish this are not covered in this application note; however, the dual package footprint that describes the hardware layout is discussed in this section.

For designs using the 32-lead PLCC, Figure 12 depicts the diagram for the PLCC package to the 44-lead PSOP package. Although the diagram looks similar to previous ones, the actual routing of the traces is different because of pin assignments.

Feature	Dimension
Total Layout Area (PLCC to PSOP)	0.800" sq. (515.50 mm^2)
X,Y	0.730 " x 1.096" (18.53 mm x 27.82 mm)
Via Size	0.025" (0.635 mm)
Trace Width	0.005" (0.127 mm)
Trace-to-Trace Clearance	0.006" (0.152 mm)
Trace-to-Pad Clearance	0.006" (0.152 mm)
Pad-to-Pad Clearance	0.008" (0.203 mm)



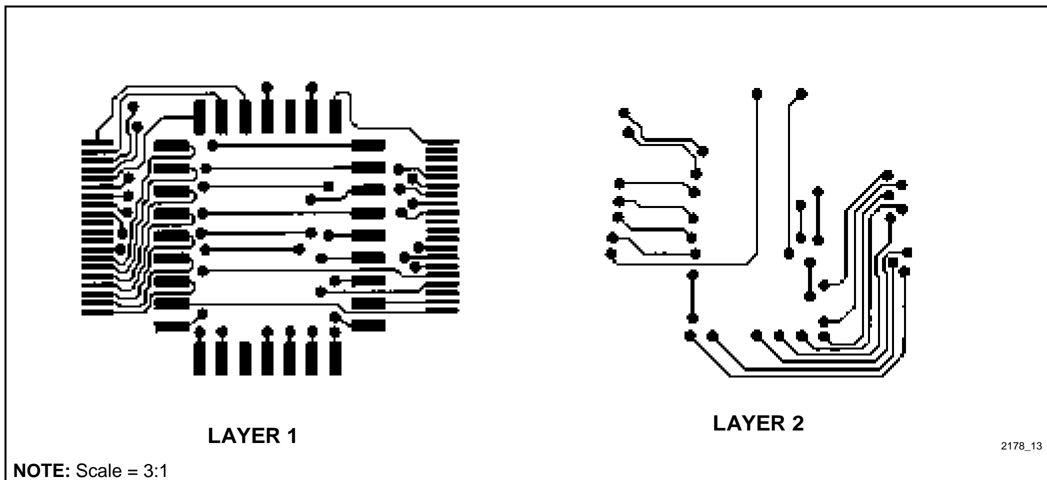
NOTE: Scale = 3:1

Figure 12. AMD 4-Mbit Sector Erase (32-Lead PLCC) to Intel 2-/4-/8-Mbit Boot Block (44-Lead PSOP)

4.3.2 AMD 4-MBIT SYMMETRICALLY-BLOCKED FLASH TO INTEL BOOT BLOCK FLASH

The PLCC 28F040 to Boot Block 40-lead TSOP layout is shown in Figure 13. The parameters that correspond to this layout are provided in the table. Again, this layout may appear similar to previous layouts but it is different due to the difference in manufacturer pin assignments.

Feature	Dimension
Total Layout Area (PLCC to TSOP)	0.558” sq. (359.29 mm^2)
X,Y	0.845 “ x 0.660” (21.45 mm x 16.75 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.005” (0.127 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)



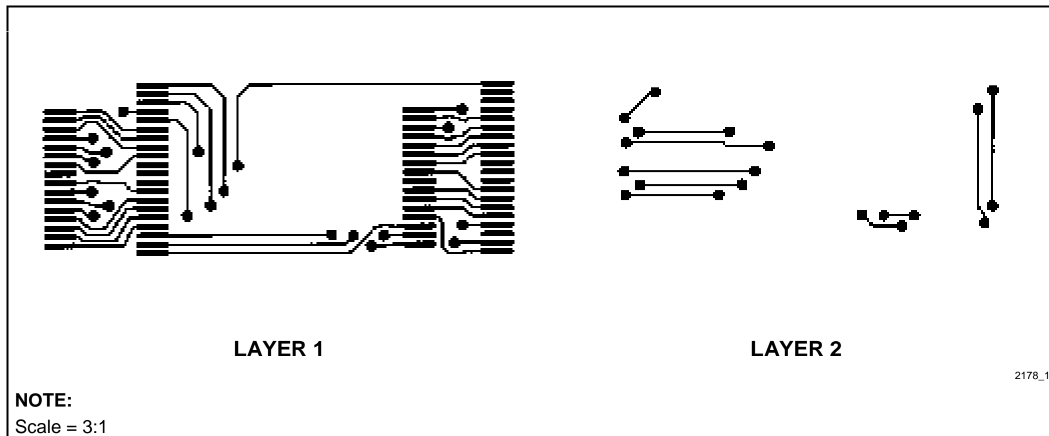
NOTE: Scale = 3:1

Figure 13. AMD 4-Mbit Sector Erase (32-Lead PLCC) to Intel 2-/4-/8-Mbit Boot Block (40-Lead TSOP)

4.3.3 AMD 4-MBIT SYMMETRICALLY-BLOCKED FLASH TO INTEL BOOT BLOCK FLASH

The AMD 29F040 is also available in a 32-lead TSOP package. If a particular design uses this package and desires the features of a Boot Block device, the diagram in Figure 14 shows how a board can be laid out such that it supports both TSOP pinouts.

Feature	Dimension
Total Layout Area (TSOP to TSOP)	0.431" sq. (277.46 mm^2)
X,Y	1.053 " x 0.409" (26.73 mm x 10.38 mm)
Via Size	0.025" (0.635 mm)
Trace Width	0.005" (0.127 mm)
Trace-to-Trace Clearance	0.006" (0.152 mm)
Trace-to-Pad Clearance	0.006" (0.152 mm)
Pad-to-Pad Clearance	0.006" (0.152 mm)



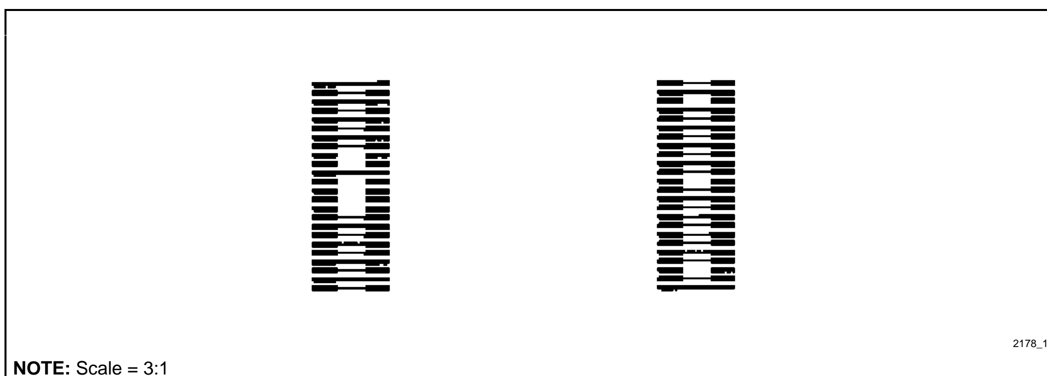
NOTE:
Scale = 3:1

Figure 14. AMD 4-Mbit Sector Erase (32-Lead TSOP) to Intel 4-Mbit Boot Block (40-Lead TSOP)

4.3.4 AMD 2-/4-/8-MBIT SECTORED ERASE FLASH TO INTEL BOOT BLOCK FLASH

AMD also offers sector erase flash devices in a 48-lead TSOP package. Although the basic functionality is similar to Intel's Boot Block flash family, each product has its own unique features that the other does not. pinouts are somewhat different. For example, AMD uses RESET in place of RP# but it does not offer a WP# pin for 5V locking and unlocking of the boot block. However for each unsupported function on a device, its corresponding pin is a NO CONNECT. The makes multi-site planning fairly easy, as Figure 15 shows. In fact, these devices can occupy the same socket, so long as the software is capable of differentiating between the two devices and selecting the appropriate software algorithm.

Feature	Dimension
Total Layout Area (TSOP to TSOP)	0.465” sq. (300.20 mm^2)
X,Y	0.953” x 0.488” (24.21 mm x 12.40 mm)
Via Size	0.025” (0.635 mm)
Trace Width	0.006” (0.152 mm)
Trace-to-Trace Clearance	0.006” (0.152 mm)
Trace-to-Pad Clearance	0.006” (0.152 mm)
Pad-to-Pad Clearance	0.006” (0.152 mm)



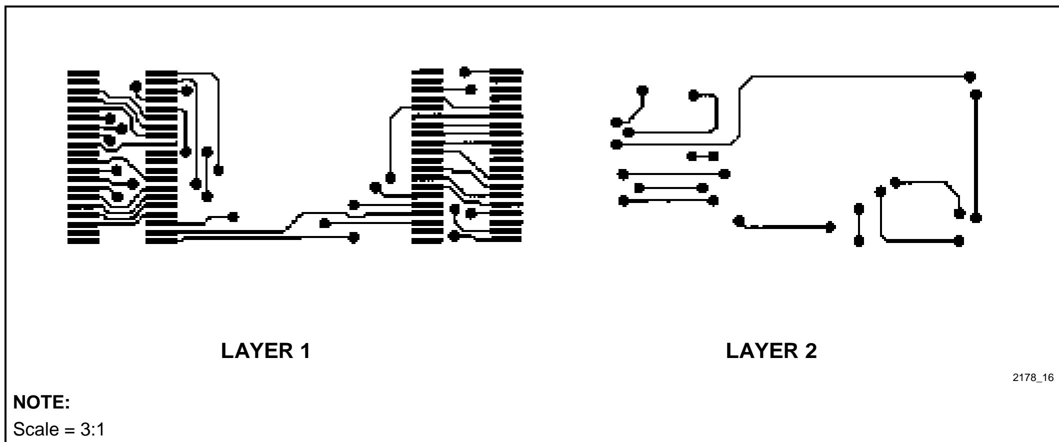
NOTE: Scale = 3:1

Figure 15. AMD 2-/4-/8-Mbit Flash (48-Lead TSOP) to Intel 2-/4-/8-Mbit Boot Block (48-Lead TSOP)

4.3.5 ATMEL 4-MBIT CMOS FLASH TO INTEL 4-MBIT BOOT BLOCK FLASH

Atmel also produces a 4-Mb symmetrically-blocked flash memory. However, they do not offer it in a PLCC package. It is available only in a 32-lead plastic DIP or a 40-lead TSOP package. The blocking of the two devices is also different: the Atmel device has 1024 equally-sized blocks of 512 bytes each. Again, software emulation schemes (which are not discussed in this document) can be employed to make one device mimic the functionality of the other. Therefore, the same board can be populated by either device, depending on market requirements. The layout in Figure 16 shows how a 40-lead TSOP footprint of the AT29C040 can co-exist on the same board as an Intel 4-Mb Boot Block flash memory. Again, note that even though the diagram looks somewhat similar to previous layouts, this layout depicts two 40-lead devices with different pinouts.

Feature	Dimension
Total Layout Area (TSOP to TSOP)	0.416" sq. (268.12 mm^2)
X,Y	1.017" x 0.409" (25.83 mm x 10.38 mm)
Via Size	0.025" (0.635 mm)
Trace Width	0.005" (0.127 mm)
Trace-to-Trace Clearance	0.006" (0.152 mm)
Trace-to-Pad Clearance	0.006" (0.152 mm)
Pad-to-Pad Clearance	0.006" (0.152 mm)



NOTE:
Scale = 3:1

Figure 16. Atmel 4-Mbit Sector Erase (40-Lead TSOP) to Intel 4-Mbit Boot Block (40-Lead TSOP)

4.3.6 SHARP 2-/4-MBIT FLASH TO INTEL BOOT BLOCK FLASH

Another NOR flash provider offering products similar to Intel is Sharp. They provide a 2-/4-Mbit flash memory in a 56-lead TSOP package. Again, availability may dictate using a 48-lead TSOP instead of the 56-lead package.

Using the multi-site layout in Figure 17, a board can be designed to accommodate both Sharp's 56-lead TSOP package and Intel's Boot Block flash family.

Feature	Dimension
Total Layout Area (TSOP to TSOP)	0.551 " sq. (355.39 mm^2)
X,Y	0.951" x 0.579" (24.16 mm x 14.71 mm)
Via Size	0.025" (0.635 mm)
Trace Width	0.006" (0.152 mm)
Trace-to-Trace Clearance	0.006" (0.152 mm)
Trace-to-Pad Clearance	0.006" (0.152 mm)
Pad-to-Pad Clearance	0.006" (0.152 mm)

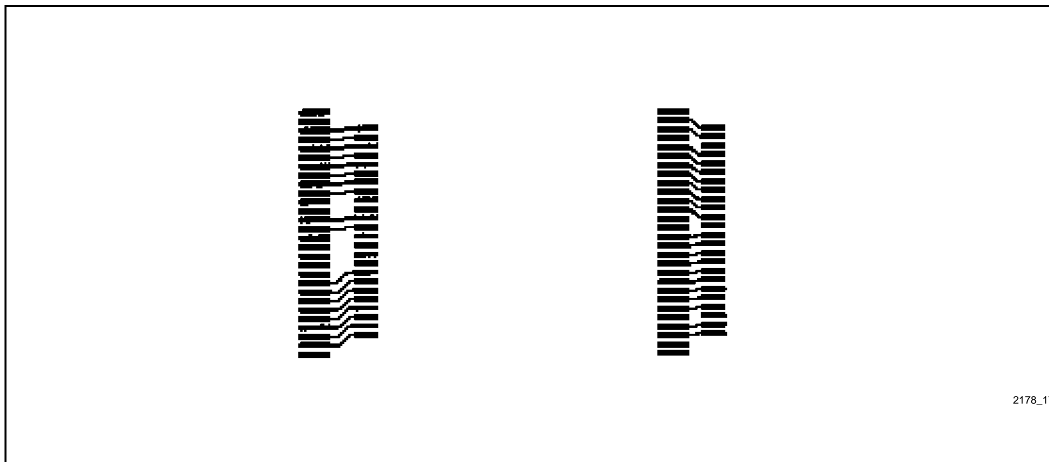


Figure 17. Sharp 2-/4-Mbit Flash (56-Lead TSOP) to Intel 2-/4-/8-Mbit Boot Block (48-Lead TSOP)

5.0 PRINTED CIRCUIT BOARD (PCB) DESIGN CONSIDERATIONS

PCB design is one of the most critical aspects of a system. It is the medium through which signals will propagate from one component to another. The board is the electrical backbone of any design. If logic levels are slightly off, they can be tweaked to perfection; however, if the inherent electrical characteristics are incorrect, no amount of tweaking will improve the design in the long term. Therefore, care should be taken to insure that board design is not only functional but also forward-looking, in anticipation of potential problem areas.

5.1 Power and Ground Planes

Power and ground planes should be designed first. The design of these planes depends on signal rise time (by far the most important), the number of signals, the physical dimensions of the board, and estimated trace widths. Power and ground planes should be placed together to maximize capacitive coupling and reduce power supply noise. Additional ground planes may be used to isolate signal routing layers; however, to guard against warping effects, power and/or ground planes should be used in pairs.

It is common knowledge that current follows the paths of least resistance. However, at high frequencies current follows the path of least inductance. This is relevant because the path of least inductance for board traces is under the conductor of the transmitted signal, as shown in Figure 18. Board designers can insure return current flow as close to the transmitted signal as possible by using many ground vias to connect ground planes together. With a mixture of power and ground planes, current has a tendency to flow through many bypass capacitors. This, unfortunately, introduces radiated noise into the system.

In high-speed designs, crosstalk can exist in the ground plane. Crosstalk between two conductors depends on their mutual inductance and mutual capacitance. Inductive crosstalk is usually larger than capacitive crosstalk in a digital environment. Returning signal current (which are traveling on the same ground plane for the most part), generate magnetic fields. These magnetic fields induce noise voltages proportional to the rate of change of the driving signal into all circuit elements in their path. Short rise time generate larger voltage as a result of mutual inductance. Slotted ground planes exacerbate the problem by forcing currents to flow together around the slot (since return signal currents cannot flow through the slot). This has the effect of increasing signal length, and therefore, mutual inductance.

5.2 Trace Considerations

Today's motherboards are stacked designs, consisting of as little as two layers to as much as eight or ten layers. When routing traces on the board, double tracking (two traces between adjacent pins) should be avoided. Additionally, triple- and four-track routing is also not a good idea. This practice can cause severe crosstalk problems. Although system designers tend to use fewer traces to minimize costs, this usually results in tightly-packed traces. Tightly-spaced traces have more crosstalk and have power handling capability. Depending on the design, tradeoffs may be necessary to accommodate system requirements.

5.3 Package Effects

Nearly all packages encounter problems at high speeds. Package lead inductance, lead capacitance, and heat dissipation are at the root of the problem. Individual pins on a package can cause the phenomenon known as ground bounce due to lead inductance of ground pins. This ground bounce is localized to the device and perceived as an internal glitch on the input signals because of the variance in the ground reference. Calculating the ground bounce magnitude necessitates knowing the rise time, lead inductance, load capacitance, and switching voltage. Of course, consideration must be given to whether the board operates at TTL or CMOS levels.

Package lead capacitance produces a slightly different effect from lead inductance. Stray capacitance between the adjacent pins of a component couples noise onto sensitive input pins. This problem grows worse with faster rise times and higher input impedance connections.

Increased heat dissipation through a package is a common side effect of most high-speed designs. As one might expect, different packages behave to temperature differently. For most logic devices, however, the relationship between temperature and power is linear. The internal temperature of a package, referred to as the junction temperature, is a function of the ambient temperature and thermal resistance. Thermal resistance is a property of cooling attachments (e.g., fans, heat sinks, etc.), package size, package material, and die attach method.

Low Frequency Current Path (Least Resistance)

High Frequency Current Path (Least Inductance)

2178_18

Figure 18. Current at High Frequencies Follows the Path of Least Inductance

6.0 CONCLUSION

The name of the game, in life as well as in business, is change: if you want to play, you have to learn to adapt. It is no mystery market needs will change: demographics will shift, purchasing trends will meander from one side to the other, and buying habits will bounce up and down like the stock market. To be successful, your designs need to be flexible.

Designing for flexibility means being able to adapt to changes as they happen, not after it is too late. Flexibility needs to be designed into the product at the beginning not after it has already hit the market. The techniques presented in this application note make it easier for your application to adapt. By designing-in multiple footprints (especially if it is within the same space as previously consumed by a component), eliminates headaches when another of life's little surprises springs up. Dual footprints can make all the difference, especially when demand outpaces supply and alternative solutions become the norm.

As a final note, a design should have as much flexibility built-in as possible. If you are not space-constrained and can handle multiple package layouts in your application, an investigation of the benefit of multi-site layouts is a good idea. The layouts presented in this application note are all two package diagrams. More layers will be needed as the number of packages supported increases. Since four layer boards are common, laying out a board that can support two or three different package types is not only possible but an excellent answer to a constantly changing environment. Change may be the only constant, but preparation minimizes its effects.

APPENDIX A
ADDITIONAL INFORMATION[1,2]

Order Number	Document
290531	*2-Mbit (128K X 16, 256K X 8)Smart Voltage Boot Block FlashFile™ Memory Family Datasheet*
290530	*4-Mbit (256K X 16, 512K x 8) SmartVoltage Boot Block FlashFile™ Memory Family Datasheet*
290539	*8-Mbit (512K X 16, 1M X 8) SmartVoltage Boot Block FlashFile™ Memory Family Datasheet*
292159	*AP-607 Multi-Site Layout Planning with Intel's FlashFile™ Components, Including ROM Capability*
292130	*AB-57 Intel's Flash memory Boot Block Architecture for Safe Firmware Updates*
292154	*AB-60 2/4/8-Mbit SmartVoltage Boot Block Flash Memory Family Overview*

NOTE:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com for technical documentation and tools.