28F016SA/DD28F032SA
SPECIFICATION UPDATE

Release Date: July 1996

Order Number: 297408-006

The 28F016SA/DD28F032SA may contain design defects or errors known as errata. Characterized errata that may cause the 28F016SA/DD28F032SAs' behavior to deviate from published specifications are documented in this specification update.

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REVISION HISTORY

Date of Revision	Version	Description
10/27/93	-001	Document includes all known errata to date: I_{CCS} Standby Current, I_{CCD} Deep Power-Down Current.
02/01/94	-002	Added: t_{AVQV} at 3.3V Erase Interruptability Standby Current When Reading the Page Buffer Updating Global Status Register Bits 0 and 1 Active Current Consumption during Sleep Mode BYTE# Level during Deep Power-Down Mode t_{AVEL} and t_{AVGL} Timing Specifications
07/01/94	-003	Deleted: t_{AVQV} at 3.3V
12/06/94	-004	Added: Completion with Command Error Indication Non-Serviced Erase Suspend Command Updated: Erase Interruptability Standby and Deep Power-Down Current Specs
01/19/95	-005	Added: WP# Control Write Timings When Using the 10H Program Command V_{PPL} Specifications at 3.3V V_{CC} Deep Power-Down Current Specs (Permanent Change) Updated: Completion with Command Error Indication and Invalid Device Operation Standby and Deep Power-Down Current Specs (Specification Errata) Deleted: Updating Global Status Register Bits 0 and 1 BYTE# Level during Deep Power-Down Mode t_{AVEL} and t_{AVGL} Timing Specs for Extended Status Register Reads
07/01/96	-006	This is the new format for the Specification Update document. It contains all identified errata published prior to this date.

PREFACE

As of July, 1996, Intel's Semiconductor Products Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This is the sixth release of the 28F016SA/DD28F032SA Specification Update. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain additional information that was not previously published.

Functional descriptions for this product are found in the *28F016SA 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory, Extended Temperature 28F016SA 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory*, *and DD28F032SA 32-Mbit (2 Mbit x 16, 4 Mbit x 8) FlashFile™ Memory* datasheets and the *16-Mbit Flash Product Family User's Manual.*

Affected Documents/Related Documents

Title	Order
28F016SA 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet	290489
Extended Temperature 28F016SA 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory Datasheet	290541
DD28F032SA 32-Mbit (2 Mbit x 16, 4 Mbit x 8) FlashFile™ Memory Datasheet	290490
16-Mbit Flash Product Family User's Manual	297372

Nomenclature

Errata are design defects or errors. These may cause the 28F016SA/DD28F032SAs' behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation.

Documentation Changes include typos, errors, or omissions from the current published specifications.

NOTE:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the product's user documentation (datasheets, manuals, etc.).

SUMMARY TABLES OF CHANGES

The following tables indicate the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the *28F016SA 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory, Extended Temperature 28F016SA 16-Mbit (1 Mbit x 16, 2 Mbit x 8) FlashFile™ Memory,* and *DD28F032SA 32-Mbit (2 Mbit x 16, 4 Mbit x 8) FlashFile™ Memory* datasheets. Intel may fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations:

Codes Used in Summary Tables

Steps

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Device Revision Codes					Page	Status	Errata
	05	06	07	08	09			
9600001	X	X	X	X		7	Fixed	Completion with Command Error Indication and Invalid Device Operations
9600002	X	X	X	X	X	9	Fix	Non-Serviced Erase Suspend Command
9600003	X	X				13	Fixed	Erase Interruptabliity
9600004	X	X	X	X		13	Fixed	WP# Control
9600005	X	X	X	X	X	14	Fix	Write Timings When Using the 10H Program
9600006	X	X				15	Fixed	Standby and Deep Power-Down Current Specs
9600007	X	X	X	X	X	16	Fix	V_{PPL} Specifications at 3.3V V_{CC}

Specification Changes

Number	Steppings					Page	Status	Specification Changes
	05	06	07	08	09			
001	X	X	X	X	X	17	Doc	Deep Power-Down Current Specs (Permanent Change)
002	X	X	X	X	X	17	Doc	Standby Current When Reading the Page Buffer
003	X	X	X	X	X	18	Doc	Active Current Consumption during Sleep Mode

Specification Clarifications

Number	Steppings					Page	Status	Specification Clarifications
						19		None in this specification update revision.

Documentation Changes

Number	Document Revision	Page	Status	Documentation Changes
001	002	20	Doc	New Device Revision Codes

IDENTIFICATION INFORMATION

Markings

Stepping	Identifier
A-Step	1. Please see Documentation Changes for description of the Device Revision Codes.

ERRATA

9600001. Completion with Command Error Indication and Invalid Device Operations

PROBLEM: Systems in which software, after initiating device automation via a queueable command sequence, writes another command(s) to the device before automation completes may initiate unintended device operations.

IMPLICATION: Designs that could encounter this condition include the following:

- Systems that use command queueing capability.
- Systems that poll for automation completion using the Extended Status Registers Command (thereby writing the Read Extended Status Register command after initiating automation).
- Systems that write the Read Compatible Status Register command after initiating device automation and before reading the Compatible Status Register (this command is actually unnecessary as the device, after receiving queueable commands or command sequences, automatically transitions to a mode where it outputs Compatible Status Register data when read).
- Systems that use the software Sleep and/or Abort commands.
- Systems that use the Erase Suspend command.
- Systems that use Page Buffer programming.

This errata only affects components listed in the Affected Products section.

These unintended operations can produce an invalid command error indication, indicated by a “1” in the following Status Register bits:

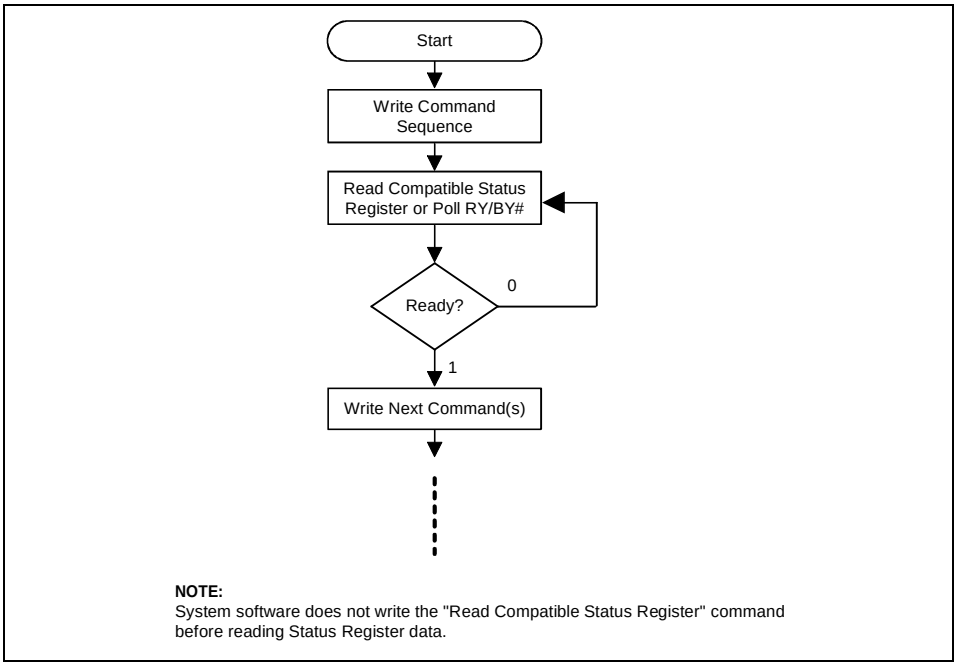
Compatible Status Register	Bit 5: Erase Status
	Bit 4: Data-Write Status
Global Status Register	Bit 5: Device Operation Status
Block Status Register (Block 0)	Bit 5: Block Operation Status

In addition, the unintended device operation can initiate inadvertent program or erase attempts to Block 0 in systems which use the Sequential/Single Load to Page Buffer Commands (74H and E0H, respectively). Data alteration can only occur if Block 0 is not locked and V_{PP} equals V_{PPH}.

WORKAROUND: The following options listed below outline possible corrective actions required to avoid this errata. (Note: Any one of the options will eliminate this errata.)

Option 1: Polling for "Ready" Indication

Systems that poll the RY/BY# pin or WSMS bit (CSR.7) for "Ready" indication before writing another command to the device will not encounter this errata. This is illustrated in the *Example System Software Flowchart, etc.* figure below, and in flowcharts 11-1 and 11-2 (without erase suspend) of the *16-Mbit Flash Product Family User's Manual*.



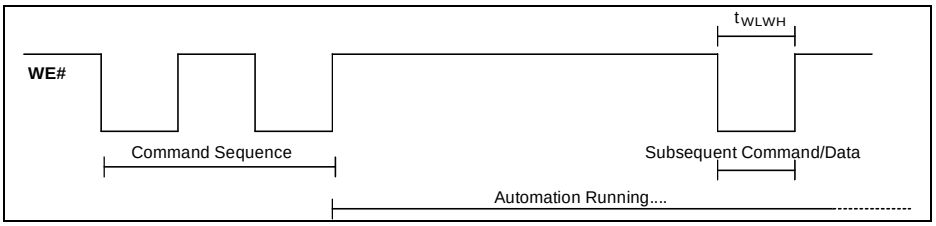
Example System Software Flowchart That Will Not Encounter "Completion with Command Error or Invalid Device Operation" Condition

Option 2: WE# and CE# Pulse Width Restrictions

For WE#-Controlled Write Operations, a WE# pulse width defined by the ranges of parameter t_{WLWH} in the table below, will result in a system that does not exhibit this errata. (Note: timings are also bounded by specifications in the device datasheet). When performing CE#-Controlled Write Operations, this restriction equally applies to the CE# pulse width (t_{ELEH}).

WE# and CE# Specifications That Will Not Cause the "Completion with Command Error or Invalid Device Operation" Condition

V_{CC} Supply Voltage	t_{WLWH}	t_{ELEH}
5V	<75 ns	<75 ns
3.3V	<100 ns	<100 ns



Timing Waveform Showing Specification Ranges That Will Not Cause the "Completion with Command Error or Invalid Device Operation" Condition

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 05H, 06H, 07H and 08H are affected.

9600002. Non-Serviced Erase Suspend Command

PROBLEM: If an Erase Suspend command is issued after completion of the Erase Cycle (either Single Block Erase or Erase All Unlocked Blocks) or too late in the Erase cycle, such that the Erase completes before the Status Register Suspend bit is set, the device will queue this unserviced Suspend request.

IMPLICATION: The following conditions are affected by this unserviced Suspend command:

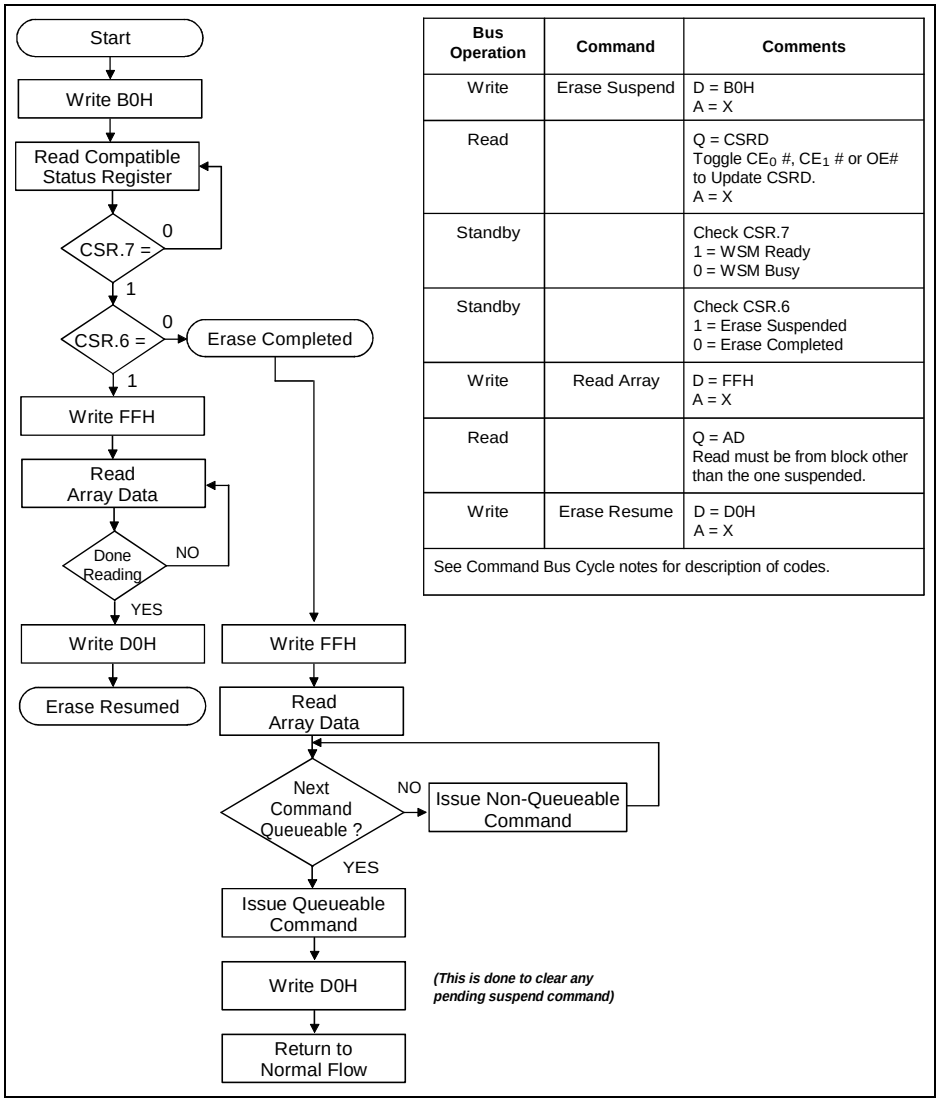
A. If another Erase command is issued at some time later, the device then assumes that the pending Suspend request is still valid and will automatically Suspend the current Erase.

B. If any queueable command is in the command queue waiting for execution while another queueable command is in progress, the Write State Machine will suspend its operation after completing the current command. (Refer to the *16-Mbit Flash Product Family User's Manual*, Section 11-1 for the queueable command list.)

Note that the device will not service the Suspend command if it is powered-down (RP# transitioning low) prior to either condition A or B.

This errata is scheduled to be fixed in an upcoming device design change.

WORKAROUND: Intel developed a software workaround to this errata, by inserting a second Resume command (D0H) following any queueable command in the Erase Suspend flowcharts. Both Erase Suspend to Read Array flowcharts (*16-Mbit Flash Product Family User's Manual*, Figures 11-3 and 11-12) detailing this workaround are attached to this errata (see the *Erase Suspend to Read Array with Compatible Status Register* and *Erase Suspend to Read Array with Extended Status Register* figures, which follow). This erratum results in the *Erase Suspend with Compatible Status Register* flowchart being incompatible with the 28F008SA *Erase Suspend* flowchart.

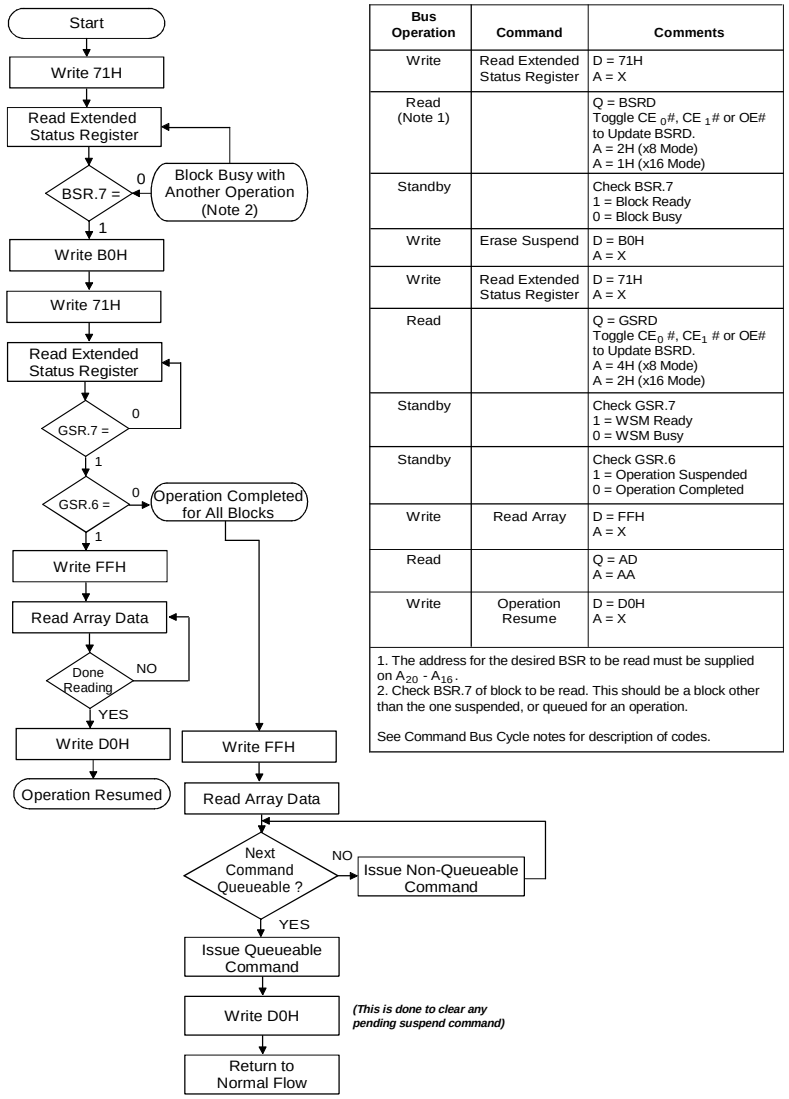


Bus Operation	Command	Comments
Write	Erase Suspend	D = B0H A = X

Read		Q = CSRD
		Toggle CE_0 #, CE_1 # or OE# to Update CSRD.
		A = X

Standby		Check CSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check CSR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	D = FFH A = X
Read		Q = AD Read must be from block other than the one suspended.
Write	Erase Resume	D = D0H A = X
See Command Bus Cycle notes for description of codes.		

Erase Suspend to Read Array with Compatible Status Register



Bus Operation	Command	Comments
Write	Read Extended Status Register	D = 71H A = X
Read (Note 1)		Q = BSRD Toggle CE_0#, CE_1# or OE# to Update BSRD. A = 2H (x8 Mode) A = 1H (x16 Mode)
Standby		Check BSR.7 1 = Block Ready 0 = Block Busy
Write	Erase Suspend	D = B0H A = X
Write	Read Extended Status Register	D = 71H A = X

Read		Q = GSRD
		Toggle CE_0 #, CE_1 # or OE# to Update BSRD.
		A = 4H (x8 Mode)
		A = 2H (x16 Mode)

Standby		Check GSR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check GSR.6 1 = Operation Suspended 0 = Operation Completed
Write	Read Array	D = FFH A = X
Read		Q = AD A = AA
Write	Operation Resume	D = D0H A = X

1. The address for the desired BSR to be read must be supplied on A_{20} - A_{16}.
2. Check BSR.7 of block to be read. This should be a block other than the one suspended, or queued for an operation.

See Command Bus Cycle notes for description of codes.

Erase Suspend to Read Array with Extended Status Register

STATUS: This erratum is intended to be fixed in a future step of this component. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 05H, 06H, 07H, 08H and 09H are affected.

9600003. Erase Interruptability

PROBLEM: The following 28F016SA and DD28F032SA features are affected for components listed in the Affected Devices section of this errata:

A. Write During Erase: Queueing a Write command when an Erase command is in progress

B. Queueing Multiple Block Erase Commands

IMPLICATION: Systems that need to queue multiple block erase commands or systems that need to queue a write during erase.

WORKAROUND: Do not attempt to send another queueable command if an Erase command is in the queue or in progress (see the *16-Mbit Flash Product Family User's Manual* Queueable Commands list, Section 11-1). However, an Erase Suspend or a Sleep Command can still be issued while an Erase is in progress.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 05H, 06H are affected.

9600004. WP# Control

PROBLEM: Block erase can prematurely terminate as the result of software Abort commands, hardware RP# activation or V_{CC} transition outside of the normal operating range. In these non-standard scenarios, there exists a small probability that the block's lock-bit will become set, locking the block if WP# is active.

IMPLICATION: Systems may inadvertently lock blocks. The system will not be able to write or erase locked blocks while WP# is held low.

WORKAROUND: System software can detect premature termination of block erase by executing the Upload Status command on device power-up. If both BSR.5 and GSR.5 are set, indicating premature block erase termination, the system should re-attempt erase with WP# inactive.

System hardware should be designed to either control WP# (both active and inactive levels must be supported) or should set WP# inactive at all times. Setting WP# always-active (i.e., connecting it to GND) is not recommended as this configuration will not enable recovery from inadvertent lock during premature block erase termination.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 05H, 06H, 07H and 08H are affected.

9600005. Write Timings When Using the 10H Program Command

PROBLEM: Modified data setup timings are required when programming using the 10H Program command sequence. This errata is scheduled to be fixed in an upcoming device design change.

IMPLICATION: Systems that use the 10H Program command are impacted.

WORKAROUND: When using the 10H Program Command, adhere to the following write specifications.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Units
t_{DVWH}	Data Setup to WE# Going High (WE#-Controlled Writes)	85			ns
t_{DVEH}	Data Setup to CE# Going High (CE#-Controlled Writes)	85			ns

V_{CC} = 5.0V ± 0.5V, TA = 0°C to +70°C

Symbol	Parameter	Min	Typ	Max	Units
t_{DVWH}	Data Setup to WE# Going High (WE#-Controlled Writes)	60			ns
t_{DVEH}	Data Setup to CE# Going High (CE#-Controlled Writes)	60			ns

Alternatively, system software can use the following commands to program the 28F016SA, Extended Temperature 28F016SA, and/or DD28F032SA.

- 40H Program
- Two-Byte Write
- Page Buffer Write to Flash

STATUS: This erratum is intended to be fixed in a future step of this component. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 05H, 06H, 07H, 08H and 09H are affected.

9600006. Standby and Deep Power-Down Current Specs

PROBLEM: The V_{CC} standby current (I_{CCS}) and deep power-down current (I_{CCD}) exceed the maximum specification values published in the 28F016SA and DD28F032SA datasheets for components listed in the Affected Products section of this erratum.

The maximum specifications for I_{CCS} and I_{CCD} are changed to the following values for these devices:

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# = Pin Set High for 3.3V Operation

Inputs	I_{CCS} Max	I_{CCD} Max
CMOS	500 µA	200 µA
TTL	4 mA	200 µA

V_{CC} = 5.0V ± 0.5V, T_A = 0°C to +70°C
3/5# = Pin Set Low for 5V Operation

Inputs	I_{CCS} Max	I_{CCD} Max
CMOS	500 µA	500 µA
TTL	4 mA	500 µA

Please note that the Reset functionality of RP# pin is preserved and customers should still be using this pin for the following purposes:

- Write Protection during system power transitions
- Device Reset to read array mode upon exit from deep power-down mode
- Termination of Write State Machine operations upon entry into deep power-down mode

IMPLICATION: Systems that utilize the deep power-down mode will experience higher current levels. This could have an effect on system battery life.

WORKAROUND: Systems needing additional power savings may power down the flash components instead of placing them in deep power-down mode.

STATUS: This erratum has been fixed. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 05H, 06H are affected.

9600007. V_{PPL} Specifications at 3.3V V_{CC}

PROBLEM: V_{PPL} is restricted to the ranges shown in the table below for operation at 3.3V V_{CC}. Operation at 5V V_{CC} is unchanged from datasheet specifications.

This errata is scheduled to be fixed in an upcoming device design change.

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# = Pin Set High for 3.3V Operation

Symbol	Parameter	Notes	Min	Typ	Max	Units	Test Conditions
$V_{PPL}1$	V_{PP} during Normal Operations		0.0		0.2		
V_{PPL} 2	V_{PP} during Normal Operations		V_{CC} – 0.2		6.5		

IMPLICATION: Systems using a 3.3V V_{CC} supply and a 12V V_{PP} supply are impacted.

WORKAROUND: Adjust V_{PP} power supply to $V_{PPL}2$ range for normal V_{PP} operations.

STATUS: This erratum is intended to be fixed in a future step of this component. Refer to Summary Table of Changes to determine the affected steppings.

AFFECTED PRODUCTS: All components with Device Revision Codes 05H, 06H, 07H, 08H, 09H are affected.

SPECIFICATION CHANGES

001. Deep Power-Down Current Specifications

PROBLEM: The V_{CC} deep power-down current (I_{CCD}) exceeds the maximum specification values published in the 28F016SA and DD28F032SA datasheets.

The maximum specifications for I_{CCD} are changed to the following values:

V_{CC} = 3.3V ± 0.3V, T_A = 0°C to +70°C
3/5# = Pin Set High for 3.3V Operation

Inputs	I_{CCD} Max
CMOS	25 µA
TTL	25 µA

V_{CC} = 5V ± 0.5V, T_A = 0°C to +70°C
3/5# = Pin Set Low for 5V Operation

Inputs	I_{CCD} Max
CMOS	25 µA
TTL	25 µA

Please note that the Reset functionality of RP# pin is preserved and customers should still be using this pin for the following purposes:

- Write Protection during system power transitions
- Device Reset to read array mode upon exit from deep power-down mode
- Termination of Write State Machine operations upon entry into deep power-down mode

002. Standby Current When Reading the Page Buffer

PROBLEM: When de-selecting the 28F016SA, Extended Temperature 28F016SA, and/or DD28F032SA, there is one condition under which the device power consumption will not decrease to the standby current level. This condition occurs when the last operation before putting the chip in standby mode is reading the page buffer. In this case, the device still consumes active power. It is therefore recommended to default back to either read array or read Status Register modes before putting the 28F016SA, Extended Temperature 28F016SA, and/or DD28F032SA in standby mode.

003. Active Current Consumption during Sleep Mode

PROBLEM: Upon issuing a Sleep command to the 28F016SA, Extended Temperature 28F016SA, and/or DD28F032SA, the system expects the device power consumption to reach the deep power-down current level. To insure that the component's power consumption reaches the deep power-down current level, the system also needs to de-select the chip by taking either or both CE_0# or CE_1# high to a CMOS level (V_{CC} ± 0.2V). If the chip is not de-selected (both CE_0# and CE_1# low at CMOS level: GND ± 0.2V) after the Sleep command is issued, the power consumption drops to the standby current level (I_{CCS}).

SPECIFICATION CLARIFICATIONS

There are no specification clarifications in this Specification Update revision.

DOCUMENTATION CHANGES

001. New Device Revision Codes

ITEM: The Upload Device Information command (99H) is used to obtain the Device Revision Codes listed below. Refer to the *16-Mbit Flash Product Family User's Manual*, Figure 11-18.

The following codes are valid:

Q = 05H

Q = 06H

Q = 07H

Q = 08H

Q = 09H

These Device Revision Codes are based on continuous improvements made in manufacturing and testing of the device and represent the current material shipped.

Note that the DD28F032SA is comprised of two die in one TSOP package. Device Revision Codes for both die should be checked to determine component errata applicability.