21153 PCI-to-PCI Bridge Configuration

Application Note

September 1998

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1.0 Introduction

This application note describes the configuration of the 21153 PCI-to-PCI bridge chip (21153) in a system. This application note is limited to the PCI configuration of the 21153 only and does not cover any hardware application topics, or describe the details of the PCI protocol.

The following topics are included in this document:

- Summary of the 21153 configuration space
- Default state of the 21153 configuration space
- Initialization guidelines for the 21153
- Sample initializations

2.0 Functional Overview

The 21153 PCI-to-PCI Bridge connects two independent PCI buses. You can implement the 21153 either on a system motherboard or backplane to provide capability for additional slots and devices, or on an option card to allow for multiple devices. You can also use the 21153 to isolate bus traffic and to provide concurrent primary and secondary bus operation.

The 21153 is a transparent device, that is, it requires no special driver software to run in a system. The 21153 does require initialization code to set up its configuration space, allocate memory and I/O space on the secondary bus of the 21153, and identify VGA devices behind the 21153. This initialization code resides in the system BIOS code or system firmware.

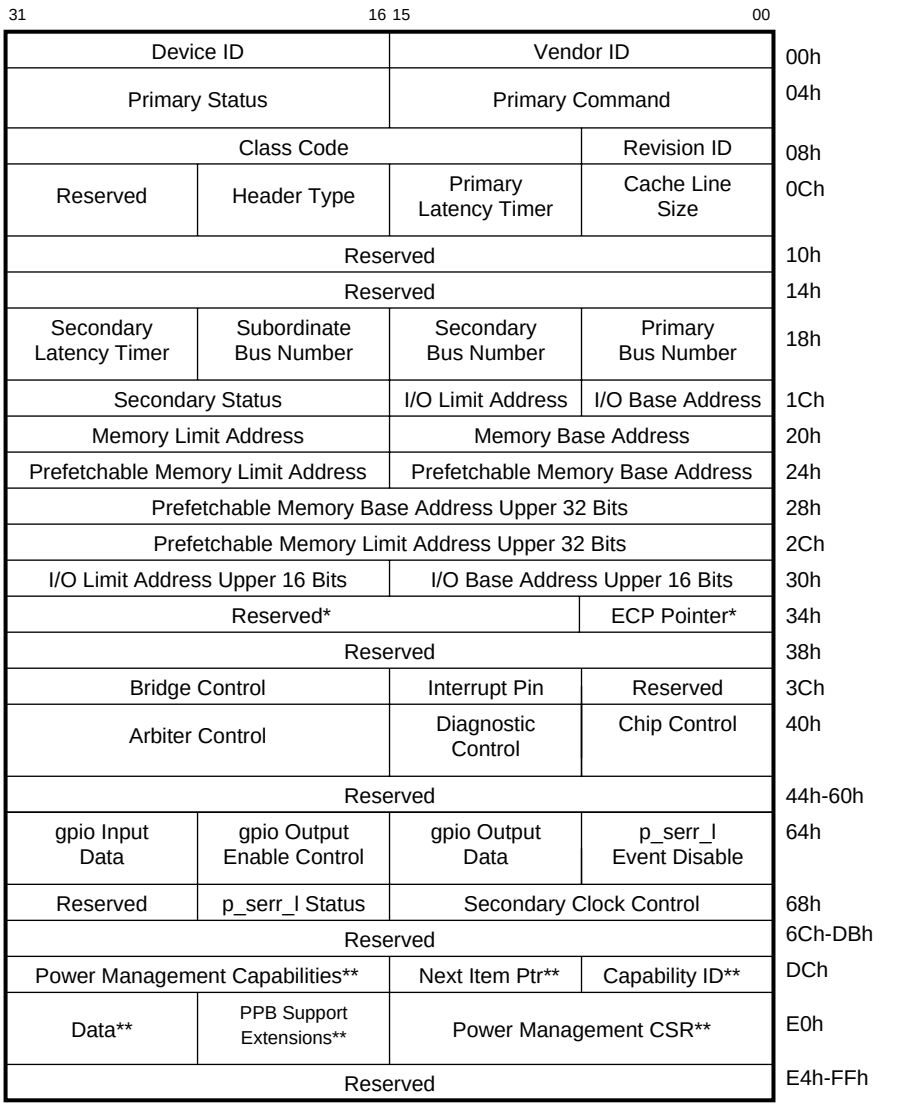
Once configured, the 21153 operates without the need for any additional software control.

3.0 21153 Configuration Space

The configuration registers of the 21153 comply with the registers of the type 1 configuration header format for PCI-to-PCI bridges, as specified in the *PCI-to-PCI Bridge Architecture Specification*. The first 16 bytes of this header are identical to those of any other PCI device. The remaining 48 bytes of the predefined header are specific to the PCI-to-PCI bridge architectural standard. The 21153 also implements 12 bytes of implementation-specific configuration space header. For a detailed description of each field, see the *21153 PCI-to-PCI Bridge Data Sheet*.

Figure 1 shows a configuration space map for the 21153.

Figure 1. 21153 Configuration Space Map



* 21153-AB only; in the 21153-AA, these registers are R/W Subsystem ID and Subsystem Vendor ID.
** These are reserved in the 21153-AA.

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Table 1 provides the bit definitions of 21153 control and status registers. For a description of these bits, see the *21153 PCI-to-PCI Bridge Data Sheet*.

Table 1. Bit Definitions (Sheet 1 of 5)

Primary Command Register—Offset 04h (Dword address 04h)		
Field Bit	**Dword Bit**	**Description**
0	0	I/O space enable
1	1	Memory space enable
2	2	Master enable
3	3	Special cycle enable
4	4	Memory write and invalidate enable
5	5	VGA snoop enable‘
6	6	Parity error response
7	7	Wait cycle control
8	8	SERR# enable
9	9	Fast back-to-back enable
15:10	15:10	Reserved

Primary Status Register—Offset 06h (Dword address 04h)		
Field Bit	**Dword Bit**	**Description**
3:0	19:16	Reserved
4	20	ECP enable[1]
5	21	66-MHz capable
6	22	Reserved
7	23	Fast back-to-back capable
8	24	Data parity detected
10:9	26:25	DEVSEL# timing
11	27	Signaled target abort
12	28	Received target abort
13	29	Received master abort
14	30	Signaled system error
15	31	Detected parity error

1. 21153-AB and later revisions only. This capability is not supported in the 21153-AA.

Table 1. Bit Definitions (Sheet 2 of 5)

Secondary Status Register—Offset 1Eh (Dword Address 1Ch)		
Field Bit	**Dword Bit**	**Description**
4:0	20:16	Reserved
5	21	66-MHz capable
6	22	Reserved
7	23	Fast back-to-back capable
8	24	Data Parity detected
10:9	26:25	**s_devsel_l** timing
11	27	Signaled target abort
12	28	Received target abort
13	29	Received master abort
14	30	Received system error
15	31	Detected parity error

Bridge Control Register—Offset 3Eh (Dword address 3Ch)		
Field Bit	**Dword Bit**	**Description**
0	16	Parity error response
1	17	SERR# forward enable
2	18	ISA enable
3	19	VGA enable
4	20	Reserved
5	21	Master abort mode
6	22	Secondary bus reset
7	23	Fast back-to-back enable
8	24	Primary master timeout
9	25	Secondary master timeout
10	26	Master timeout status
11	27	Master timeout SERR# enable
15:12	31:28	Reserved

Chip Control Register—Offset 40h (Dword address 40h)		
Field Bit	**Dword Bit**	**Description**
0	0	Reserved
1	1	Memory write disconnect control
3:2	3:2	Reserved
4	4	Secondary bus prefetch disable
5	5	Live insertion mode
7:6	7:6	Reserved

Table 1. Bit Definitions (Sheet 3 of 5)

Diagnostic Control Register—Offset 41h (Dword address 40h)		
Field Bit	**Dword Bit**	**Description**
0	8	Chip reset
2:1	10:9	Test mode
7:3	15:11	Reserved

Arbiter Control Register—Offset 42h (Dword address 40h)		
Field Bit	**Dword Bit**	**Description**
10:0	25:16	Arbiter control
15:11	31:26	Reserved

p_serr_l Event Disable Register—Offset 64h (Dword address 64h)		
Field Bit	**Dword Bit**	**Description**
0	0	Reserved
1	1	Posted write parity error
2	2	Posted write nondelivery
3	3	Target abort during posted write
4	4	Master abort on posted write
5	5	Delayed write nondelivery
6	6	Delayed read - no data from target
7	7	Reserved

gpio Output Data Register—Offset 65h (Dword address 64h)		
Field Bit	**Dword Bit**	**Description**
3:0	11:8	**gpio** output write-1-to-clear
7:4	15:12	**gpio** output write-1-to-set

gpio Output Enable Control Register—Offset 66h (Dword address 64h)		
Field Bit	**Dword Bit**	**Description**
3:0	19:16	**gpio** output enable write-1-to-clear
7:4	23:20	**gpio** output enable write-1-to-set

gpio Input Data Register—Offset 67h (Dword address 64h)		
Field Bit	**Dword Bit**	**Description**
3:0	27:24	Reserved
7:4	31:28	**gpio** input

Table 1. Bit Definitions (Sheet 4 of 5)

Secondary Clock Control Register—Offset 68h (Dword address 68h)		
Field Bit	**Dword Bit**	**Description**
1:0	1:0	Slot 0 clock disable
3:2	3:2	Slot 1 clock disable
5:4	5:4	Slot 2 clock disable
7:6	7:6	Slot 3 clock disable
8	8	Device 1 clock disable
9	9	Device 2 clock disable
10	10	Device 3 clock disable
11	11	Device 4 clock disable
12	12	Device 5 clock disable
13	13	The 21153 clock disable
15:14	15:14	Reserved

p_serr_l Status Register—Offset 6Ah (Dword address 68h)		
Field Bit	**Dword Bit**	**Description**
0	16	Address parity error
1	17	Posted write data parity error
2	18	Posted write nondelivery
3	19	Target abort during posted write
4	20	Master abort during posted write
5	21	Delayed write nondelivery
6	22	Delayed read-no data from target
7	23	Delayed transaction master timeout

Power Management Capabilities Register—Offset DEh (Dword address DCh)[1]		
Field Bit	**Dword Bit**	**Description**
2:0	18:16	Power management revision
3	19	PME# clock required
4	20	Auxiliary power support
5	21	Device-specific initialization
8:6	24:22	Reserved
9	25	D1 power state support
10	26	D2 power state support
15:11	31:27	PME# support

1. 21153-AB and later revisions only. This capability is not supported in the 21153-AA.

Table 1. Bit Definitions (Sheet 5 of 5)

Power Management Control and Status Register—Offset E0h (Dword address E0h[1]		
Field Bit	**Dword Bi**	**Description**
1:0	1:0	Power state (PWR_STATE)
7:2	7:2	Reserved
8	8	PME# enable (PME_EN)
12:9	12:9	Data select (DATA_SEL)
14:13	14:13	Data scale (DATA_SCALE)
15	15	PME# status (PME_STAT)

1. 21153-AB only. In the 21153-AA, these registers are reserved.

PPB Support Extensions Register—Offset E2h (Dword address E0h)[1]		
Field Bit	**Dword Bit**	**Description**
5:0	21:16	Reserved
6	22	B2_B3 support
7	23	Bus power/clock control enable (BPCC_EN)

1. 21153-AB only. In the 21153-AA, these registers are reserved.

4.0 Initial Conditions

After system reset, the 21153 is initialized to the following state:

- Memory, I/O and master enables all reset to zero (disabled). The 21153 does not respond to any memory or I/O transactions on either the primary or secondary bus.
- Primary, secondary, and subordinate bus numbers are all reset to zero. You must initialize these bus numbers before you can configure any devices downstream of the 21153.
- Prefetchable memory, nonprefetchable memory, and I/O base and limit address registers are all zero. This does not mean that these address ranges are turned off. In fact, a memory range of addresses 000FFFFF (hex) - 00000000 (hex) and an I/O range of addresses 0FFF (hex) - 0000 (hex) are defined for downstream forwarding. Because the enables are off, no memory or I/O transactions are forwarded, however. Before turning on those enables, initialize these address ranges. To turn off downstream forwarding, set the address base to a value greater than the address limit.
- The primary and secondary master latency timers are set to zero. The 21153 will relinquish the bus after the first data transfer when the 21153's primary bus grant has been deasserted. The single exception is Memory Write and Invalidate (MWI) transactions.
- Cache line size is set to zero. No cache line boundaries are observed, and memory write and invalidate commands are forwarded as memory write commands.
- Parity checking, **p_serr_l** assertion, VGA modes, and ISA modes are all disabled.
- All device-specific features are disabled (reset to 0).

4.1 Configuration Register Values After Reset

Table 2 lists the value of the 21153 configuration registers after reset. Reserved registers are not listed and are always read as zero.

Table 2. Configuration Register Values After Reset (Sheet 1 of 2)

Byte Address	Register Name	Reset Value
00-01h	Vendor ID	1011h
02-03h	Device ID	0025h
04-05h	Primary command	0000h
06-07h	Primary status	0280h[1] 0290h[2]
08h	Revisions ID	Initially 00h[3]
09-0Bh	Class Code	060400h
0Ch	Cache line size	00h
0Dh	Primary latency timer	00h
0Eh	Header type	01h
18h	Primary bus number	00h
19h	Secondary bus number	00h
1Ah	Subordinate bus number	00h
1Bh	Secondary latency timer	00h
1Ch	I/O base address	01h
1Dh	I/O limit address	01h
1E-1Fh	Secondary status	0280h
20-21h	Memory base address	0000h
22-23h	Memory limit address	0000h
24-25h	Prefetchable memory base address	0001h
26-27h	Prefetchable memory limit address	0001h
28-2Bh	Prefetchable memory base address upper 32 bits	00000000h
2C-2Fh	Prefetchable memory limit address upper 32 bits	00000000h
30-31h	I/O base address upper 16 bits	0000h
32-33h	I/O limit address upper 16 bits	0000h
34-35h	Subsystem vendor ID	0000h[1]
34h	ECP Pointer	00DCh[2]
36-37h	Subsystem ID	0000h[1]
3Dh	Interrupt pin	00h
3E-3Fh	Bridge control	0000h
40h	Chip control	00h
41h	Diagnostic control	00h
42-43h	Arbiter control	0200h
64h	**p_serr_l** event disable	00h
65h	**gpio** output data	00h
66h	**gpio** output enable control	00h
67h	**gpio** input data	00h
68-69h	Secondary clock control[4]	—

Table 2. Configuration Register Values After Reset (Sheet 2 of 2)

Byte Address	Register Name	Reset Value
6Ah	**p_serr-l** status	00h
DCh	Capability ID	01h[5]
DDh	Next item ptr	00h[5]
DE-DFh	Power Management capabilities	0001h[5]
E0-E1h	Power management CSR	0000h[5]
E2h	PPB support extensions	00h(**bpcce**=1)[5]
E3h	Data register	00h[5]

NOTES:
1. 21153-AA only.
2. 21153-AB and later revisions.
3. Dependent on the revision of the device. The first revision is read as 00h; subsequent revisions increment by 1.
4. The value of this register is dependent upon the serial clock disable shift function that occurs during secondary bus reset.
5. 21153-AB only. In the 21153-AA, these registers are reserved.

4.2 Arbiter Values After Reset

After reset, the 21153 is initialized to the following state:

- All external masters are assigned to the low priority group, and the 21153 is assigned to the high priority group. The 21153 receives highest priority on the target bus every other transaction, and priority rotates evenly among the other masters.
- The 21153 parks the secondary bus at itself until transactions start occurring on the secondary bus. After a transaction has occurred, the secondary bus is parked at the last master to use the bus. If the internal arbiter is disabled, the 21153 parks the secondary bus only when the reconfigured grant signal, **s_req_1<0>**, is asserted and the secondary bus is idle.

5.0 System Initialization

The *PCI-to-PCI Bridge Architecture Specification* provides guidelines for initialization. Some of this information is included here to aid initialization code development.

When the 21153 or any other PCI-to-PCI bridge is present in a system, either on the system board or on a PCI option card, system BIOS or system firmware is required to provide the following functions during the initialization process:

- Assigning PCI bus numbers
- Allocating address ranges (prefetchable memory, nonprefetchable memory, and I/O)
- Writing the interrupt request (IRQ) number into each device
- Initializing the PCI display subsystem (if present)

The JTAG test access port controller and the instruction register output latches are initialized when the **trst_1** input is asserted. The test access port controller enters the test-logic reset state. The instruction register is reset to hold the bypass register instruction. During test-logic reset state, all JTAG test logic is disabled, and the chip performs normal functions. The test access port controller leaves this state only when an appropriate JTAG test operation sequence is sent on the **tms** and **tck** pins.

6.0 Assigning PCI Bus Numbers

The system BIOS must assign PCI bus numbers to each PCI-to-PCI bridge in the system. The order of the PCI bus numbers and when they are assigned is not specified.

The following requirements must be followed:

- All buses located downstream of a PCI-to-PCI bridge must reside between the secondary bus number and the subordinate bus number (inclusive).
- Bus number ranges in parallel branches of PCI bus hierarchy must be mutually exclusive.

7.0 Allocating Address Ranges

The system BIOS must map all devices residing behind the bridge into one of the 21153 address ranges. Address ranges supported by the 21153 are I/O space, prefetchable memory, and nonprefetchable memory (also called memory-mapped I/O). As shown in Table 3, the address ranges have the following characteristics:

Table 3. Characteristics of Address Ranges

Address Range	Maximum Range	Minimum Granularity
I/O	2^{32} Bytes (4GB)	4KB
Prefetchable memory	2^{64} Bytes	1MB
Nonprefetchable memory (memory-mapped I/O)	2^{32} Bytes (4GB)	1MB

8.0 Mapping I/O Space Using ISA Mode

When an ISA or EISA bus is in the system, I/O space can become fragmented. An ISA address uses only 10 bits of addressing, giving a maximum 1KB of address space. Because ISA devices decode only the lowest 10 bits, these addresses are aliased throughout the entire I/O space.

The bottom 256 bytes of a 1 KB chunk point to system-specific addresses. The top 768 bytes are used for general I/O. EISA systems use the entire 64KB space by dividing the space into 16, 4 KB slots, and use a slot-specific control strobe to point to a particular slot. Slot 0 is generally allocated to the motherboard.

PCI-to-PCI and PCI-to-EISA bridges typically perform full 32-bit addressing, using positive decoding for the bottom 256 bytes of the first 1K chunk and subtractive decoding for the upper 768 bytes of each 1K chunk. Although the top 768 bytes of each chunk might be used for general ISA/EISA devices, the bottom 256 bytes in all slots except for slot 0 (the bottom 4K slots) are available for use by PCI devices.

The 21153 provides a mode that allows mapping into the low 256 bytes of each 1K chunk. When the ISA mode bit is set, the 21153 forwards only downstream transactions addressing the low 256 bytes of each 1 K chunk inside the defined address range. This allows mapping of PCI devices into I/O space when there is an ISA or EISA bus in the system. When mapping a device downstream of the 21153 with ISA mode set, bits <9:8> of the device's I/O base address should be 00.

9.0 Using the 21153 Modes

The 21153 can be configured to support VGA-compatible devices.

When a VGA-compatible device is located downstream of a PCI-to-PCI bridge, set the VGA mode bit in 21153 configuration space in every PCI-to-PCI bridge between the VGA device and the most primary PCI bus. Setting this bit configures the 21153 to pass all VGA frame buffer memory addresses and all VGA I/O addresses downstream.

When a graphics device that does not have VGA-compatibility is located downstream of the 21153, you must configure the bridge to forward only VGA palette writes by setting the VGA snoop bit in the 21153 configuration space. This bit must be set in every PCI-to-PCI bridge between the most primary PCI bus and the graphics device.

If both types of devices are located downstream of the 21153, setting the VGA mode bit is sufficient for proper operation. Setting both the VGA mode and the VGA snoop bits results in the same behavior as setting only the VGA mode bit.

For more information about VGA support in PCI systems, refer to the *PCI-to-PCI Bridge Architecture Specification.*

10.0 Sample 21153 Initializations

This section provides several sample initializations of the 21153.

10.1 Initializing the 21153 for Hierarchical Configuration Accesses

To initialize the 21153 so that configuration transactions can be forwarded, use the values in Table 4 to write the following bridge configuration registers (values in hex):

Table 4. Bridge Configuration Register Values

Dword Offset	Register	Value	Notes
04h	Primary status/command	FFFF0000h	Clear all status bits. Make sure memory, I/O, and master enables are turned off.
18h	Subordinate/secondary/primary bus numbers	00xxyyzzh	xx=subordinate bus number yy=secondary bus number zz=primary bus number

The important points are:

- Turn off memory, I/O, and master enables to prevent memory and I/O transactions from crossing the bridge.
- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.

10.2 Initializing the 21153 for I/O and Configuration Forwarding

To initialize the 21153 so that I/O and configuration transactions can be forwarded, use the values in Table 5 to write the following bridge configuration registers (values in hex):

Table 5. I/O and Configuration Transaction Values

Dword Offset	Register	Value	Notes
18h	Subordinate/secondary/primary bus numbers	00xxyyzzh	xx=subordinate bus number yy=secondary bus number zz=primary bus number
1Ch	Secondary status/ I/O limit address/ I/O base address	FFFFx0yh	Clear status bits. x=I/O limit address bits <15:12> y=I/O base address bits <15:12>
20h	Memory limit/memory base	0000FFFFh	Turn off downstream memory address range.
24h	PF memory limit/ PF memory base	0000FFFFh	Turn off downstream PF memory address range.
3Ch	Bridge control	000x0000h	x=0 (no ISA bus in system) x=4 (ISA bus in system)
04h	Primary status/command	FFFF0005h	Clear status bits. Turn on I/O enable for downstream I/O. Turn on master enable for upstream I/O. **Write this register last**.

The important points are:

- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.
- Initialize I/O base and limit registers to define a downstream window.
- Turn off both memory ranges.
- If an (E)ISA bus is in the system, turn on ISA mode.
- Turn on I/O and master enables. **Write this register last.**

Note: Setting the master enable bit also enables forwarding of the memory transactions upstream.

10.3 Initializing the 21153 for Memory and Configuration Forwarding

To initialize the 21153 so that memory and configuration transactions can be forwarded, use the values in Table 6 to write the following bridge configuration registers (values in hex):

Table 6. Memory and Configuration Transactions

Dword Offset	Register	Value	Notes
18h	Subordinate/secondary/primary bus numbers	00xxyyzzh	xx=subordinate bus number yy=secondary bus number zz=primary bus number
1Ch	Secondary status/ I/O limit address/ I/O base address	FFFF00FFh	Clear status bits. Turn off I/O address range.
20h	Memory limit/ memory base	xxx0yyy0h	xxx=nonprefetchable memory limit address <31:20> yyy=nonprefetchable memory base address <31:20>
24h	PF memory limit/ PF memory base	xxx0yyy0h	xxx=prefetchable memory limit address <31:20> yyy=prefetchable memory base address <31:20>
04h	Primary status/command	FFFF0006h	Clear status bits. Turn on memory enable for downstream memory. Turn on master enable for upstream memory. **Write this register last**.

The important points are:

- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.
- Turn off I/O range.
- Initialize either or both nonprefetchable and prefetchable memory ranges.
- Turn on memory and master enables. **Write this register last.**

Note: Setting the master enable bit also enables forwarding of the I/O transactions upstream.

10.4 Initializing the 21153 for Memory, I/O, and Configuration Forwarding

To initialize the 21153 so that memory, I/O, and configuration transactions can be forwarded, use the values in Table 7 to write the following bridge configuration registers (values in hex):

Table 7. Memory, I/O, and Configuration Transactions

Dword Offset	Register	Value	Notes
18h	Subordinate/Secondary/primary bus numbers	00xxyyzzh	xx-subordinate bus number yy=secondary bus number zz=primary bus number
1Ch	Secondary status/ I/O limit address I/O base address	FFFFx0y0h	Clear status bits. x=I/O limit address bits <15:12> y=I/O base address bits <15:12>
20h	Memory limit/memory base	xxx0yyy0h	xxx=prefetchable memory limit address <31:20> yyy=nonprefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
24h	PF memory limit/PF memory base	xxx0yyy0h	xxx=prefetchable memory limit address <31:20> yyy=prefetchable memory base address <31:20> To disable this range, write 0000FFFFh.
3Ch	Bridge control	000x0000h	x=0 (no ISA bus in system) x=4 (ISA bus in system)
04h	Primary status/command	FFFF0007h	Clear status bits. Turn on I/O enable for downstream I/O. Turn on memory enable for downstream memory. Turn on master enable for upstream memory and I/O. **Write this register last**.

The important points are:

- Initialize PCI bus numbers for forwarding of configuration transactions across the bridge.
- Initialize the I/O range.
- Initialize either or both nonprefetchable and prefetchable memory ranges.
- Turn on memory and master enables. **Write this register last.**

11.0 Initializing VGA Modes in the 21153

The following sections provide examples of initializing VGA mode and VGA snoop mode.

11.1 VGA Mode

If a VGA device resides behind the 21153, enable VGA mode. To enable VGA mode, write bit 18 of configuration address 3Ch. Simply modify the contents of the write to this register shown in previous sections. For example:

Dword Offset	Register	Value	Notes
3Ch	Bridge control	000x0000h	x=8 (VGA mode; no ISA bus in system) x=C (VGA mode; ISA bus in system

You must write this register before memory, I/O, and master enables located at configuration address 04h are set.

11.2 VGA Snoop Mode

If a graphics device requiring VGA snoop mode resides behind the 21153, you must write bit 5 of configuration address 04h. Simply modify the contents of the write to this register shown in previous sections. For example:

Dword Offset	Register	Value	Notes
04h	Primary status/command	FFFF002xh	x=7 (Set memory, I/O, and master enable if all memory and I/O ranges are used) x=5 (Set I/O and master enable if only the I/O range is used

12.0 Initializing Optional Registers in the 21153

This section describes initialization of optional 21153 features. The features are not required for basic bridge operation. It is recommended that you write these registers before (or in the same access as) setting the memory, I/O, and master enables in configuration address 04h. Otherwise, order is not important.

12.1 Enabling Parity and Checking Errors

Table 8 lists the accesses to enable parity checking on both interfaces and to forward **serr#** from the secondary to the primary interface.

Table 8. Enabling Parity and Checking Errors

Dword Offset	Register	Value	Notes
3Ch	Bridge control	000x0000h	x=3 (No ISA bus in system, no VGA behind 21153) x=7 (ISA bus in system, no VGA behind 21153) x=B (No ISA bus in system, VGA behind 21153) x=F (ISA bus in system, VGA behind 21153)
04h	Primary status/ command	FFFF01xyh	Clear status bite. x=4 (No VGA snoop mode) x=6 (VGA snoop mode) y=[0,5,6,7] ([Configuration only, I/O only, memory only, all] enabled for downstream forwarding) **Write this register last**.

12.2 Enabling Timers and Setting Cache Line Size

Table 9 lists the accesses to enable the master latency timers, the target wait timers, and the burst count to desired values. The setting of cache line size is also shown.

Table 9. Enabling Timers and Setting Cache Line Size

Dword Offset	Register	Value	Notes
0Ch	Primary MLT/cache line size	0000xxyyh	xx=primary master latency timer value (low 3 bits=0) yy=cache line size
18h	Secondary MLT/subordinate/ secondary/primary bus numbers	wwxxyyzzh	ww=secondary master latency timer value (low 3 bits=0) xx=subordinate bus number yy=secondary bus number zz=primary bus number

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