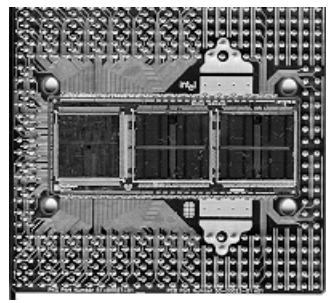
PENTIUM® PRO PROCESSOR WITH 1 MB L2 CACHE AT 200 MHZ

- **Large integrated cache for multiprocessing systems**
- **Binary compatible with applications running on previous members of the Intel microprocessor family**
- **Optimized for 32-bit applications running on advanced 32-bit operating systems**
- **Dynamic Execution microarchitecture**
- **Single package includes Pentium® Pro processor CPU, cache and system bus interface**
- **Scaleable up to four processors and 4 GB memory**
- **Separate dedicated external system bus, and dedicated internal full-speed cache bus**
- **8 KB/8 KB separate data and instruction, nonblocking, level one cache**
- **Data integrity and reliability features include ECC, Fault Analysis/Recovery, and Functional Redundancy Checking**
- **Fits Intel Pentium Pro processor 387-Pin Socket 8**
  - **— Meets All AC timings and levels of Pentium Pro processor**
  - **— 50% lighter package vs. ceramic**
  - **— Scratch resistant anodized aluminum heat spreader**
  - **— Designed for LIF and ZIF sockets**

The Pentium® Pro processor with 1 MB L2 cache is designed for high-end 4 way multiprocessor capable server systems. The Pentium Pro processor with 1 MB L2 cache delivers more performance than previous generation processors through an innovation called Dynamic Execution. This is the next step beyond the superscalar architecture implemented in the Pentium processor. This makes possible the advanced 3D visualization and interactive capabilities required by today's high-end commercial and technical applications and tomorrow's emerging applications. The Pentium Pro processor with 1 MB L2 cache also includes advanced data integrity, reliability, and serviceability features for mission critical applications.



January 1998

Order Number: 243570-001

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FIGURES

TABLES

1.0. INTRODUCTION

The Pentium Pro processor with 1 MB L2 cache is a multichip module targeted for use in high-end 4-way multiprocessor capable server systems. The component package contains an Intel Pentium Pro processor core, and 1 MB of L2 cache. The 1 MB cache is built using two of the 512 KB SRAM die found in the 512 KB version of the Pentium Pro processor. While the 512 K version uses a conventional ceramic package, the Pentium Pro processor with 1 MB L2 cache integrates the three die in a plastic package with an aluminum heat spreader. This 387-pin package is compatible with the current Pentium Pro processor footprint. The Pentium Pro processor with 1 MB L2 cache routes all of the processor's high-speed cache interface bus through balanced nets on a thin film interconnect substrate to the two L2 SRAMs. This allows for internal component operation speeds of 200 MHz between the Pentium Pro processor and the L2 cache die.

Figure 1 shows how a typical Pentium Pro processor system is implemented.

1.1. Terminology

A '#' symbol after a signal name refers to an active low signal. This means that a signal is in the active state (based on the name of the signal) when driven low. For example, when FLUSH# is low a flush has been requested. When Nonmaskable Interrupt (NMI) is high, a nonmaskable interrupt has occurred. In the case of lines where the name does not imply an active state but describes part of a binary sequence (such as address or data), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D#[3:0] = 'LHLH' also refers to a hex 'A'. (H= High logic level, L= Low logic level)

The word **Preliminary** appears occasionally. Check with your local Field Applications Engineer for recent information.

1.2. References

The following are referenced within this specification:

- *Pentium® Pro Processor I/O Buffer Models—IBIS Format* (on World Wide Web page http://www.intel.com)
- AP-523, *Pentium® Pro Processor Power Distribution Guidelines* (Order Number 242764)
- AP-524, *Pentium® Pro Processor GTL+ Layout Guidelines* (Order Number 242765)
- AP-525, *Pentium® Pro Processor Thermal Design Guidelines* (Order Number 242766)
- *Pentium® Pro Processor Family Developer's Manual, Volume 1: Specifications* (Order Number 242690)
- *Pentium® Pro Processor Family Developer's Manual, Volume 2: Programmer's Reference Manual* (Order Number 242691)
- *Pentium® Pro Processor Family Developer's Manual, Volume 3: Operating System Writer's Guide* (Order Number 242692)
- *Pentium® Pro Specification Update* (Order Number 242689)

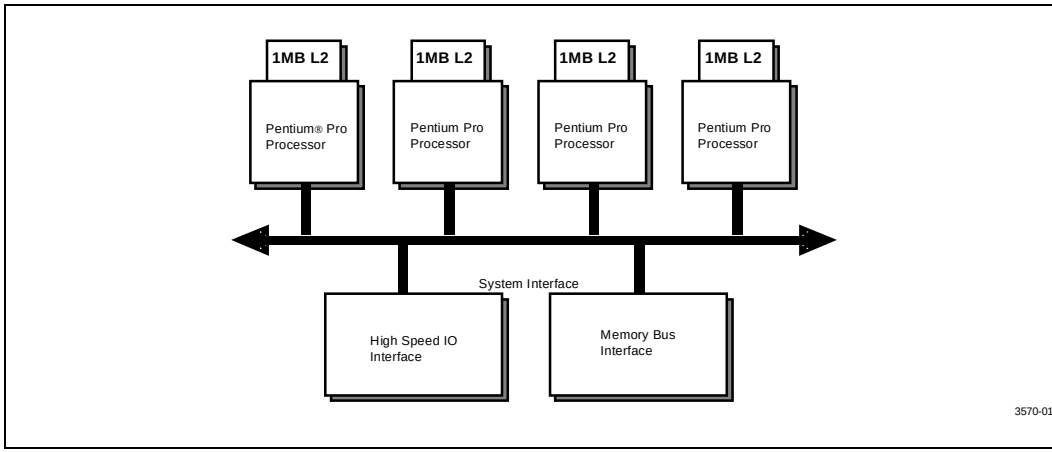


Figure 1. Pentium® Pro Processor with 1 MB L2 Cache Block Diagram

2.0. ELECTRICAL SPECIFICATIONS

2.1. The Pentium® Pro Processor Bus and V_{REF}

Most of the Pentium Pro processor signals use a **variation** of the low voltage Gunning Transceiver Logic (GTL) signaling technology.

The Pentium Pro processor bus specification is similar to the GTL specification but has been enhanced to provide larger noise margins and reduced ringing. This is accomplished by increasing the termination voltage level and controlling the edge rates. Because this specification is different from the standard GTL specification, it is referred to as **GTL+** in this document.

The GTL+ signals are open-drain and require external termination to a supply that provides the high signal level. The GTL+ inputs use differential receivers which require a reference signal (V_{REF}). Termination (usually a resistor on each end of the signal trace) is used to pull the bus up to the high voltage level and to control reflections on the stub-free transmission line. V_{REF} is used by the receivers to determine if a signal is a logical 0 or a logical 1. See Table 8 for the bus termination voltage specifications for GTL+, and Section 4.0. for the GTL+ Interface Specification.

There are 8 V_{REF} pins on the Pentium Pro processor to ensure that internal noise will not affect the performance of the I/O buffers. Pins A1, C7, S7 and Y7 (V_{REF}[3:0]) must be tied together and pins A47, U41, AE47 and AG45 (V_{REF}[7:4]) must be tied together. The two groups may also be tied to each other if desired.

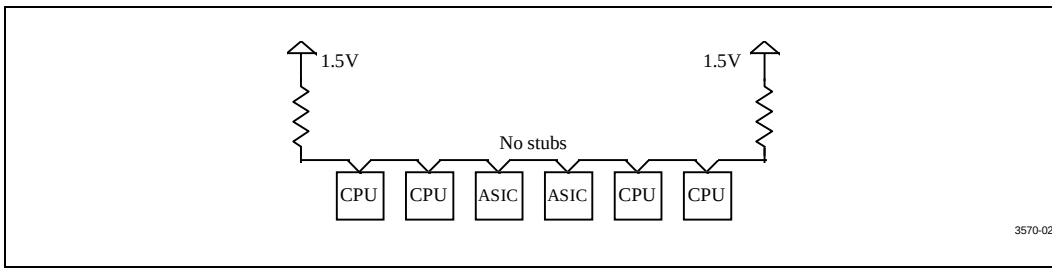


Figure 2. GTL+ Bus Topology

The GTL+ bus depends on incident wave switching. Therefore timing calculations for GTL+ signals are based on **flight time** as opposed to capacitive deratings. Analog signal simulation of the Pentium Pro processor bus including trace lengths is highly recommended when designing a system with a heavily loaded GTL+ bus. See Intel's World Wide Web page (http://www.intel.com) to download the buffer models for the Pentium Pro processor in IBIS format.

2.2. Power Management: Stop Grant and Auto HALT

The Pentium Pro processor allows the use of Stop Grant and Auto HALT modes to immediately reduce the power consumed by the device. When enabled, these cause the clock to be stopped to most of the CPU's internal units and thus significantly reduces power consumption by the CPU as a whole.

Stop Grant is entered by asserting the STPCLK# pin of the Pentium Pro processor. When STPCLK# is recognized by the Pentium Pro processor, it will stop execution and will not service interrupts. It will continue snooping the bus. Stop Grant power is specified assuming no snoop hits occur.

Auto HALT is a low-power state entered when the Pentium Pro processor executes a halt (HLT) instruction. In this state, the Pentium Pro processor behaves as if it executed a halt instruction, and it additionally powers-down most internal units. In Auto HALT, the Pentium Pro processor will recognize all interrupts and snoops. Auto HALT power is specified assuming no snoop hits or interrupts occur.

The low-power stand-by mode of Stop Grant or Auto HALT can be defined by a **Low-Power Enable** configuration bit to be either the lowest power achievable by the Pentium Pro processor (Stop Grant power), or a power state in which the clock distribution is left running (Idle power). "Low-power stand-by" **disabled** leaves the core logic running, while "Low-power stand-by" **enabled** allows the Pentium Pro processor to enter its lowest power mode.

2.3. Power and Ground Pins

There are 4 pins defined on the package for voltage identification (VID). These pins specify the voltage required by the CPU die. These have been added to cleanly support voltage specification variations on the Pentium Pro processor and future processors. See Section 2.6. for an explanation of the voltage identification pins.

For clean on-chip power distribution, the Pentium Pro processor has 47 V_{CC} (power) and 101 V_{SS} (ground) inputs. On the circuit board, **all** V_{CC}P pins must be connected to a voltage island. Similarly, **all** V_{SS} pins must be connected to a system ground plane. See Figure 26 for the locations of power and ground pins.

2.4. Decoupling Recommendations

Due to the large number of transistors and high internal clock speeds, the Pentium Pro processor can create large, short duration transient (switching) current surges that occur on internal clock edges which can cause power planes to spike above and below their nominal value if not properly controlled. The Pentium Pro processor is also capable of generating large average current swings between low and full power states, called **Load-Change Transients**, which can cause power planes to sag below their nominal value if bulk decoupling is not adequate. See Figure 3 for an example of these current fluctuations. Care must be taken in the board design to guarantee that the voltage provided to the Pentium Pro processor remains within the specifications listed in this volume. Failure to do so may result in timing violations and/or a reduced lifetime of the component.

Adequate decoupling capacitance should be placed near the power pins of the Pentium Pro processor. Low inductance capacitors such as the 1206 package surface mount capacitors are recommended for the best high frequency electrical performance. Forty (40) 1 µF 1206-style capacitors with a ±22% tolerance make a good starting point for simulations as this is our recommended decoupling when using a Pentium Pro Processor Voltage Regulator Module. Inductance should be reduced by connecting capacitors directly to the V_{CC}P and V_{SS} planes with minimal trace length between the component pads and vias to the plane. Be sure to include the effects of board inductance within the simulation. Also, when choosing the capacitors to use, bear in mind the operating temperatures they will see and the tolerance that they are rated at. Type Y5S or better are recommended (±22% tolerance over the temperature range -30 °C to +85 °C).

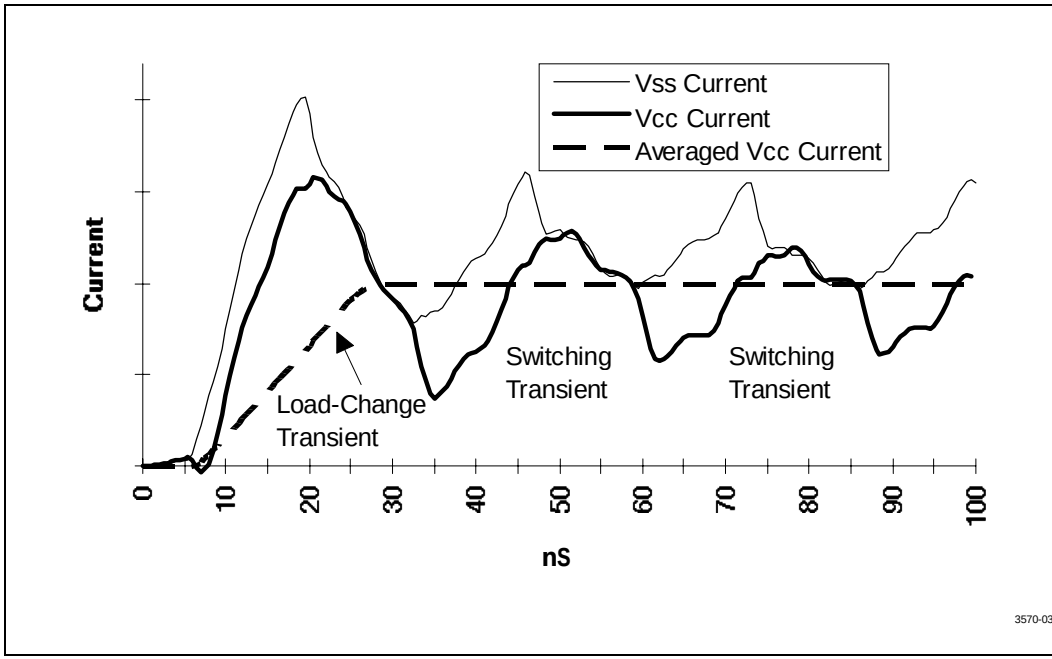


Figure 3. Transient Types

Bulk capacitance with a low Effective Series Resistance (ESR) should also be placed near the Pentium Pro processor in order to handle changes in average current between the low-power and normal operating states. About 4000 µF of capacitance with an ESR of 5 mΩ makes a good starting point for simulations, although more capacitance may be needed to bring the ESR down to this level due to the current technology in the industry. The Pentium Pro Processor Voltage Regulator Modules already contain this bulk capacitance. Be sure to determine what is available on the market before choosing parameters for the models. Also, include power supply response time and cable inductance in a full simulation.

See AP-523, *Pentium® Pro Processor Power Distribution Guidelines* (Order Number 242764), for power modeling for the Pentium Pro processor.

2.4.1. GTL+ DECOUPLING

Although the Pentium Pro processor GTL+ bus receives power external to the Pentium Pro processor, it should be noted that this power supply will also require the same diligent decoupling methodologies as the processor. Notice that the existence of external power entering through the I/O buffers causes the V_{SS} current to be higher than the V_{CC} current as evidenced in Figure 3.

2.4.2. PHASE LOCK LOOP (PLL) DECOUPLING

Isolated analog decoupling is required for the internal PLL. This should be equivalent to 0.1 µF of ceramic capacitance. The capacitor should be type Y5R or better and should be across the PLL1 and PLL2 pins of the Pentium Pro processor. ("Y5R" implies ±15% tolerance over the temperature range -30 °C to +85 °C.)

2.5. BCLK Clock Input Guidelines

The BCLK input directly controls the operating speed of the GTL+ bus interface. All GTL+ external timing parameters are specified with respect to the rising edge of the BCLK input. Clock multiplying within the processor is provided by an internal Phase Lock Loop (PLL) which requires a constant frequency BCLK input. Therefore the BCLK frequency cannot

be changed dynamically. It can however be changed when RESET# is active assuming that all reset specifications are met for the clock and the configuration signals.

The Pentium Pro processor core frequency must be configured during reset by using the A20M#, IGNNE#, LINT1/NMI, and LINT0/INTR pins. The value on these pins during RESET#, and until two clocks beyond the end of the RESET# pulse, determines the multiplier that the PLL will use for the internal core clock. See Appendix A for the definition of these pins during reset. At all other times their functionality is defined as the compatibility signals that the pins are named after. These signals are 3.3 V tolerant and may be driven by existing logic devices. This is important for both functions of the pins.

Supplying a bus clock multiplier this way is required in order to increase processor performance without changing the processor design, and to maintain the bus frequency such that system boards can be designed to function properly as CPU frequencies increase.

2.5.1. SETTING THE CORE CLOCK TO BUS CLOCK RATIO

Table 31 lists the configuration pins and the values that must be driven at reset time in order to set the core clock to bus clock ratio. Figure 4 shows the timing relationship required for the clock ratio signals with respect to RESET# and BCLK. CRESET# from an 82453GX (or 82453KX or 82440FX) is shown since its timing is useful for controlling the multiplexing function that is required for sharing the pins.

Using CRESET# (CMOS reset), the circuit in Figure 5 can be used to share the pins. The pins of the processors are bussed together to allow any one of them to be the compatibility processor. The component used as the multiplexer must not have outputs that drive higher than 3.3 V in order to meet the Pentium Pro processor's 3.3 V tolerant buffer specifications. The multiplexer output current should be limited to 200 mA maximum, in case the $V_{CC}P$ supply to the processor ever fails.

The pull-down resistors between the multiplexer and the processor (1 KΩ) force a ratio of 2x into the processor in the event that the Pentium Pro processor powers up before the multiplexer and/or the chip set. This prevents the processor from ever seeing a ratio higher than the final ratio.

If the multiplexer were powered by $V_{CC}P$, CRESET# would still be unknown until the 3.3 V supply came up to power the CRESET# driver. A pull-down can be used on CRESET# instead of the four between the multiplexer and the Pentium Pro processor. In this case, the multiplexer must be designed such that the compatibility inputs are truly ignored as their state is unknown.

In any case, the compatibility inputs to the multiplexer must meet the input specifications of the multiplexer. This may require a level translation before the multiplexer inputs unless the inputs and the signals driving them are already compatible.

For FRC mode processors, one multiplexer will be needed per FRC pair, and the multiplexer will need to be clocked using BCLK to meet setup and hold times to the processors. This may require the use of high speed programmable logic.

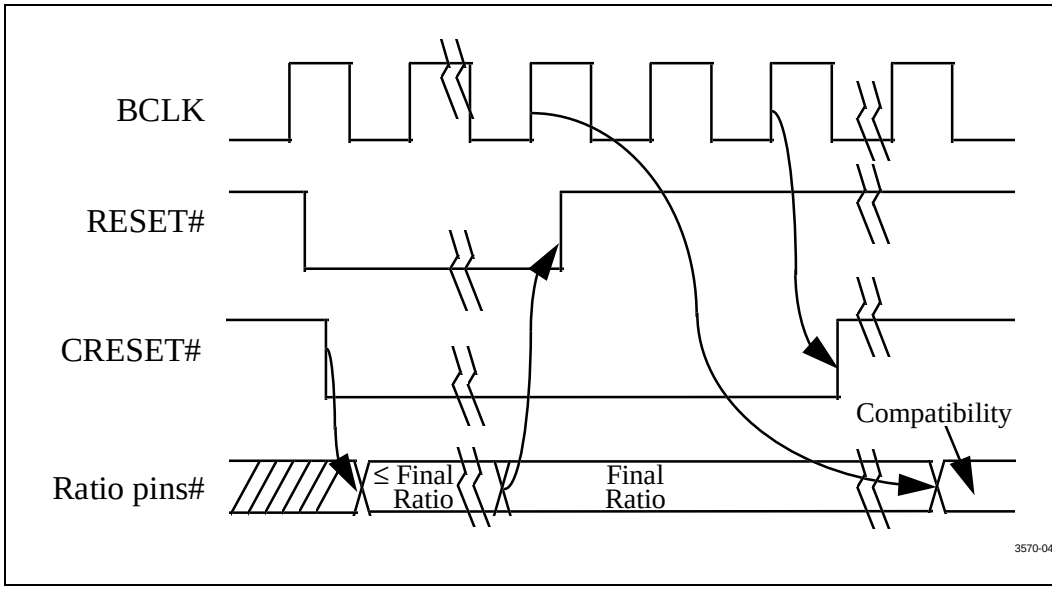


Figure 4. Timing Diagram of Clock Ratio Signals

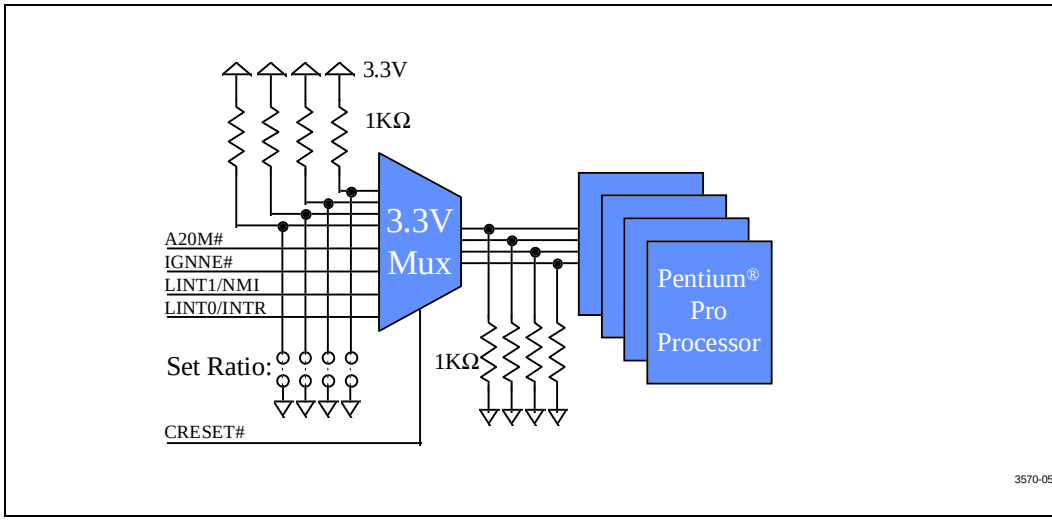


Figure 5. Example Schematic for Clock Ratio Pin Sharing

2.6. Voltage Identification

There are four Voltage Identification Pins on the Pentium Pro processor package. These pins can be used to support automatic selection of power supply voltage. These pins are not signals but are each either an open circuit in the package or a short circuit to V_{SS}.

The opens and shorts define the voltage required by the processor. This has been added to cleanly support voltage specification variations on future Pentium Pro processors. These pins are named VID0 through VID3 and the definition of these pins is shown in Table 1. A '1' in this table refers to an open pin and '0' refers to a short to ground. **The $V_{CC}P$ power supply should supply the voltage that is requested *or* disable itself**.

Table 1. Voltage Identification Definition[1,2]

VID[3:0]	Voltage Setting	VID[3:0]	Voltage Setting
0000	3.5	1000	2.7
0001	3.4	1001	2.6
0010	3.3	1010	2.5
0011	3.2	1011	2.4
0100	3.1	1100	2.3
0101	3.0	1101	2.2
0110	2.9	1110	2.1
0111	2.8	1111	No CPU Present

NOTES:

1. Nominal setting requiring regulation to ±5% at the Pentium® Pro processor $V_{CC}P$ pins under all conditions. Support not expected for 2.1 V—2.3 V.
2. 1= Open circuit; 0= Short to V_{SS}

Support for a wider range of VID settings will benefit the system in meeting the power requirements of future Pentium Pro processors. Note that the '1111' (or all opens) ID can be used to detect the absence of a processor in a given socket as long as the power supply used does not affect these lines.

To use these pins, they may need to be pulled up by an external resistor to another power source. The power source chosen should be one that is guaranteed to be stable whenever the supply to the voltage regulator is stable. This will prevent the possibility of the Pentium Pro processor supply running up to 3.5 V in the event of a failure in the supply for the VID lines. Note that the specification for the Pentium Pro Processor Voltage Regulator Modules allows the use of these signals either as TTL compatible levels or as opens and shorts. Using them as TTL compatible levels will require the use of pull-up resistors to 5 V if the input voltage to the regulator is 5 V and the use of a voltage divider if the input voltage to the regulator is 12 V. The resistors chosen should not cause the current through a VID pin to exceed its specification in Table 3. There must not be any other components on these signals if the VRM uses them as opens and shorts.

2.7. JTAG Connection

The debug port described in the *Pentium® Pro Processor Family Developer's Manual, Volume 1: Specifications* (Order Number 242690), should be at the start and end of the JTAG chain with TDI to the first component coming from the Debug Port and TDO from the last component going to the Debug Port. The recommended pull-up value for Pentium Pro processor TDO pins is 240 Ω. Due to the voltage levels supported by the Pentium Pro processor JTAG logic, it is recommended that the Pentium Pro processors and any other 3.3 V logic level components within the system be first in the JTAG chain. A translation buffer should be used to connect to the rest of the chain unless a 5 V component can be used next that is capable of accepting a 3.3 V input. Similar considerations must be made for TCK, TMS and TRST#. Components may need these signals buffered to match required logic levels.

In a multiprocessor system, be cautious when including empty Pentium Pro processor sockets in the scan chain. All sockets in the scan chain must have a processor installed to complete the chain or the system must support a method to bypass the empty sockets.

See the *Pentium® Pro Processor Family Developer's Manual, Volume 1: Specifications* (Order Number 242690), for full information on putting a debug port in the JTAG chain.

2.8. Signal Groups

In order to simplify the following discussion, signals have been combined into groups by buffer type. **All outputs are open drain** and require an external

high-level source provided externally by the termination or a pull-up resistor.

GTL+ input signals have differential input buffers which use V_{REF} as their reference signal. GTL+ output signals require termination to 1.5 V. Later in this document, the term “GTL+ Input” refers to the GTL+ input group as well as the GTL+ I/O group when receiving. Similarly, “GTL+ Output” refers to the GTL+ output group as well as the GTL+ I/O group when driving.

The 3.3 V tolerant, Clock, APIC and JTAG inputs can each be driven from ground to 3.3 V. The 3.3 V tolerant, APIC, and JTAG outputs can each be pulled high to as much as 3.3 V. See Table 7 for specifications.

The groups and the signals contained within each group are shown in Table 2. Note that the signals ASZ[1:0]#, ATTR[7:0]#, BE[7:0]#, BREQ#[3:0], DEN#, DID[7:0]#, DSZ[1:0]#, EXF[4:0]#, LEN[1:0]#, SMMEM#, and SPLCK# are all GTL+ signals that are shared onto another pin. Therefore they do not appear in this table.

2.8.1. ASYNCHRONOUS VS. SYNCHRONOUS

All GTL+ signals are synchronous. All of the 3.3 V tolerant signals can be applied asynchronously, except when running two processors in FRC mode. To run in FRC mode, synchronization logic is required on all signals (except PWRGOOD) going to both processors. Also note the timing requirements for PICCLK with respect to BCLK. With FRC enabled, PICCLK must be ¼X BCLK and synchronized with respect to BCLK. PICCLK must always lag BCLK by at least 1 ns and no more than 5 ns.

2.9. PWRGOOD

PWRGOOD is a 3.3 V tolerant input. It is expected that this signal will be a **clean** indication that clocks and the system 3.3 V, 5 V and $V_{CC}P$ supplies are stable and within their specifications. Clean implies that the signal will remain low (capable of sinking leakage current) without glitches, from the time that the power supplies are turned on until they come within specification. The signal will then transition monotonically to a high (3.3 V) state. Figure 6 illustrates the relationship of PWRGOOD to other system signals. PWRGOOD can be driven inactive at any time, but power and clocks must again be stable before the rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 13 and be followed by a 1mS RESET# pulse, per Table 10.

This signal must be supplied to the Pentium Pro processor as it is used to protect internal circuits against voltage sequencing issues. Use of this signal is recommended for added reliability.

This signal does not need to be synchronized for FRC operation. It should remain high throughout boundary scan testing.

Table 2. Signal Groups

Group Name	Signals
GTL+ Input	BPRI#, BR[3:1]#[1], DEFER#, RESET#, RS[2:0]#, RSP#, TRDY#
GTL+ Output	PRDY#
GTL+ I/O	A[35:3]#, ADS#, AERR#, AP[1:0]#, BERR#, BINIT#, BNR#, BP[3:2]#, BPM[1:0]#, BR0#, D[63:0]#, DBSY#, DEP[7:0]#, DRDY#, FRCERR, HIT#, HITM#, LOCK#, REQ[4:0]#, RP#
3.3 V Tolerant Input	A20M#, FLUSH#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PREQ#, PWRGOOD[2], SMI#, STPCLK#
3.3 V Tolerant Output	FERR#, IERR#, THERMTRIP#[3]
Clock[4]	BCLK
APIC Clock[4]	PICCLK
APIC I/O[4]	PICD[1:0]
JTAG Input[4]	TCK, TDI, TMS, TRST#
JTAG Output[4]	TDO
Power/Other[5]	CPUPRES#, PLL1, PLL2, TESTHI, TESTLO, UP#, V_{CC}P, V_{CC}5, VID[3:0], V_{REF}[7:0], V_{SS}

NOTES:

1. The BR0# pin is the only BREQ# signal that is bi-directional. The internal BREQ# signals are mapped onto BR# pins after the agent ID is determined.
2. See PWRGOOD in Section 2.9.
3. See THERMTRIP# in Section 2.10.
4. These signals are tolerant to 3.3 V. Use a 150 Ω pull-up resistor on PICD[1:0] and 240Ω on TDO.
5. CPUPRES# is a ground pin defined to allow a designer to detect the presence of a processor in a socket. (preliminary)
   PLL1 and PLL2 are for decoupling the internal PLL (see Section 2.4.2.).
   TESTHI pins should be tied to V_{CC}P. A 10K pull-up may be used. See Section 2.11.
   TESTLO pins should be tied to V_{SS}. A 1K pull-down may be used. See Section 2.11.
   UP# is an open in the Pentium® Pro processor.
   V_{CC}P is the primary power supply.
   V_{CC}5 is unused by Pentium Pro processor.
   VID[3:0] lines are described in Section 2.6.
   V_{REF} [7:0] are the reference voltage pins for the GTL+ buffers.
   V_{SS} is ground.

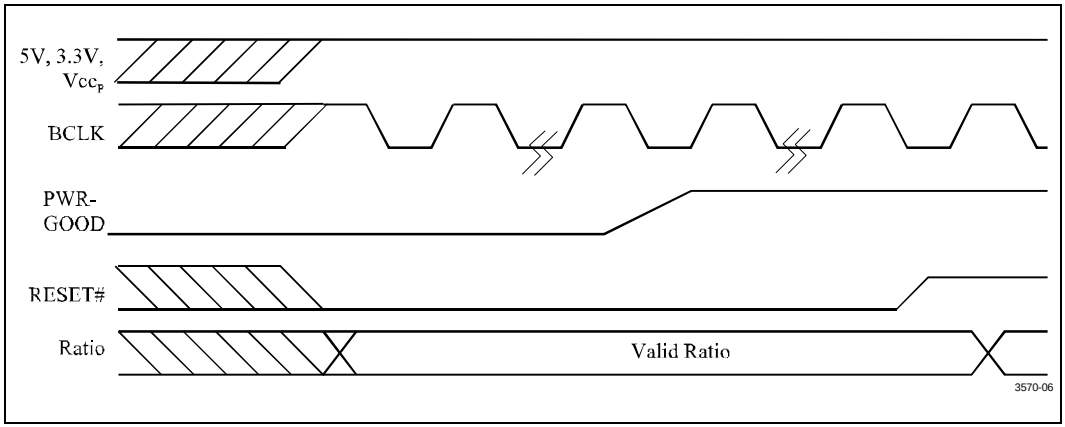


Figure 6. PWRGOOD Relationship at Power-On

2.10. THERMTRIP#

The Pentium Pro processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds ~135 °C. This is signaled to the system by the THERMTRIP# pin. Once activated, the signal remains latched, and the processor stopped, until RESET# goes active. There is no hysteresis built into the thermal sensor itself, so as long as the die temperature drops below the trip level, a RESET# pulse will reset the processor and execution will continue. If the temperature has not dropped beyond the trip level, the processor will continue to drive THERMTRIP# and remain stopped.

2.11. Unused Pins

All RESERVED pins must remain unconnected. All pins named TESTHI must be pulled up, no higher than $V_{CC}P$, and may be tied directly to $V_{CC}P$. All pins named TESTLO must be pulled low and may be tied directly to V_{SS}.

PICCLK must be driven with a clock input, and the PICD[1:0] lines must each be pulled-up to 3.3 V with a separate 150 Ω resistor, even when the APIC will not be used.

For reliable operation, always connect unused inputs to an appropriate signal level. Unused GTL+ inputs should be pulled-up to V_{TT}. Unused active low 3.3 V tolerant inputs should be connected to 3.3 V with a 150 Ω resistor and unused active high inputs should be connected to ground (V_{SS}). A resistor must also be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for fully testing the processor after board assembly.

For unused pins, it is suggested that ~10 KΩ resistors be used for pull-ups (except for PICD[1:0] discussed above), and ~1 KΩ resistors be used as pull-downs. **Never tie a pin directly to a supply other than the processor's own $V_{CC}P$ supply or to V_{SS}.**

2.12. Maximum Ratings

Table 3 contains Pentium Pro processor stress ratings only. Functional operation at the absolute maximum and minimum is not implied nor guaranteed. The Pentium Pro processor should not receive a clock while subjected to these conditions. Functional operating conditions are given in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability. Furthermore, although the Pentium Pro processor contains protective circuitry to resist damage from static electric discharge, one should always take precautions to avoid high static voltages or electric fields.

Table 3. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit	Notes
$T_{Storage}$	Storage Temperature	-65	40	°C	
T_{Bias}	Case Temperature under Bias	-65	110	°C	
$V_{CC}P$(Abs)	Primary Supply Voltage with respect to V_{SS}	-0.5	Operating Voltage + 1.4	V	2
V_{IN}	GTL+ Buffer DC Input Voltage with respect to V_{SS}	-0.5	$V_{CC}P$+ 0.5 but not to exceed 4.3	V	3
V_{IN3}	3.3 V Tolerant Buffer DC Input Voltage with respect to V_{SS}	-0.5	$V_{CC}P$+ 0.9 but not to exceed 4.7	V	4
I_I	Maximum input current		200	mA	5
I_{VID}	Maximum VID pin current		5	mA	

NOTES:

1. Functional operation at the absolute maximum and minimum is not implied or guaranteed.
2. Operating voltage is the voltage that the component is designed to operate at. See Table 4 and Table 5.
3. Parameter applies to the GTL+ signal groups only.
4. Parameter applies to 3.3 V tolerant, APIC, and JTAG signal groups only.
5. Current may flow through the buffer ESD diodes when $V_{IH} > V_{CC}P$+1.1 V, as in a power supply fault condition or while power supplies are sequencing. Thermal stress should be minimized by cycling power off if the $V_{CC}P$ supply fails.

2.13. DC Specifications

Table 4 through Table 7 list the DC specifications associated with the Pentium Pro processor. Specifications are valid only while meeting the processor specifications for case temperature, clock frequency and input voltages. **Care should be taken to read all notes associated with each parameter.**

The Pentium Pro processor with 1 MB L2 cache dissipates more power than the Pentium Pro processor with 256 KB or 512 KB L2 cache. DC-DC converter for the Pentium Pro processor with 512 KB L2 cache Pmax limit, need to be re-designed for new Pmax values as well as new $V_{CC}P$ values. There are two options for this redesign. (Table 4 and Table 5 list the specifications for these two options.) The first option is to increase the current available from the DC-DC converter to "$I_{CC}P1$" while keeping the normal 3.3 $V_{CC}P$. The second option is to ignore the VID[0:3] value from the processor, and supply 3.2 V $V_{CC}P$ (typical) instead. This will require a lower "$I_{CC}P2$" current and a tighter limit for undershoot and overshoot values for the power supply in the range of +/- 0.1 V. The benefit of the second option is the lower "Pmax2" power dissipation requirement as compared to the "Pmax1", which is required from the first option. The Pentium Pro processor with 1 MB L2 cache is tested to satisfy either solution.

Most of the signals on the Pentium Pro processor are in the GTL+ signal group. These signals are specified to be terminated to 1.5 V. The DC specifications for these signals are listed in Table 6. Care should be taken to read all notes associated with each parameter.

To allow compatibility with other devices, some of the signals are 3.3 V tolerant and can therefore be terminated or driven to 3.3 V. The DC specifications for these 3.3 V tolerant inputs are listed in Table 7. Care should be taken to read all notes associated with each parameter.

Table 4. Power and Voltage Specifications (Option 1)

Symbol	Parameter	Min	Typical	Max	Unit	Notes
$V_{CC}P1$	Primary V_{CC}	3.135	3.3	3.465	V	1
Pmax1	Thermal Design Power		43	47	W	3
$I_{CC}P1$	$V_{CC}P1$ Current			15.0	A	2
I_{SGntP}	Stop Grant Current	0.3		1.2	A	4
T_C	Operational Case Temperature	0		80	°C	

Table 5. Power and Voltage Specifications (Option 2)

Symbol	Parameter	Min	Typical	Max	Unit	Notes
$V_{CC}P2$	Primary V_{CC}	3.1	3.2	3.3	V	
Pmax2	Thermal Design Power		40	44	W	3
$I_{CC}P2$	$V_{CC}P2$ Current			14.25	A	2
I_{SGntP}	Stop Grant Current	0.3		1.2	A	4
T_C	Operational Case Temperature	0		80	°C	

NOTES:

All other DC specifications, AC specifications and timings are identical to the Pentium® Pro processor with 256 K and 512 K L2 cache components.

1. To meet this 5% tolerance, the equivalent of forty (40) 1 µF capacitors (1206 packages) should be placed near the power pins of the device. At least 40 µF of capacitance should exist on the power planes, with less than 250 pH of inductance and 4 mΩ resistance between the capacitance and the pins of the processor, assuming a regulator setting of +/-1%.
2. Max current is measured at Max V_{CC}, all CMOS pins driven with V_{IH}= $V_{CC}P$ and V_{IL}=0V during the execution of Max I_{CC} and Max I_{CC}-StopGrant/AutoHalt Tests.
3. Maximum values are measured at typical V_{CC} but take into account the thermal time constant of the package. Typical values are not tested, but suggest the maximum power expected in a system during actual operation. If designing the system to the typical power level, a fail safe mechanism should be used to guarantee the component Tcase specification in case of workload anomalies.
4. Values are measured at typical $V_{CC}P$ by asserting the STPCLK# pin or by executing the HALT instruction, with the Low_Power_Enable bit set to enabled. Min values are not tested but guaranteed by design.

Table 6. GTL+ Signal Groups DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.3	V_{REF} -0.2	V	1, See Table 8
V_{IH}	Input High Voltage	V_{REF} + 0.2	$V_{CC}P$	V	1
V_{OL}	Output Low Voltage	0.30	0.60	V	2
V_{OH}	Output High Voltage	—	—	V	See V_{TT} max in Table 8
I_{OL}	Output Low Current	36	48	mA	2
I_L	Leakage Current		±100	mA	3
I_{REF}	Reference Voltage Current		± 15	mA	4
C_{GTL+}	GTL+ Pin Capacitance		8.5	pF	5

NOTES:

1. V_{REF} worst case, not nominal. Noise on V_{REF} should be accounted for.
2. Parameter measured into a 25 Ω resistor to 1.5 V. Min. V_{OL} and max. I_{OL} are guaranteed by design/characterization.
3. ($0 \le V_{PIN} \le V_{CC}P$)
4. Total current for all V_{REF} pins. Section 2.1. details the V_{REF} connections.
5. Total of I/O buffer, package parasitics and 0.5 pF for a socket. Capacitance values guaranteed by design for all GTL+ buffers.

Table 7. Non-GTL+[1] Signal Groups DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	3.6	V	
V_{OL}	Output Low Voltage		0.4 0.2	V V	2 3
V_{OH}	Output High Voltage	N/A	N/A	V	All Outputs Open-Drain
I_L	Input Leakage Current		±100	mA	4
C_{TOL}	3.3 V Tol. Pin Capacitance		10	pF	Except BCLK & TCK, 5
C_{CLK}	BCLK Input Capacitance		9	pF	5
C_{TCK}	TCK Input Capacitance		8	pF	5

NOTES:

1. Table 7 applies to the 3.3 V tolerant, APIC, and JTAG signal groups.
2. Parameter measured at 4 mA (for use with TTL inputs).
3. Parameter guaranteed by design at 100 µA (for use with CMOS inputs).
4. ($0 \le Vpin \le V_{CC}P$)
5. Total of I/O buffer, package parasitics and 0.5 pF for a socket. Capacitance values are guaranteed by design.

2.14. GTL+ Bus Specifications

The GTL+ bus must be routed in a daisy-chain fashion with termination resistors at each end of every signal trace. These termination resistors are placed between the ends of the signal trace and the V_{TT} voltage supply and generally are chosen to approximate the board impedance. The valid high and low levels are determined by the input buffers using a reference voltage called V_{REF}. Table 8 lists the nominal specifications for the GTL+ termination voltage (V_{TT}) and the GTL+ reference voltage (V_{REF}). It is important that the printed circuit board impedance be specified and held to a ±20% tolerance, and that the intrinsic trace capacitance for the GTL+ signal group traces is known**. For more details on GTL+, see the GTL+ interface specification in the *Pentium® Pro Processor Family Developer's Manual, Volume 1: Specifications* (Order Number 242690).**

Table 8. GTL+ Bus Voltage Specifications

Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{TT}	Bus Termination Voltage	1.35	1.5	1.65	V	±10%
V_{REF}	Input Reference Voltage	2/3 V_{TT}-2%	2/3 V_{TT}	2/3 V_{TT} +2%	V	±2%, 1

NOTE:

1. V_{REF} should be created from V_{TT} by a voltage divider of 1% resistors.

2.15. AC Specifications

Table 9 through Table 16 list the AC specifications associated with the Pentium Pro processor. Timing Diagrams begin with Figure 8. The AC specifications are broken into categories. Table 9 contains the clock specifications, Table 11 and Table 12 contain the GTL+ specifications, Table 13 is the 3.3 V tolerant Signal group specifications, Table 14 contains timings for the reset conditions, Table 15 covers APIC bus timing, and Table 16 covers Boundary Scan timing.

All AC specifications for the GTL+ signal group are relative to the rising edge of the BCLK input. All GTL+ timings are referenced to V_{REF} for both '0' and '1' logic levels unless otherwise specified.

Care should be taken to read all notes associated with a particular timing parameter.

Table 9. Bus Clock AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
	Core Frequency	150	200	MHz		@ 200 MHz,1
	Bus Frequency	50.00	66.67	MHz		1
T1:	BCLK Period	15	20	ns	8	
T2:	BCLK Period Stability		300	ps		2, 3
T3:	BCLK High Time	4		ns	8	@>2.0 V, 2
T4:	BCLK Low Time	4		ns	8	@<0.8 V, 2
T5:	BCLK Rise Time	0.3	1.5	ns	8	(0.8 V - 2.0 V), 2
T6:	BCLK Fall Time	0.3	1.5	ns	8	(2.0 V- 0.8 V), 2

NOTES:

1. The internal core clock frequency is derived from the bus clock. A clock ratio must be driven into the Pentium® Pro processor on the signals LINT[1:0], A20M# and IGNNE# at reset. See the descriptions for these signals in Appendix A.
2. Not 100% tested. Guaranteed by design/characterization.
3. Measured on rising edge of adjacent BCLKs at 1.5 V.
   The jitter present must be accounted for as a component of BCLK skew between devices.
   Clock jitter is measured from one rising edge of the clock signal to the next rising edge at 1.5 V. To remain within the clock jitter specifications, all clock periods must be within 300 ps of the ideal clock period for a given frequency. For example, a 66.67 MHz clock with a nominal period of 15 ns, must not have any single clock period that is greater than 15.3 ns or less than 14.7 ns. To ensure 1:1 relationship between the amplitude of the input jitter and the internal and external clocks, the jitter frequency spectrum should not have any power spectrum peaking between 100 kHz and 10 MHz. A spectrum analyzer can display the frequency spectrum of the clock driver in your system.

Table 10. Supported Clock Ratios[1]

Component	2X	5/2X	3X	7/2X	4X
200 MHz		X	X		X

NOTE:

1. Only those indicated by an 'X' are tested during the manufacturing test process.

Table 11. GTL+ Signal Groups AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T7A:	GTL+ Output Valid Delay H→L	0.80	4.4	ns	9	1
T7B:	GTL+ Output Valid Delay L→H	0.80	3.9	ns	9	1
T8:	GTL+ Input Setup Time	2.2		ns	10	2, 3, 4
T9:	GTL+ Input Hold Time	0.70		ns	10	4
T10:	RESET# Pulse Width	1		ms	13, 14	5

NOTES:

1. Valid delay timings for these signals are specified into an idealized 25 Ω resistor to 1.5 V with V_{REF} at 1.0 V. Minimum values guaranteed by design. See the GTL+ interface specification in the *Pentium® Pro Processor Family Developer's Manual, Volume 1: Specifications* (Order Number 242690), for the actual test configuration.
2. A minimum of 3 clocks must be guaranteed between 2 active-to-inactive transitions of TRDY#.
3. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
4. Specification takes into account a 0.3 V/ns edge rate and the allowable V_{REF} variation. Guaranteed by design.
5. After V_{CC}, V_{TT}, V_{REF}, BCLK and the clock ratio become stable.

Table 12. GTL+ Signal Groups Ringback Tolerance

	Parameter	Min	Unit	Figure	Notes
α:	Overshoot	100	mV	12	1
τ:	Minimum Time at High	1.5	ns	12	1
ρ:	Amplitude of Ringback	-100	mV	12	1
δ:	Duration of Square wave Ringback	N/A	ns	12	1
ϕ:	Final Settling Voltage	100	mV	12	1

NOTE:

1. Specified for an edge rate of 0.3—0.8 V/ns. See the GTL+ interface specification in the *Pentium® Pro Processor Family Developer's Manual, Volume 1: Specifications* (Order Number 242690), for the definition of these terms, and for the generic waveforms. All values determined by design/characterization.

Table 13. 3.3 V Tolerant Signal Groups AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T11:	3.3 V Tolerant Output Valid Delay	1	8	ns	9	1
T12:	3.3 V Tolerant Input Setup Time	5		ns	10	2, 3, 4, 5, 7
T13:	3.3 V Tolerant Input Hold Time	1.5		ns	10	7
T14:	3.3 V Tolerant Input Pulse Width, except PWRGOOD	2		BCLKs	9	Both levels
T15:	PWRGOOD Inactive Pulse Width	10		BCLKs	9, 14	6

NOTES:

1. Valid delay timings for these signals are specified into 150 Ω to 3.3 V. See Figure 7 for a capacitive derating curve.
2. These inputs may be driven asynchronously. However, to guarantee recognition on a specific clock, the setup and hold times with respect to BCLK must be met.
3. These signals must be driven synchronously in FRC mode.
4. A20M#, IGNNE#, INIT# and FLUSH# can be asynchronous inputs, but to guarantee recognition of these signals following a synchronizing instruction such as an I/O write instruction, they must be valid with active RS[2:0]# signals of the corresponding synchronizing bus transaction.
5. INTR and NMI are only valid in APIC disable mode. LINT[1:0]# are only valid in APIC enabled mode.
6. When driven inactive, or after Power, V_{REF}, BCLK, and the ratio signals are stable.
7. Specified over the clock rise time (T_r) and fall time (T_f) ranges of 0.3 ns to 2 ns for these signals, between 0.8 V and 2.0 V (as defined by Figure 8).

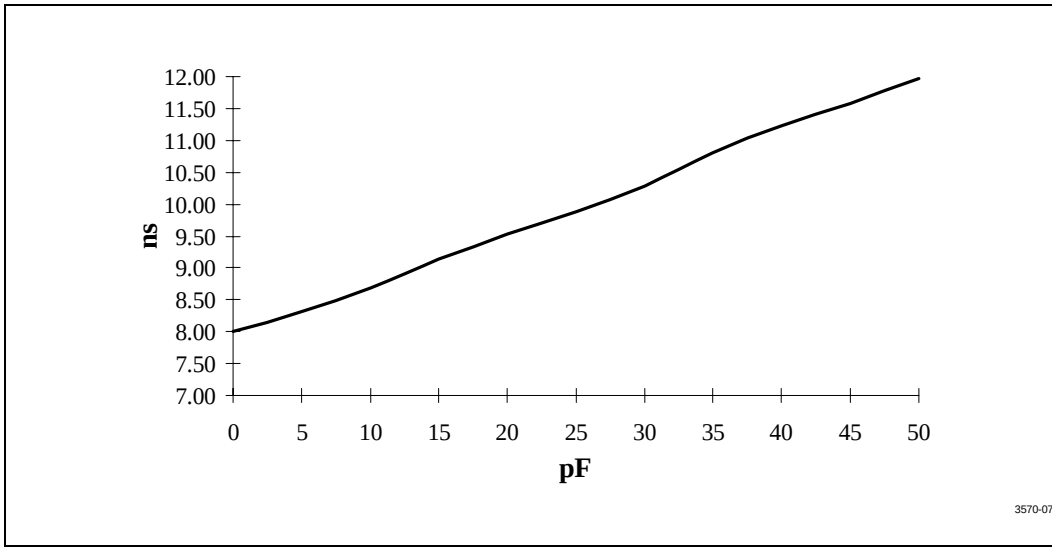


Figure 7. 3.3 V Tolerant Group Derating Curve

Table 14. Reset Conditions AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T16:	Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time	4		BCLKs	13	Before deassertion of RESET#
T17:	Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time	2	20	BCLKs	13	After clock that deasserts RESET#
T18:	Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Setup Time	1		ms	13	Before deassertion of RESET#
T19:	Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Delay Time		5	BCLKs	13	After assertion of RESET# [1]
T20:	Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Hold Time	2	20	BCLKs	13, 14	After clock that deasserts RESET#

NOTE:

1. For a reset, the clock ratio defined by these signals must be a safe value (their final or lower multiplier) within this delay unless PWRGOOD is being driven inactive.

Table 15. APIC Clock and APIC I/O AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T21A:	PICCLK Frequency	2	33.3	MHz		
T21B:	FRC Mode BCLK to PICCLK offset	1	5	ns	11	1
T22:	PICCLK Period	30	500	ns	8	
T23:	PICCLK High Time	12		ns	8	
T24:	PICCLK Low Time	12		ns	8	
T25:	PICCLK Rise Time	1	5	ns	8	
T26:	PICCLK Fall Time	1	5	ns	8	
T27:	PICD[1:0] Setup Time	8		ns	10	2
T28:	PICD[1:0] Hold Time	2		ns	10	2, 5
T29:	PICD[1:0] Valid Delay	2.1	10	ns	9	2, 3, 4, 5

NOTES:

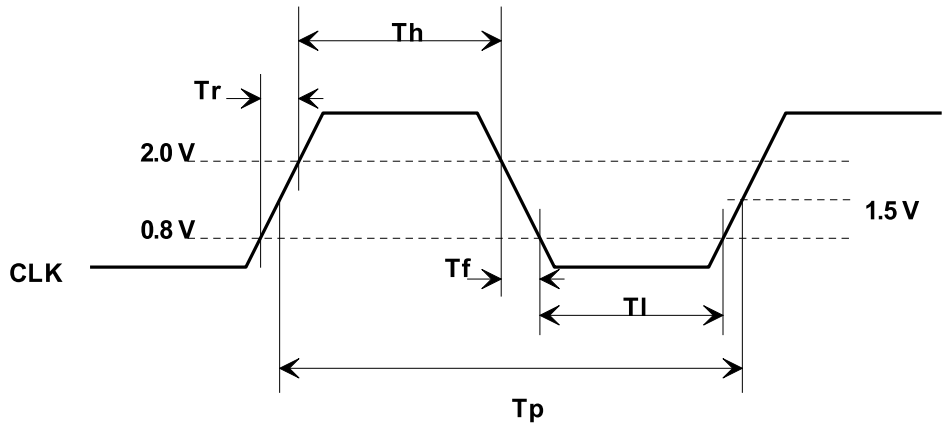
1. With FRC enabled PICCLK must be ¼X BCLK and synchronized with respect to BCLK. PICCLK must always lag BCLK by at least 1 ns and no more than 5 ns.
2. Referenced to PICCLK Rising Edge.
3. For open drain signals, Valid Delay is synonymous with Float Delay.
4. Valid delay timings for these signals are specified into 150 Ω to 3.3 V.
5. Specified over the rise time (T_r) and fall time (T_f) ranges of 0.3 ns to 2 ns for these signals, between 0.8 V and 2.0 V (as defined by Figure 8).

Table 16. Boundary Scan Interface AC Specifications

T#	Parameter	Min	Max	Unit	Figure	Notes
T30:	TCK Frequency	—	16	MHz		
T31:	TCK Period	62.5	—	ns	8	
T32:	TCK High Time	25		ns	8	@2.0 V, 1
T33:	TCK Low Time	25		ns	8	@0.8 V, 1
T34:	TCK Rise Time		5	ns	8	(0.8 V-2.0 V), 1, 2
T35:	TCK Fall Time		5	ns	8	(2.0 V-0.8 V), 1, 2
T36:	TRST# Pulse Width	40		ns	16	1, Asynchronous
T37:	TDI, TMS Setup Time	5		ns	15	3
T38:	TDI, TMS Hold Time	14		ns	15	3
T39:	TDO Valid Delay	1	10	ns	15	4, 5
T40:	TDO Float Delay		25	ns	15	1, 4, 5
T41:	All Nontest Outputs Valid Delay	2	25	ns	15	4, 6, 7
T42:	All Nontest Outputs Float Delay		25	ns	15	1, 4, 6, 7
T43:	All Nontest Inputs Setup Time	5		ns	15	3, 6, 7, 8
T44:	All Nontest Inputs Hold Time	13		ns	15	3, 6, 7, 8

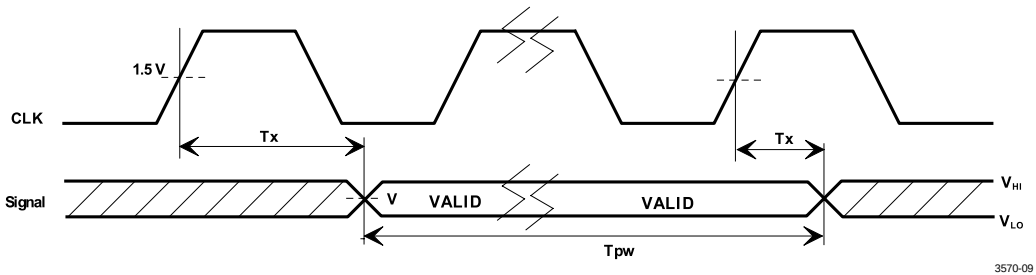
NOTES:

1. Not 100% tested. Guaranteed by design/characterization.
2. 1 ns can be added to the maximum TCK rise and fall times for every 1 MHz below 16 MHz.
3. Referenced to TCK rising edge.
4. Referenced to TCK falling edge.
5. Valid delay timing for this signal is specified into 150 Ω terminated to 3.3 V.
6. Nontest Outputs and Inputs are the normal output or input signals (besides TCK, TRST#, TDI, TDO and TMS). These timings correspond to the response of these signals due to boundary scan operations. PWRGOOD should be driven high throughout boundary scan testing.
7. During Debug Port operation, use the normal specified timings rather than the boundary scan timings.
8. Specified over the rise time (T_r) and fall time (T_f) ranges of 0.3 ns to 2 ns for these signals, between 0.8 V and 2.0 V (as defined by Figure 8).



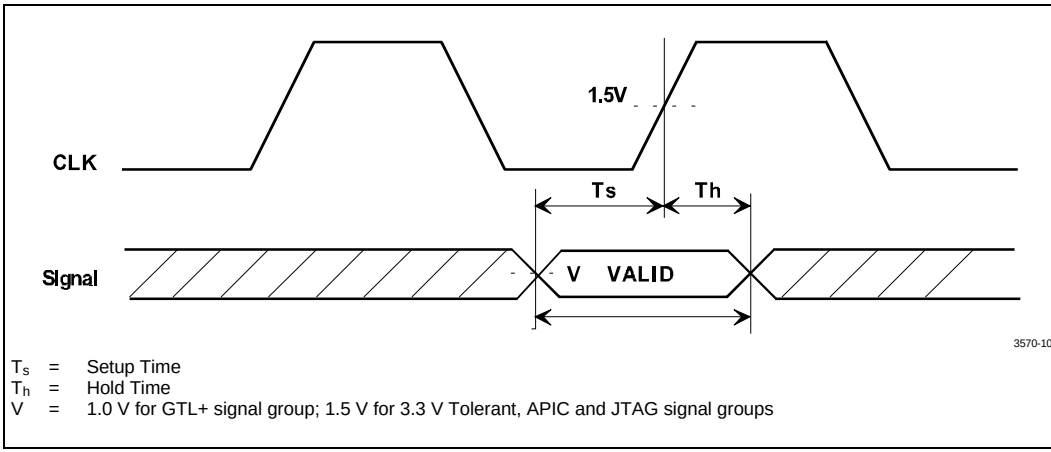
T_r = Rise Time
T_f = Fall Time
T_h = High Time
T_l = Low Time
T_p = Period

Figure 8. Generic Waveform



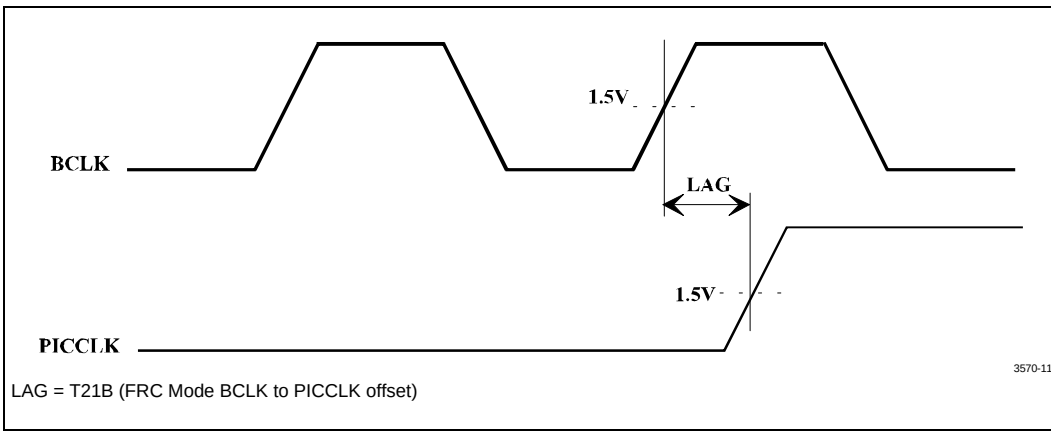
Tx = Valid Delay
Tpw = Pulse Width
V = 1.0 V for GTL+ signal group; 1.5 V for 3.3 V Tolerant, APIC, and JTAG signal groups
V_{HI} = GTL+ signals must achieve a DC high level of at least 1.2 V
V_{LO} = GTL+ signals must achieve a DC low level of at most 0.8 V

Figure 9. Valid Delay Timings



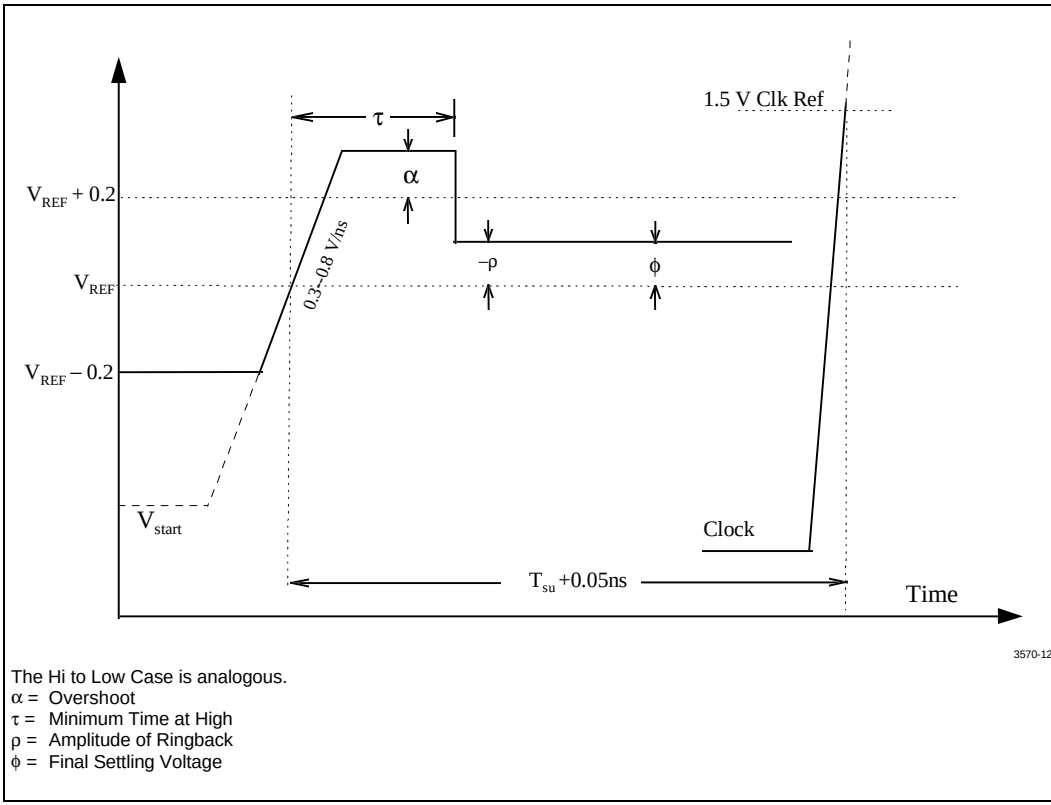
T_s = Setup Time
T_h = Hold Time
V = 1.0 V for GTL+ signal group; 1.5 V for 3.3 V Tolerant, APIC and JTAG signal groups

Figure 10. Setup and Hold Timings



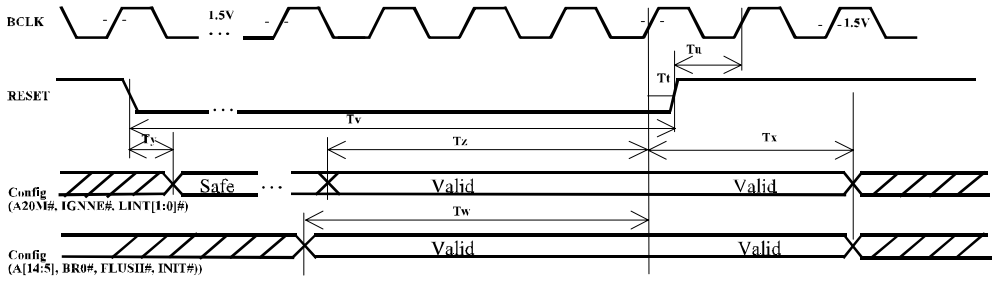
LAG = T21B (FRC Mode BCLK to PICCLK offset)

Figure 11. FRC Mode BCLK to PICCLK Timing



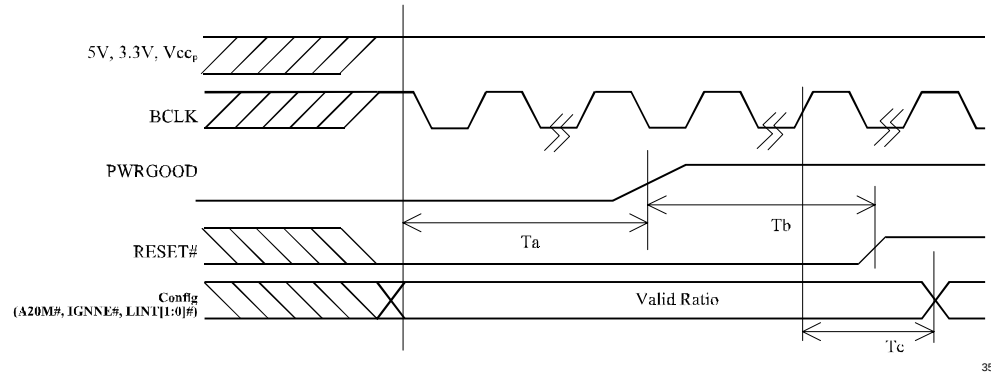
The Hi to Low Case is analogous.
α = Overshoot
τ = Minimum Time at High
ρ = Amplitude of Ringback
ϕ = Final Settling Voltage

Figure 12. Low to High GTL+ Receiver Ringback Tolerance



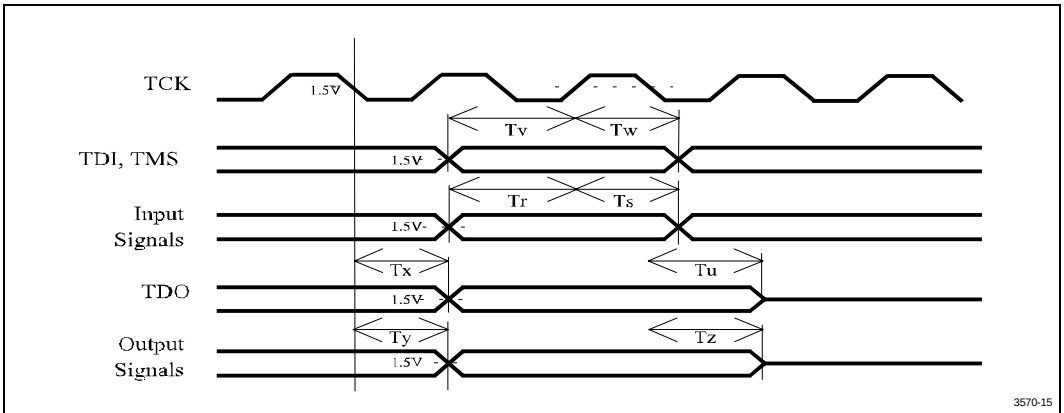
Tt = T9 (GTL+ Input Hold Time)
Tu = T8 (GTL+ Input Setup Time)
Tv = T10 (RESET# Pulse Width)
Tw = T16 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Setup Time)
Tx = T17 (Reset Configuration Signals (A[14:5]#, BR0#, FLUSH#, INIT#) Hold Time)
T20 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Hold Time)
Ty = T19 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Delay Time)
Tz = T18 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Setup Time)

Figure 13. Reset and Configuration Timings



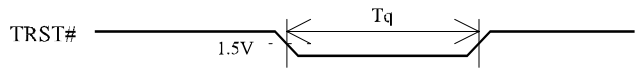
Ta = T15 (PWRGOOD Inactive Pulse Width)
Tb = T10 (RESET# Pulse Width)
Tc = T20 (Reset Configuration Signals (A20M#, IGNNE#, LINT[1:0]#) Hold Time)

Figure 14. Power-On Reset and Configuration Timings



Tr = T43 (All Nontest Inputs Setup Time)
Ts = T44 (All Nontest Inputs Hold Time)
Tu = T40 (TDO Float Delay)
Tv = T37 (TDI, TMS Setup Time)
Tw = T38 (TDI, TMS Hold Time)
Tx = T39 (TDO Valid Delay)
Ty = T41 (All Nontest Outputs Valid Delay)
Tz = T42 (All Nontest Outputs Float Delay)

Figure 15. Test Timings (Boundary Scan)



Tq = T36 (TRST# Pulse Width)

Figure 16. Test Reset Timings

3.0. GTL+ INTERFACE SPECIFICATION

For the generic GTL+ interface specification, see the *Pentium® Pro Processor Family Developer's Manual Volume 1: Specifications* (Order Number 242690), Chapter 12.

4.0. 3.3 V TOLERANT SIGNAL QUALITY SPECIFICATIONS

The signals that are 3.3 V tolerant should also meet signal quality specifications to guarantee that the components read data properly and to ensure that incoming signals do not affect the long term reliability of the component. There are three signal quality parameters defined for the 3.3 V tolerant signals. They are Overshoot/Undershoot, Ringback and Settling Limit. All three signal quality parameters are shown in Figure 17. The *Pentium® Pro Processor I/O Buffer Models—IBIS Format* (on World Wide Web page http://www.intel.com) contain models for simulating 3.3 V tolerant signal distribution.

4.1. Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage allowed above the nominal high voltage or below V_{SS}. The overshoot/undershoot guideline limits transitions beyond $V_{CC}P$ or V_{SS} due to the fast signal edge rates. See Figure 17. The processor can be damaged by repeated overshoot events on 3.3 V tolerant buffers if the charge is large

enough (i.e., if the overshoot is great enough). However, excessive ringback is the dominant harmful effect resulting from overshoot or undershoot (i.e., violating the overshoot/undershoot guideline will make satisfying the ringback specification difficult). The **overshoot/undershoot guideline is 0.8 V** and assumes the absence of diodes on the input. These guidelines should be verified in simulations **without the on-chip ESD protection diodes present** because the diodes will begin clamping the 3.3 V tolerant signals beginning at approximately 1.5 V above $V_{CC}P$ and 0.5 V below V_{SS}. If signals are not reaching the clamping voltage, then this is not an issue. A system should not rely on the diodes for overshoot/undershoot protection as this will negatively affect the life of the components and make meeting the ringback specification very difficult.

4.2. Ringback Specification

Ringback refers to the amount of reflection seen after a signal has undergone a transition. **The ringback specification is the voltage that the signal rings back to after achieving its farthest excursion.** See Figure 17 for an illustration of ringback. Excessive ringback can cause false signal detection or extend the propagation delay. The ringback specification applies to the input pin of each receiving agent. Violations of the signal Ringback specification are not allowed under any circumstances.

Ringback can be simulated with or without the input protection diodes that can be added to the input buffer model. However, signals that reach the clamping voltage should be evaluated further. See Table 17 for the signal ringback specifications for Non-GTL+ signals.

Table 17. Signal Ringback Specifications

Transition	Maximum Ringback (with input diodes present)
0→1	2.5 V
1→0	0.8 V

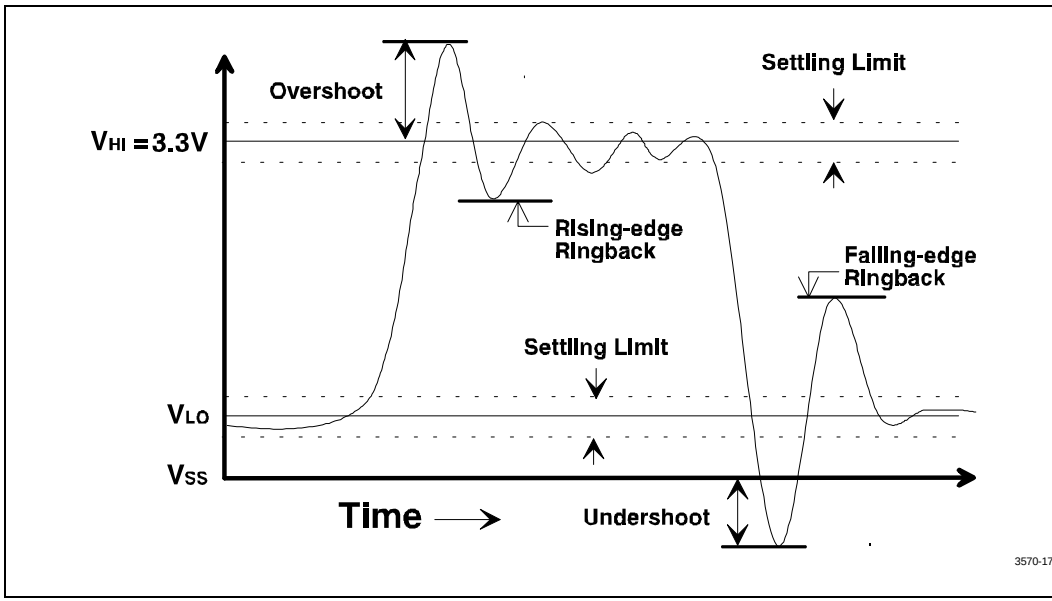


Figure 17. 3.3 V Tolerant Signal Overshoot/Undershoot and Ringback

4.3. Settling Limit Guideline

A Settling Limit defines the maximum amount of ringing at the receiving pin that a signal must be limited to before its next transition. The amount allowed is 10% of the total signal swing (V_{HI} -V_{LO}) above and below its final value. A signal should be within the settling limits of its final value, when either in its high state of low state, before it transitions again.

Signals that are not within their settling limit before transitioning are at risk of unwanted oscillations which could jeopardize signal integrity. Simulations to verify Settling Limit may be done either with or without the input protection diodes present. Violation of the Settling Limit guideline is acceptable if simulations of 5-10 successive transitions do not show the amplitude of the ringing increasing in the subsequent transitions.

5.0. THERMAL SPECIFICATIONS

This section defines the thermal specification of the Pentium Pro processor with 1 MB L2 cache.

5.1. Thermal Parameters

This section defines terms used for the Pentium Pro processor with 1 MB L2 cache thermal analysis.

5.1.1. AMBIENT TEMPERATURE

Ambient temperature, T_A , is the temperature of the ambient air surrounding the package. In a system environment, ambient temperature is the temperature of the air upstream from the package and in its close vicinity; or in an active cooling system, it is the inlet air to the active cooling device.

5.1.2. MEASURING CASE TEMPERATURE

To ensure functionality and reliability, the Pentium Pro processor with 1 MB L2 cache is specified for proper operation when T_C (case temperature) is within the specified range in Table 4. Special care is required when measuring the case temperature to ensure an accurate temperature measurement. Thermocouples, which must be calibrated prior to measurement, are often used to measure T_C. When measuring the temperature of the surface which is at a different temperature from surrounding ambient air, errors could be introduced in the measurements if not conducted properly. The measurement errors could be due to having a poor thermal contact between the thermocouple junction and the surface, heat loss by radiation, or by conduction through thermocouple heads.

To verify that the proper T_C is maintained, it should be measured at the top of the package on the heat spreader (package side, opposite of the pins). The measurement is made in the same way with or without a heat sink attached. When a heat sink is attached, a hole (smaller than .150" in diameter) should be drilled through the heat sink to allow probing the package surface. See Figure 18 for an illustration of how to measure T_C. Figure 19 shows the location to measure T_C.

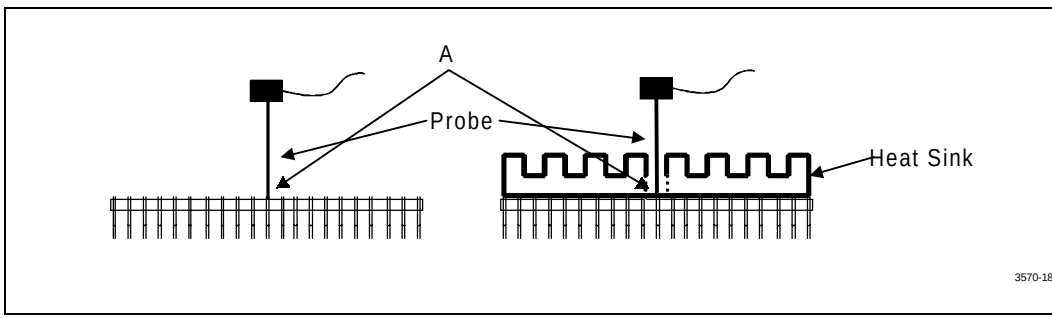


Figure 18. Technique for Measuring T_C on Processor

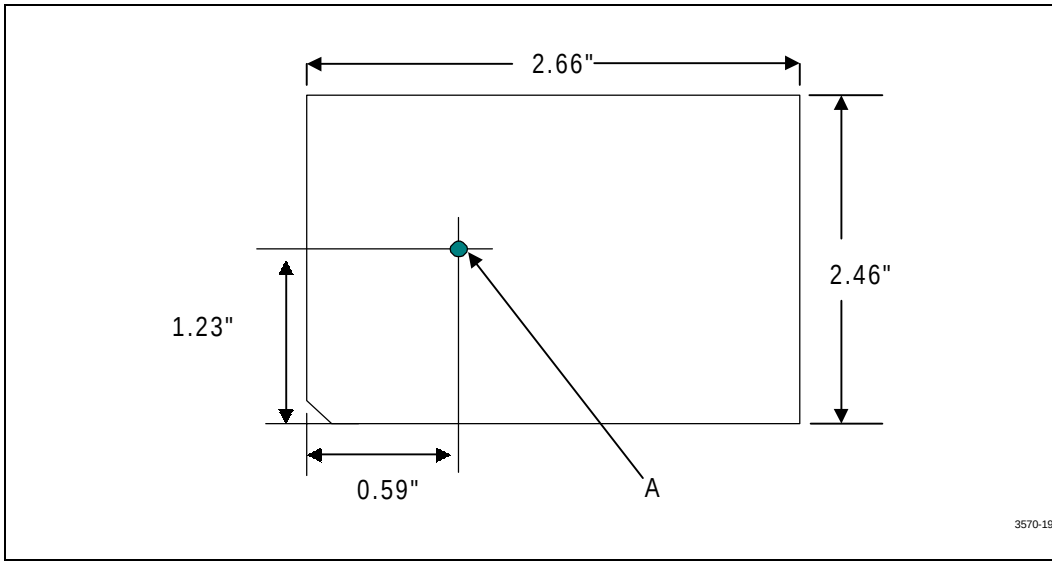


Figure 19. Location for T_C Measurement on Back Plate (not to scale)

To minimize the measurement errors, Intel recommends the following approach:

- Use 36 gauge or finer diameter K, T, or J type thermocouples.
- Attach the thermocouple bead or junction to the center of the package top surface using high thermal conductivity cements.
- The thermocouple should be attached at a 90° angle as shown in Figure 18.
- The hole size should be smaller than 0.150" in diameter and the hole should be filled with grease.
- Make sure there is no contact between thermocouple cement and heat sink base. The contact will affect the thermocouple reading.

5.1.3. THERMAL RESISTANCE

The thermal resistance value for the case-to-ambient, Θ_{CA}, is used as a measure of the cooling solution's thermal performance. Θ_{CA} is comprised of the case-to-sink thermal resistance, Θ_{CS}, and sink-to-ambient thermal resistance, Θ_{SA}. Θ_{CS} is a measure of the thermal resistance along the heat flow path from the top of the IC package to the bottom of the thermal cooling solution. This value is strongly dependent on the material, conductivity, and the thickness of the thermal interface used. Θ_{SA} values depend on the material, thermal conductivity, and geometry of the thermal cooling solution as well as on the airflow rates.

The parameters are defined by the following relationships.

$\Theta_{CA} = (T_C - T_A) / P_D$

$\Theta_{CA} = \Theta_{CS} + \Theta_{SA}$

Where: Θ_{CA} = Case-to-Ambient thermal resistance (°C/W)

Θ_{CS} = Case-to-Sink thermal resistance (°C/W)

Θ_{SA} = Sink-to-Ambient thermal resistance (°C/W)

T_C = Case temperature at the defined location (°C)

T_A = Ambient temperature (°C)

P_D = Device power dissipation (W)

5.2. Thermal Analysis

5.2.1. TYPICAL PASSIVE HEAT SINK DESIGNS

Table 18 and Table 19 provide the dimensions of the three heat sinks used to generate the data in Table 20 to Table 22.

These heat sinks designs are for reference only. **For the definition of the pedestal, refer to Section** 6.2.

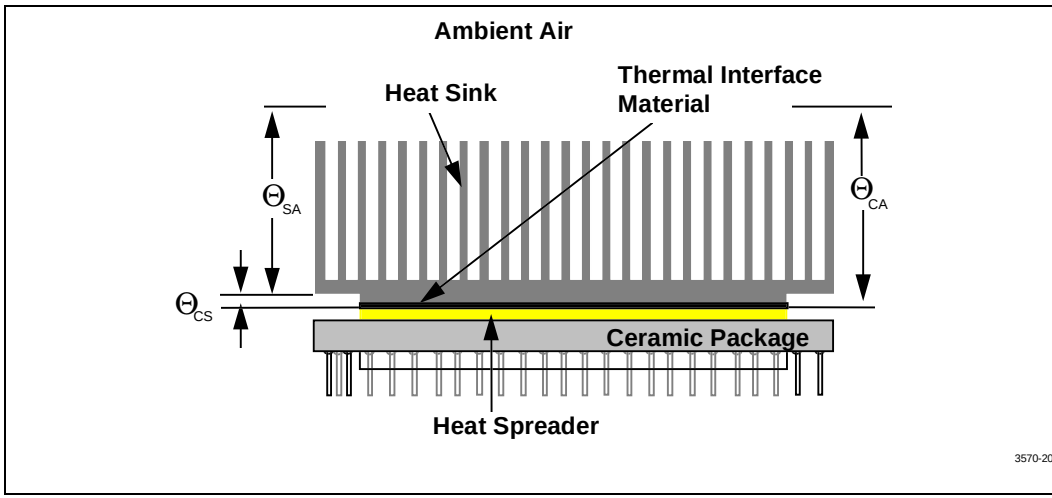


Figure 20. Thermal Resistance Relationships

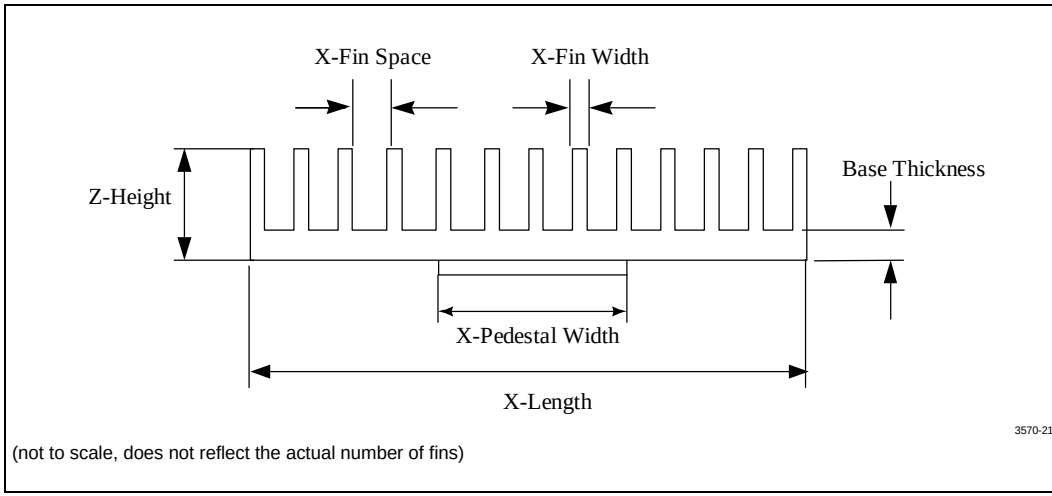
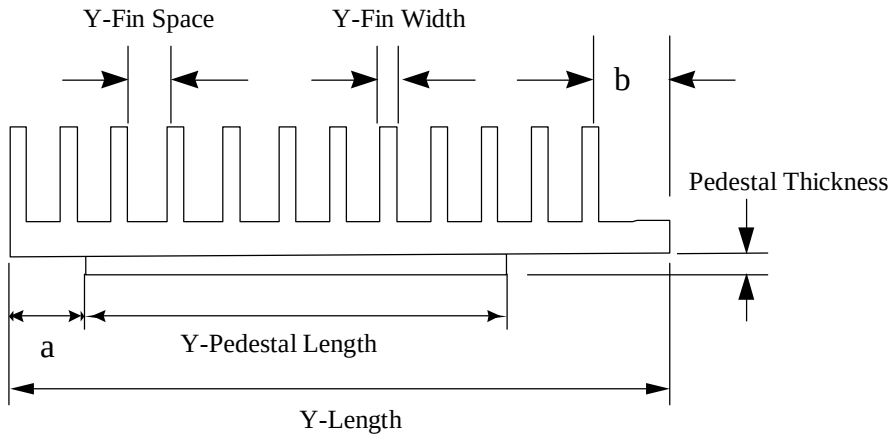


Figure 21. Typical Heat Sink Dimensions (View from Side-X)



(not to scale, does not reflect the actual number of fins)

Figure 22. Typical Heat Sink Dimensions (View from Side-Y)

Table 18. Typical Heat Sink Designs (View from Side-X)

Heat Sink Design	Z-Height	X-Length	Base Thickness	X-Fin Width	X-Fin Space	X-Pedestal Width
A	1.00"	2.5"	0.155"	0.085"	0.183"	1.2"
B	1.32"	3.0"	0.170"	0.050"	0.218"	1.2"
C	1.32"	3.6"	0.165"	0.060"	0.212"	1.2"

Table 19. Typical Heat Sink Designs (View from Side-Y)

Heat Sink Design	Y-Length	Y-Fin Width	Y-Fin Space	Y-Pedestal Length	Pedestal Thickness	a	b
A	3.15"	0.090"	0.127"	2.1"	0.020"	0.25"	0.24"
B	3.15"	0.200"	0.126"	2.1"	0.020"	0.25"	0.34"
C	3.15"	0.200"	0.131"	2.1"	0.020"	0.25"	0.30"

5.2.2. TABLES AND CURVES FOR PASSIVE HEAT SINKS VS. AIR FLOW RATES

Table 20. Θ_{CA} For Different Passive Heat Sink Sizes and 50 - 300 LFM Air Flow Rates

	Θ_{CA}[°C/W] vs. Air Flow Rate [LFM]					
Heat Sink Size	50	100	150	200	250	300
A 2.5" x 3.15" x 1.00"	2.09	1.70	1.50	1.32	1.19	1.09
B 3.0" x 3.15" x 1.32"	1.50	1.26	1.13	1.01	0.92	0.86
C 3.6" x 3.15" x 1.32"	1.30	1.10	0.99	0.89	0.81	0.76

Table 21. Θ_{CA} For Different Passive Heat Sink Sizes and 350 - 600 LFM Air Flow Rates

	Θ_{CA} [°C/W] vs. Air Flow Rate [LFM]					
Heat Sink Size	350	400	450	500	550	600
A 2.5" x 3.15" x 1.00"	1.02	0.96	0.92	0.88	0.85	0.83
B 3.0" x 3.15" x 1.32"	0.82	0.78	0.75	0.73	0.70	0.69
C 3.6" x 3.15" x 1.32"	0.72	0.69	0.67	0.64	0.62	0.61

Table 22. Θ_{CA} For Different Passive Heat Sink Sizes and 650 - 800 LFM Air Flow Rates

	Θ_{CA} [°C/W] vs. Air Flow Rate [LFM]			
Heat Sink Size	650	700	750	800
A 2.5" x 3.15" x 1.00"	0.81	0.79	0.77	0.76
B 3.0" x 3.15" x 1.32"	0.67	0.66	0.64	0.63
C 3.6" x 3.15" x 1.32"	0.59	0.58	0.57	0.56

NOTE:

Θ_{CA} is calculated based on the following formula:

$\Theta_{CA} = (T_C - T_A) / P$

where T_C is the package case temperature, T_A is the ambient temperature, and P is the total power dissipation from the processor. Θ_{CA} values shown in this table are typical values. The actual Θ_{CA} values depend on the heat sink design, interface between heat sink and package, the air flow in the system, and thermal interactions between the processor and surrounding components, through the PCB, and the ambient temperature.

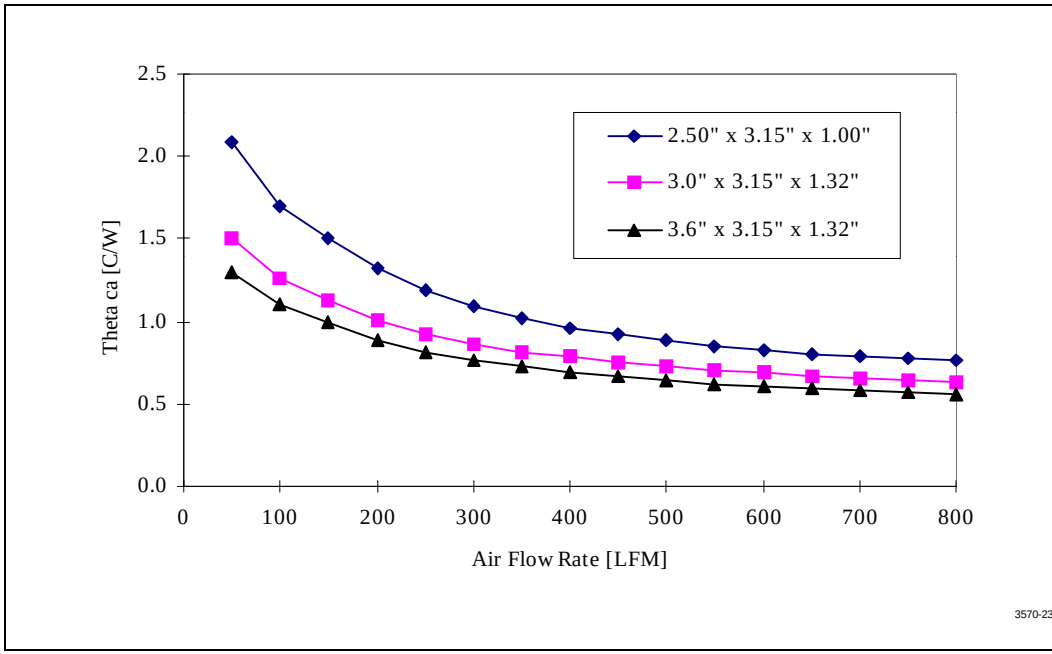


Figure 23. Θ_{CA} for Different Heat Sink Sizes vs. Air Flow Rates

Table 23. Θ_{CA} for Different Fan Heat Sinks and Air Flow Rates

		Θ_{CA} [°C/W] vs External Air Flow Rate [LFM]				
Fan Heat Sink Design	Overall Size	0	50	100	150	200
Single fan	2.50" x 3.15" x 1.25"	1.25	1.25	1.22	1.19	1.17
Dual fan	2.55" x 3.20" x 1.00"	0.81	0.79	0.80	0.80	0.80

5.2.3. FAN HEAT SINK DESIGNS

A fan heat sink can also be used for cooling the Pentium Pro processor. Table 23 shows Θ_{CA} for a single-fan design and for a design with two small fans. Two small fans are more effective than one larger fan. Also, notice the minimal impact of external airflow over the fan heat sinks.

5.2.4. EFFECT OF THERMAL GREASE AND PEDESTAL SIZE ON THERMAL PERFORMANCE

Thermal performance of the interface material between the package top surface and the heat sink base is determined by the following factors:

- Thermal conductivity of the interface material
- The contact area of the interface material between the package surface and the heat sink base
- The interface material thickness after heat sink assembly

The higher the thermal resistance, the less efficient an interface is at transferring heat. That is, the higher the thermal resistance, the higher the temperature drop across the interface. Thermal resistance increases with interface material thickness. The higher the thermal conductivity (K) of the interface material, the lower the thermal resistance is. In addition, the larger pedestal size corresponding to a larger contact area results in lower thermal resistance assuming the interface thickness remains the same. However, the interface thickness is determined by the flatness of the package surface and the heat sink base. The higher the flatness, the thicker the interface. Although a pedestal will result in a smaller contact area, a pedestal may end up with a thinner interface thickness. For the package surface with less flatness around the package edge, a pedestal may significantly reduce the interface thickness, resulting in better thermal performance despite reducing the contact area.

6.0. MECHANICAL SPECIFICATIONS

The following figures and table show the package dimensions for the Pentium Pro processor with 1 MB L2 cache.

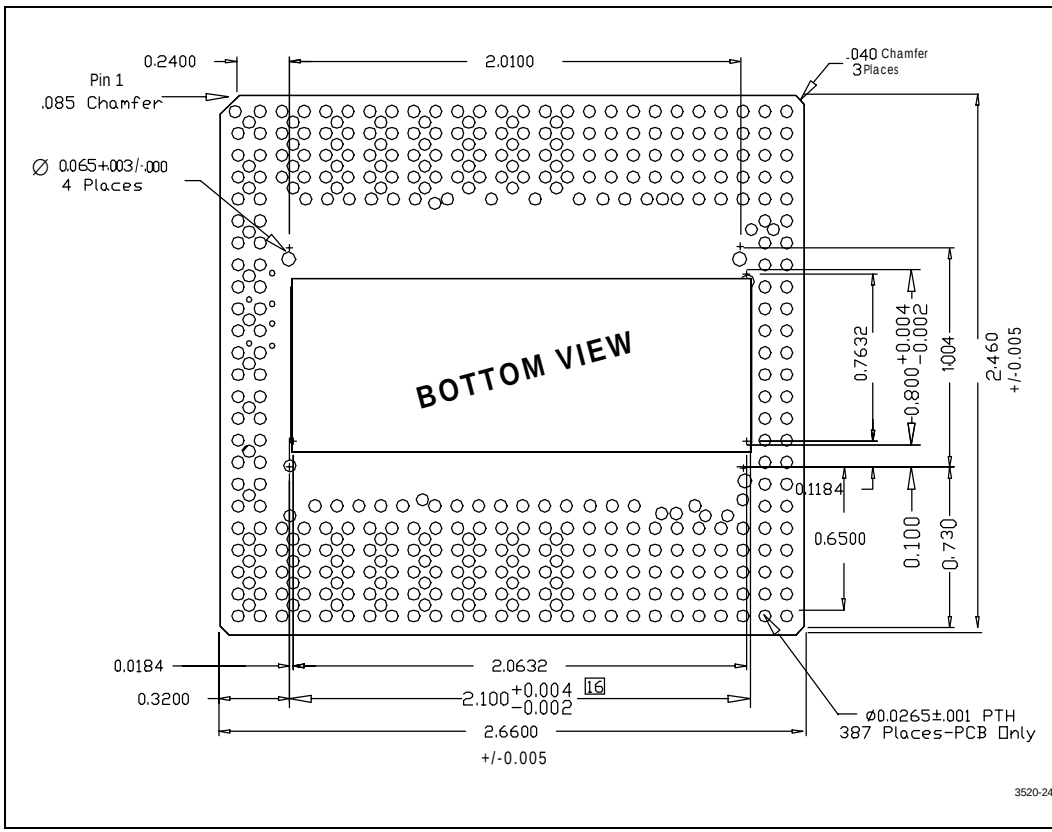


Figure 24. Pentium® Pro Processor with 1 MB L2 Cache Pin Side

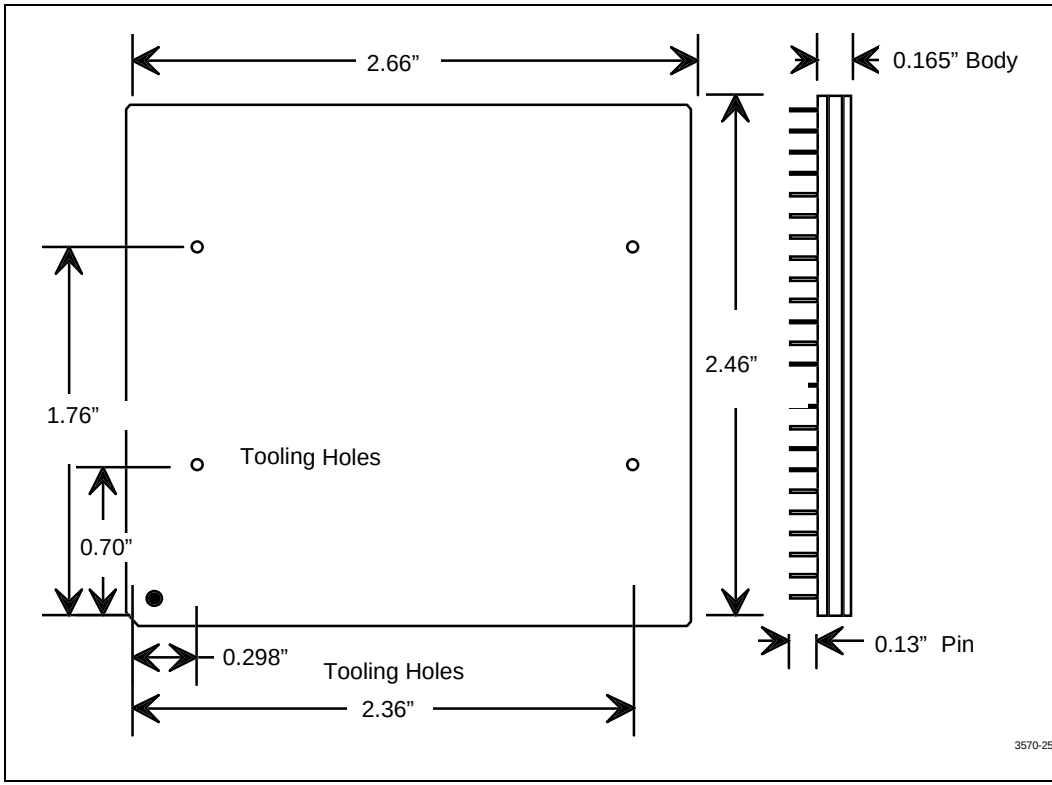


Figure 25. Top View of Package

Table 24. Pentium® Pro Processor with 1 MB L2 Cache Package

Parameter	Value
Package Type	Plastic PGA with integrated Anodized Aluminum heat spreader
Total Pins	387
Pin Array	Modified Staggered PGA (Pentium® Pro processor footprint)
Pin Length	0.130" +/- 0.005" (no fillet)
Pin Diameter	0.018" +/- 0.002" (rounded end)
Pin Finish	Gold plated, for use in ZIF or LIF sockets only
Package Length	2.66" +/-0.005" (7.76 cm +/- 0.013)
Package Width	2.46" +/-0.005" (6.25 cm +/- 0.013)
Package Body (not including pins)	0.165" +/- 0.010" (0.419 cm +/- 0.025)
Flatness	See Section 6.2.
Heat Spreader Size	2.66" x 2.46" (7.76 cm x 6.25 cm) with four (4) through package tooling holes
Tooling Holes Diameter	0.062" diameter[1]
Weight	45 grams

NOTE:

1. Do not use the tooling holes for heat sink attach or component hold down mechanics. Intel will not guarantee the position, size or the existence of these holes.

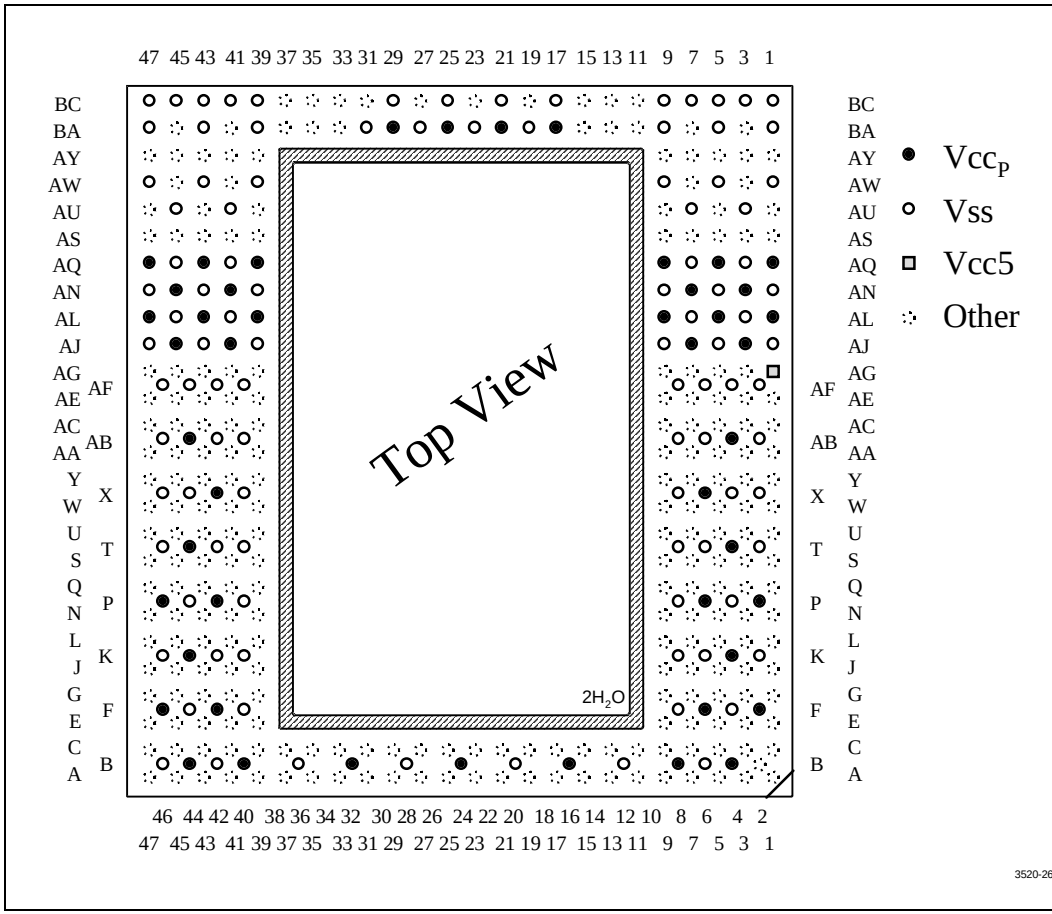


Figure 26. Pentium® Pro Processor Top View with Power Pin Locations

6.1. Pinout

Table 25 is the pin listing in pin number order. Table 26 is the pin listing in pin name order. Please see Section 2.8. to determine a signal's I/O type. Bus signals are described in Appendix A and the other pins are described in Section 2.0. and in Table 2.

Table 25. Pin Listing in Pin # Order

Pin #	Signal Name
A1	$V_{REF}0$
A3	STPCLK#
A5	TCK
A7	TRST#
A9	IGNNE#
A11	A20M#
A13	TDI
A15	FLUSH#
A17	THERMTRIP#
A19	BCLK
A21	RESERVED
A23	TESTHI
A25	TESTHI
A27	D1#
A29	D3#
A31	D5#
A33	D8#
A35	D9#
A37	D14#
A39	D10#
A41	D11#
A43	D13#
A45	D16#
A47	$V_{REF}4$
B2	CPUPRES#
B4	$V_{CC}P$
B6	V_{SS}
B8	$V_{CC}P$
B12	V_{SS}
B16	$V_{CC}P$
B20	V_{SS}
B24	$V_{CC}P$
B28	V_{SS}
B32	$V_{CC}P$
B36	V_{SS}
B40	$V_{CC}P$
B42	V_{SS}
B44	$V_{CC}P$
B46	V_{SS}
C1	A35#
C3	IERR#
C5	BERR#
C7	$V_{REF}1$
C9	FRCERR
C11	INIT#
C13	TDO
C15	TMS
C17	FERR#
C19	PLL1
C21	TESTLO
C23	PLL2
C25	D0#
C27	D2#

Table 25. Pin Listing in Pin # Order (Continued)

C29	D4#
C31	D6#
C33	D7#
C35	D12#
C37	D15#
C39	D17#
C41	D20#
C43	D18#
C45	D19#
C47	D21#
E1	A29#
E3	A30#
E5	A32#
E7	A33#
E9	A34#
E39	D22#
E41	D23#
E43	D25#
E45	D24#
E47	D26#
F2	$V_{CC}P$
F4	V_{SS}
F6	$V_{CC}P$
F8	V_{SS}
F40	V_{SS}
F42	$V_{CC}P$
F44	V_{SS}
F46	$V_{CC}P$
G1	A22#
G3	A24#
G5	A27#
G7	A26#
G9	A31#
G39	D27#
G41	D29#
G43	D30#
G45	D28#
G47	D31#
J1	A19#
J3	A21#
J5	A20#
J7	A23#
J9	A28#
J39	D32#
J41	D35#
J43	D38#
J45	D33#
J47	D34#
K2	V_{SS}
K4	$V_{CC}P$
K6	V_{SS}
K8	V_{SS}
K40	V_{SS}
K42	V_{SS}
K44	$V_{CC}P$
K46	V_{SS}
L1	RESERVED
L3	A16#
L5	A15#
L7	A18#
L9	A25#
L39	D37#
L41	D40#

Table 25. Pin Listing in Pin # Order (Continued)

L43	D43#
L45	D36#
L47	D39#
N1	A12#
N3	A14#
N5	A11#
N7	A13#
N9	A17#
N39	D44#
N41	D45#
N43	D47#
N45	D42#
N47	D41#
P2	$V_{CC}P$
P4	V_{SS}
P6	$V_{CC}P$
P8	V_{SS}
P40	V_{SS}
P42	$V_{CC}P$
P44	V_{SS}
P46	$V_{CC}P$
Q1	A9#
Q3	A7#
Q5	A5#
Q7	A8#
Q9	A10#
Q39	D51#
Q41	D52#
Q43	D49#
Q45	D48#
Q47	D46#
S1	A6#
S3	A4#
S5	A3#
S7	$V_{REF}2$
S9	AP1#
S39	D59#
S41	D57#
S43	D54#
S45	D53#
S47	D50#
T2	V_{SS}
T4	$V_{CC}P$
T6	V_{SS}
T8	V_{SS}
T40	V_{SS}
T42	V_{SS}
T44	$V_{CC}P$
T46	V_{SS}
U1	AP0#
U3	RSP#
U5	BPRI#
U7	BNR#
U9	BR3#
U39	DEP7#
U41	$V_{REF}6$
U43	D60#
U45	D56#
U47	D55#
W1	SMI#
W3	BR1#
W5	REQ4#
W7	REQ1#

Table 25. Pin Listing in Pin # Order (Continued)

W9	REQ0#
W39	DEP2#
W41	DEP4#
W43	D63#
W45	D61#
W47	D58#
X2	V_{SS}
X4	V_{SS}
X6	$V_{CC}P$
X8	V_{SS}
X40	V_{SS}
X42	$V_{CC}P$
X44	V_{SS}
X46	V_{SS}
Y1	REQ3#
Y3	REQ2#
Y5	DEFER#
Y7	$V_{REF}3$
Y9	TRDY#
Y39	PRDY#
Y41	RESET#
Y43	DEP1#
Y45	DEP6#
Y47	D62#
AA1	BR2#
AA3	DRDY#
AA5	DBSY#
AA7	HITM#
AA9	LOCK#
AA39	BPM1#
AA41	PICD0
AA43	PICCLK
AA45	PREQ#
AA47	DEP5#
AB2	V_{SS}
AB4	$V_{CC}P$
AB6	V_{SS}
AB8	V_{SS}
AB40	V_{SS}
AB42	V_{SS}
AB44	$V_{CC}P$
AB46	V_{SS}
AC1	RESERVED
AC3	HIT#
AC5	BR0#
AC7	RP#
AC9	RS0#
AC39	BP3#
AC41	BPM0#
AC43	BINIT#
AC45	DEP0#
AC47	DEP3#
AE1	RESERVED
AE3	ADS#
AE5	RS1#
AE7	RS2#
AE9	AERR#
AE39	TESTHI
AE41	PICD1
AE43	BP2#
AE45	RESERVED
AE47	$V_{REF}5$
AF2	V_{SS}

Table 25. Pin Listing in Pin # Order (Continued)

AF4	V_{SS}
AF6	V_{SS}
AF8	V_{SS}
AF40	V_{SS}
AF42	V_{SS}
AF44	V_{SS}
AF46	V_{SS}
AG1	$V_{CC}5$
AG3	UP#
AG5	RESERVED
AG7	PWRGOOD
AG9	RESERVED
AG39	RESERVED
AG41	LINT1/NMI
AG43	LINT0/INTR
AG45	$V_{REF}7$
AG47	RESERVED
AJ1	V_{SS}
AJ3	$V_{CC}P$
AJ5	V_{SS}
AJ7	$V_{CC}P$
AJ9	V_{SS}
AJ39	V_{SS}
AJ41	$V_{CC}P$
AJ43	V_{SS}
AJ45	$V_{CC}P$
AJ47	V_{SS}
AL1	$V_{CC}P$
AL3	V_{SS}
AL5	$V_{CC}P$
AL7	V_{SS}
AL9	$V_{CC}P$
AL39	$V_{CC}P$
AL41	V_{SS}
AL43	$V_{CC}P$
AL45	V_{SS}
AL47	$V_{CC}P$
AN1	V_{SS}
AN3	$V_{CC}P$
AN5	V_{SS}
AN7	$V_{CC}P$
AN9	V_{SS}
AN39	V_{SS}
AN41	$V_{CC}P$
AN43	V_{SS}
AN45	$V_{CC}P$
AN47	V_{SS}
AQ1	$V_{CC}P$
AQ3	V_{SS}
AQ5	$V_{CC}P$
AQ7	V_{SS}
AQ9	$V_{CC}P$
AQ39	$V_{CC}P$
AQ41	V_{SS}
AQ43	$V_{CC}P$
AQ45	V_{SS}
AQ47	$V_{CC}P$
AS1	VID0
AS3	VID1
AS5	VID2
AS7	VID3
AS9	RESERVED
AS39	TESTLO

Table 25. Pin Listing in Pin # Order (Continued)

AS41	TESTLO
AS43	TESTLO
AS45	TESTLO
AS47	RESERVED
AU1	RESERVED
AU3	V_{SS}
AU5	RESERVED
AU7	V_{SS}
AU9	RESERVED
AU39	RESERVED
AU41	V_{SS}
AU43	RESERVED
AU45	V_{SS}
AU47	RESERVED
AW1	V_{SS}
AW3	RESERVED
AW5	V_{SS}
AW7	RESERVED
AW9	V_{SS}
AW39	V_{SS}
AW41	RESERVED
AW43	V_{SS}
AW45	RESERVED
AW47	V_{SS}
AY1	RESERVED
AY3	RESERVED
AY5	RESERVED
AY7	RESERVED
AY9	RESERVED
AY39	RESERVED
AY41	RESERVED
AY43	RESERVED
AY45	RESERVED
AY47	RESERVED
BA1	V_{SS}
BA3	RESERVED
BA5	V_{SS}
BA7	RESERVED
BA9	V_{SS}
BA11	RESERVED
BA13	TESTLO
BA15	TESTLO
BA17	$V_{CC}P$
BA19	V_{SS}
BA21	$V_{CC}P$
BA23	V_{SS}
BA25	$V_{CC}P$
BA27	V_{SS}
BA29	$V_{CC}P$
BA31	V_{SS}
BA33	TESTLO
BA35	RESERVED
BA37	TESTLO
BA39	V_{SS}
BA41	RESERVED
BA43	V_{SS}
BA45	RESERVED
BA47	V_{SS}
BC1	V_{SS}
BC3	V_{SS}
BC5	V_{SS}
BC7	V_{SS}
BC9	V_{SS}

Table 25. Pin Listing in Pin # Order (Continued)

BC11	RESERVED
BC13	TESTLO
BC15	TESTLO
BC17	V_{SS}
BC19	RESERVED
BC21	V_{SS}
BC23	RESERVED
BC25	V_{SS}
BC27	RESERVED
BC29	V_{SS}
BC31	RESERVED
BC33	TESTLO
BC35	RESERVED
BC37	TESTLO
BC39	V_{SS}
BC41	V_{SS}
BC43	V_{SS}
BC45	V_{SS}
BC47	V_{SS}

Table 26. Pin Listing in Alphabetic Order

Signal Name	Pin #
A3#	S5
A4#	S3
A5#	Q5
A6#	S1
A7#	Q3
A8#	Q7
A9#	Q1
A10#	Q9
A11#	N5
A12#	N1
A13#	N7
A14#	N3
A15#	L5
A16#	L3
A17#	N9
A18#	L7
A19#	J1
A20#	J5
A20M#	A11
A21#	J3
A22#	G1
A23#	J7
A24#	G3
A25#	L9
A26#	G7
A27#	G5
A28#	J9
A29#	E1

Table 26. Pin Listing in Alphabetic Order
(Continued)

Signal Name	Pin #
A30#	E3
A31#	G9
A33#	E7
A34#	E9
A35#	C1
ADS#	AE3
AERR#	AE9
AP0#	U1
AP1#	S9
BCLK	A19
BERR#	C5
BINIT#	AC43
BNR#	U7
BP2#	AE43
BP3#	AC39
BPM0#	AC41
BPM1#	AA39
BPRI#	U5
BR0#	AC5
BR1#	W3
BR2#	AA1
BR3#	U9
CPUPRES#	B2
D0#	C25
D1#	A27
D2#	C27
D3#	A29
D4#	C29
D5#	A31
D6#	C31
D7#	C33
D8#	A33
D9#	A35
D10#	A39
D11#	A41
D12#	C35
D13#	A43
D14#	A37
D15#	C37
D16#	A45
D17#	C39
D18#	C43
D19#	C45
D20#	C41
D21#	C47
D22#	E39
D23#	E41
D24#	E45
D25#	E43
D26#	E47
D27#	G39
D28#	G45
D29#	G41
D30#	G43
D31#	G47
D32#	J39
D33#	J45
D34#	J47
D35#	J41
D36#	L45
D37#	L39

Table 26. Pin Listing in Alphabetic Order
(Continued)

Signal Name	Pin #
D38#	J43
D39#	L47
D40#	L41
D41#	N47
D42#	N45
D43#	L43
D44#	N39
D45#	N41
D46#	Q47
D47#	N43
D48#	Q45
D49#	Q43
D50#	S47
D51#	Q39
D52#	Q41
D53#	S45
D54#	S43
D55#	U47
D56#	U45
D57#	S41
D58#	W47
D59#	S39
D60#	U43
D61#	W45
D62#	Y47
D63#	W43
DBSY#	AA5
DEFER#	Y5
DEP0#	AC45
DEP1#	Y43
DEP2#	W39
DEP3#	AC47
DEP4#	W41
DEP5#	AA47
DEP6#	Y45
DEP7#	U39
DRDY#	AA3
FERR#	C17
FLUSH#	A15
FRCERR	C9
HIT#	AC3
HITM#	AA7
IERR#	C3
IGNNE#	A9
INIT#	C11
LINT0/INTR	AG43
LINT1/NMI	AG41
LOCK#	AA9
PICCLK	AA43
PICD0	AA41
PICD1	AE41
PLL1	C19
PLL2	C23
PRDY#	Y39
PREQ#	AA45
PWRGOOD	AG7
REQ0#	W9
REQ1#	W7
REQ2#	Y3
REQ3#	Y1
REQ4#	W5

Table 26. Pin Listing in Alphabetic Order
(Continued)

Signal Name	Pin #
RESERVED	A21
RESERVED	L1
RESERVED	AC1
RESERVED	AE1
RESERVED	AE45
RESERVED	AG5
RESERVED	AG9
RESERVED	AG39
RESERVED	AG47
RESERVED	AS9
RESERVED	AS47
RESERVED	AU1
RESERVED	AU5
RESERVED	AU9
RESERVED	AU39
RESERVED	AU43
RESERVED	AU47
RESERVED	AW3
RESERVED	AW7
RESERVED	AW41
RESERVED	AW45
RESERVED	AY1
RESERVED	AY3
RESERVED	AY5
RESERVED	AY7
RESERVED	AY9
RESERVED	AY39
RESERVED	AY41
RESERVED	AY43
RESERVED	AY45
RESERVED	AY47
RESERVED	BA3
RESERVED	BA7
RESERVED	BA11
RESERVED	BA35
RESERVED	BA41
RESERVED	BA45
RESERVED	BC11
RESERVED	BC19
RESERVED	BC23
RESERVED	BC27
RESERVED	BC31
RESERVED	BC35
RESET#	Y41
RP#	AC7
RS0#	AC9
RS1#	AE5
RS2#	AE7
RSP#	U3
SMI#	W1
STPCLK#	A3
TCK	A5
TDI	A13
TDO	C13
TESTHI	A23
TESTHI	A25
TESTHI	AE39
TESTLO	C21
TESTLO	AS39
TESTLO	AS41
TESTLO	AS43

Table 26. Pin Listing in Alphabetic Order
(Continued)

Signal Name	Pin #
TESTLO	AS45
TESTLO	BA13
TESTLO	BA15
TESTLO	BA33
TESTLO	BA37
TESTLO	BC13
TESTLO	BC15
TESTLO	BC33
TESTLO	BC37
THERMTRIP#	A17
TMS	C15
TRDY#	Y9
TRST#	A7
UP#	AG3
$V_{CC}5$	AG1
$V_{CC}P$	B4
$V_{CC}P$	B8
$V_{CC}P$	B16
$V_{CC}P$	B24
$V_{CC}P$	B32
$V_{CC}P$	B40
$V_{CC}P$	B44
$V_{CC}P$	F2
$V_{CC}P$	F6
$V_{CC}P$	F42
$V_{CC}P$	F46
$V_{CC}P$	K4
$V_{CC}P$	K44
$V_{CC}P$	P2
$V_{CC}P$	P6
$V_{CC}P$	P42
$V_{CC}P$	P46
$V_{CC}P$	T4
$V_{CC}P$	T44
$V_{CC}P$	X6
$V_{CC}P$	X42
$V_{CC}P$	AB4
$V_{CC}P$	AB44
$V_{CC}P$	AJ3
$V_{CC}P$	AJ7
$V_{CC}P$	AJ41
$V_{CC}P$	AJ45
$V_{CC}P$	AL1
$V_{CC}P$	AL5
$V_{CC}P$	AL9
$V_{CC}P$	AL39
$V_{CC}P$	AL43
$V_{CC}P$	AL47
$V_{CC}P$	AN3
$V_{CC}P$	AN7
$V_{CC}P$	AN41
$V_{CC}P$	AN45
$V_{CC}P$	AQ1
$V_{CC}P$	AQ5
$V_{CC}P$	AQ9
$V_{CC}P$	AQ39
$V_{CC}P$	AQ43
$V_{CC}P$	AQ47
$V_{CC}P$	BA17
$V_{CC}P$	BA21
$V_{CC}P$	BA25

Table 26. Pin Listing in Alphabetic Order
(Continued)

Signal Name	Pin #
$V_{CC}P$	BA29
VID0	AS1
VID1	AS3
VID2	AS5
VID3	AS7
$V_{REF}0$	A1
$V_{REF}1$	C7
$V_{REF}2$	S7
$V_{REF}3$	Y7
$V_{REF}4$	A47
$V_{REF}5$	AE47
$V_{REF}6$	U41
$V_{REF}7$	AG45
V_{SS}	B6
V_{SS}	B12
V_{SS}	B20
V_{SS}	B28
V_{SS}	B36
V_{SS}	B42
V_{SS}	B46
V_{SS}	F4
V_{SS}	F8
V_{SS}	F40
V_{SS}	F44
V_{SS}	K2
V_{SS}	K6
V_{SS}	K8
V_{SS}	K40
V_{SS}	K42
V_{SS}	K46
V_{SS}	P4
V_{SS}	P8
V_{SS}	P40
V_{SS}	P44
V_{SS}	T2
V_{SS}	T6
V_{SS}	T8
V_{SS}	T40
V_{SS}	T42
V_{SS}	T46
V_{SS}	X2
V_{SS}	X4
V_{SS}	X8
V_{SS}	X40
V_{SS}	X44
V_{SS}	X46
V_{SS}	AB2
V_{SS}	AB6
V_{SS}	AB8
V_{SS}	AB40
V_{SS}	AB42
V_{SS}	AB46
V_{SS}	AF2
V_{SS}	AF4
V_{SS}	AF6
V_{SS}	AF8
V_{SS}	AF40
V_{SS}	AF42
V_{SS}	AF44
V_{SS}	AF46
V_{SS}	AJ1

Table 26. Pin Listing in Alphabetic Order
(Continued)

Signal Name	Pin #
V_{SS}	AJ5
V_{SS}	AJ9
V_{SS}	AJ39
V_{SS}	AJ43
V_{SS}	AJ47
V_{SS}	AL3
V_{SS}	AL7
V_{SS}	AL41
V_{SS}	AL45
V_{SS}	AN1
V_{SS}	AN5
V_{SS}	AN9
V_{SS}	AN39
V_{SS}	AN43
V_{SS}	AN47
V_{SS}	AQ3
V_{SS}	AQ7
V_{SS}	AQ41
V_{SS}	AQ45
V_{SS}	AU3
V_{SS}	AU7
V_{SS}	AU41
V_{SS}	AU45
V_{SS}	AW1
V_{SS}	AW5
V_{SS}	AW9
V_{SS}	AW39
V_{SS}	AW43
V_{SS}	AW47
V_{SS}	BA1
V_{SS}	BA5
V_{SS}	BA9
V_{SS}	BA19
V_{SS}	BA23
V_{SS}	BA27
V_{SS}	BA31
V_{SS}	BA39
V_{SS}	BA43
V_{SS}	BA47
V_{SS}	BC1
V_{SS}	BC3
V_{SS}	BC5
V_{SS}	BC7
V_{SS}	BC9
V_{SS}	BC17
V_{SS}	BC21
V_{SS}	BC25
V_{SS}	BC29
V_{SS}	BC39
V_{SS}	BC41
V_{SS}	BC43
V_{SS}	BC45
V_{SS}	BC47

6.2. Introduction of Flatness

The Pentium Pro processor with 1 MB L2 cache has a characterized flatness due to its new packaging technology. The flatness is defined as a variance from a planar and homogenous surface. In this document, warpage and flatness are often used interchangeably. The warpage describes the depth of the nonflat surface. The warpage is measured in mils, and a reference point to highest variation along the Z axis. As an example, one can use a precise file along the top surface of the back plate of the processor from one corner the other corner. There will be a gap between the file and the back plate. The processor back plate shows homogenous warpage which is shown in Figure 27. (The lowest spot is at the center and the highest spot is at the corners.)

6.3. Critical Zone and Pedestal Area

If a reference point is the center of the back plate, warpage increases towards to the sides and to the corners. The flatness specification is defined in two ways:

1. Critical zone flatness
2. Overall back plate flatness

The critical zone is defined as the optimal heat sink contact area given the flatness associated with this product. This has been based on several test results and optimizations. The critical area is defined as a 2.1" x 1.3" rectangular area which centers on the die area of the processor. The heat sink and pedestal shape are shown in Figure 28.

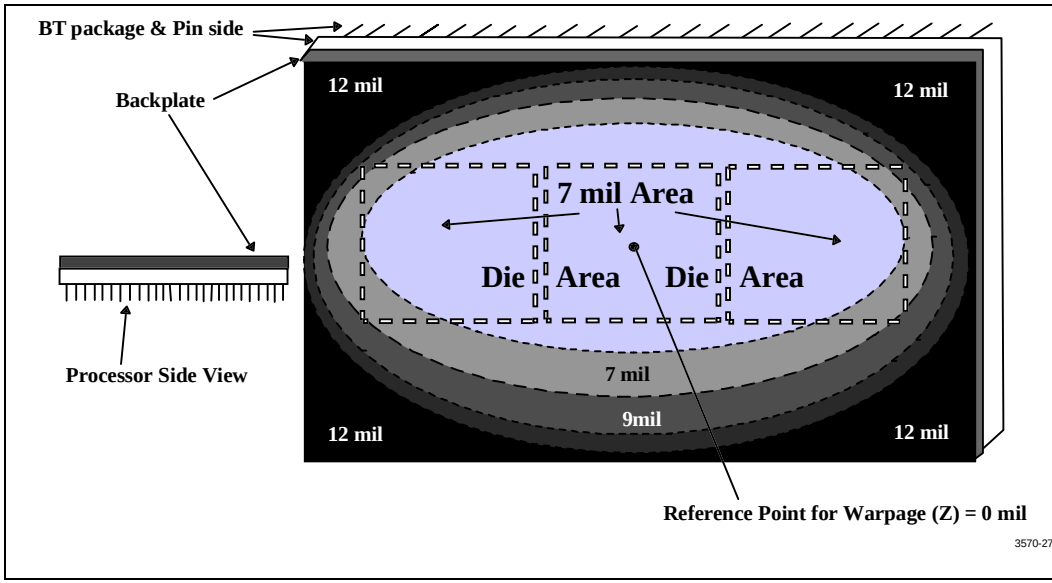


Figure 27. Processor Top View with Back Plate Warpage Mapping

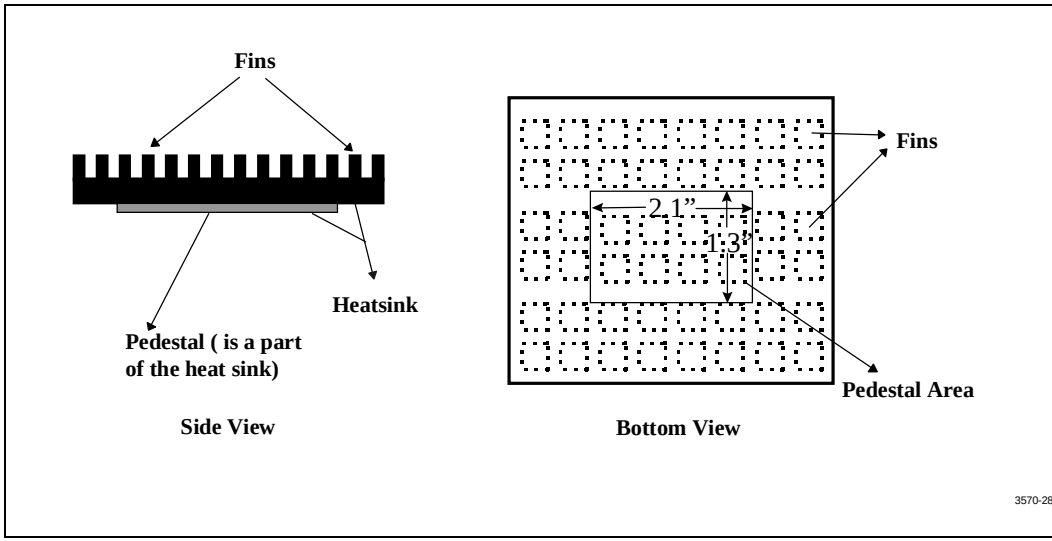


Figure 28. Pedestal Shape Bottom and Side View

The thickness of the pedestal may vary depending on the heat sink vendor. System designers need to consider their system issues in order to optimize their thermal solution. Pedestal size is specified in Table 28 for optimal performance. Flatness in the direction of Z-axis is specified in Table 27.

Table 27. Flatness Specification

Area (Centered)	Maximum Warpage
2.1" x 1.3"	0.0070"
2.66" x2.46" (Total package area)	0.012"

Table 28. Pedestal Specification

Dimensions	Minimum Specification (in inches)
Length	2.1
Width	1.3
Thickness (step)	0.015

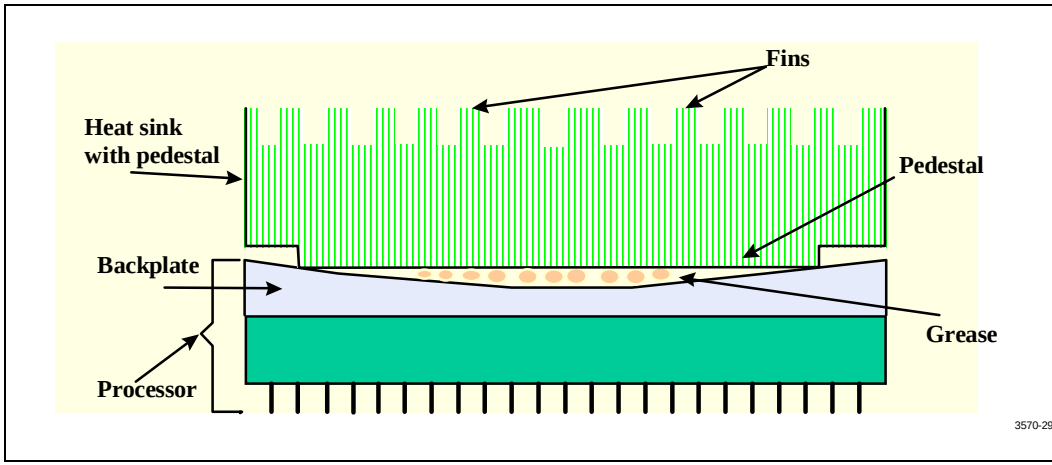


Figure 29. Heat Sink with Pedestal Placement on Processor Side View

6.3.1. BACKPLATE PRESSURE SPECIFICATION

For the specified pedestal area of 2.1" X 1.3" (which is the critical zone), the maximum backplate pressure is not to exceed 20 lbs.

6.4. Heat Sink Design Recommendations

OEMs may choose to design their heat sink solutions in various ways. Figure 29 shows how a heat sink with a pedestal attaches to the top of the processor. OEMs may choose not to use a pedestal type of heat sink solution if thermal analysis shows that the case temperature stays under the maximum operating temperature given in Table 4.

6.4.1. FAN HEAT SINK

Another option is to design a fan heat sink along with a pedestal as the thermal solution. Figure 30 demonstrates an example fan heat sink. The dimensions for a possible 2-fan heat sink are listed in Table 29. The location of the fans and attachment clips depend on the system requirements.

Table 29. Dimensions for Figure 30

	Dimension Table
A	3.5" + .25/-0.0
B	2.0" + .25/ -0.0
C	3.20" maximum
D	3.00" maximum
E	1.30" maximum
F	0.185" +/- .015" (clip spacing)
G	0.015" minimum, .050" maximum
H	1.475" maximum
I	0.950" clip attachment spacing

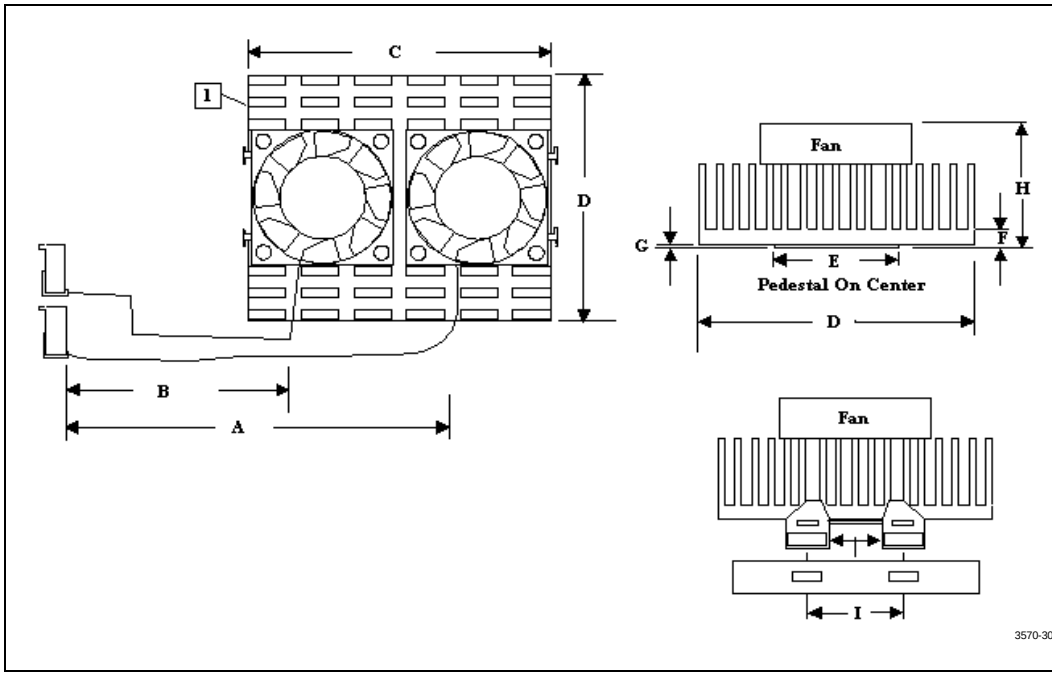


Figure 30. Example Fan Heat Sink

6.5. Lid Strength Specification

The lid of a Pentium Pro processor with 1 MB L2 cache can sustain 10 pounds of force. Exceeding this limit puts the part at risk and makes its behavior unpredictable. The lid is the pin side cover.

6.6. Coplanarity Specification

Coplanarity, here, is defined as the variation along the z-axis, between the lower most pin (located in the middle of the package) and the highest pin (located on the corners of the package). Coplanarity is specified not to exceed 15 mils. Refer to Figure 31 for details.

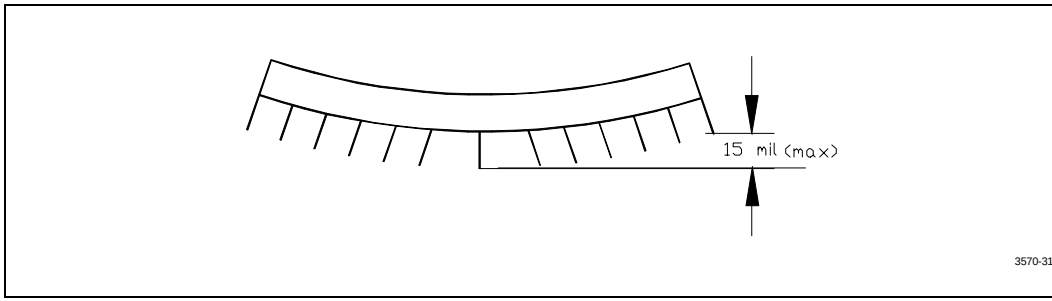


Figure 31. Coplanarity Specification

6.7. Predicted Storage Failure Rates

The anticipated failure rate, based on the storage temperature and relative humidity, is shown in Figure 32, as a graph. This graph reflects the moisture storage predictions at 40 °C/85% relative humidity. The diamond line shows the estimated failure rate over time based on HAST 130 °C/85% relative humidity monitors and an activation energy of 0.777 eV. The square line offers a worst case estimation from the same monitor data set using a lower confidence interval of 60%.

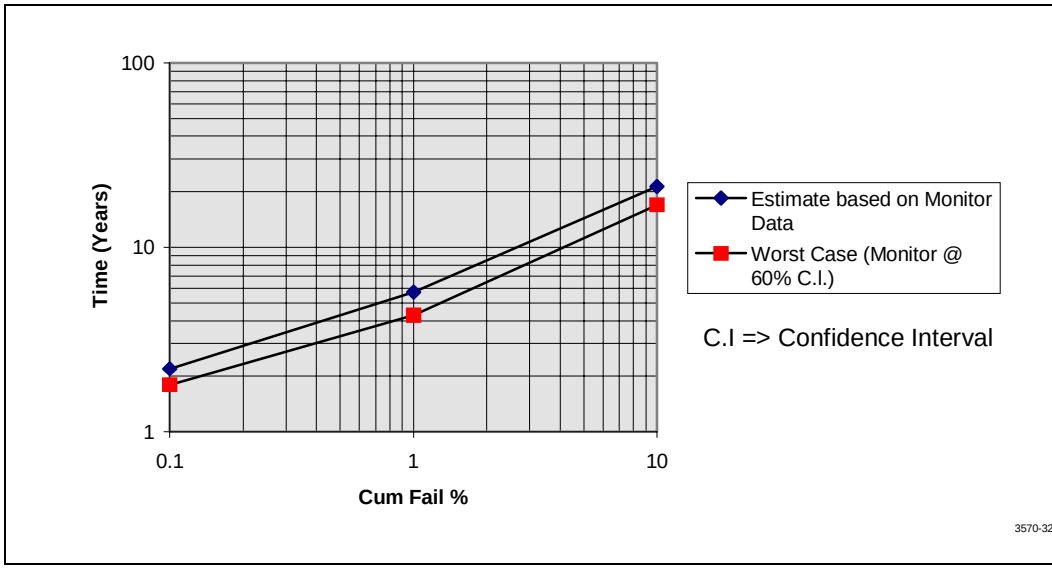


Figure 32. Expected Storage Failure Rates in Stringent Storage Conditions

APPENDIX A
SIGNAL LISTING

This appendix provides an alphabetical listing of all Pentium Pro processor signals. **Pins that do not appear here are not considered bus signals and are described in Table 2.**

A.0. ALPHABETICAL LISTING OF SIGNALS

A.1. A[35:3]# (I/O)

The A[35:3]# signals are the address signals. They are driven during the two-clock Request Phase by the request initiator. The signals in the two clocks are referenced Aa[35:3]# and Ab[35:3]#. During both clocks, A[35:24]# signals are protected with the AP1# parity signal, and A[23:3]# signals are protected with the AP0# parity signal.

The Aa[35:3]# signals are interpreted based on information carried during the first Request Phase clock on the REQa[4:0]# signals.

For memory transactions as defined by REQa[4:0]# = {XX01X,XX10X,XX11X}, the Aa[35:3]# signals define a 2^{36}-byte physical memory address space. The cacheable agents in the system observe the Aa[35:3]# signals and begin an internal snoop. The memory agents in the system observe the Aa[35:3]# signals and begin address decode to determine if they are responsible for the transaction completion. Aa[4:3]# signals define the critical word, the first data chunk to be transferred on the data bus. Cache line transactions use the burst order described in *Pentium® Pro Processor Family Developer's Manual, Volume 1: Specifications* (Order Number 242690), to transfer the remaining three data chunks.

For Pentium Pro processor IO transactions as defined by REQa[4:0]# = 1000X, the signals Aa[16:3]# define a 64K+3 byte physical IO space. The IO agents in the system observe the signals and begin address decode to determine if they are responsible for the transaction completion. Aa[35:17]# are always zero. Aa16# is zero unless the IO space being accessed is the first three bytes of a 64 KByte address range.

For deferred reply transactions as defined by REQa[4:0]# = 00000, Aa[23:16]# carry the deferred ID. This signal is the same deferred ID supplied by the request initiator of the original transaction on Ab[23:16]#/DID[7:0]# signals. Pentium Pro processor bus agents that support deferred replies sample the deferred ID and perform an internal match against any outstanding transactions waiting for deferred replies. During a deferred reply, Aa[35:24]# and Aa[15:3]# are reserved.

For the branch-trace message transaction as defined by REQa[4:0]# = 01001 and for special and interrupt acknowledge transactions, as defined by REQa[4:0]# = 01000, the Aa[35:3]# signals are reserved and undefined.

During the second clock of the Request Phase, Ab[35:3]# signals perform identical signal functions for all transactions. For ease of description, these functions are described using new signal names. Ab[31:24]# are renamed the attribute signals ATTR[7:0]#. Ab[23:16]# are renamed the Deferred ID signals DID[7:0]#. Ab[15:8]# are renamed the eight-byte enable signals BE[7:0]#. Ab[7:3]# are renamed the extended function signals EXF[4:0]#.

Table 30. Request Phase Decode

Ab[31:24]#	Ab[23:16]#	Ab[15:8]#	Ab[7:3]#
ATTR[7:0]#	DID[7:0]#	BE[7:0]#	EXF[4:0]#

On the active-to-inactive transition of RESET#, each Pentium Pro processor bus agent samples A[35:3]# signals to determine its power-on configuration.

A.2. A20M# (I)

The A20M# signal is the address-20 mask signal in the PC Compatibility group. If the A20M# input signal is asserted, the Pentium Pro processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap around at the one Mbyte boundary. Only assert A20M# when the processor is in real mode. The effect of asserting

A20M# in protected mode is undefined and may be implemented differently in future processors.

Snoop requests and cache-line write back transactions are unaffected by A20M# input. Address 20 is not masked when the processor samples external addresses to perform internal snooping.

A20M# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, A20M# must be valid with active RS[2:0]# signals of the corresponding I/O Write bus transaction. In FRC mode, A20M# must be synchronous to BCLK.

During active RESET#, the Pentium Pro processor begins sampling the A20M#, IGNNE#, and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. After the PLL-lock time, the core clock becomes stable and is locked to the external bus clock. On the active-to-inactive transition of RESET#, the Pentium Pro processor latches A20M#, IGNNE#, and LINT[1:0] and freezes the frequency ratio internally. See Table 31.

A.3. ADS# (I/O)

The ADS# signal is the address Strobe signal. It is asserted by the current bus owner for one clock to indicate a new Request Phase. A new Request Phase can only begin if the In-order Queue has less than the maximum number of entries defined by the power-on configuration (1 or 8), the Request Phase is not being stalled by an active BNR# sequence and the ADS# associated with the previous Request Phase is sampled inactive. Along with the ADS#, the request initiator drives A[35:3]#, REQ[4:0]#, AP[1:0]#, and RP# signals for two clocks. During the second Request Phase clock, ADS# must be inactive. RP# provides parity protection for REQ[4:0]# and ADS# signals during both clocks. If the transaction is part of a bus locked operation, LOCK# must be active with ADS#.

If the request initiator continues to own the bus after the first Request Phase, it can issue a new request every three clocks. If the request initiator needs to release the bus ownership after the Request Phase, it can deactivate its BREQn#/BPRI# arbitration signal as early as with the activation of ADS#.

All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. On sampling the asserted ADS#, all agents load the new transaction in the In-order Queue and update internal counters. The Error, Snoop, Response, and Data Phase of the transaction are defined with respect to ADS# assertion.

Table 31. Bus Clock Ratios Versus Pin Logic Levels

Ratio of Core Clock to Bus Clock	LINT[1]/NMI	LINT[0]/INTR	IGNNE#	A20M#
2	L	L	L	L
2	H	H	H	H
3	L	L	H	L
4	L	L	L	H
RESERVED	L	L	H	H
5/2	L	H	L	L
7/2	L	H	H	L
RESERVED	L	H	L	H
RESERVED	L	H	H	H
RESERVED	ALL OTHER COMBINATIONS			

A.4. AERR# (I/O)

The AERR# signal is the address parity error signal. Assuming the AERR# driver is enabled during the power-on configuration, a bus agent can drive AERR# active for exactly one clock during the Error Phase of a transaction. AERR# must be inactive for a minimum of two clocks. The Error Phase is always three clocks from the beginning of the Request Phase.

On observing active ADS#, all agents begin parity and protocol checks for the signals valid in the two Request Phase clocks. Parity is checked on AP[1:0]# and RP# signals. AP1# protects A[35:24]#, AP0# protects A[23:3]# and RP# protects REQ[4:0]#. A parity error without a protocol violation is signaled by AERR# assertion.

If AERR# observation is enabled during power-on configuration, AERR# assertion in a valid Error Phase aborts the transaction. All bus agents remove the transaction from the In-order Queue and update internal counters. The Snoop Phase, Response Phase, and Data Phase of the transaction are aborted. All signals in these phases must be deasserted two clocks after AERR# is asserted, even if the signals have been asserted before AERR# has been observed. Specifically if the Snoop Phase associated with the aborted transaction is driven in the next clock, the snoop results, including a STALL condition (HIT# and HITM# asserted for one clock), are ignored. All bus agents must also begin an arbitration reset sequence and deassert BREQn#/BPRI# arbitration signals on sampling AERR# active. A current bus owner in the middle of a bus lock operation must keep LOCK# asserted and assert its arbitration request BPRI#/BREQn# after keeping it inactive for two clocks to retain its bus ownership and guarantee lock atomicity. All other agents, including the current bus owner not in the middle of a bus lock operation, must wait at least 4 clocks before asserting BPRI#/BREQn# and beginning a new arbitration.

If AERR# observation is enabled, the request initiator can retry the transaction up to n times until it reaches the retry limit defined by its implementation. (The Pentium Pro processor retries once.) After n retries, the request initiator treats the error as a hard error. The request initiator asserts BERR# or enters the Machine Check Exception handler, as defined by the system configuration.

If AERR# observation is disabled during power-on configuration, AERR# assertion is ignored by all bus agents except a central agent. Based on the Machine Check Architecture of the system, the central agent can ignore AERR#, assert NMI to execute NMI handler, or assert BINIT# to reset the bus units of all agents and execute an MCE handler.

A.5. AP[1:0]# (I/O)

The AP[1:0]# signals are the address parity signals. They are driven by the request initiator during the two Request Phase clocks along with ADS#, A[35:3]#, REQ[4:0]#, and RP#. AP1# covers A[35:24]#. AP0# covers A[23:3]#. A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This rule allows parity to be high when all the covered signals are high.

Provided “AERR# drive” is enabled during the power-on configuration, all bus agents begin parity checking on observing active ADS# and determine if there is a parity error. On observing a parity error on any one of the two Request Phase clocks, the bus agent asserts AERR# during the Error Phase of the transaction.

A.6. ASZ[1:0]# (I/O)

The ASZ[1:0]# signals are the memory address-space size signals. They are driven by the request initiator during the first Request Phase clock on the REQa[4:3]# pins. The ASZ[1:0]# signals are valid only when REQa[1:0]# signals equal 01B, 10B, or 11B, indicating a memory access transaction. The ASZ[1:0]# decode is defined in Table 32.

Table 32. ASZ[1:0]# Signal Decode

ASZ[1:0]#		Description
0	0	0 <= A[35:3]# < 4 GB
0	1	4 GB <= A[35:3]# < 64 GB
1	X	Reserved

If the memory access is within the 0-to-(4GByte-1) address space, ASZ[1:0]# must be 00B. If the memory access is within the 4Gbyte-to-(64 GByte-1) address space, ASZ[1:0]# must be 01B. All

Table 33. ATTR[7:0]# Field Descriptions

ATTR[7:3]#	ATTR[2]#	ATTR[1:0]#			
XXXXX	X	11	10	01	00
Reserved	Potentially Speculatable	Write-Back	Write-Protect	Write-Through	UnCacheable

observing bus agents that support the 4Gbyte (32 bit) address space must respond to the transaction only when ASZ[1:0]# equals 00. All observing bus agents that support the 64GByte (36-bit) address space must respond to the transaction when ASZ[1:0]# equals 00B or 01B.

A.7. ATTR[7:0]# (I/O)

The ATTR[7:0]# signals are the attribute signals. They are driven by the request initiator during the second Request Phase clock on the Ab[31:24]# pins. The ATTR[7:0]# signals are valid for all transactions. The ATTR[7:3]# are reserved and undefined. The ATTR[2:0]# are driven based on the Memory Range Register attributes and the Page Table attributes. Table 33 defines ATTR[3:0]# signals.

A.8. BCLK (I)

The BCLK (clock) signal is the Execution Control group input signal. It determines the bus frequency. All agents drive their outputs and latch their inputs on the BCLK rising edge.

The BCLK signal indirectly determines the Pentium Pro processor's internal clock frequency. Each Pentium Pro processor derives its internal clock from BCLK by multiplying the BCLK frequency by a ratio as defined and allowed by the power-on configuration. See Table 31.

All external timing parameters are specified with respect to the BCLK signal.

A.9. BE[7:0]# (I/O)

The BE[7:0]# signals are the byte-enable signals. They are driven by the request initiator during the second Request Phase clock on the Ab[15:8]# pins. These signals carry various information depending on the REQ[4:0]# value.

For memory or I/O transactions (REQa[4:0]# = {10000B, 10001B, XX01XB, XX10XB, XX11XB}) the byte-enable signals indicate that valid data is requested or being transferred on the corresponding byte on the 64 bit data bus. BE0# indicates D[7:0]# is valid, BE1# indicates D[15:8]# is valid,..., BE7# indicates D[63:56]# is valid.

For Special transactions ((REQa[4:0]# = 01000B) and (REQb[1:0]# = 01B)), the BE[7:0]# signals carry special cycle encodings as defined in Table 34. All other encodings are reserved.

Table 34. Special Transaction Encoding on BE[7:0]#

BE[7:0]#	Special Cycle
0000 0000	Reserved
0000 0001	Shutdown
0000 0010	Flush
0000 0011	Halt
0000 0100	Sync
0000 0101	Flush Acknowledge
00000 0110	Stop Clock Acknowledge
00000 0111	SMI Acknowledge
Other	Reserved

For Deferred Reply, Interrupt Acknowledge, and Branch Trace Message transactions, the BE[7:0]# signals are undefined.

A.10. BERR# (I/O)

The BERR# signal is the Error group Bus Error signal. It is asserted to indicate an unrecoverable error without a bus protocol violation.

The BERR# protocol is as follows: If an agent detects an unrecoverable error for which BERR# is a valid error response and BERR# is sampled inactive, it asserts BERR# for three clocks. An agent can assert BERR# only after observing that the signal is inactive. An agent asserting BERR# must deassert the signal in two clocks if it observes that another agent began asserting BERR# in the previous clock.

BERR# assertion conditions are defined by the system configuration. Configuration options enable the BERR# driver as follows:

- Enabled or disabled
- Asserted optionally for internal errors along with IERR#
- Optionally asserted by the request initiator of a bus transaction after it observes an error
- Asserted by any bus agent when it observes an error in a bus transaction

BERR# sampling conditions are also defined by the system configuration. Configuration options enable the BERR# receiver to be enabled or disabled. When a central agent samples an active BERR# signal, it can forward the BERR# as an NMI or BINIT# to one of the processors. The Pentium Pro processor does not support BERR# sampling (always disabled).

A.11. BINIT# (I/O)

The BINIT# signal is the bus initialization signal. If the BINIT# driver is enabled during the power on configuration, BINIT# is asserted to signal any bus condition that prevents reliable future information.

The BINIT# protocol is as follows: If an agent detects an error for which BINIT# is a valid error response, and BINIT# is sampled inactive, it asserts BINIT# for three clocks. An agent can assert BINIT# only after observing that the signal is inactive. An agent asserting BINIT# must deassert the signal in two clocks if it observes that another agent began asserting BINIT# in the previous clock.

If BINIT# observation is enabled during power-on configuration, and BINIT# is sampled asserted, all bus state machines are reset. All agents reset their rotating ID for bus arbitration to the state after reset, and internal count information is lost. The L1 and L2 caches are not affected.

If BINIT# observation is disabled during power-on configuration, BINIT# is ignored by all bus agents except a central agent that must handle the error in a manner appropriate to the system architecture.

A.12. BNR# (I/O)

The BNR# signal is the Block Next Request signal in the Arbitration group. The BNR# signal is used to assert a bus stall by any bus agent who is unable to accept new bus transactions to avoid an internal transaction queue overflow. During a bus stall, the current bus owner cannot issue any new transactions.

Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges. A valid bus stall involves assertion of BNR# for one clock on a well-defined clock edge (T1), followed by de-assertion of BNR# for one clock on the next clock edge (T1+1). BNR# can first be sampled on the second clock edge (T1+1) and must always be ignored on the third clock edge (T1+2). An extension of a bus stall requires one clock active (T1+2), one clock inactive (T1+3) BNR# sequence with BNR# sampling points every two clocks (T1+1, T1+3,...).

After the RESET# active-to-inactive transition, bus agents might need to perform hardware initialization of their bus unit logic. Bus agents intending to create a request stall must assert BNR# in the clock after RESET# is sampled inactive.

After BINIT# assertion, all bus agents go through a similar hardware initialization and can create a request stall by asserting BNR# four clocks after BINIT# assertion is sampled.

On the first BNR# sampling clock that BNR# is sampled inactive, the current bus owner is allowed to issue one new request. Any bus agent can immediately reassert BNR# (four clocks from the previous assertion or two clocks from the previous de-assertion) to create a new bus stall. This throttling mechanism enables independent control on every new request generation.

Table 35. BR[3:0]# Signals Rotating Interconnect

Bus Signal	Agent 0 Pins	Agent 1 Pins	Agent 2 Pins	Agent 3 Pins
BREQ0#	BR0#	BR3#	BR2#	BR1#
BREQ1#	BR1#	BR0#	BR3#	BR2#
BREQ2#	BR2#	BR1#	BR0#	BR3#
BREQ3#	BR3#	BR2#	BR1#	BR0#

If BNR# is deasserted on two consecutive sampling points, new requests can be freely generated on the bus. After receiving a new transaction, a bus agent can require an address stall due to an anticipated transaction-queue overflow condition. In response, the bus agent can assert BNR#, three clocks from active ADS# assertion and create a bus stall. Once a bus stall is created, the bus remains stalled until BNR# is sampled asserted on subsequent sampling points.

A.13. BP[3:2]# (I/O)

The BP[3:2]# signals are the System Support group Breakpoint signals. They are outputs from the Pentium Pro processor that indicate the status of breakpoints.

A.14. BPM[1:0]# (I/O)

The BPM[1:0]# signals are more System Support group breakpoint and performance monitor signals. They are outputs from the Pentium Pro processor that indicate the status of breakpoints and programmable counters used for monitoring Pentium Pro processor performance.

A.15. BPRI# (I)

The BPRI# signal is the Priority-agent Bus Request signal. The priority agent arbitrates for the bus by asserting BPRI#. The priority agent is always be the next bus owner. Observing BPRI# active causes the current symmetric owner to stop issuing new requests, unless such requests are part of an ongoing locked operation.

If LOCK# is sampled inactive two clocks from BPRI# driven asserted, the priority agent can issue a new request within four clocks of asserting BPRI#. The priority agent can further reduce its arbitration latency to two clocks if it samples active ADS# and inactive LOCK# on the clock in which BPRI# was driven active and to three clocks if it samples active ADS# and inactive LOCK# on the clock in which BPRI# was sampled active. If LOCK# is sampled active, the priority agent must wait for LOCK# deasserted and gains bus ownership in two clocks after LOCK# is sampled deasserted. The priority agent can keep BPRI# asserted until all of its requests are completed and can release the bus by de-asserting BPRI# as early as the same clock edge on which it issues the last request.

On observation of active AERR#, RESET#, or BINIT#, BPRI# must be deasserted in the next clock. BPRI# can be reasserted in the clock after sampling the RESET# active-to-inactive transition or three clocks after sampling BINIT# active and RESET# inactive. On AERR# assertion, if the priority agent is in the middle of a bus-locked operation, BPRI# must be re-asserted after two clocks, otherwise BPRI# must stay inactive for at least 4 clocks.

After the RESET# inactive transition, Pentium Pro processor bus agents begin BPRI# and BNR# sampling on BNR# sample points. When both BNR# and BPRI# are observed inactive on a BNR# sampling point, the APIC units in Pentium Pro processors on a common APIC bus are synchronized.

A.16. BR0#(I/O), BR[3:1]# (I)

The BR[3:0]# pins are the physical bus request pins that drive the BREQ[3:0]# signals in the system. The BREQ[3:0]# signals are interconnected in a rotating manner to individual processor pins. Table 35 gives the rotating interconnect between the processor and bus signals.

During power-up configuration, the central agent must assert the BR0# bus signal. All symmetric

agents sample their BR[3:0]# pins on active-to-inactive transition of RESET#. The pin on which the agent samples an active level determines its agent ID. All agents then configure their pins to match the appropriate bus signal protocol, as shown in Table 36.

Table 36. BR[3:0]# Signal Agent IDs

Pin Sampled Active on RESET#	Agent ID
BR0#	0
BR3#	1
BR2#	2
BR1#	3

A.17. BREQ[3:0]# (I/O)

The BREQ[3:0]# signals are the Symmetric-agent Arbitration Bus signals (called bus request). A symmetric agent n arbitrates for the bus by asserting its BREQn# signal. Agent n drives BREQn# as an output and receives the remaining BREQ[3:0]# signals as inputs.

The symmetric agents support distributed arbitration based on a round-robin mechanism. The rotating ID is an internal state used by all symmetric agents to track the agent with the lowest priority at the next arbitration event. At power-on, the rotating ID is initialized to three, allowing agent 0 to be the highest priority symmetric agent. After a new arbitration event, the rotating ID of all symmetric agents is updated to the agent ID of the symmetric owner. This update gives the new symmetric owner lowest priority in the next arbitration event.

A new arbitration event occurs either when a symmetric agent asserts its BREQn# on an Idle bus (all BREQ[3:0]# previously inactive), or the current symmetric owner de-asserts BREQm# to release the bus ownership to a new bus owner n. On a new arbitration event, based on BREQ[3:0]#, and the rotating ID, all symmetric agents simultaneously determine the new symmetric owner. The symmetric owner can park on the bus (hold the bus) provided that no other symmetric agent is requesting its use. The symmetric owner parks by keeping its BREQn# signal active. On sampling active BREQm# asserted by another symmetric agent, the symmetric owner de-asserts BREQn# as soon as possible to release the bus. A symmetric owner stops issuing new requests that are not part of an existing locked operation upon observing BPRI# active.

A symmetric agent can not deassert BREQn# until it becomes a symmetric owner. A symmetric agent can reassert BREQn# after keeping it inactive for one clock.

On observation of active AERR#, RESET#, or BINIT#, the BREQ[3:0]# signals must be deasserted in the next clock. BREQ[3:0]# can be reasserted in the clock after sampling the RESET# active-to-inactive transition or three clocks after sampling BINIT# active and RESET# inactive. On AERR# assertion, if bus agent n is in the middle of a bus-locked operation, BREQn# must be re-asserted after two clocks, otherwise BREQ[3:0]# must stay inactive for at least 4 clocks.

A.18. D[63:0]# (I/O)

The D[63:0]# signals are the data signals. They are driven during the Data Phase by the agent responsible for driving the data. These signals provide a 64-bit data path between various Pentium Pro processor bus agents. 32-byte line transfers require four data transfer clocks with valid data on all eight bytes. Partial transfers require one data transfer clock with valid data on the byte(s) indicated by active byte enables BE[7:0]#. Data signals not valid for a particular transfer must still have correct ECC (if data bus ECC is selected). If BE0# is asserted, D[7:0]# transfers the least significant byte. If BE7# is asserted, D[63:56]# transfers the most significant byte.

The data driver asserts DRDY# to indicate a valid data transfer. If the Data Phase involves more than one clock the data driver also asserts DBSY# at the beginning of the Data Phase and de-asserts DBSY# no earlier than on the same clock that it performs the last data transfer.

A.19. DBSY# (I/O)

The DBSY# signal is the Data-bus Busy signal. It indicates that the data bus is busy. It is asserted by the agent responsible for driving the data during the Data Phase, provided the Data Phase involves more than one clock. DBSY# is asserted at the beginning of the Data Phase and may be deasserted on or after the clock on which the last data is driven. The data

bus is released one clock after DBSY# is deasserted.

When normal read data is being returned, the Data Phase begins with the Response Phase. Thus the agent returning read data can assert DBSY# when the transaction reaches the top of the In-order Queue and it is ready to return response on RS[2:0]# signals. In response to a write request, the agent driving the write data must drive DBSY# active after the write transaction reaches the top of the In-order Queue and it sees active TRDY# with inactive DBSY# indicating that the target is ready to receive data. For an implicit write back response, the snoop agent must assert DBSY# active after the target memory agent of the implicit write back asserts TRDY#. Implicit write back TRDY# assertion begins after the transaction reaches the top of the In-order Queue, and TRDY# de-assertion associated with the write portion of the transaction, if any is completed. In this case, the memory agent guarantees assertion of implicit write back response in the same clock in which the snooping agent asserts DBSY#.

A.20. DEFER# (I)

The DEFER# signal is the defer signal. It is asserted by an agent during the Snoop Phase to indicate that the transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory agent or I/O agent. For systems that involve resources on a system bus other than the Pentium Pro processor bus, a bridge agent can accept the DEFER# assertion responsibility on behalf of the addressed agent.

When HITM# and DEFER# are both active during the Snoop Phase, HITM# is given priority and the transaction must be completed with implicit write back response. If HITM# is inactive, and DEFER# active, the agent asserting DEFER# must complete the transaction with a Deferred or Retry response.

If DEFER# is inactive, or HITM# is active, then the transaction is committed for in-order completion and snoop ownership is transferred normally between the requesting agent, the snooping agents, and the response agent.

If DEFER# is active with HITM# inactive, the transaction commitment is deferred. If the defer agent completes the transaction with a retry response, the requesting agent must retry the transaction. If the defer agent returns a deferred response, the requesting agent must freeze snoop state transitions associated with the deferred transaction and issues of new order-dependent transactions until the corresponding deferred reply transaction. In the meantime, the ownership of the deferred address is transferred to the defer agent and it must guarantee management of conflicting transactions issued to the same address.

If DEFER# is active in response to a newly issued bus-lock transaction, the entire bus-locked operation is re-initiated regardless of HITM#. This feature is useful for a bridge agent in response to a split bus-locked operation. It is recommended that the bridge agent extend the Snoop Phase of the first transaction in a split locked operation until it can either guarantee ownership of all system resources to enable successful completion of the split sequence or assert DEFER# followed by a Retry Response to abort the split sequence.

A.21. DEN# (I/0)

The DEN# signal is the defer-enable signal. It is driven to the bus on the second clock of the Request Phase on the EXF1#/Ab4# pin. DEN# is asserted to indicate that the transaction can be deferred by the responding agent.

A.22. DEP[7:0]# (I/O)

The DEP[7:0]# signals are the data bus ECC protection signals. They are driven during the Data Phase by the agent responsible for driving D[63:0]#. The DEP[7:0]# signals provide optional ECC protection for the data bus. During power-on configuration, DEP[7:0]# signals can be enabled for either ECC checking or no checking.

The ECC error correcting code can detect and correct single-bit errors and detect double-bit or nibble errors. The *Pentium® Pro Processor Family Developer's Manual, Volume 1: Specifications* (Order Number 242690), provides more information about ECC.

DEP[7:0]# provide valid ECC for the entire data bus on each data clock, regardless of which bytes are valid. If checking is enabled, receiving agents check the ECC signals for all 64 data signals.

A.23. DID[7:0]# (I/O)

The DID[7:0]# signals are Deferred Identifier signals. They are transferred using A[23:16]# signals by the request initiator. They are transferred on Ab[23:16]# during the second clock of the Request Phase on all transactions, but only defined for deferrable transactions (DEN# asserted). DID[7:0]# is also transferred on Aa[23:16]# during the first clock of the Request Phase for Deferred Reply transactions.

The deferred identifier defines the token supplied by the request initiator. DID[7:4]# carry the request initiators' agent identifier and DID[3:0]# carry a transaction identifier associated with the request. This configuration limits the bus specification to 16 bus masters with each one of the bus masters capable of making up to 16 requests.

Every deferrable transaction issued on the Pentium Pro processor bus which has not been guaranteed completion (has not successfully passed its Snoop Result Phase) will have a unique Deferred ID. This includes all outstanding transactions which have not had their snoop result reported, or have had their snoop results deferred. After a deferrable transaction passes its Snoop Result Phase without DEFER# asserted, its Deferred ID may be reused. Similarly, the deferred ID of a transaction which was deferred may be reused after the completion of the snoop window of the deferred reply.

DID[7]# indicates the agent type. Symmetric agents use 0. Priority agents use 1. DID[6:4]# indicates the agent ID. Symmetric agents use their arbitration ID. The Pentium Pro processor has four symmetric agents, so does not assert DID[6]#. DID[3:0]# indicates the transaction ID for an agent. The transaction ID must be unique for all transactions issued by an agent which have not reported their snoop results.

Table 37. DID[7:0]# Encoding

DID[7]	DID[6:4]	DID[3:0]
Agent Type	Agent ID	Transaction ID

The Deferred Reply agent transmits the DID[7:0]# (Ab[23:16]#) signals received during the original transaction on the Aa[23:16]# signals during the Deferred Reply transaction. This process enables the original request initiator to make an identifier match and wake up the original request waiting for completion.

A.24. DRDY# (I/O)

The DRDY# signal is the Data Phase data-ready signal. The data driver asserts DRDY# on each data transfer, indicating valid data on the data bus. In a multicycle data transfer, DRDY# can be deasserted to insert idle clocks in the Data Phase. During a line transfer, DRDY# is active for four clocks. During a partial 1-to-8 byte transfer, DRDY# is active for one clock. If a data transfer is exactly one clock, then the entire Data Phase may consist of only one clock active DRDY# and inactive DBSY#. If DBSY# is asserted for a 1-to-8 byte transfer, then the data bus is not released until one clock after DBSY# is deasserted.

A.25. DSZ[1:0]# (I/O)

The DSZ[1:0]# signals are the data-size signals. They are transferred on REQb[4:3]# signals in the second clock of Request Phase by the requesting agent. The DSZ[1:0]# signals define the data transfer capability of the requesting agent. For the Pentium Pro processor, DSZ#= 00, always.

A.26. EXF[4:0]# (I/O)

The EXF[4:0]# signals are the Extended Function signals and are transferred on the Ab[7:3]# signals by the request initiator during the second clock of the Request Phase. The signals specify any special functional requirement associated with the transaction based on the requester mode or capability. The signals are defined in Table 38.

Table 38. EXF[4:0]# Signal Definitions

EXF	NAME	External Functionality	When Activated
EXF4#	SMMEM#	SMM Mode	After entering SMM mode
EXF3#	SPLCK#	Split Lock	The first transaction of a split bus lock operation
EXF2#	Reserved	Reserved	
EXF1#	DEN#	Defer Enable	The transactions for which Defer or Retry Response is acceptable.
EXF0#	Reserved	Reserved	

A.27. FERR# (O)

The FERR# signal is the PC Compatibility group Floating-point Error signal. The Pentium Pro processor asserts FERR# when it detects an unmasked floating-point error. FERR# is included for compatibility with systems using DOS-type floating-point error reporting.

A.28. FLUSH# (I)

When the FLUSH# input signal is asserted, the Pentium Pro processor bus agent writes back all internal cache lines in the Modified state and invalidates all internal cache lines. At the completion of a flush operation, the Pentium Pro processor issues a Flush Acknowledge transaction to indicate that the cache flush operation is complete. The Pentium Pro processor stops caching any new data while the FLUSH# signal remains asserted.

FLUSH# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, FLUSH# must be valid along with RS[2:0]# in the Response Phase of the corresponding I/O Write bus transaction. In FRC mode, FLUSH# must be synchronous to BCLK.

On the active-to-inactive transition of RESET#, each Pentium Pro processor bus agent samples FLUSH# to determine its power-on configuration. See Table 31.

A.29. FRCERR (I/O)

The FRCERR signal is the Error group Functional-redundancy-check Error signal. If two Pentium Pro processors are configured in an FRC pair, as a single “logical” processor, then the checker processor asserts FRCERR if it detects a mismatch between its internally sampled outputs and the master processor’s outputs. The checker’s FRCERR output pin is connected to the master’s FRCERR input pin.

For point-to-point connections, the checker always compares against the master’s outputs. For bussed single-driver signals, the checker compares against the signal when the master is the only allowed driver. For bussed multiple-driver Wire-OR signals, the checker compares against the signal only if the master is expected to drive the signal low.

FRCERR is also toggled during the Pentium Pro processor’s reset action. A Pentium Pro processor asserts FRCERR for approximately 1 second after RESET’s active-to-inactive transition if it executes its built-in self-test (BIST). When BIST execution completes, the Pentium Pro processor de-asserts FRCERR if BIST completed successfully and continues to assert FRCERR if BIST fails. If the Pentium Pro processor does not execute the BIST action, then it keeps FRCERR asserted for approximately 20 clocks and then de-asserts it.

The Pentium® Pro Processor Family Developer’s Manual, Volume 1: Specifications (Order Number 242690), describes how a Pentium Pro processor can be configured as a master or a checker.

A.30. HIT# (I/O), HITM# (I/O)

The HIT# and HITM# signals are Snoop-hit and Hit-modified signals. They are snoop results asserted by any Pentium Pro processor bus agent in the Snoop Phase.

Any bus agent can assert both HIT# and HITM# together for one clock in the Snoop Phase to indicate that it requires a snoop stall. When a stall condition is sampled, all bus agents extend the Snoop Phase by two clocks. The stall can be continued by reasserting HIT# and HITM# together every other clock for one clock.

A caching agent must assert HITM# for one clock in the Snoop Phase if the transaction hits a Modified line, and the snooping agent must perform an implicit write back to update main memory. The snooping agent with the Modified line makes a transition to Shared state if the original transaction is Read Line or Read Partial, otherwise it transitions to Invalid state. A Deferred Reply transaction may have HITM# asserted to indicate the return of unexpected data.

A snooping agent must assert HIT# for one clock during the Snoop Phase if the line does not hit a Modified line in its write back cache and if at the end of the transaction it plans to keep the line in Shared state. Multiple caching agents can assert HIT# in the same Snoop Phase. If the requesting agent observes HIT# active during the Snoop Phase it can not cache the line in Exclusive or Modified state.

On observing a snoop stall, the agents asserting HIT# and HITM# independently reassert the signal after one inactive clock so that the correct snoop result is available, in case the Snoop Phase terminates after the two clock extension.

A.31. IERR# (O)

The IERR# signal is the Error group Internal Error Signal. A Pentium Pro processor asserts IERR# when it observes an internal error. It keeps IERR# asserted until it is turned off as part of the Machine Check Error handler, or with RESET# or BINIT# assertion. An NMI handler in software can indirectly accomplish the deassertion of IERR# via RESET# or BINIT# assertion.An internal error can be handled in several ways inside the processor based on its power-on configuration. If Machine Check Exception (MCE) is enabled, IERR# causes an MCE entry. IERR# can also be directed on the BERR# pin to indicate an error. Usually BERR# is sampled back by all processors to enter MCE or it can be redirected as an NMI by the central agent.

A.32. IGNNE# (I)

The IGNNE# signal is the Intel Architecture Compatibility group Ignore Numeric Error signal. If IGNNE# is asserted, the Pentium Pro processor ignores a numeric error and continues to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the Pentium Pro processor freezes on a noncontrol floating-point instruction if a previous instruction caused an error.

IGNNE# has no effect when the NE bit in control register 0 is set.

IGNNE# is an asynchronous input. However, to guarantee recognition of this signal following an I/O write instruction, IGNNE# must be valid along with RS[2:0]# in the Response Phase of the corresponding I/O Write bus transaction. In FRC mode, IGNNE# must be synchronous to BCLK.

During active RESET#, the Pentium Pro processor begins sampling the A20M#, IGNNE# and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Table 31. After the PLL-lock time, the core clock becomes stable and is locked to the external bus clock. On the active-to-inactive transition of RESET#, the Pentium Pro processor latches A20M# and IGNNE# and freezes the frequency ratio internally. Normal operation on the two signals continues two clocks after RESET# inactive is sampled.

A.33. INIT# (I)

The INIT# signal is the Execution Control group initialization signal. Active INIT# input resets integer registers inside all Pentium Pro processors without affecting their internal (L1 or L2) caches or their floating-point registers. Each Pentium Pro processor begins execution at the power-on reset vector configured during power-on configuration regardless of whether INIT# has gone inactive. The processor continues to handle snoop requests during INIT# assertion.

INIT# can be used to help performance of MS-DOS* extenders written for the Intel 80286 processor. INIT# provides a method to switch from protected mode to real mode while maintaining the contents of the internal caches and floating-point state. INIT# can not be used in lieu of RESET# after power-up.

On active-to-inactive transition of RESET#, each Pentium Pro processor bus agent samples INIT# signals to determine its power-on configuration. Two clocks after RESET# is sampled deasserted, these signals begin normal operation.

INIT# is an asynchronous input. In FRC mode, INIT# must be synchronous to BCLK.

A.34. INTR (I)

The INTR signal is the Interrupt Request signal. The INTR input indicates that an external interrupt has been generated. The interrupt is maskable using the IF bit in the EFLAGS register. If the IF bit is set, the Pentium Pro processor vectors to the interrupt handler after the current instruction execution is completed. Upon recognizing the interrupt request, the Pentium Pro processor issues a single Interrupt Acknowledge (INTA) bus transaction. INTR must remain active until the INTA bus transaction to guarantee its recognition.

INTR is sampled on every rising BCLK edge. INTR is an asynchronous input but recognition of INTR is guaranteed in a specific clock if it is asserted synchronously and meets the setup and hold times. INTR must also be deasserted for a minimum of two clocks to guarantee its inactive recognition. In FRC mode, INTR must be synchronous to BCLK. On power-up the LINT[1:0] signals are used for power-on-configuration of clock ratios. Both these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. Because APIC is enabled after reset, LINT[1:0] is the default configuration.

A.35. LEN[1:0]# (I/O)

The LEN[1:0]# signals are data-length signals. They are transmitted using REQb[1:0]# signals by the request initiator in the second clock of Request Phase. LEN[1:0]# define the length of the data transfer requested by the request initiator as defined in Table 39. The LEN[1:0]#, HITM#, and RS[2:0]# signals together define the length of the actual data transfer.

Table 39. LEN[1:0]# Data Transfer Lengths

LEN[1:0]#	Request Initiator's Data Transfer Length
00	0-8 Bytes
01	16 Bytes
10	32 Bytes
11	Reserved

A.36. LINT[1:0] (I)

The LINT[1:0] signals are the Execution Control group Local Interrupt signals. When APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the same signals for the Pentium processor. Both signals are asynchronous inputs. In FRC mode, LINT[1:0] must be synchronous to BCLK.

During active RESET#, the Pentium Pro processor continuously samples the A20M#, IGNNE# and LINT[1:0] values to determine the ratio of core-clock frequency to bus-clock frequency. See Table 31. After the PLL-lock time, the core clock becomes stable and is locked to the external bus clock. On the active-to-inactive transition of RESET#, the Pentium Pro processor latches the ratio internally.

Both these signals must be software configured by programming the APIC register space to be used either as NMI/INTR or LINT[1:0] in the BIOS. Because APIC is enabled after reset, LINT[1:0] is the default configuration.

A.37. LOCK# (I/O)

The LOCK# signal is the Arbitration group bus lock signal. For a locked sequence of transactions, LOCK# is asserted from the first transaction's Request Phase through the last transaction's Response Phase. A locked operation can be prematurely aborted (and LOCK# deasserted) if AERR# or DEFER# is asserted during the first bus transaction of the sequence. The sequence can also be prematurely aborted if a hard error (such as a hard failure response or AERR# assertion beyond the retry limit) occurs on any one of the transactions during the locked operation.

When the priority agent asserts BPRI# to arbitrate for bus ownership, it waits until it observes LOCK# deasserted. This enables symmetric agents to retain bus ownership throughout the bus locked operation and guarantee the atomicity of lock. If AERR# is asserted up to the retry limit during an ongoing locked operation, the arbitration protocol ensures that the lock owner receives the bus ownership after arbitration logic is reset. This result is accomplished by requiring the lock owner to reactivate its arbitration request one clock ahead of other agents' arbitration request. LOCK# is kept asserted throughout the arbitration reset sequence.

A.38. NMI (I)

The NMI signal is the Nonmaskable Interrupt signal. It is the state of the LINT1 signal when APIC is disabled. Asserting NMI causes an interrupt with an internally supplied vector value of 2. An external interrupt-acknowledge transaction is not generated. If NMI is asserted during the execution of an NMI service routine, it remains pending and is recognized after the IRET is executed by the NMI service routine. At most, one assertion of NMI is held pending.

NMI is rising-edge sensitive. Recognition of NMI is guaranteed in a specific clock if it is asserted synchronously and meets the setup and hold times. If asserted asynchronously, active and inactive pulse widths must be a minimum of two clocks. In FRC mode, NMI must be synchronous to BCLK.

A.39. PICCLK (I)

The PICCLK signal is the Execution Control group APIC Clock signal. It is an input clock to the Pentium Pro processor for synchronous operation of the APIC bus. PICCLK must be synchronous to BCLK in FRC mode.

A.40. PICD[1:0] (I/O)

The PICD[1:0] signals are the Execution Control group APIC Data signals. They are used for bi-directional serial message passing on the APIC bus.

A.41. PWRGOOD (I)

PWRGOOD is driven to the Pentium Pro processor by the system to indicate that the clocks and power supplies are within their specification. See Section 2.9. for additional details. This signal will not affect FRC operation.

A.42. REQ[4:0]# (I/O)

The REQ[4:0]# signals are the Request Command signals. They are asserted by the current bus owner in both clocks of the Request Phase. In the first clock, the REQa[4:0]# signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, REQb[4:0]# signals carry additional information to define the complete transaction type. REQb[4:2]# is reserved. REQb[1:0]# signals transmit LEN[1:0]# (the data transfer length information). In both clocks, REQ[4:0]# and ADS# are protected by parity RP#.

All receiving agents observe the REQ[4:0]# signals to determine the transaction type and participate in the transaction as necessary, as shown in Table 40.

Table 40. Transaction Types Defined by REQa#/REQb# Signals

	REQa[4:0]#					REQb[4:0]#				
Transaction	**4**	**3**	**2**	**1**	**0**	**4**	**3**	**2**	**1**	**0**
Deferred Reply	0	0	0	0	0	X	X	X	X	X
Rsvd (Ignore)	0	0	0	0	1	X	X	X	X	X
Interrupt Acknowledge	0	1	0	0	0	DSZ#		X	0	0
Special Transactions	0	1	0	0	0	DSZ#		X	0	1
Rsvd (Central agent response)	0	1	0	0	0	DSZ#		X	1	X
Branch Trace Message	0	1	0	0	1	DSZ#		X	0	0
Rsvd (Central agent response)	0	1	0	0	1	DSZ#		X	0	1
Rsvd (Central agent response)	0	1	0	0	1	DSZ#		X	1	X
I/O Read	1	0	0	0	0	DSZ#		X	LEN#	
I/O Write	1	0	0	0	1	DSZ#		X	LEN#	
Rsvd (Ignore)	1	1	0	0	X	DSZ#		X	X	X
Memory Read & Invalidate	ASZ#		0	1	0	DSZ#		X	LEN#	
Rsvd (Memory Write)	ASZ#		0	1	1	DSZ#		X	LEN#	
Memory Code Read	ASZ#		1	D/C#=0	0	DSZ#		X	LEN#	
Memory Data Read	ASZ#		1	D/C#=1	0	DSZ#		X	LEN#	
Memory Write (may not be retried)	ASZ#		1	W/WB#=0	1	DSZ#		X	LEN#	
Memory Write (may not be retried)	ASZ#		1	W/WB#=1	1	DSZ#		X	LEN#	

A.43. RESET# (I)

The RESET# signal is the Execution Control group reset signal. Asserting RESET# resets all Pentium Pro processors to known states and invalidates their L1 and L2 caches without writing back Modified (M state) lines. For a power-on type reset, RESET# must stay active for at least one millisecond after $V_{CC}P$ and CLK have reached their proper DC and AC specifications. On observing active RESET#, all bus agents must deassert their outputs within two clocks.

A number of bus signals are sampled at the active-to-inactive transition of RESET# for the power-on configuration. The configuration options are described in the *Pentium® Pro Processor Family Developer's Manual, Volume 1: Specifications* (Order Number 242690), and in the pertinent signal descriptions in this appendix.

Unless its outputs are tristated during power-on configuration, after active-to-inactive transition of RESET#, the Pentium Pro processor optionally executes its built-in self-test (BIST) and begins program execution at reset-vector 0_000F_FFF0H or 0_FFFF_FFF0H.

A.44. RP# (I/O)

The RP# signal is the Request Parity signal. It is driven by the request initiator in both clocks of the Request Phase. RP# provides parity protection on ADS# and REQ[4:0]#. When a Pentium Pro processor bus agent observes an RP# parity error on any one of the two Request Phase clocks, it must assert AERR# in the Error Phase, provided "AERR# drive" is enabled during the power-on configuration.

A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. This definition allows parity to be high when all covered signals are high.

A.45. RS[2:0]# (I)

The RS[2:0]# signals are the Response Status signals. They are driven by the response agent (the agent responsible for completion of the transaction at the top of the In-order Queue). Assertion of RS[2:0]# to a nonzero value for one clock completes the Response Phase for a transaction. The response encodings are shown in Table 41. Only certain response combinations are valid, based on the snoop result signaled during the transaction's Snoop Phase.

The RS[2:0]# assertion for a transaction is initiated when all of the following conditions are met:

- All bus agents have observed the Snoop Phase completion of the transaction.
- The transaction is at the top of the In-order Queue.
- RS[2:0]# are sampled in the Idle state

The response driven depends on the transaction as described below:

- The response agent returns a hard-failure response for any transaction in which the response agent observes a hard error.
- The response agent returns a Normal with data response for a read transaction with HITM# and DEFER# deasserted in the Snoop Phase, when the addressed agent is ready to return data and samples inactive DBSY#.
- The response agent returns a Normal without data response for a write transaction with HITM# and DEFER# deasserted in the Snoop Phase, when the addressed agent samples TRDY# active and DBSY# inactive, and it is ready to complete the transaction.
- The response agent must return an Implicit write back response in the next clock for a read transaction with HITM# asserted in the Snoop Phase, when the addressed agent samples TRDY# active and DBSY# inactive.
- The addressed agent must return an Implicit write back response in the clock after the following sequence is sampled for a write transaction with HITM# asserted:
  1. TRDY# active and DBSY# inactive
  2. Followed by TRDY# inactive
  3. Followed by TRDY# active and DBSY# inactive
- The defer agent can return a Deferred, Retry, or Split response anytime for a read transaction with HITM# deasserted and DEFER# asserted.
- The defer agent can return Deferred, Retry, or Split response when it samples TRDY# active and DBSY# inactive for a write transaction with HITM# deasserted and DEFER# asserted.

Table 41. Transaction Response Encodings

RS[2:0]	Description	HITM#	DEFER#
000	Idle State	N/A	N/A
001	Retry Response. The transaction is canceled and must be retried by the initiator.	0	1
010	Defer Response. The transaction is suspended. The defer agent will complete it with a defer reply	0	1
011	Reserved	0	1
100	Hard Failure. The transaction received a hard error. Exception handling is required.	X	X
101	Normal without data	0	0
110	Implicit Write Back Response. Snooping agent will transfer the modified cache line on the data bus.	1	X
111	Normal with data	0	0

A.46. RSP# (I)

The RSP# signal is the Response Parity signal. It is driven by the response agent during assertion of RS[2:0]#. RSP# provides parity protection for RS[2:0]#.

A correct parity signal is high if an even number of covered signals are low and low if an odd number of covered signals are low. During Idle state of RS[2:0]# (RS[2:0]#=000), RSP# is also high since it is not driven by any agent guaranteeing correct parity.

Pentium Pro processor bus agents can check RSP# at all times and if a parity error is observed, treat it as a protocol violation error. If the BINIT# driver is enabled during configuration, the agent observing RSP# parity error can assert BINIT#.

A.47. SMI# (I)

System Management Interrupt is asserted asynchronously by system logic. On accepting a System Management Interrupt, the Pentium Pro processor saves the current state and enters SMM mode. It issues an SMI Acknowledge Bus transaction and then begins program execution from the SMM handler.

A.48. SMMEM# (I/O)

The SMMEM# signal is the System Management Mode Memory signal. It is driven on the second clock of the Request Phase on the EXF4#/Ab7# signal. It is asserted by the Pentium Pro processor to indicate that the processor is in System Management Mode and is executing out of SMRAM space.

A.49. SPLCK# (I/O)

The SPLCK# signal is the Split Lock signal. It is driven in the second clock of the Request Phase on the EXF3#/Ab6# signal of the first transaction of a locked operation. It is driven to indicate that the locked operation will consist of four locked transactions. Note that SPLCK# is asserted only for locked operations and only in the first transaction of the locked operation.

A.50. STPCLK# (I)

The STPCLK# signal is the Stop Clock signal. When asserted, the Pentium Pro processor enters a low-power state, the stop-clock state. The processor issues a Stop Clock Acknowledge special transaction, and stops providing internal clock signals to all units except the bus unit and the APIC unit. The processor continues to snoop bus transactions and service interrupts while in stop clock state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock.

STPCLK# is an asynchronous input. In FRC mode, STPCLK# must be synchronous to BCLK.

A.51. TCK (I)

The TCK signal is the System Support group Test Clock signal. TCK provides the clock input for the test bus (also known as the test access port). Make certain that TCK is active before initializing the TAP.

A.52. TDI(I)

The TDI signal is the System Support group test-data-in signal. TDI transfers serial test data into the Pentium Pro processor. TDI provides the serial input needed for JTAG support.

A.53. TDO (O)

The TDO signal is the System Support group test-data-out signal. TDO transfers serial test data out from the Pentium Pro processor. TDO provides the serial output needed for JTAG support.

A.54. TMS (I)

The TMS signal is an additional System Support group JTAG-support signal.

A.55. TRDY (I)

The TRDY# signal is the target Ready signal. It is asserted by the target in the Response Phase to indicate that the target is ready to receive write or implicit write back data transfer. This enables the request initiator or the snooping agent to begin the appropriate data transfer. There will be no data transfer after a TRDY# assertion if a write has zero length indicated in the Request Phase. The data transfer is optional if an implicit write back occurs for a transaction which writes a full cache line (the Pentium Pro processor will perform the implicit write back).

TRDY# for a write transaction is driven by the addressed agent when:

- The transaction has a write or write back data transfer.
- It has a free buffer available to receive the write data.
- A minimum of 3 clocks after ADS# for the transaction.
- The transaction reaches the top-of-the-In-order Queue.
- A minimum of 1 clock after RS[2:0]# active assertion for transaction “n-1” (after the transaction reaches the top of the In-order Queue).

TRDY# for an implicit write back is driven by the addressed agent when:

- The transaction has an implicit write back data transfer indicated in the Snoop Result Phase.
- It has a free cache line buffer to receive the cache line write back.
- If the transaction also has a request initiated transfer, that the request initiated TRDY# was asserted and then deasserted (TRDY# must be deasserted for at least one clock between the TRDY# for the write and the TRDY# for the implicit write back).
- A minimum of 1 clock after RS[2:0]# active assertion for transaction “n-1” (after the transaction reaches the top of the In-order Queue).

TRDY# for a write or an implicit write back may be deasserted when:

- Inactive DBSY# and active TRDY# are observed.
- DBSY# is observed inactive on the clock TRDY# is asserted.
- A minimum of three clocks can be guaranteed between two active-to-inactive transitions of TRDY#.
- The response is driven on RS[2:0]#.
- Inactive DBSY# and active TRDY# are observed for a write, and TRDY# is required for an implicit write back.

A.56. TRST (I)

The TRST# signal resets the JTAG logic.

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