# CE6210
# DVB-C Cable Demodulator

Data Sheet

June 2006

## Features

- DVB-C EN300429 and ITU-T J.83 annex A/C compliant QAM demodulator
- Conventional IF and low IF input supported
- QAM constellations 16, 32, 64, 128 and 256
- Symbol rates up to 9 MBaud
- Blind acquisition of all symbol rates
- Blind acquisition of QAM constellations
- Single IF filter bandwidth for all symbol rates
- Signal level, BER and SNR indicators
- Programmable IF/RF AGC take-over point
- Power down mode under software control
- Parallel and serial MPEG outputs
- External 4 or 27 MHz clock or single low-cost 10 MHz crystal
- Small package size LQFP64 7x7 mm
- Power consumption <300 mW at 6.9 MBaud
- 5 V tolerant 2-wire bus control interface
- 5 V tolerant GPIO port and AGC outputs

**Ordering Information**

DJCE6210 882133 64-pin LQFP Trays
WJCE6210 882214 64-pin LQFP* Trays

*Pb free

**-40°C to +85°C**

- RF level detect facility via a separate ADC
- Very low driver software overhead due to on-chip state-machine control.
- General purpose programmable timer

## Applications

- Set-top boxes
- Digital cable ready TV applications
- Cable modems
- SMATV/MATV receivers

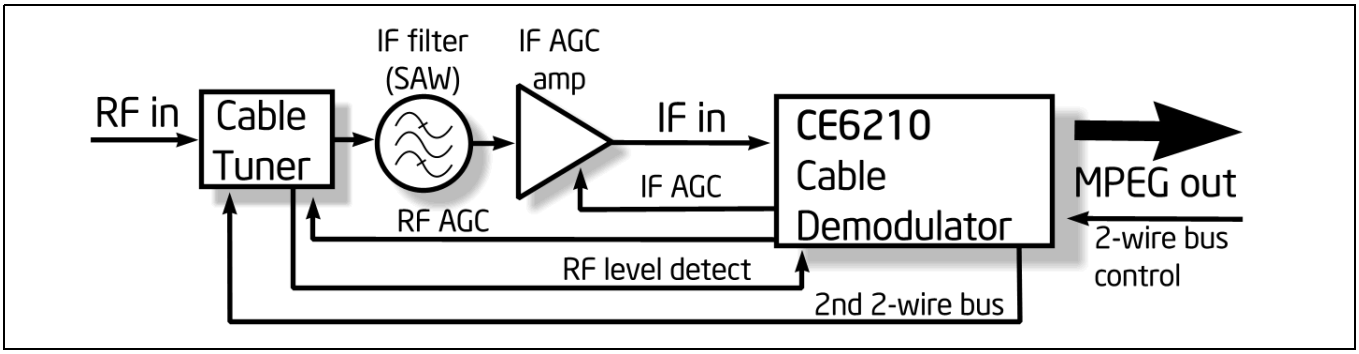


**Figure 1 - System Diagram**



Intel Corporation D55750-001

## Description

The CE6210 is a DVB-C and ITU-T annex A/C QAM demodulator. This low power cable demodulator includes standard Intel features of auto signal acquisition, fast blind-scan capability, software/ hardware power down, RF level, BER and SNR detection. The CE6210 represents the latest in QAM demodulation for DVB cable. Together with a cable tuner, a full digital cable receiver front-end can be realized. Either conventional intermediate frequencies such as 36 or 44 MHz or low intermediate frequencies can be used - see application below. The CE6210 requires only a single channel filter bandwidth of 8 MHz nominal for full DVB and ITU-T annex A/C performance. The low power consumption, small package form factor and integrated software/hardware power-down modes help reduce the system BoM (bill of materials) in cost sensitive applications. The device is packaged in a 7 x 7 mm 64-pin LQFP.

## Functional Description

The CE6210 accepts an analog signal from the tuner, either at low Intermediate Frequency (IF) or conventional IF up to 50 MHz, and delivers an MPEG2 compliant transport stream. It contains a single 10-bit analog-to-Digital Converter (ADC), a digital QAM demodulator and Forward Error Correcting (FEC) decoder. The QAM demodulator supports QAM constellations 16 to 256. Both the QAM demodulator and the FEC are DVB and ITU-T J.83 annex A/C compliant.

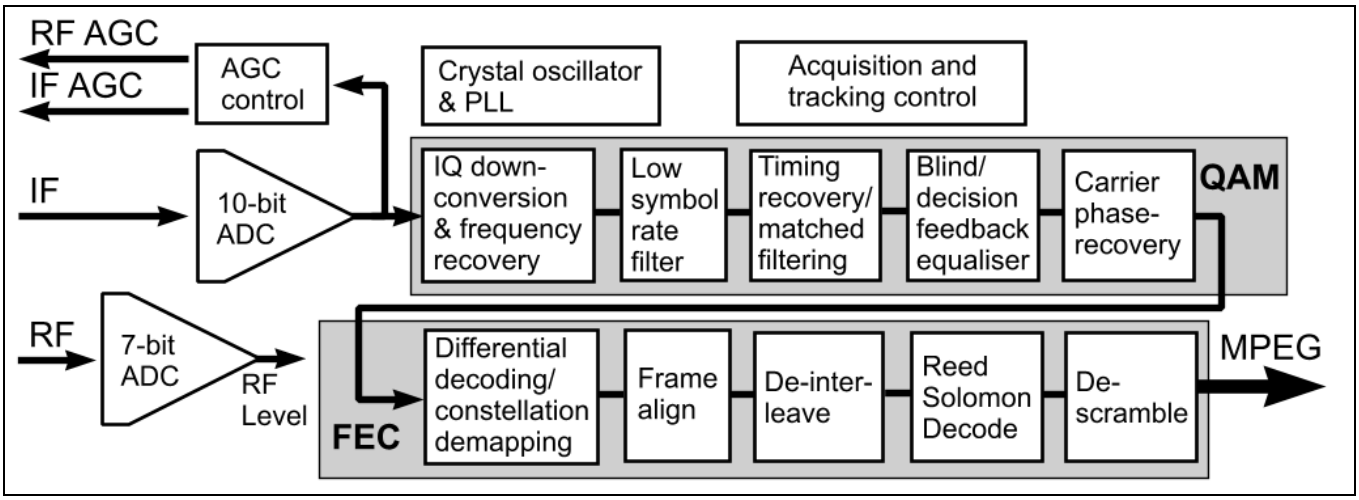


**Figure 2 - CE6210 Functional Diagram**

The ADC uses a fixed sample rate greater than four times the maximum symbol rate. Hence for 1 to 9 MBaud applications, the signal has to be sampled at a frequency around 36 MHz. The spectrum of the analog signal being sampled may be located at near-zero IF (e.g. centered at 9 MHz) or it may be located at a conventional IF such as 36.2 MHz or 43.5 MHz.

First consider the case of IF sampling a 1 to 7 MBaud QAM signal centered at 36.2 MHz intermediate frequency. The sampling frequency chosen for this application is 28.9 MHz. This sampling process will fold the 36.2 MHz IF spectrum to one centered at 7.3 MHz.

Second consider the case of IF sampling a 1 to 6 MBaud QAM signal centered at 43.5 MHz IF. The sampling frequency chosen for this application is 25 MHz. This sampling process will result in a QAM spectrum centered at 6.5 MHz.

In the second case the sampling process results in spectral inversion. Even in first case the IF spectrum may be spectrally inverted. However, spectral inversion is not an issue with CE6210 since it automatically detects and corrects for this in the digital domain.

The digital signal is first mixed down to baseband. However, as a result of tuning errors this signal will not be centered at zero frequency. CE6210 has an automatic frequency control (AFC) loop that can track out tuning errors and hence in the tracking phase this signal will be centered at zero frequency. The AFC loop can typically compensate for +/-350 kHz frequency offsets. Larger offsets can be corrected by programming on-chip registers.

The baseband signal is filtered to reduce the effect of adjacent channels. Additional on-chip digital filtering is provided for low symbol rate applications. For example, it is possible to demodulate and decode a 1 MBaud QAM signal using only one external 8 MHz SAW filter.

CE6210 has complete blind acquisition capability. It can automatically search and lock on to any QAM constellation in the set 16, 32, 64, 128 and 256. It can compensate for spectral inversion. It can also automatically acquire a symbol rate in the range 1 to 7 MBaud correcting for any tuning errors and adapting the filter bandwidths to signal bandwidth. All these functions are implemented using a sophisticated built-in control state machine with no software intervention.

The symbol-spaced equalizer in the CE6210 is designed to acquire the QAM signal in blind mode, i.e., with no training sequence, and then to track the signal in the decision feedback mode. The equalizer has a feed-forward segment and a feedback segments. The tap partitioning between feed-forward and feedback is fully programmable.

The symbol timing and phase recovery functions with the CE6210 are fully digital. The timing recovery phase locked loop has a built in timing sweep to enable the CE6210 to lock on to unknown symbol rates. The phase recovery loop has been optimised to overcome phase noise degradation caused by typical tuners.

The CE6210 QAM demodulator has built in control mechanisms to overcome signal degradation due to impulse noise in cable systems. The most significant bits of the demodulated I/Q symbols are differentially decoded to remove multiples of 90 degree phase ambiguity in demodulation. The QAM symbols are then demapped into a bit stream, using the constellation definitions provided by DVB and ITU-T. The number of bits per symbol is eight for QAM-256, seven for QAM-128, six for QAM-64, five for QAM-32 and four for QAM-16.

The bitstream is aligned into bytes and then into 204-byte frames by the Frame Alignment Unit. These frames are deinterleaved as defined by DVB to improve the resilience of the system to error bursts. The (204,188) Reed-Solomon decoder, which follows the deinterleaver, can correct up to eight byte-errors per frame. This also generates an uncorrectable error flag for blocks with more than eight byte-errors. In addition, the CE6210 Reed-Solomon decoder keeps a count of the number of uncorrectable blocks and the number of bit errors corrected. The former will give an indication on the quality of the MPEG output and the latter provides the Bit Error Rate in QAM demodulation.

The decoder packets are then descrambled to reverse the energy dispersal function introduced by the transmitter. The output of the device is a stream of regularly spaced MPEG packets. The MPEG byte clock frequency is automatically adapted to be the minimum needed for a given symbol rate and QAM constellation. Alternatively the MPEG bytes can be clocked out using an externally provided byte clock. There is also an option for bit-serial output.

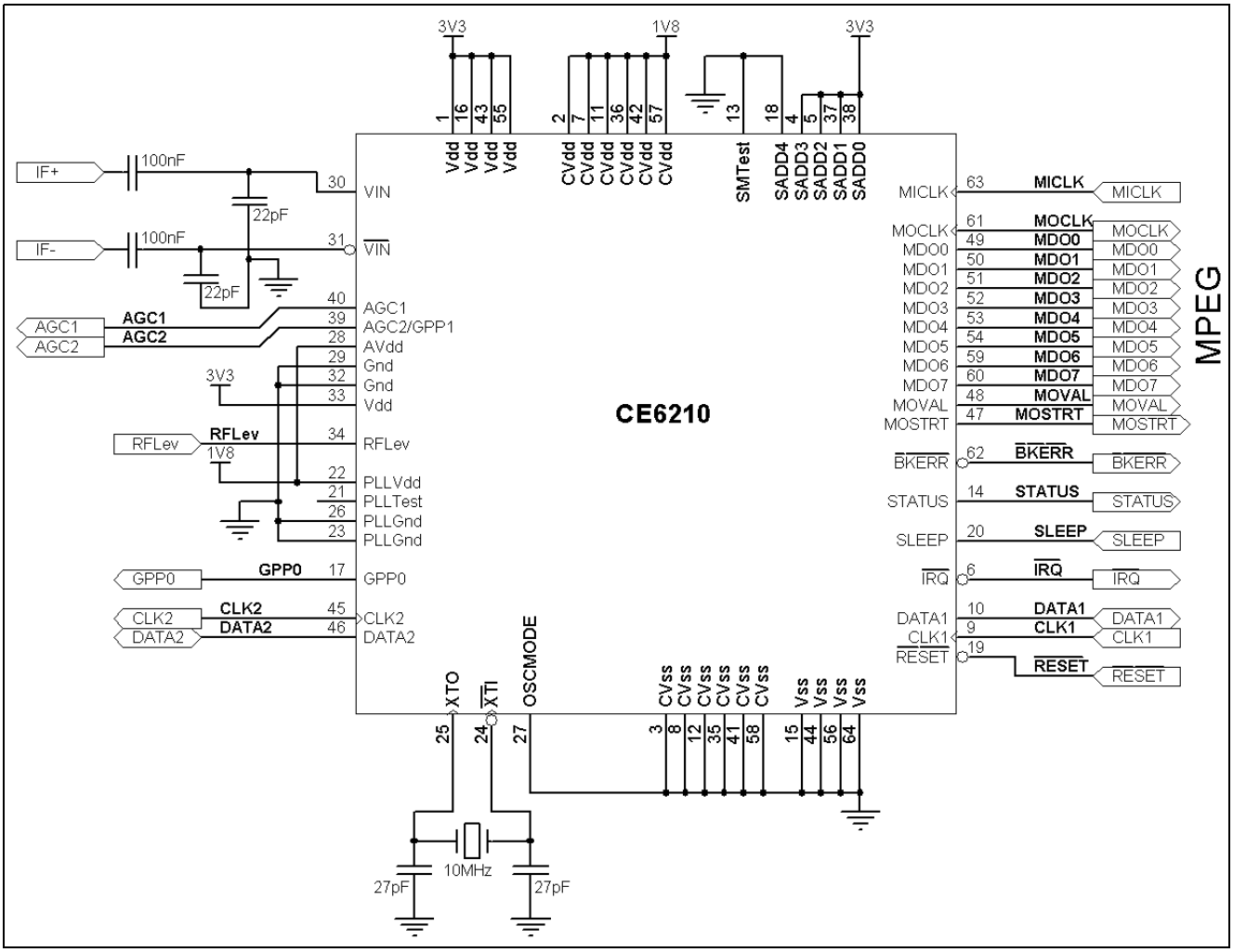


**Figure 3 - Typical CE6210 Application**

# 1.0 Pin & Package Details

## 1.1 Pin Outline

Figure 4 below shows the pin functions of the CE6210.

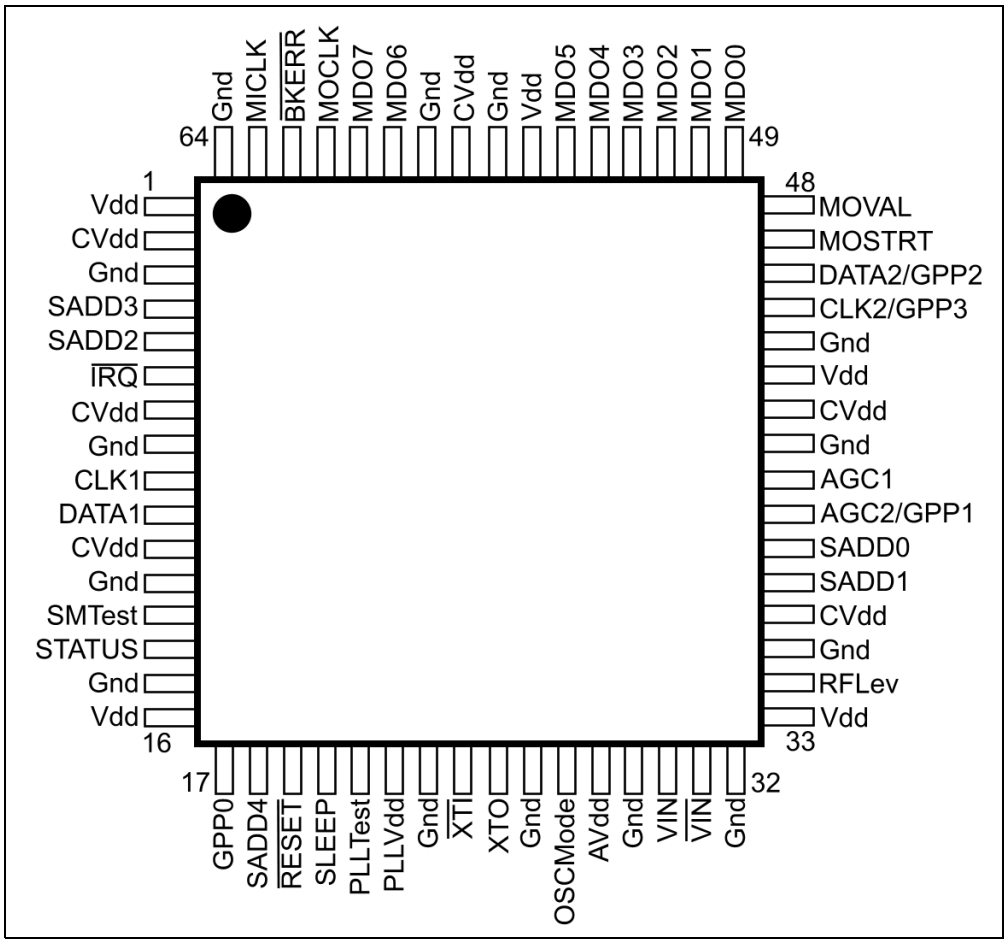


**Figure 4 - Pin Outline**

## 1.2 Pin Allocation

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | Vdd | 17 | GPP0 | 33 | Vdd | 49 | MDO0 |
| 2 | CVdd | 18 | SADD4 | 34 | RFLev | 50 | MDO1 |
| 3 | Gnd | 19 | $\overline{\text{RESET}}$ | 35 | Gnd | 51 | MDO2 |
| 4 | SADD3 | 20 | SLEEP | 36 | CVdd | 52 | MDO3 |
| 5 | SADD2 | 21 | PLLTest | 37 | SADD1 | 53 | MDO4 |
| 6 | $\overline{\text{IRQ}}$ | 22 | PLLVdd | 38 | SADD0 | 54 | MDO5 |
| 7 | CVdd | 23 | Gnd | 39 | AGC2/GPP1 | 55 | Vdd |

**Table 1 - Pin Names - numeric**

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 8 | Gnd | 24 | XTI | 40 | AGC1 | 56 | Gnd |
| 9 | CLK1 | 25 | XTO | 41 | Gnd | 57 | CVdd |
| 10 | DATA1 | 26 | Gnd | 42 | CVdd | 58 | Gnd |
| 11 | CVdd | 27 | OSCMode | 43 | Vdd | 59 | MDO6 |
| 12 | Gnd | 28 | AVdd | 44 | Gnd | 60 | MDO7 |
| 13 | SMTest | 29 | Gnd | 45 | CLK2 | 61 | MOCLK |
| 14 | STATUS | 30 | VIN | 46 | DATA2 | 62 | BKERR |
| 15 | Gnd | 31 | VIN | 47 | MOSTRT | 63 | MICLK |
| 16 | Vdd | 32 | Gnd | 48 | MOVAL | 64 | Gnd |

**Table 1 - Pin Names - numeric (continued)**

| Function | Pin | Function | Pin | Function | Pin | Function | Pin |
|---|---|---|---|---|---|---|---|
| AGC1 | 40 | Gnd | 12 | MDO2 | 51 | SADD1 | 37 |
| AGC2/GPP1 | 39 | Gnd | 15 | MDO3 | 52 | SADD2 | 5 |
| AVdd | 28 | Gnd | 23 | MDO4 | 53 | SADD3 | 4 |
| $\overline{\text{BKERR}}$ | 62 | Gnd | 26 | MDO5 | 54 | SADD4 | 18 |
| CLK1 | 9 | Gnd | 29 | MDO6 | 59 | SLEEP | 20 |
| CLK2 | 45 | Gnd | 32 | MDO7 | 60 | SMTest | 13 |
| CVdd | 2 | Gnd | 35 | MICLK | 63 | STATUS | 14 |
| CVdd | 7 | Gnd | 41 | MOCLK | 61 | Vdd | 1 |
| CVdd | 11 | Gnd | 44 | MOSTRT | 47 | Vdd | 16 |
| CVdd | 36 | Gnd | 56 | MOVAL | 48 | Vdd | 33 |
| CVdd | 42 | Gnd | 58 | OSCMode | 27 | Vdd | 43 |
| CVdd | 57 | Gnd | 64 | PLLTest | 21 | Vdd | 55 |
| DATA1 | 10 | GPP0 | 17 | PLLVdd | 22 | VIN | 30 |
| DATA2 | 46 | $\overline{\text{IRQ}}$ | 6 | $\overline{\text{RESET}}$ | 19 | $\overline{\text{VIN}}$ | 31 |
| Gnd | 3 | MDO0 | 49 | RFLev | 34 | $\overline{\text{XTI}}$ | 24 |
| Gnd | 8 | MDO1 | 50 | SADD0 | 38 | XTO | 25 |

**Table 2 - Pin Names - alphabetical order**

## 1.3 Pin Description

**Pin Description Table**

| Pin No | Name | Pin Description | I/O | Type | V [1] | mA |
|---|---|---|---|---|---|---|
| **MPEG pins** | | | | | | |
| 47 | MOSTRT | MPEG packet start | O | CMOS Tristate | 3.3 | 1 |
| 48 | MOVAL | MPEG data valid | O | | 3.3 | 1 |
| 49-54, 59-60 | MDO(0:5) MDO(6:7) | MPEG data outputs | O | | 3.3 | 1 |
| 61 | MOCLK | MPEG output clock | O | | 3.3 | 1 |
| 62 | $\overline{\text{BKERR}}$ | Block error output | O | | 3.3 | 1 |
| 63 | MICLK | MPEG input clock | I | CMOS | 3.3 | |
| 14 | STATUS | Status output | O | | 3.3 | 1 |
| 6 | $\overline{\text{IRQ}}$ | Interrupt output | O | Open drain | 5 | 6 |
| **Control pins** | | | | | | |
| 9 | CLK1 | Serial clock | I | CMOS | 5 | |
| 10 | DATA1 | Serial data | I/O | Open drain | 5 | 6 |
| 24 | $\overline{\text{XTI}}$ | Low phase noise crystal oscillator | I | CMOS | 1.8 | |
| 25 | XTO | | I/O | | 1.8 | |
| 20 | SLEEP | Device power down | I | | 5 | |
| 4, 5,18,37,38 | SADD(4:0) | Serial address set | I | | 3.3 | |
| 13 | SMTest | Production test (only set low) | I | | 3.3 | |
| 45 | CLK2 | Serial clock tuner | I/O | Open drain | 5 | 6 |
| 46 | DATA2 | Serial data tuner | I/O | | 5 | 6 |
| 40 | AGC1 | Primary AGC | O | | 5 | 6 |
| 39 | AGC2/GPP1 | Secondary AGC or general I/O | I/O | | 5 | 6 |
| 17 | GPP0 | General purpose I/O | I/O | | 5 | 6 |
| 19 | RESET | Device reset - active low | I | CMOS | 5 | |

**Pin Description Table (continued)**

| Pin No | Name | Pin Description | I/O | Type | V [1] | mA |
|---|---|---|---|---|---|---|
| 27 | OSCMode | Crystal oscillator mode:<br>Low = crystal oscillator<br>High = external clock | I | CMOS | 3.3 | |
| 21 | PLLTest | PLL test - do not connect | O | (tristated) | | |
| **Analog inputs** | | | | | | |
| 30 | VIN | ADC positive input | I | Analog input nominally ±400 mV AC coupled | | |
| 31 | VIN | ADC negative input | I | | | |
| 34 | RFLev | RF level ADC input | I | Analog input nominally 3.3 V for max. level | 3.3 | |
| **Supply pins** | | | | | | |
| 28 | AVdd | ADC analog supply [2] | S | | 1.8 | |
| 2, 7, 11, 36, 42, 57 | CVdd | Core logic power | S | | | |
| 22 | PLLVdd | PLL supply [2] | S | | | |
| 1, 16, 33, 43, 55 | Vdd | I/O ring power<br>(#33 is to ADC only [2]) | S | | 3.3 | |
| 3, 8, 12, 15, 23, 26, 29, 32, 35, 41, 44, 56, 58, 64 | Gnd | Core, analog and I/O grounds [3] | S | | 0 | |

1. This column is the nominal maximum for a given pin. Pins listed as 5 V can tolerate voltages up to 5 V (inputs have threshold voltages related to the 3V3 supply).
2. Pins #22, #28 and #33 should have separate supply lines from the digital supplies of the same voltage.
3. Decoupling capacitors should be used from every Gnd pin to its adjacent supply pin, with the capacitor as close as possible to the pins. Pin #26 is provided to allow the oscillator to be ringed.

# 2.0 Interfaces

## 2.1 2-wire Bus

### 2.1.1 Host

The primary 2-wire bus serial interface uses pins:

- DATA1 (pin #10) serial data, the most significant bit is sent first.
- CLK1 (pin #9) serial clock.

The 2-wire bus address is determined by applying Vdd or Gnd to the SADD[4:0] pins.

In CNIM evaluation applications, the 2-wire bus address is 0001 111 R/$\overline{W}$ with the pins connected as follows:

| ADDR[7] | ADDR[6] | ADDR[5] | ADDR[4] | ADDR[3] | ADDR[2] | ADDR[1] |
|---|---|---|---|---|---|---|
| Not programmable | | SADD[4] | SADD[3] | SADD[2] | SADD[1] | SADD[0] |
| Gnd | Gnd | Gnd | Vdd | Vdd | Vdd | Vdd |

When the CE6210 is powered up, the $\overline{\text{RESET}}$ pin 9 should be held low for at least 50 ms after Vdd has reached normal operation levels. As the $\overline{\text{RESET}}$ pin goes high, the logic levels on SADD[4:0] are latched as the 2-wire bus address. ADDR[0] is the R/$\overline{W}$ bit.

The circuit works as a slave transmitter with the address lsb set high or as a slave receiver with the lsb set low. In receive mode, the first data byte is written to the RADD virtual register, which forms the register address. The RADD register takes an 8-bit value that determines which of 256 possible register addresses is written to by the following byte. Not all addresses are valid and many are reserved registers that must not be changed from their default values. Multiple byte reads or writes will auto-increment the value in RADD, but care should be taken not to access the reserved registers accidentally.

Following a valid chip address, the 2-wire bus STOP command resets the RADD register to 00. If the chip address is not recognized, the CE6210 will ignore all activity until a valid chip address is received. The 2-wire bus START command does NOT reset the RADD register to 00. This allows a combined 2-wire bus message, to point to a particular read register with a write command, followed immediately with a read data command. If required, this could next be followed with a write command to continue from the latest address. RADD would not be sent in this case. Finally, a STOP command should be sent to free the bus.

When the 2-wire bus is addressed (after a recognized STOP command) with the read bit set, the first byte read out is the contents of register 00.

### 2.1.2 Tuner

The CE6210 has two GPP (general purpose port) pins which are normally configured to provide a secondary 2-wire bus, allowing the main serial bus to be connected through to the tuner only when it is necessary to communicate with the tuner.

This reduces the electrical noise seen by the tuner and improves the performance. The allocation of the pins is: pin 45 = CLK2 or GPP3; pin 46 = DATA2 or GPP2.

Pass-through mode is selected by setting register Tuner_Ctl (0x56) [b0] = ‘1’, otherwise, if this bit is ‘0’, then there is no connection between the two serial buses. In this same register, bit [b2] must also be set to a ‘1’ to enable the pins for serial use rather than as general purpose port pins. See also register GPP_Ctl address 0x55 for details of using these pins as GPPs.

### 2.1.3 Examples of 2-wire Bus Messages:

| | | | | |
|---|---|---|---|---|
| KEY: | S | Start condition | W | Write (= 0) |
| | P | Stop condition | R | Read (= 1) |
| | A | Acknowledge | NA | NOT Acknowledge |
| | *Italics* | CE6210 output | RADD | Register Address |

Write operation - as a slave receiver:

| S | DEVICE ADDRESS | W | ***A*** | RADD (n) | ***A*** | DATA (reg n) | ***A*** | DATA (reg n+1) | ***A*** | P |
|---|---|---|---|---|---|---|---|---|---|---|

Read operation - CE6210 as a slave transmitter:

| S | DEVICE ADDRESS | R | ***A*** | ***DATA (reg 0)*** | A | ***DATA (reg 1)*** | A | ***DATA (reg 2)*** | NA | P |
|---|---|---|---|---|---|---|---|---|---|---|

Write/read operation with repeated start - CE6210 as a slave transmitter:

| S | DEVICE ADDRESS | W | ***A*** | RADD (n) | ***A*** | S | DEVICE ADDRESS | R | ***A*** | ***DATA (reg n)*** | A | ***DATA (reg n+1)*** | NA | P |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

### 2.1.4 Primary 2-wire Bus Timing

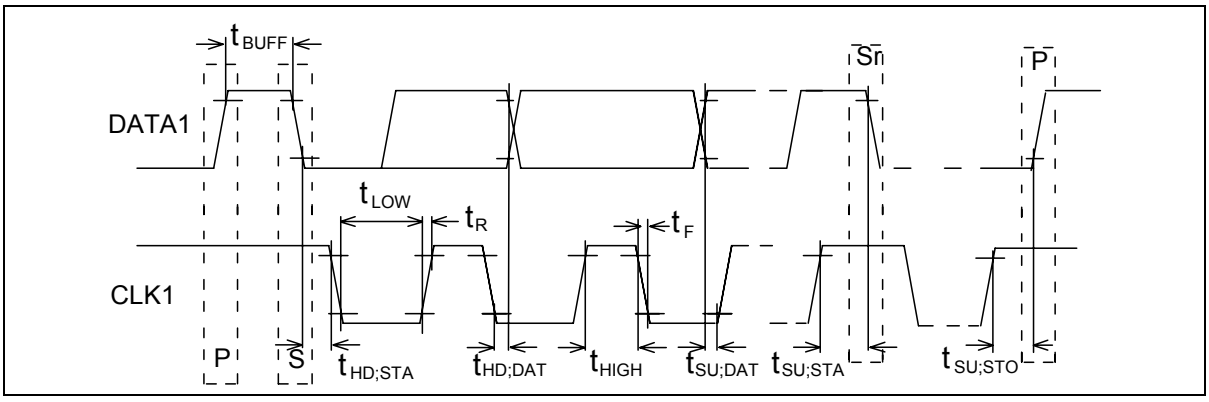


**Figure 5 - Primary 2-wire Bus Timing**

Where: S = Start

Sr = Restart, i.e., start without stopping first

P = Stop

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| CLK clock frequency (Primary) | $f_{CLK}$ | 0 | 400 [1] | kHz |
| Bus free time between a STOP and START condition. | $t_{BUFF}$ | 200 | | ns |
| Hold time (repeated) START condition. | $t_{HD;STA}$ | 200 | | ns |
| LOW period of CLK clock. | $t_{LOW}$ | 1300 | | ns |
| HIGH period of CLK clock. | $t_{HIGH}$ | 600 | | ns |
| Set-up time for a repeated START condition. | $t_{SU;STA}$ | 200 | | ns |
| Data hold time (when input). | $t_{HD;DAT}$ | 100 | | ns |
| Data set-up time | $t_{SU;DAT}$ | 100 | | ns |
| Rise time of both CLK and DATA signals. | $t_R$ | | note [2] | ns |
| Fall time of both CLK and DATA signals, (100pF to ground). | $t_F$ | 20 | | ns |
| Set-up time for a STOP condition. | $t_{SU;STO}$ | 200 | | ns |

**Table 3 - Timing of 2-Wire Bus**

1. If operating with an external 4 MHz clock, the serial clock frequency is reduced to 100 kHz maximum.
2. The rise time depends on the external bus pull up resistor. Loading prevents full speed operation.

## 2.2 MPEG

### 2.2.1 Data Output Header Format

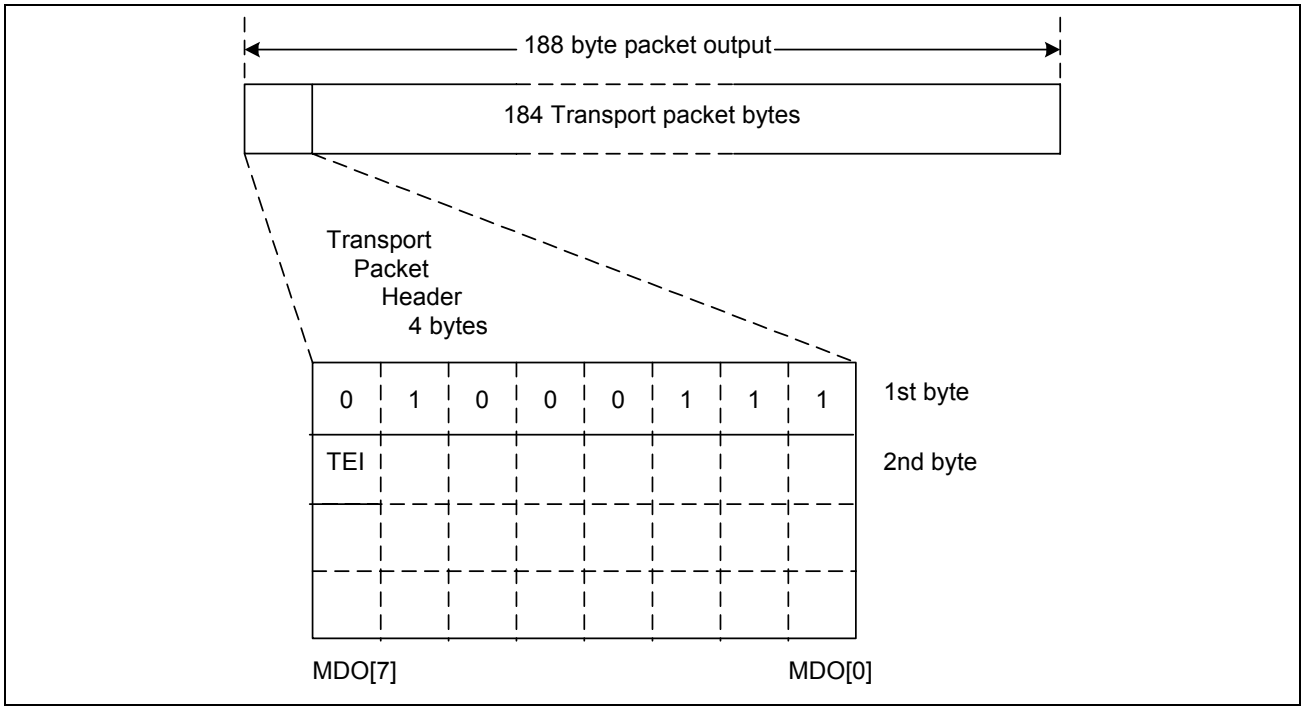


**Figure 6 - DVB Transport Packet Header Byte**

After decoding the 188-byte MPEG packet, it is output on the MDO pins in 188 consecutive clock cycles.

Additionally when the TEI_En bit in the MCLK_CTL register (0x77) is set high (default), the TEI bit of any uncorrectable packet will automatically be set to '1'. If TEI_En bit is low then TEI bit will not be changed (but note that if this bit is already 1, for example, due to a channel error which has not been corrected, it will remain high at output).

### 2.2.2 MPEG Data Output Signals

The $\overline{\text{MPEGEN}}$ bit in the CONFIG register must be set low to enable the MPEG data pins as outputs. The maximum movement in the packet synchronization byte position is limited to ±1 output clock period. MOCLK will be a continuously running clock once symbol lock has been achieved, and is derived from the symbol clock. MOCLK is shown in Figure 7 with MOCLKINV = '1', the default state, see register 0x50.

All output data and signals (MDO[7:0], MOSTRT, MOVAL & $\overline{\text{BKERR}}$) change on the negative edge of MOCLK (MOCLKINV = 1) to present stable data and signals on the positive edge of the clock.

A complete packet is output on MDO[7:0] on 188 consecutive clocks and the MDO[7:0] pins will remain low during the inter-packet gaps. MOSTRT goes high for the first byte clock of a packet. MOVAL goes high on the first byte of a packet and remains high until the last byte has been clocked out. $\overline{\text{BKERR}}$ goes low on the first byte of a packet where uncorrectable bytes are detected and will remain low until the last byte has been clocked out.

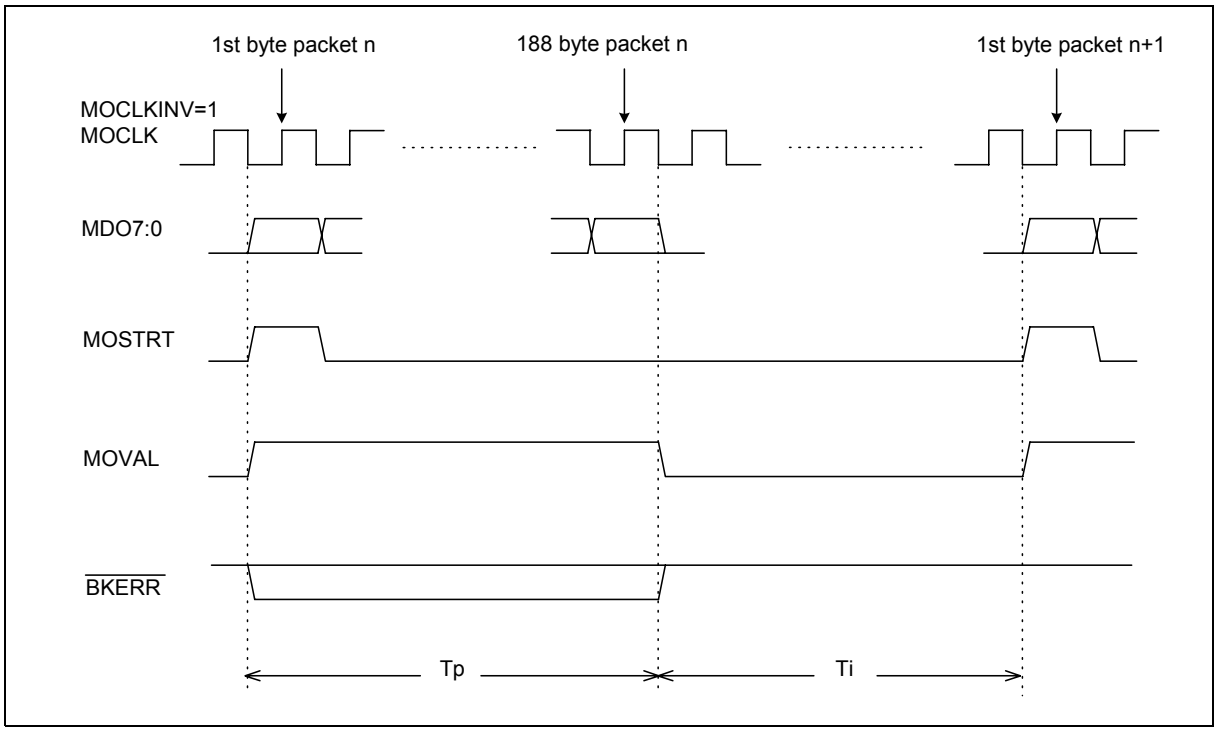


**Figure 7 - MPEG Output Data Waveforms**

### 2.2.3 MPEG Output Timing

Maximum delay conditions: Vdd = 3.0 V, CVdd = 1.62 V, Tamb = 85$^{o}$C, Output load = 10 pF.

Minimum delay conditions: Vdd = 3.6 V, CVdd = 1.98 V, Tamb = -40$^{o}$C, Output load = 10 pF.

MOCLK frequency = 45.06 MHz.

### 2.2.4 MOCLKINV = 1

| Parameter | Delay Conditions | | Units |
|---|---|---|---|
| | Maximum | Minimum | |
| Data output delay $t_D$ | 3.0 | 1.0 | ns |
| Setup Time $t_{SU}$ | 7.0 | 10.0 | |
| Hold Time $t_H$ | 7.0 | 10.0 | |

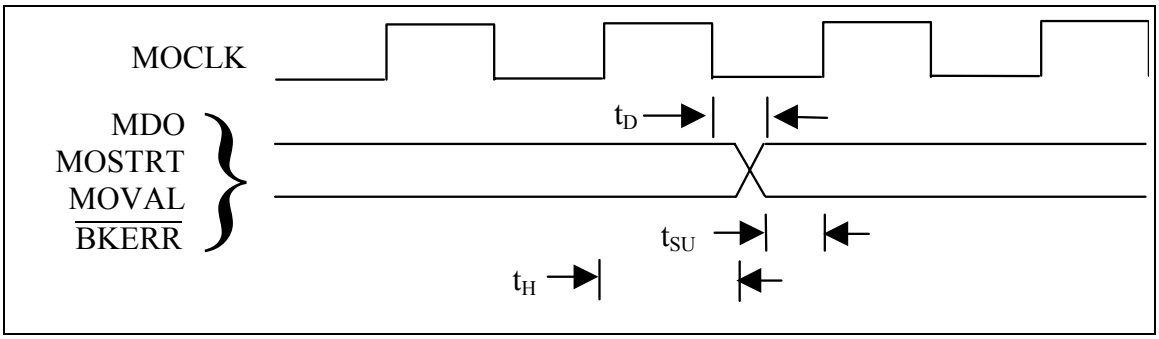


**Figure 8 - MPEG Timing - MOCLKINV = 1**

### 2.2.5 MOCLKINV = 0

MDOSWAP = 0

| Parameter | Delay Conditions | | Units |
|---|---|---|---|
| | Maximum | Minimum | |
| Data output delay $t_D$ | 3.0 | 1.0 | ns |
| Setup Time $t_{SU}$ | 18.0 | 20.0 | |
| Hold Time $t_H$ | 1.0 | 0.2 | |

The hold time is better when MOCLKINV = 1, therefore this should be used if possible.

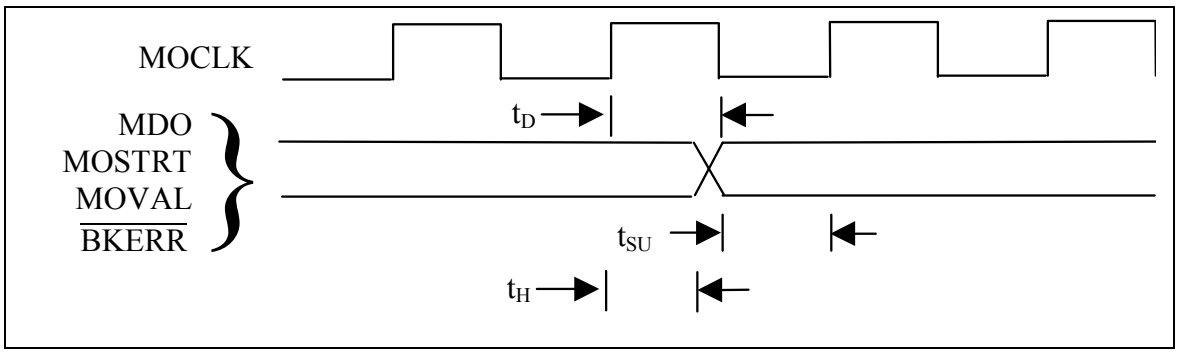


**Figure 9 - MPEG Timing - MOCLKINV = 0**

# 3.0 Electrical Characteristics

## 3.1 Recommended Operating Condition

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Core power supply voltage | CVdd | 1.71 | 1.8 | 1.89 | V |
| Periphery power supply voltage | Vdd | 3.13 | 3.3 | 3.47 | V |
| Input clock frequency (note [1]) | Fxt1 | 3.99 | | 27.01 | MHz |
| Crystal oscillator frequency | Fxt2 | 9.99 | | 16.01 | MHz |
| CLK1 clock frequency [2] (with 10 MHz or above) | Fclk1 | | | 400 | kHz |
| Ambient operating temperature | | -40 | | 85 | °C |

1. When not using a crystal, XTI may be driven from an external source over the frequency range shown.
2. The maximum serial clock speed on the primary 2-wire bus is related to the input clock frequency and is limited to 100 kHz with a 4.0 MHz clock.

## 3.2 Absolute Maximum Ratings

**Maximum Operating Conditions**

| Parameter | Symbol | Min. | Max | Unit |
|---|---|---|---|---|
| Power supply | Vdd | -0.3 | 4.5 | V |
| | CVdd | -0.3 | 2.3 | |
| Voltage on input pins (5 V rated) | Vi | -0.3 | 5.5 | V |
| Voltage on input pins (3.3 V rated) | Vi | -0.3 | 6.5 | V |
| Voltage on input pins (1.8 V rated, e.g., $\overline{XTI}$) | Vi | -0.3 | CVdd + 0.3 | V |
| Voltage on output pins (5 V rated) | Vo | -0.3 | 5.5 | V |
| Voltage on output pins (3.3 V rated) | Vo | -0.3 | Vdd + 0.3 | V |
| Voltage on output pins (1.8 V rated, e.g., XTO) | Vo | -0.3 | CVdd + 0.3 | V |
| Storage temperature | Tstg | -55 | 150 | °C |
| Operating ambient temperature | Top | -40 | 85 | °C |
| Junction temperature | Tj | | 125 | °C |
| ESD protection (human body model) | | 4 | | kV |

Note 1: Stresses exceeding these listed under 'Absolute Ratings' may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

### 3.3 Crystal Specification

Parallel resonant fundamental frequency (preferred) 9.99 to 16.01 MHz.

Tolerance over operating temperature range ±25 ppm.

Tolerance overall ±50 ppm.

Nominal load capacitance 30 pF.

Equivalent series resistance <50 Ω

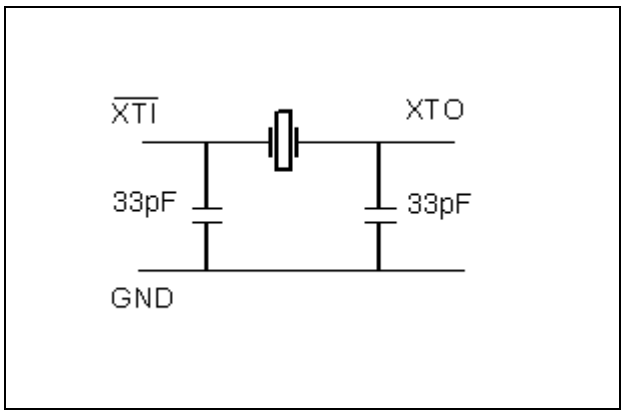


**Figure 10 - Crystal Oscillator Circuit**

#### 3.3.1 Selection of External Components

The capacitor values used must ensure correct operation of the Pierce oscillator such that the total loop gain is greater than unity. Correct selection of the two capacitors is very important and the following method is recommended to obtain values for C1 and C2.

#### 3.3.1.1 Loop Gain Equation

Although oscillation may still occur if the loop gain is just above 1, a loop gain of between 5 and 25 is optimum to ensure that oscillations will occur across all variations in temperature, process and supply voltage, and that the circuit will exhibit good start-up characteristics.

$$A = \frac{C_{out} \cdot g_m}{C_{in}} \left[ \frac{C_{out} + C_{in}}{R_f . C_{in}} + \frac{1}{Z_{in}} + \frac{1}{Z_o} \right]^{-1} \quad \textbf{- Equation 1}$$

$$Z_{in} = \frac{1}{(2.\pi.f.C_{out})^2 . ESR} \quad \textbf{- Equation 2}$$

#### 3.3.1.2 List of Equation Parameters

**A** total loop gain (between 5 and 25)

**Cin** C1 + Cpar

**Cout** C2 + Cpar

**Cpar** parasitic capacitance associated with each oscillator pin ($\overline{XTI}$ and XTO). It consists of track capacitances, package capacitance and cell input capacitance. Normally Cpar ≈ 4 pF.

**Zo** 9.143 kΩ - output impedance of amplifier at 1.8 V operation - typical

**gm** 8.736mA/V - transconductance of amplifier at 1.8 V operation -typical

**Rf** 2.3MΩ - internal feedback resistor

**ESR** maximum equivalent series resistance of crystal - given by crystal manufacturer (Ω)

**f** fundamental frequency of crystal (Hz)

#### 3.3.1.3 Calculating Crystal Power Dissipation

To calculate the power dissipated in a crystal the following equation can be used:

$$P_c = \frac{V_{pp}^2}{8.Z_{in}} \qquad \textbf{- Equation 3}$$

**Pc** = power dissipated in crystal at resonant frequency (W)

**Vpp** = maximum peak to peak output swing of amplifier is 1.8 V for all CVdd

**Zin** = crystal network impedance (see Equation 2)

#### 3.3.1.4 Capacitor Values

Using the loop gain limits ($5 \leq A \leq 25$), the maximum and minimum values for C1 and C2 can be calculated with Equation 4 below.

$$C_{in} = C_{out} = \sqrt{\left[\frac{g_m}{A} - \frac{2}{R_f} - \frac{1}{Z_o}\right].\frac{1}{(2.\pi.f)^2.ESR}} \quad \text{when: } C_1 = C_2 = C_{out} - C_{par} \qquad \textbf{- Equation 4}$$

Note: Equation 4 was derived from Equation 1 and Equation 2 using the premise that C1 = C2.

Within these limits, any value for C1 and C2 can now be selected. Normally C1 and C2 are chosen such that the resulting crystal load capacitance $C_L$ (see Equation 5) is close to the crystal manufacturers recommended $C_L$ (standard values for $C_L$ are 15 pF, 20 pF and 30 pF). The crystal will then operate very near its specified frequency.

$$C_L = \frac{C_{out} \cdot C_{in}}{C_{out} + C_{in}} + C_{par12} \qquad \textbf{- Equation 5}$$

$\mathbf{C_{par12}}$ = parasitic capacitance between the $\overline{XTI}$ and XTO pins. It consists of the IC package's pin-to-pin capacitance (including any socket used) and the printed circuit board's track-to-track capacitance.

$\mathbf{C_{par12}} \approx 2$pF.

If some frequency pulling can be tolerated, a crystal load capacitance different from the crystal manufacturer's recommended $C_L$ may be acceptable. Larger values of $C_L$ tend to reduce the influence of circuit variations and tolerances on frequency stability. Smaller values of $C_L$ tend to reduce startup time and crystal power dissipation. Care must however be taken that $C_L$ does not fall outside the crystal pulling range or the circuit may fail to start up

altogether. It is also possible to quote $C_L$ to the crystal manufacturer who can then cut a crystal to order which will resonate, under the specified load conditions, at the desired frequency.

Finally the power dissipation in the crystal must be checked. If Pc is too high C1 and C2 must be reduced. If this is not feasible C2 alone may be reduced. Unbalancing C1 and C2 will, however, require checking if the loop gain condition is still satisfied. This must be done using Equation 1.

Note: $2 \geq \frac{C_2}{C_1} \geq 0.5$

### 3.3.1.5 Oscillator/Clock Application Notes

- On the printed circuit board, the tracks to the crystal and capacitors must be made as short as possible. Other signal tracks must not be allowed to cross through this area. The component tracks should preferably be ringed by a ground track connected to the chip ground (0 V) on adjacent pins either side of the crystal pins. It is also advisable to provide a ground plane for the circuit to reduce noise.
- External clock signals, applied to $\overline{XTI}$ and/or XTO, **must not exceed the cell supply limits (i.e., 0 V and CVdd)** and current into or out of $\overline{XTI}$ and/or XTO must be limited to less than 10mA to avoid damaging the cell's amplitude clamping circuit.
- An external, DC coupled, single ended square wave clock signal may be applied to $\overline{XTI}$ if OSCMODE = 0. To limit the current taken from the signal source a resistor should be placed between the clock source and $\overline{XTI}$. The recommended value for this series resistor is 470 Ω for a clock signal switching between **0 V** and **CVdd (1V8)**. The current the clock source needs to source/sink is then ≤1.9 mA. The XTO pin must be left unconnected in this configuration.
- AC coupling of a single ended external clock to $\overline{XTI}$, with OSCMODE = 0, is not recommended. The duty cycle of the OSCOUT signal cannot be guaranteed in such a configuration.
- AC coupling of a single ended external clock to $\overline{XTI}$, with OSCMODE = 1, is possible. It is recommended that the circuit shown in Figure 11 be used to correctly bias the oscillator inputs: The common-mode voltage VCM for $\overline{XTI}$ and XTO, (set by the 15 kΩ and 22 kΩ resistors) must be 800 mV < VCM < CVdd and the amplitude Vpp of the clock signal must be >400 mV.

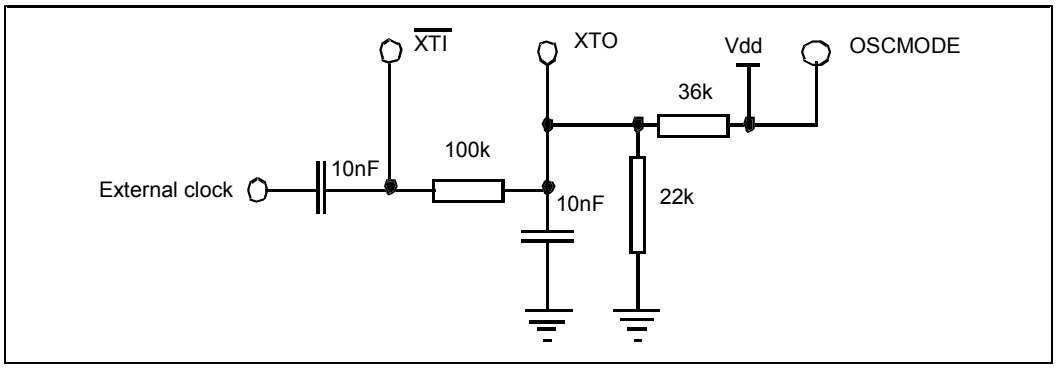


**Figure 11 - External Clocking via AC Coupling**

- External, differential clock signals may be applied to $\overline{XTI}$ and XTO if OSCMODE = 1. The common-mode voltage VCM for the differential clock signals must be 800 mV < VCM < CVdd, and the peak-to-peak signal amplitude Vpp must be >400 mV. It is recommended that differential clock signals have VCM = 1.0 V. For Vpp > 400 mV a resistor of ≥390 Ω in series with $\overline{XTI}$ or XTO may be required to limit the current taken from or supplied to the clock sources.

## 3.4 Electrical Characteristics

Conditions (unless specified otherwise):Tamb = 25°CCVdd = 1.8 VVdd = 3.3 V

**DC Electrical Characteristics**

| Parameter | Conditions/Pin | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Core voltage | | CVdd | 1.71 | 1.8 | 1.89 | V |
| Peripheral voltage | | Vdd | 3.13 | 3.3 | 3.47 | V |
| Core current | Default settings | CIdd | | 120 | | mA |
| Peripheral current | | Idd | | 2.2 | | mA |
| Total power | | Ptot1 | | 223 | | mW |
| Total power (stand-by) | ADCs powered down.<br>MPEG outputs tri-stated | Ptot2 | | 2.55 | | mW |
| Total power (sleep) | Pin 20 = logic ‘1’ & ADCs powered down | Ptot3 | | 0.10 | | mW |
| Output low level | 2, 6 or 12 mA per output (see section 1.3, Pin Description) | Vol | | | 0.4 | V |
| Output high level | 2, 6 or 12 mA per output | Voh | 2.4 | | | V |
| Output leakage | Tri-state when off or open-drain when high | | | | ±1 | µA |
| Output capacitance | All outputs except XTO, CLK1 & open-drain types. Excludes packaging contribution (~0.35pF) | | | 2.7 | | pF |
| | Open-drain outputs.<br>Excludes packaging contribution (~0.35pF) | | | 3.3 | | pF |
| Input low level | | Vil | | | 0.8 | V |
| Input high level | | Vih | 2.0 | | | V |
| Input leakage | Vin = 0 or Vdd | | | | ±1 | µA |
| Input capacitance | Excludes packaging contribution (~0.35pF) | | | 1.5 | | pF |

**AC Electrical Characteristics**

| Parameter | Conditions/Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| ADC Full-scale input single range (single-ended or differential) | Differential source is recommended | | 1.6 | | Vpp |
| ADC analog input resistance | Per input pin | | 25 | | kΩ |
| ADC input common mode voltage level | | | 0.9[1] | | V |
| RF ADC Full-scale input single range (single-ended) | | | 3.3 | | Vpp |
| RF ADC analog input resistance | | | 25 | | kΩ |
| RF ADC input common mode voltage | | | 1.65[2] | | V |
| System clock frequency | | 30.00 | | 100 | MHz |
| Input clock frequency (note [3]) | See Section 3.3.1.5 for details. | 3.99 | | 27.01 | MHz |
| Crystal oscillator frequency | See Section 3.3 for details | 9.99 | | 16.01 | MHz |
| CLK1 clock frequency [4] (with 10 MHz xtal or above) | | | | 400 | kHz |
| MPEG clock input frequency | On pin #63 | note [5] | | 65 [6] | MHz |

1. Actually CVdd/2
2. Actually Vdd/2
3. When not using a crystal, $\overline{\text{XTI}}$ may be driven from an external source over the frequency range shown.
4. The maximum serial clock speed on the primary 2-wire bus is related to the input clock frequency and is limited to 100 kHz with a 4.0 MHz clock.
5. Must be calculated from the data input rate.
6. Must be lower than the system clock.