CE6230 - COFDM demodulator with USB interface for PC-TV

Data Sheet

March 29, 2007

Revision 1,1

Legal Statements

Contents

List of Figures

List of Tables

Revision History

Date	Revision	Reference #	Description
11 September 2006	1.0		Original release
29 March 2007	1.1		Added Theta-JA data

1   Introduction

1.1   Related Documents

Table 1.1 Document References

Title	Number	Location
Universal Serial Bus Specification, Revision 2.0, 27th April 2000		http://www.usb.org/home
Universal Serial Bus Device Class Definition for Video Devices, Revision 1.1, 1st June 2005		http://www.usb.org/developers/devclass_docs
Universal Serial Bus Device Class Definition for Video Devices: MPEG2-TS Payload, Revision 1.1, 1st June 2005		http://www.usb.org/developers/devclass_docs
Recommendation ITU-R BT.656-4, 1998		http://www.itu.int/
NorDig Unified Requirements for profiles Basic TV, Enhanced, Interactive and Internet for Digital Integrated Receiver Decoders for use in cable, satellite, terrestrial and IP-based networks, version 1.0.2		http://www.nordig.org/
CE6353 DVB-T Demodulator Design Manual – April 2006	D56169-002	Intel® CE 6353 DVB-T Demodulator - Overview

2   System

2.1   Features

- Nordig Unified and ETSI 300 744 compliant
- Superior Single Frequency Network performance
- Unique active impulse-noise filtering
- Single SAW operation on 6, 7 & 8 MHz OFDM
- Excellent performance with any echo profile: pre, post, inside or outside the guard interval
- Automatic co-channel and adjacent-channel interference suppression
- Fast AGC and good Doppler performance for portable applications
- Large frequency capture range to enable channel acquisition with triple offsets
- Clock generation from single low-cost 24.0 MHz crystal
- IF sampling at 36.17, 43.5 or 5 - 10 MHz from a single crystal frequency
- Channel bandwidth of 6, 7 & 8 MHz
- Blind acquisition capability (including 2K/8K mode detect)
- Automatic spectral inversion detection
- Fast auto-acquisition technology
- Very low software overhead
- Access to channel SNR, pre- and post-Viterbi bit error rates
- 7-bit ADC for RF signal level measurement

- USB 2.0 compliant interface, 1.1 compatible
- On-chip 8051 microcontroller with 12K program and 4K data RAM.
- Hardware MPEG2 PID filters (enables USB1.1 operation)
- Infra-red port for remote control signal decode in software
- Self or bus powered modes
- 8 general purpose ports

- Full chip control over USB bus
- 3.3/1.8V operation
- 80 pin LQFP
- Low external component count
- Evaluation board and comprehensive software
- Full front end (NIM) reference design available

Applications

- Terrestrial PC applications
- Digital terrestrial TV set-top boxes
- Digital terrestrial integrated televisions

2.2   Applications

The CE6230 is designed to be used in a low-cost USB DVB-T receiver module. The system is shown in Figure 1.

Figure 1 USB DVB-T receiver module
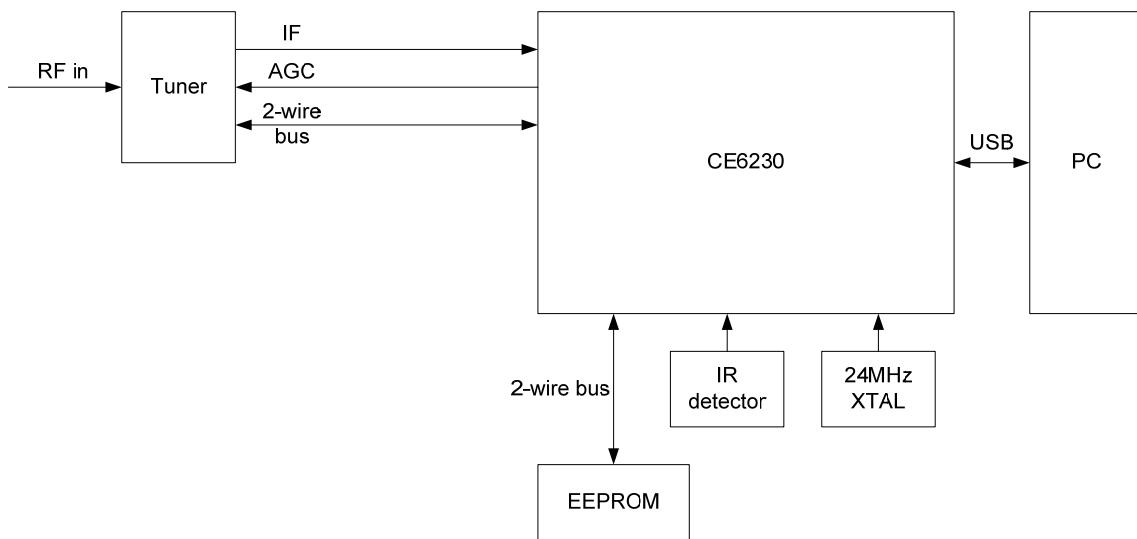
Figure 2 Block diagram
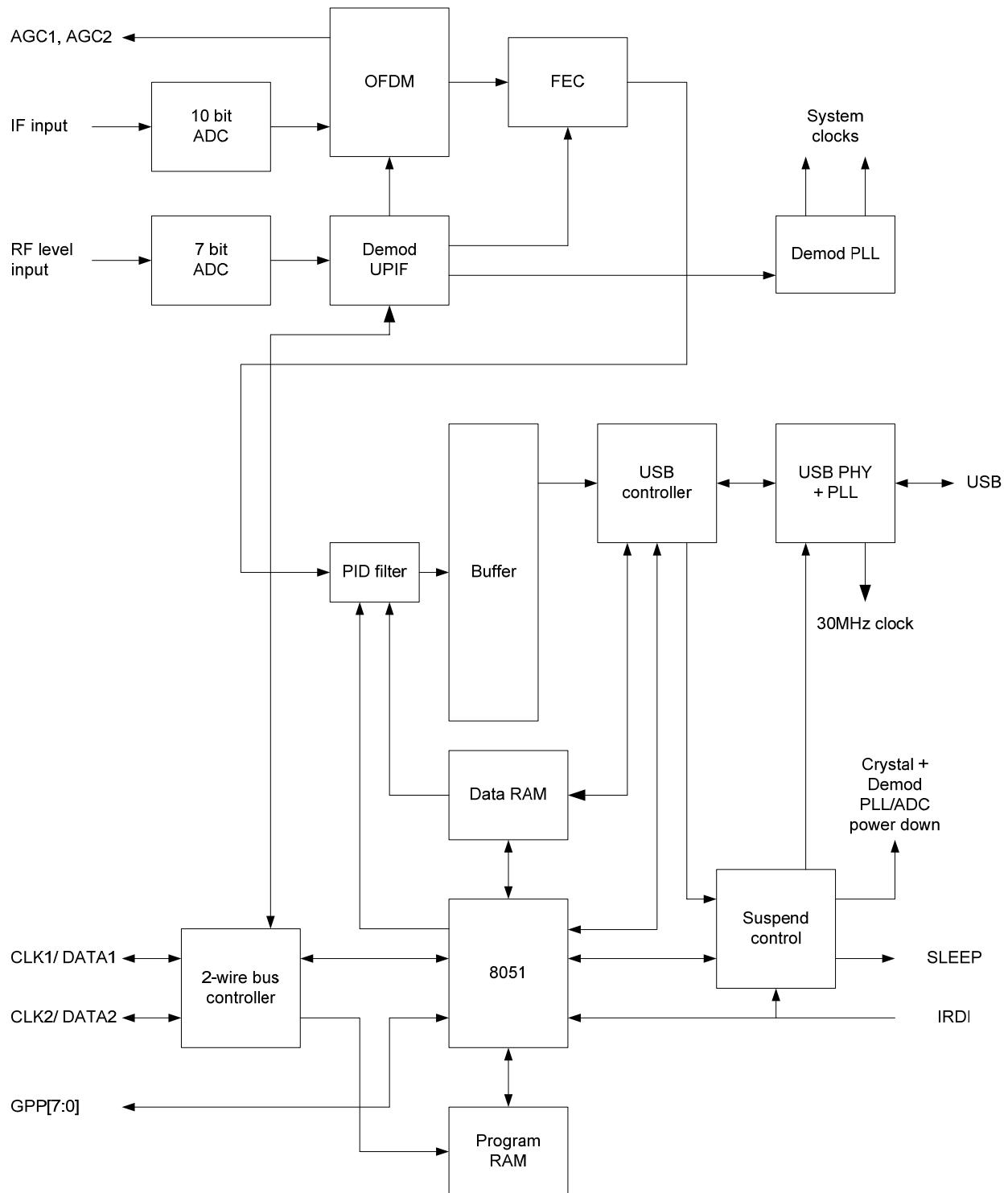
3   Pin definitions

Pin	Name	Pin description	I/O	Note	V	mA
Not connected						
1, 2, 67, 68, 70, 71,74,75 76,77,80			-	-	-	-
2-wire bus						
4	CLK1	EEPROM Master 2-wire bus clock	I/O	Open drain Fall time control	5	6
5	DATA1	EEPROM Master 2-wire bus data	I/O	Open drain Fall time control	5	6
27	CLK2	Tuner Master 2-wire bus clock	I/O	Open drain Fall time control	5	6
28	DATA2	Tuner Master 2-wire bus data	I/O	Open drain Fall time control	5	6
32	ADFMT	EEPROM address format	I	CMOS	3.3	
Crystal						
59	XTIB	Low phase noise oscillator cell. A 24 MHz crystal must be used	I	CMOS		
60	XTO		I	CMOS		
GPP's						
3,8,16,17,18 19,20,23,	GPP(7:0)	General Purpose Ports	I/O	CMOS Tristate / push-pull	3.3	6
AGC						
24	AGC1	IF AGC o/p	O	Open drain	5	6
25	AGC2	RF AGC o/p, should be tied to ground when not used	O	Open drain	5	6
42	RFLEV	RF AGC level indicator input	I	Analog		
Control						
29	SLEEP	Suspend mode power down for rest of PCB. High = suspend, low = powered	O	CMOS	3.3	1
69	RESETB	Active low reset pin	I	CMOS	5	
Infra-red						
62	IRDI	Infra-red input	I	CMOS	3.3	
USB						
47	USBP	USB positive data	I/O	Differential Analog		
48	USBM	USB negative data	I/O	Differential Analog		
46	RES1K5	USB pull up resistor	I/O		3.3	
55	RES6K2	USB bias resistor	I/O		0	
Digital power pins						
34	PLLVDD	PLL and clocking supply	S		1.8	
35	PLLGND	PLL ground supply	S		0	
9,11, 13, 26,56.79	CVDD	Demodulator core logic power supply	S		1.8	
15,57,64	CUVDD	USB core logic power supply	S		1.8	
6,21,73	IVDD	I/O ring power supply	S		3.3	
7, 10, 12, 14, 22, 33, 58, 61,72,78	VSS	Logic Core and I/O ground	S		0	

Pin	Name	Pin description	I/O	Note	V	mA
ADC pins						
38	AIN	ADC positive input	I	Differential Analog		
39	AINB	ADC negative input	I	Differential Analog		
ADC power pins						
36	AVDD	ADC analog supply	S		1.8	
40, 37	AGND	ADC analog supply	S		0	
41	AVD33	ADC I/O and RF level ADC supply	S		3.3	
44	DVDD	ADC digital supply	S		1.8	
43	DGND	ADC digital ground	S		0	
USB power pins						
50	VDDD33	USB PHY Digital I/O supply	S		3.3	
51	VDDL18	USB PHY Logic supply	S		1.8	
45, 53	VDDA33	USB PHY Analog supply	S		3.3	
52	VSSD	USB PHY Digital ground	S		0	
49, 54	VSSA	USB PHY Analog ground	S		0	
TEST						
63, 65, 66	TEST	Test pins	I	Connect to ground	0	
30, 31	TEST	Test pins	I	Connect to VDD33	3.3	

3.1.1   Pull-Up / Pull-Down Resistors

Pin RES1K5 must be connected to a 1.5 kohm (+/- 5%) resistor tied to 3.3V. This is used for the USB bus pull-up.

Pin RES6K2 must be connected to a 6.2 kohm (+/- 1.0%) resistor tied to ground. This is used to bias the USB band gap reference. A 0.1 µF capacitor should be connected in parallel with this.

4   Pin diagram

Figure 3 80-Pin QFP Package Diagram
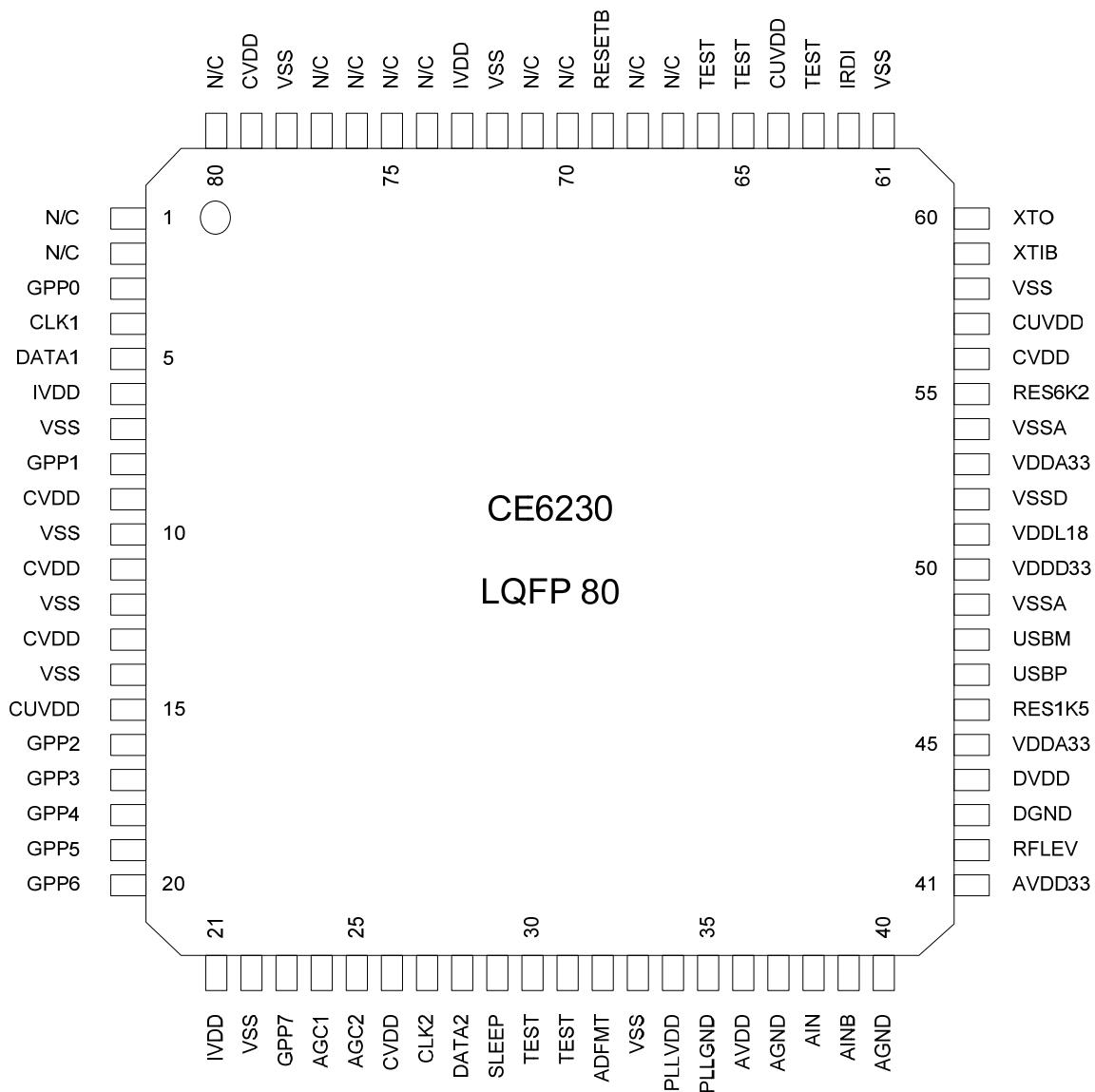
5   Pin list

Table 5.1 Package Pin List

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	N/C	21	IVDD	41	AVD33	61	VSS
2	N/C	22	VSS	42	RFLEV	62	IRDI
3	GPP0	23	GPP7	43	DGND	63	TEST
4	CLK1	24	AGC1	44	DVDD	64	CUVDD
5	DATA1	25	AGC2	45	VDDA33	65	TEST
6	IVDD	26	CVDD	46	RES1K5	66	TEST
7	VSS	27	CLK2	47	USBP	67	N/C
8	GPP1	28	DATA2	48	USBM	68	N/C
9	CVDD	29	SLEEP	49	VSSA	69	RESETB
10	VSS	30	TEST	50	VDDD33	70	N/C
11	CVDD	31	TEST	51	VDDL18	71	N/C
12	VSS	32	ADFMT	52	VSSD	72	VSS
13	CVDD	33	VSS	53	VDDA33	73	IVDD
14	VSS	34	PLLVDD	54	VSSA	74	N/C
15	CUVDD	35	PLLGND	55	RES6K2	75	N/C
16	GPP2	36	AVDD	56	CVDD	76	N/C
17	GPP3	37	AGND	57	CUVDD	77	N/C
18	GPP4	38	AIN	58	VSS	78	VSS
19	GPP5	39	AINB	59	XTIB	79	CVDD
20	GPP6	40	AGND	60	XTO	80	N/C

6   Application schematic

Figure 4 Typical application schematic

7　　8051 Microprocessor
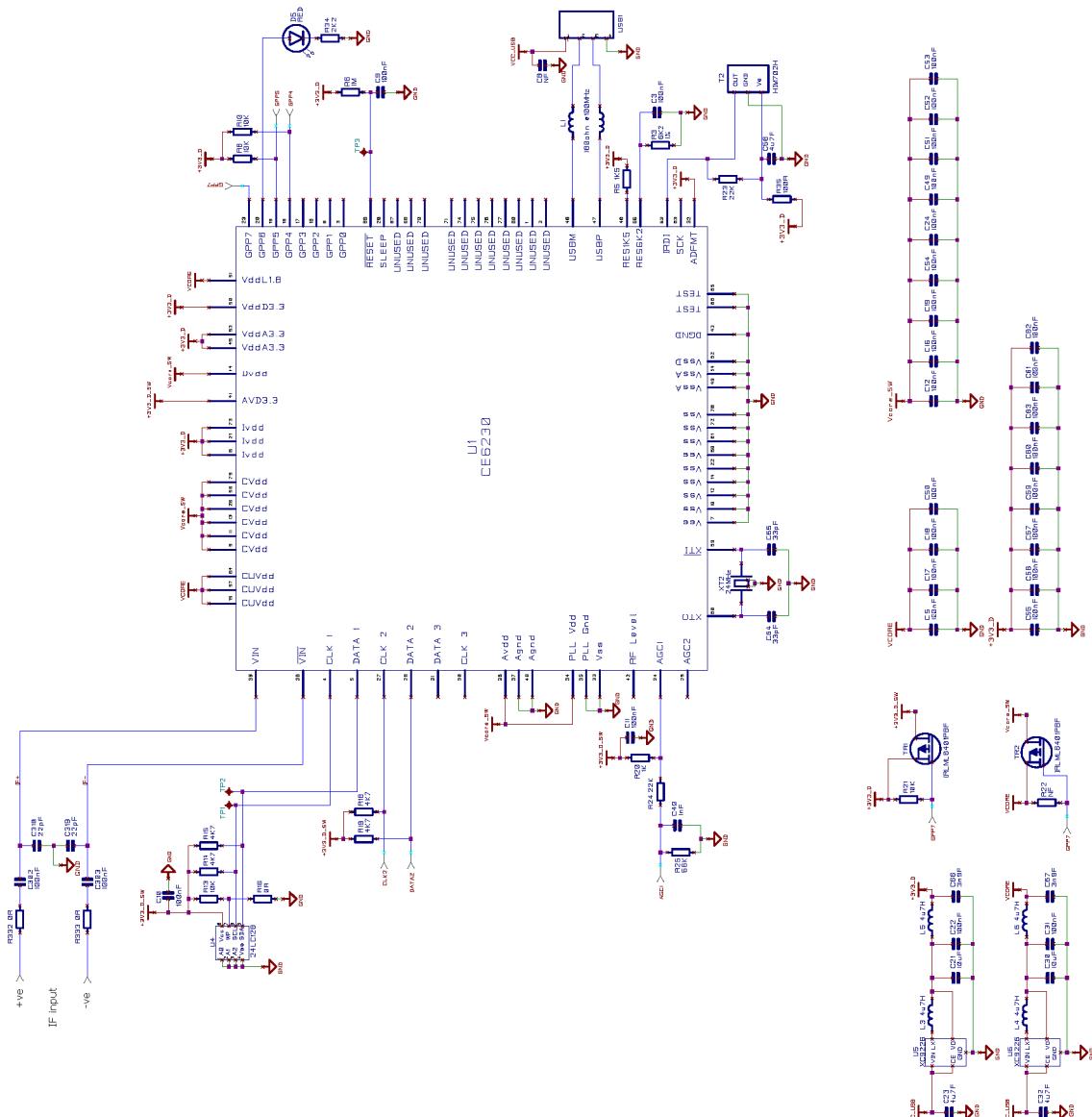
The CE6230 is controlled by an internal 8051-compatible microprocessor. This is connected to 3 internal memories. The "Internal RAM" is 256 bytes. The "Program RAM" is 12 Kbytes. The "Data RAM" (or "External RAM") is 4Kbytes. There is no ROM inside the CE6230. The Program RAM can be written-to by the 8051 and by the 2-wire bus controller. The Data RAM can be written-to and read-from by the USB controller. The Data RAM can be read by PID Filter.

The 8051 is clocked at 30 MHz and the basic instruction cycle is four 30 MHz cycles. There are 3 timers in the 8051. There are no serial ports. There are 7 interrupts used in the CE6230:

Name	Sensitive	Purpose
INT0_N	Edge	Infra-red falling edge detection
INT1_N	Level	USB interrupts
INT2	Edge	Infra-red rising edge detection
INT3_N	Edge or level	Demodulator interrupts
INT4	Level	2-wire bus and PID Filter interrupts
INT5_N	Edge or level	External interrupt input from GPP(7)
SUSPI	Level	Suspend interrupt

7.1　　Internal data memory

Internal Data Memory is mapped in **Error! Reference source not found.**. The memory space is shown divided into three blocks which are generally referred to as the Lower 128, the Upper 128, and SFR space.

Internal Data Memory addresses are always one byte wide, which implies an address space of only 256 bytes. However, the addressing modes for internal RAM can in fact accommodate 384 bytes, using a simple trick. Direct addresses higher than 7FH are one memory space, and indirect addresses higher than 7FH access a different memory space. Thus Figure 6 shows the Upper 128 and SFR (Special function register) space occupying the same block of addresses 80H through FFH, although they are physically separate entities.

The lower 128 bytes of RAM are as mapped in Figure 6.

The lowest 32 bytes are grouped into 4 banks of 8 registers (R0 – R7). Two bits in the Program Status Word (PSW) select which register bank is in use. This allows more efficient use of code space, since register instructions are shorter than instructions that use direct addressing.

The next 16 bytes above the register bank form a block of bit-addressable memory apace. The 8051 instruction set includes a selection of single-bit instructions, and the 128 bits in this area can be directly addressed by these instructions. The bit addresses in this area are 00H through 7FH.

All of the bytes in the Lower 128 can be accessed by either direct or indirect addressing. The Upper 128 can only be accessed by indirect addressing.

Figure 5 Internal RAM organisation

```
        ┌─ FFh  ┌──────────────────┐  ┌──────────────────┐  FFh
        │       │                  │  │                  │
  Upper │       │  Accessible by   │  │  Accessible by   │
   128  ┤       │indirect addressing│  │ direct addressing│
  bytes │       │      only        │  │      only        │
        │       │                  │  │                  │
        └─ 80h  │                  │  │                  │  80h
        ┌─ 7Fh  ├──────────────────┤  └────────┬─────────┘
        │       │7Fh           78h │           │
  Lower │       │                  │           ▲
   128  ┤       │ Accessible by    │      SFR's
  bytes │       │ direct and       │  (Special Function Registers)
        │       │ indirect addressing│
        │       │                  │
        └─ 20h  │07h           00h │
                └──────────────────┘
```

```
              Lower 128 bytes

        7Fh  ┌──────────────────┐
             │                  │
             │                  │
             │    Direct RAM    │
             │                  │
        30h  │                  │
        2Fh  ├──────────────────┤  ┐
             │7Fh           78h │  │
             │                  │  ├ Bit-addressable space
             │  Bit-addressable │  │ (bit addresses 00-7Fh)
             │    registers     │  │
        20h  │07h           00h │  ┘
       ┌1Fh ─├──────────────────┤
   11 ─┤     │      Bank 3      │
       └18h ─├──────────────────┤
       ┌17h ─│                  │
   10 ─┤     │      Bank 2      │
       └10h ─├──────────────────┤
       ┌0Fh ─│                  │
   01 ─┤     │      Bank 1      │
       └08h ─├──────────────────┤
       ┌07h ─│                  │  ◄── Reset value of
   00 ─┤     │      Bank 0      │      Stack Pointer
       └00h ─└──────────────────┘

   Bank select bits
      PSW 4,3
```

8 Demodulator Functional Description

A functional block diagram of the CE6230 OFDM demodulator is shown in Figure 6. This accepts an IF analogue signal and delivers a stream of demodulated soft decision data to the on-chip Viterbi decoder. Clock, timing and frequency synchronization operations are all digital and there are no analogue control loops except the AGC. The frequency capture range is large enough for all practical applications. This demodulator has novel algorithms to combat impulse noise as well as co-channel and adjacent channel interference. If the modulation is hierarchical, the OFDM outputs both high and low priority data streams. Only one of these streams is FEC-decoded, but the FEC can be switched from one stream to another with minimal interruption to the transport stream.

Figure 6 OFDM demodulator diagram
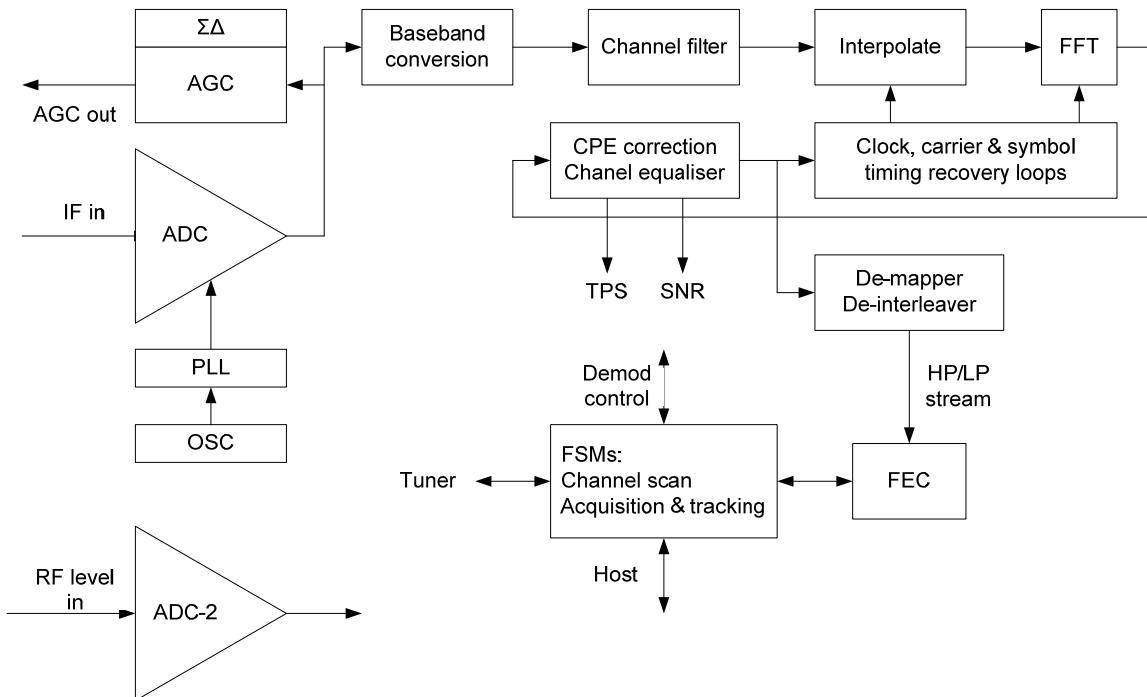
The FEC module shown in Figure 7 consists of a concatenated convolutional (Viterbi) and Reed-Solomon decoder separated by a depth-12 convolutional de-interleaver. The Viterbi decoder operates on 5-bit soft decisions to provide the best performance over a wide range of channel conditions. The trace-back depth of 128 ensures minimum loss of performance due to inevitable survivor truncation, especially at high code rates. Both the Viterbi and Reed-Solomon decoders are equipped with bit-error monitors. The former provides the bit error rate (BER) at the OFDM output. The latter is the more useful measure as it gives the Viterbi output BER. The error collecting intervals of these are programmable over a very wide range.

Figure 7 FEC block diagram

HP/LP stream from OFDM → Viterbi decoder → MPEG frame aligner → De-interleaver

Pre-Vierbi BER ← BER monitor

Reed-Solomon decoder → Descrambler → USB → PC

Uncorrected block count ← UBC monitor

Post-Vierbi BER ← BER monitor
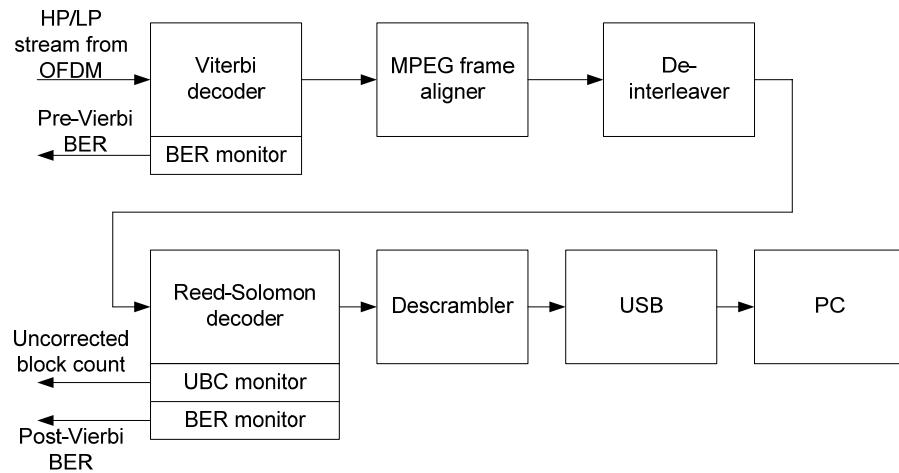
The FSM controller shown in Figure 6controls both the demodulator and the FEC. The controller facilitates the automated search of all parameters or any sub-set of parameters of the received signal. This mechanism provides the fast channel scan and acquisition performance, whilst requiring minimal software overhead in the driver.

The algorithms and architectures used in the CE6230 have been optimized to minimize power consumption.

8.1   Analogue-to-Digital Converter

The CE6230 has a high performance 10-bit analogue-to-digital converter (ADC) which can sample a 6, 7 or 8 MHz bandwidth OFDM signal, with its spectrum centred at:

• 36.17 MHz IF

• 43.75 MHz IF

• 5 - 10 MHz near-zero IF

An on-chip programmable phase locked loop (PLL) is used to generate the ADC sampling clock. The PLL is highly programmable allowing a wide choice of sampling frequencies to suit any IF frequency, and all signal bandwidths.

The CE6230 features a 7-bit RF signal level monitor ADC in addition to the main 10-bit ADC.

8.2   Automatic Gain Control

An AGC module compares the absolute value of the digitized signal with a programmable reference. The error signal is filtered and is used to control the gain of the amplifier. A sigma-delta modulated output is provided, which has to be RC low-pass filtered to obtain the voltage to control the amplifier.

The bandwidth of the AGC is set to a large value for quick acquisition then reduced to a small value for tracking.

The AGC is free running during OFDM channel changes and locks to the new channel while the tuner lock is being established. This is one of the features of CE6230 used to minimize acquisition time. A robust AGC lock mechanism is provided and the other parts of the CE6230 begin to acquire only after the AGC has locked.

8.3   IF to Baseband Conversion

Sampling a 36.17 MHz IF signal at 45 MHz results in a spectrally inverted OFDM signal centred at approximately 8.9 MHz. The first step of the demodulation process is to convert this signal to a complex (in-phase and quadrature) signal in baseband. A correction for spectral inversion is implemented during this conversion process. Note also that the CE6230 has control mechanisms to search automatically for an unknown spectral inversion status.

8.4   Adjacent Channel Filtering

Adjacent channels, in particular the Nicam digital sound signal associated with analogue channels, are filtered prior to the FFT.

8.5   Interpolation and Clock Synchronisation

CE6230 uses digital timing recovery and this eliminates the need for an external VCXO. The ADC samples the signal at a fixed rate, for example, 45.0 MHz. Conversion of the 45.0 MHz signal to the OFDM sample rate is achieved using the time-varying interpolator. The OFDM sample rate is 64/7 MHz for 8 MHz and this is scaled by factors 6/8 and 7/8 for 6 and 7 MHz channel bandwidths. The nominal ratio of the ADC to OFDM sample rate is programmed in a CE6230 register (defaults are for 45 MHz sampling and 8 MHz OFDM). The clock recovery phase locked loop in the CE6230 compensates for inaccuracies in this ratio due to uncertainties of the frequency of the sampling clock.

8.6   Carrier Frequency Synchronisation

There can be frequency offsets in the signal at the input to OFDM, partly due to tuner step size and partly due to broadcast frequency shifts, typically 1/6 MHz. These are tracked out digitally, up to 1 MHz in 2 K and 8 K modes, without the need for an analogue frequency control (AFC) loop.

The default frequency capture range has been set to ±286 kHz in the 2 K and 8 K mode. However, these values can be increased, if necessary, by programming an on-chip register (CAPT_RANGE). It is recommended that a larger capture range be used for channel scan in order to find channels with broadcast frequency shifts, without having to adjust the tuner. After the OFDM module has locked (the AFC will have been previously disabled), the frequency offset can be read from an on-chip register.

8.7   Symbol Timing Synchronisation

This module computes the optimum sample position to trigger the FFT in order to eliminate or minimize inter-symbol interference in the presence of multi-path distortion. Furthermore, this trigger point is continuously updated to dynamically adapt to time-variations in the transmission channel.

8.8   Fast Fourier Transform

The FFT module uses the trigger information from the timing synchronization module to set the start point for an FFT. It then uses either a 2 K or 8 K FFT to transform the data from the time domain to the frequency domain. An extremely hardware-efficient and highly accurate algorithm has been used for this purpose.

8.9　　Common Phase Error Correction

This module subtracts the common phase offset from all the carriers of the OFDM signal to minimize the effect of the tuner phase noise on system performance.

8.10　　Channel Equalisation

This consists of two parts. The first part involves estimating the channel frequency response from pilot information.

Efficient algorithms have been used to track time-varying channels with a minimum of hardware.

The second part involves applying a correction to the data carriers based on the estimated frequency response of the channel. This module also generates dynamic channel state information (CSI) for every carrier in every symbol.

8.11　　Impulse Filtering

CE6230 contains several mechanisms to reduce the impact of impulse noise on system performance.

8.12　　Transmission Parameter Signalling (TPS)

An OFDM frame consists of 68 symbols and a superframe is made up of four such frames. There is a set of TPS carriers in every symbol and all these carry one bit of TPS. These bits, when combined, include information about the transmission mode, guard ratio, constellation, hierarchy and code rate, as defined in ETS 300 744. In addition, the first eight bits of the cell identifier are contained in even frames and the second eight bits of the cell identifier are in odd frames. The TPS module extracts all the TPS data, and presents these to the processor in a structured manner.

8.13　　De-Mapper

This module generates soft decisions for demodulated bits using the channel-equalized in-phase and quadrature components of the data carriers as well as per-carrier channel state information (CSI). The de-mapping algorithm depends on the constellation (QPSK, 16 QAM or 64 QAM) and the hierarchy ($\alpha = 0, 1, 2$ or 4). Soft decisions for both low- and high-priority data streams are generated.

8.14　　Symbol and Bit De-Interleaving

The OFDM transmitter interleaves the bits within each carrier and also the carriers within each symbol. The de-interleaver modules consist largely of memory to invert these interleaving functions and present the soft decisions to the FEC in the original order.

8.15　　Viterbi Decoder

The Viterbi decoder accepts the soft decision data from the OFDM demodulator and outputs a decoded bit-stream.

The decoder does the de-puncturing of the input data for all code rates other than 1/2. It then evaluates the branch metrics and passes these to a 64-state path-metric updating unit, which in turn outputs a 64-bit word to the survivor

memory. The Viterbi decoded bits are obtained by tracing back the survivor paths in this memory. A trace-back depth of 128 is used to minimize any loss in performance, especially at high code rates. The decoder re-encodes the decoded bits and compares these with received data (delayed) to compute bit errors at its input, on the assumption that the Viterbi output BER is significantly lower than its input BER.

8.16   MPEG Frame Aligner

The Viterbi decoded bit stream is aligned into 204-byte frames. A robust synchronization algorithm is used to ensure correct lock and to prevent loss of lock due to noise impulses.

8.17   De-interleaver

Errors at the Viterbi output occur in bursts and the function of the de-interleaver is to spread these errors over a number of 204-byte frames to give the Reed-Solomon decoder a better chance of correcting these. The de-interleaver is a memory unit which implements the inverse of the convolutional interleaving function introduced by the transmitter.

8.18   Reed-Solomon Decoder

Every 188-byte transport packet is encoded by the transmitter into a 204-byte frame, using a truncated version of a systematic (255,239) Reed-Solomon code. The corresponding (204,188) Reed-Solomon decoder is capable of correcting up to eight byte errors in a 204-byte frame. It may also detect frames with more than eight byte errors.

In addition to efficiently performing this decoding function, the Reed-Solomon decoder in CE6230 keeps a count of the number of bit errors corrected over a programmable period and the number of uncorrectable blocks. This information can be used to compute the post-Viterbi BER.

8.19   De-scrambler

The de-scrambler de-randomizes the Reed-Solomon decoded data by generating the exclusive-OR of this with a pseudo-random bit sequence (PRBS). This outputs 188-byte MPEG transport packets. The TEI bit of the packet header will be set if required to indicate uncorrectable packets.

9 USB implementation

The CE6230 provides 3 USB endpoints:

- Endpoint 0 is the default control endpoint. This is used for all control operations of the CE6230. The format of the data is completely user-defined (except for standard USB commands).

- Endpoint 1 is an Interrupt IN endpoint. This can be used by the 8051 to report events (such as infra-red key-presses) to the host PC. The format of the data is completely user-defined.

- Endpoint 2 is either an Isochronous IN endpoint or a Bulk IN endpoint.. This is used to transfer MPEG transport stream data to the PC. This is a hardware interface – once set up, the transfers will occur independently of the 8051.

In isochronous transfer mode the CE6230 has the ability to insert a header before each MPEG transport stream transfer. The length of the header can be from 1 to 4 bytes but will usually be set to 2 for compliance with the Device Class Definition for Video Devices with MPEG2-TS Payload.

The CE6230 can support up to 3 USB configurations (1 to 3), each of which can have up to 3 interfaces (0 to 2). There can be up to 15 alternate settings (0 to 14) for each interface.

All control operations use endpoint 0.

9.1 Suspend mode

USB devices must support a suspend mode in which the current drawn from the bus must be less than 500 µA. For remote-wakeup enabled devices this limit is raised to 2.5 mA, but only when the remote-wakeup feature has been enabled by the PC. The PC requests device suspend mode by stopping USB activity for more than 3 ms.

9.2 Infra-Red detector

The infra-red detector should be connected to pin IRDI. A rising edge on IRDI will set interrupt INT2, a falling edge will set INT0_N. These interrupts, together with the 8051 timers, can be used to measure the pulse widths on the infra-red symbols. The 8051 can decode the pulse sequence into a keypad code which can be sent over interrupt endpoint 1 to the PC.

If the device is configured as remote-wakeup capable remote-wakeup using pin IRDI should work automatically without requiring software intervention.

10   Electrical characteristics

Test conditions unless otherwise stated.

Tamb = 0 - 70ºC, Vdd = 3.3V ± 5% and 1.8V ± 5%

10.1   Recommended Operating Conditions

Table 10.1 Recommended operating conditions

Symbol	Parameter		Min	Typ	Max	Units
VDD	Power supply voltage:	periphery	3.14	3.3	3.47	V
CVDD		core	1.71	1.8	1.89	V
IDD_P	Power supply current:	Periphery[1]		50		mA
IDD_C		core[2]		185		mA
XTI	Crystal frequency		- 100ppm	24.0	+ 100ppm	MHz
T_{OP}	Operating ambient temperature		0	-	70	ºC
T_{RESET}	Reset Time after Valid Power	Vcc MIN = 3.0V	40	-	90	mS
Rja	Theta-JA (θJA), Still Air [3]			44		ºC /W

[1]   Current from the 3.3 V supply will be dependent on the external loads.
[2]   Decoding 8k, 64QAM, guard interval 1/4 , code rate 2/3.
[3]   Theta-JA (θJA) is the junction-to-ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

Neither performance nor reliability is guaranteed outside these limits. Extended operation outside these limits might adversely affect device reliability.

10.2   Absolute Maximum Ratings

Table 10.2 Absolute maximum ratings

Symbol	Parameter		Min	Max	Units
VDD	Power supply voltage:	periphery	-0.5	5.0	V
CVDD		core	-0.5	2.5	V
V_I	Voltage on input pins (5 V rated)		-0.5	7.0	V
V_I	Voltage on input pins (3.3 V rated)		-0.5	VDD + 0.5	V
V_O	Voltage on input pins (5 V rated)		-0.5	7.0	V
V_O	Voltage on input pins (3.3 V rated)		-0.5	VDD + 0.5	V
T_{STG}	Storage temperature		-55	150	ºC
T_J	Junction temperature		-40	125	ºC

Note: Stresses exceeding these listed under absolute maximum ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

10.3　DC Electrical Characteristics

Table 10.3 DC electrical characteristics

Symbol	Parameter	Conditions	Pins	Min	Typ	Max	Units
VDD	Operating voltage:　　periphery			3.14	3.3	3.47	V
CVDD	core			1.71	1.8	1.89	V
IDD_C	Supply current	1.71<CVDD<1.89			185		mA
I_{SUSP} CE6230	Suspend supply current	Host computer disconnected			95		µA
I_{SUSP} SYSTEM	Suspend supply current	Host computer connected			295		µA
Outputs							
V_{OH}		IOH 2mA 3.14<VDD<3.47	SLEEP	2.4	-	-	V
V_{OH}		IOH 6mA 3.14<VDD<3.47	GPP(7:0)	2.4	-	-	V
V_{OL}	Output levels	IOL 2mA 3.14<VDD<3.47	SLEEP	-	-	0.4	V
V_{OL}		IOL 6mA 3.14<VDD<3.47	GPP(7:0), CLK1, CLK2, DATA1, DATA2, AGC1, AGC2	-	-	0.4	V
	Output capacitance	Not including track	SLEEP	-	3.0	-	pF
			GPP(7:0), CLK1, CLK2, DATA1, DATA2, AGC1, AGC2	-	3.6	-	pF
I_{LZ}	Output leakage current (tri-state)			-	-	1	µA
Inputs							
V_{IH}	Input levels	3.14<VDD<3.47 -0.5 ≥ Vin ≥ VDD+0.5V	GPP(7:0), ADFMT, IRDI	2.0	-	-	V
V_{IH}	Input levels	3.14<VDD<3.47 -0.5 ≥ Vin ≥ +5.5V	DATA1, DATA2, CLK1, CLK2, RESETB	2.0	-	-	V
V_{IL}	Input levels	3.14<VDD<3.47	All inputs	-	-	0.8	V
	Input leakage current		IRDI, ADFMT, RESETB	-	-	±1	µA
	Input capacitance	Capacitances do not include track		-	1.5	-	pF
	Input capacitance		CLK1, CLK2, DATA(1:2), GPP(7:0)	-	3.3	-	pF

10.4　Crystal specification

Parallel resonant fundamental frequency (preferred)	24.00 MHz
Tolerance overall, including frequency accuracy and over temperature	± 100ppm
Equivalent series resistance (ESR)	30 Ohms ideal – 50 Ohms maximum.
Typical load capacitance (CL)	20 pF
Drive level	1 mW

Value of C1, C2 (parallel capacitors in the application) for an ESR of 30 Ohms – 33pF

11 Package Information

DIMENSION LIST (FOOTPRINT: 2.00)

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A1	0.100±0.050	STANDOFF
3	A2	1.400±0.050	PKG THICKNESS
4	D	12.000±0.200	LEAD TIP TO TIP
5	D1	10.000±0.100	PKG LENGTH
6	E	12.000±0.200	LEAD TIP TO TIP
7	E1	10.000±0.100	PKG WIDTH
8	L	0.600±0.150	FOOT LENGTH
9	L1	1.000 REF.	LEAD LENGTH
10	T	$0.150^{+0.05}_{-0.06}$	LEAD THICKNESS
11	T1	0.127±0.030	LEAD BASE METAL THICKNESS
12	a	0°~7°	FOOT ANGLE
13	b	0.180±0.050	LEAD WIDTH
14	b1	0.160±0.030	LEAD BASE METAL WIDTH
15	e	0.400 BASE	LEAD PITCH
16	H (REF.)	(7.600)	CUM. LEAD PITCH
17	aaa	0.200	PROFILE OF LEAD TIPS
18	bbb	0.200	PROFILE OF MOLD SURFACE
19	ccc	0.080	FOOT COPLANARITY
20	ddd	0.080	FOOT POSITION

NOTES :

| S/N	DESCRIPTION		SPECIFICATION
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXPECT EJECTION AND PIN 1 MARKING.		Ra0.8~2.0um
3	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):		MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):		MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
7	COMPLIANT TO JEDEC STANDARD: MS-026		

C0.60X45°
(4X)

DETAIL X

b

T

T1

b1

SECTION N-N

R0.30 TYP
ALL AROUND

0.20 Min.

0° Min.

R0.10~0.20

A

A2

ccc C

H

0.25 BASE

GAGE PLANE

R0.10~0.20

SEATING
PLANE

A1

C

e

N

N

α

L

L1

b

⊕ ddd(M) C A-B D
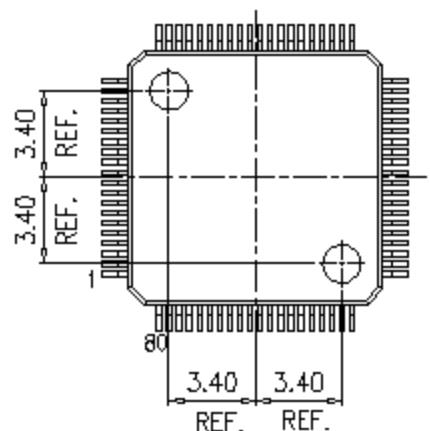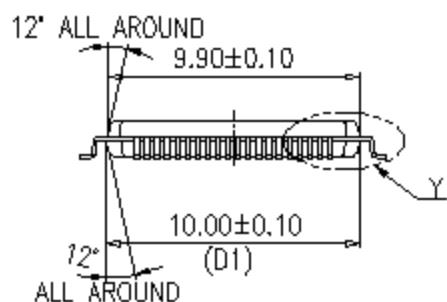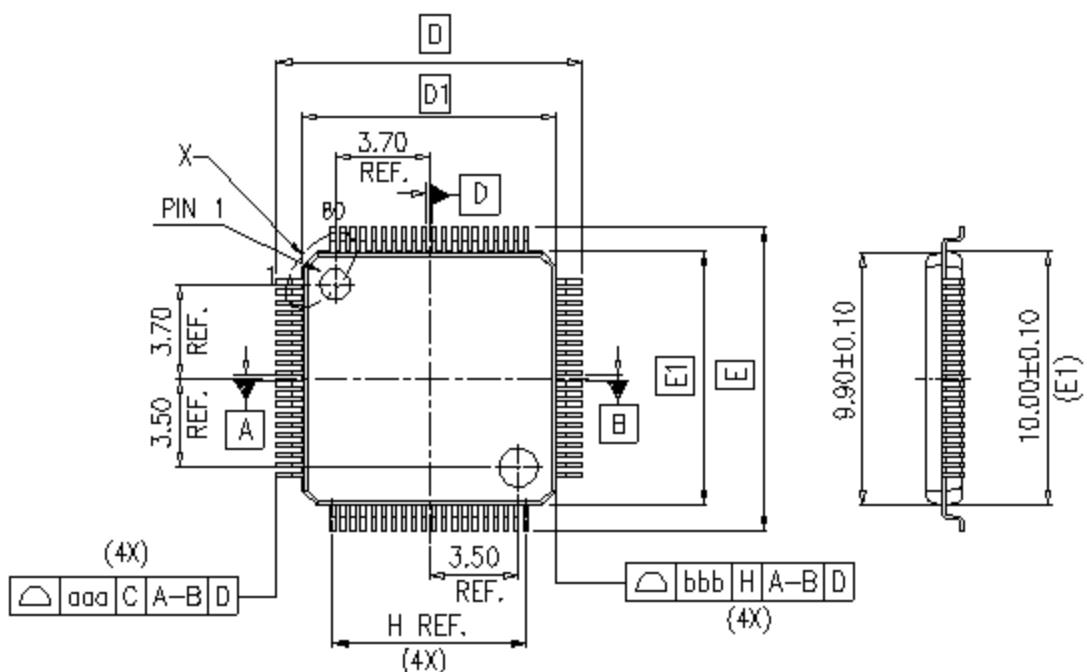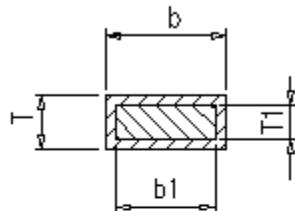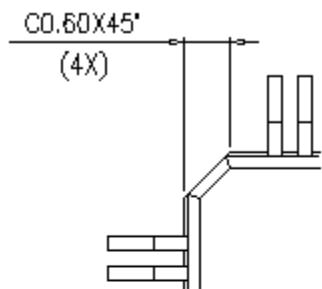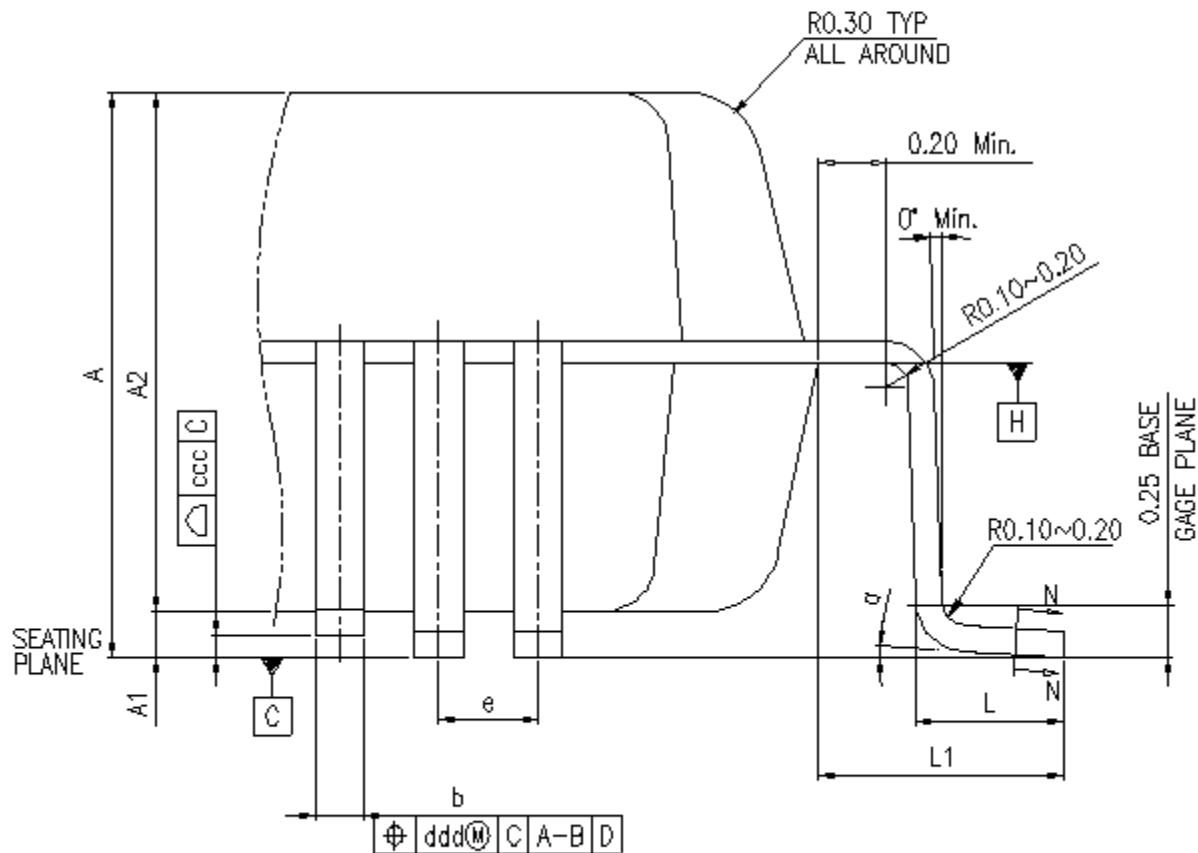
DETAIL Y

12　　　Abbreviations and symbols

ACRONYM	Description
ACI	Adjacent Channel Interferer
ACQ	Acquisition
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BA	Byte Align(er)
BCH	Bose, Chaudhuri & Hocquenghem (coding scheme applied to TPS data)
BDI	Bit Deinterleave
BER	Bit Error Ratio
CAS	Co and Adjacent channel interference suppression
CCI	Co-Channel Interferer
CHC	Channel Corrector
COFDM	Coded Orthogonal Frequency Division Multiplexing
CP	Continuous Pilot
CPE	Common Phase Error
CRL	Carrier recovery loop
CSI	Channel State Information
CSR	Control and Status Registers
DMP	Symbol Demapper
DVB	Digital Video Broadcasting
ETSI	European Telecommunications Standards Institute
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FSM	Finite State Machine
I2S	An audio bus standard
ISR	Interrupt Service Routine
ITB	IF to Baseband Conversion
ITP	Digital interpolator
PID	Packet Identifier
PPM	Pilot Processing Module
REC656	A digital video standard
SCR	Slope corrector
SDI	Symbol Deinterleave
SFR	Special Function Register
SOF	Start of frame
SP	Scattered pilot
SYR	Symbol timing recovery
TPS	Transmission Parameter Signalling
TRL	Timing Recovery Loop
TS	Transport Stream
TWB	2-Wire Bus
USB	Universal Serial Bus