CE6251 – Dual COFDM demodulator with PID filters and MRC diversity

Data Sheet

May 16, 2008

Revision 0,6

Subject to change without notice

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Abbreviations and symbols

ACRONYM	Description
ACI	Adjacent Channel Interferer
ACQ	Acquisition
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BA	Byte Align(er)
BCH	Bose, Chaudhuri & Hocquenghem (coding scheme applied to TPS data)
BDI	Bit Deinterleave
BER	Bit Error Ratio
CAS	Co and Adjacent channel interference suppression
CCI	Co-Channel Interferer
CHC	Channel Corrector
COFDM	Coded Orthogonal Frequency Division Multiplexing
CP	Continuous Pilot
CPE	Common Phase Error
CRL	Carrier recovery loop
CSI	Channel State Information
CSR	Control and Status Registers
DMP	Symbol Demapper
DVB	Digital Video Broadcasting
DVR	Diversity
ETSI	European Telecommunications Standards Institute
FEC	Forward Error Correction
FFT	Fast Fourier Transform
FSM	Finite State Machine
ITB	IF to Baseband Conversion
ITP	Digital interpolator
PID	Packet Identifier
PPM	Pilot Processing Module
SCR	Slope corrector
SDI	Symbol Deinterleave
SP	Scattered pilot
SYR	Symbol timing recovery
TPS	Transmission Parameter Signalling
TRL	Timing Recovery Loop
TS	Transport Stream
TWB	2-Wire Bus
UPIF	Micro-Processor interface
UBC	Uncorrectable Block Count

Revision History

Date	Revision	Reference #	Description
17 November 2006	0.1		Original
17 November 2006	0.2		Corrected error with crystal frequency
17 November 2006	0.3		Reset period set to TBD
31 January 2007	0.4		Removed reference to USB 1.1 in feature list
19 April 2007	0.5		Minor corrections
16 May 2008	0.6		Updated TS output control

1 Introduction

1.1 Related Documents

Table 1.1 Document References

Title	Number	Location
DVB Framing structure, Channel coding and modulation for digital terrestrial television, EN300 744 v1.4.1		
NorDig Unified Requirements for profiles Basic TV, Enhanced, Interactive and Internet for Digital Integrated Receiver Decoders for use in cable, satellite, terrestrial and IP-based networks, version 1.0.2		http://www.nordig.org/
CE6353 DVB-T Demodulator Design Manual – April 2006	D56169-002	Intel® CE 6353 DVB-T Demodulator - Overview

2 System

2.1 Features

Dual Channel DVB-T Demodulator optimised for:
- Watch and Record applications
- Portable diversity applications

Diversity mode
Dual Parallel/serial MPEG stream output
Optional PID Filtered transport stream multiplexing to one MPEG port
Nordig Unified and ETSI 300 744 compliant
Superior Single Frequency Network performance
Unique active impulse-noise filtering
Single SAW operation on 6, 7 & 8 MHz OFDM
RF level detect ADC on-chip to indicate signal power for each channel
Excellent performance with any echo profile: pre, post, inside or outside the guard interval
Automatic co-channel and adjacent-channel interference suppression
Fast AGC and good Doppler performance for portable applications
Large frequency capture range to enable channel acquisition with triple offsets
IF sampling at 36.17, 43.5 or 5 - 10 MHz from a single crystal frequency
Channel bandwidth of 6, 7 & 8 MHz
Blind acquisition capability (including 2K/8K mode detect)
Automatic spectral inversion detection
Fast auto-scan and acquisition technology
Very low software overhead
Access to channel SNR, pre- and post-Viterbi bit error rates
On-chip PLL clock generation using a single 20.48MHz crystal

Hardware MPEG2 PID filters (enables low bandwidth operation, can be turned off)
8 general purpose ports, 2 dedicated and 6 shared function

3.3/1.2V operation
80 pin LQFP
Low external component count
Industrial Temperature range -10 to 80°C
Evaluation board and comprehensive software
Full front end (NIM) reference design available

Applications

Terrestrial PC applications
Digital terrestrial TV set-top boxes
Digital terrestrial integrated televisions
Portable TV receivers

2.2 Application

The CE6251 is designed to be used in a low-cost DVB-T receiver module. The system is shown in Figure 1.

Figure 1 Dual DVB-T receiver module

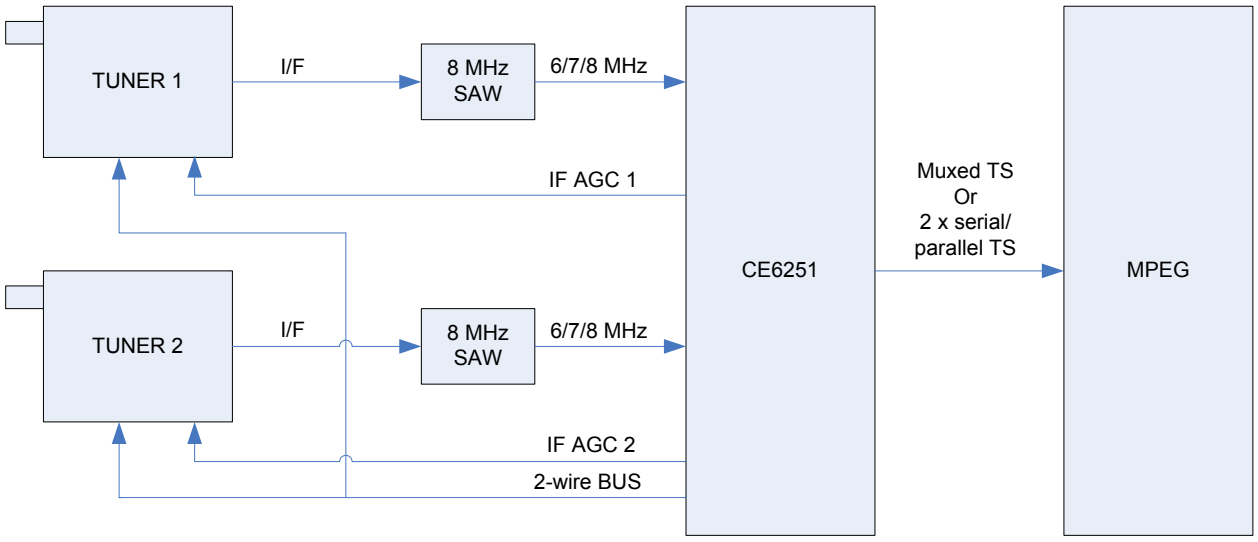
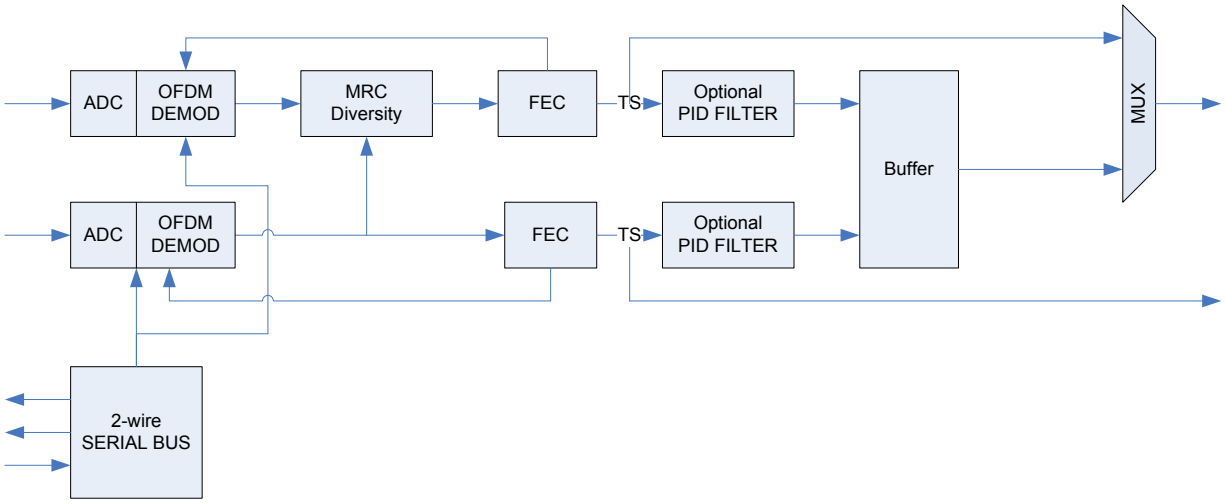


Figure 2 Block diagram



3 Package Information

3.1 Thermal

Table 3.1 Thermal

Parameter	Minimum	Maximum
Ambient Operating temperature Range	-10°C	80°C
Storage Temperature	-55°C	150°C
Maximum junction temperature T_{jmax}		125°C
Rja - Theta-JA (θJA), Still Air [1]		38ºC /W

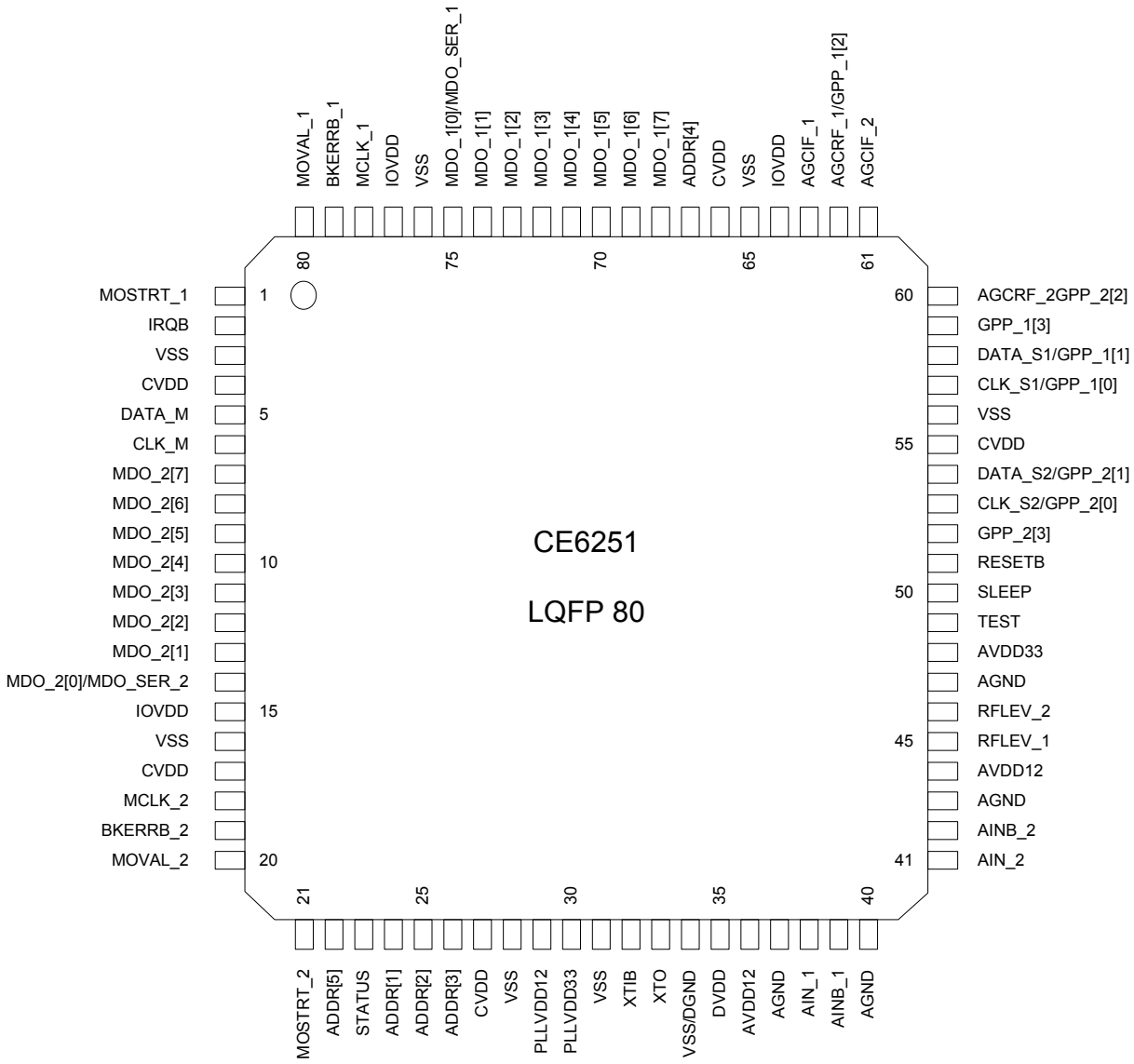
[1] Theta-JA (θJA) is the junction-to-ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

3.2 Package Pin Out

Table 3.2 Package Pin List

PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION	PIN	FUNCTION
1	MOSTRT_1	21	MOSTRT_2	41	AIN_2	61	AGCIF_2
2	IRQB	22	ADDR[[5]	42	AINB_2	62	AGCRF_1/ GPP_1[2]
3	VSS	23	STATUS	43	AGND	63	AGCIF_1
4	CVDD	24	ADDR[1]	44	AVDD12	64	IOVDD
5	DATA_M	25	ADDR[2]	45	RFLEV_1	65	VSS
6	CLK_M	26	ADDR[3]	46	RFLEV_2	66	CVDD
7	MDO_2[7]	27	CVDD	47	AGND	67	ADDR[4]
8	MDO_2[6]	28	VSS	48	AVDD33	68	MDO_1[7]
9	MDO_2[5]	29	PLLVDD12	49	TEST	69	MDO_1[6]
10	MDO_2[4]	30	PLLVDD33	50	SLEEP	70	MDO_1[5]
11	MDO_2[3]	31	VSS	51	RESETB	71	MDO_1[4]
12	MDO_2[2]	32	XTIB	52	GPP2[3]	72	MDO_1[3]
13	MDO_2[1]	33	XTO	53	CLK_S2/ GPP_2[0]	73	MDO_1[2]
14	MDO_2[0]/ MDO_SER_2	34	VSS/DGND	54	DATA_S2/ GPP_2[1]	74	MDO_1[1]
15	IOVDD	35	DVDD	55	CVDD	75	MDO_1[0]/ MDO_SER_1
16	VSS	36	AVDD12	56	VSS	76	VSS
17	CVDD	37	AGND	57	CLK_S1/ GPP_1[0]	77	IOVDD
18	MCLK_2	38	AIN_1	58	DATA_S1/ GPP_1[1]	78	MCLK_1
19	BKERRB_2	39	AINB_1	59	GPP_1[3]	79	BKERRB_1
20	MOVAL_2	40	AGND	60	AGCRF_2/ GPP_2[2]	80	MOVAL_1

Figure 3 80-Pin QFP Package Diagram



3.2.1 Ordering Information

WJCE6251 888887	80 Pin	LQFP*	Trays

*. Pb Free Matte Tin

3.3 Pin definitions

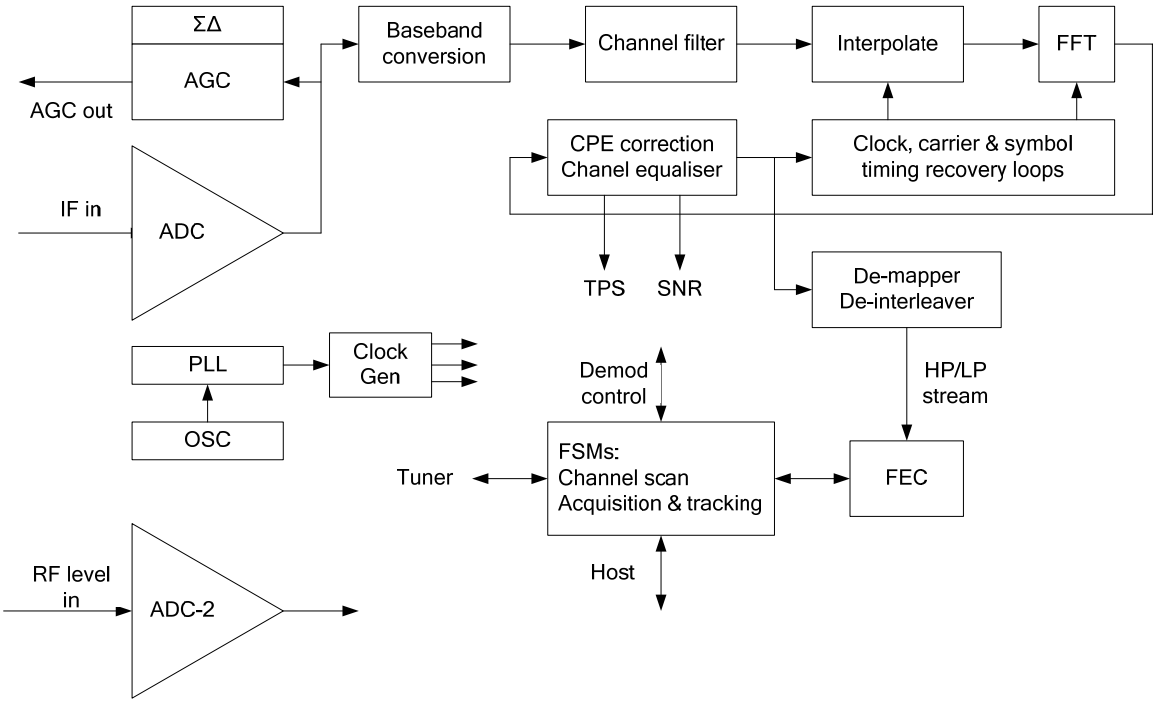
Pin	Name	Pin description	I/O	Note	V	mA
MPEG output channel 1						
1	MOSTRT_1	MPEG packet start	O	CMOS Tristate	3.3	2
75	MDO_1[0] / MDO_SER_1	MPEG data output/ Serial MPEG data output	O	CMOS Tristate	3.3	2
68, 69, 70, 71, 72, 73, 74	MDO_1[7:1]	MPEG data output	O	CMOS Tristate	3.3	2
78	MCLK_1	MPEG clock output	O	CMOS Tristate	3.3	12
79	BKERRB_1	Block error active low output	O	CMOS Tristate	3.3	2
80	MOVAL_1	MPEG data valid	O	CMOS Tristate	3.3	2
MPEG output channel 2						
21	MOSTRT_2	MPEG packet start	O	CMOS Tristate	3.3	2
14	MDO_2[0]/ MDO_SER_2	MPEG data output/ Serial MPEG data output	O	CMOS Tristate	3.3	2
7, 8, 9, 10, 11, 12, 13	MDO_2[7:1]	MPEG data output	O	CMOS Tristate	3.3	2
18	MCLK_2	MPEG clock output	O	CMOS Tristate	3.3	12
19	BKERRB_2	Block error active low output	O	CMOS Tristate	3.3	2
20	MOVAL_2	MPEG data valid	O	CMOS Tristate	3.3	2
2-wire bus						
6	CLK_M	Master 2-wire bus clock	I/O	CMOS	5	8
5	DATA_M	Master 2-wire bus data	I/O	Open drain	5	8
57	CLK_S1/ GPP1[0]	Serial clock slave output to tuner 1/ General Purpose Port.	I/O	Open drain	5	2
58	DATA_S1/ GPP1[1]	Serial data slave output to tuner 1/ General Purpose Port.	I/O	Open drain	5	2
53	CLK_S2/ GPP2[0]	Serial clock slave output to tuner 2/ General Purpose Port.	I/O	Open drain	5	2
54	DATA_S2/ GPP2[1]	Serial data slave output to tuner 2/ General Purpose Port.	I/O	Open drain	5	2
22, 24, 25, 26, 67	ADDR[5:1]	Serial bus address select input, hardwired to desired value. ADDR[0] = 0, selects channel 1 ADDR[0] = 1, selects channel 2	I	CMOS	3.3	
Crystal						
32	XTIB	Low phase noise oscillator cell. XTIB also used as EXT_CLK input	I	Analog		
33	XTO		I/O	Analog		
GPP's						
59	GPP1[3]	General Purpose Port	I/O	Open drain	5	8
52	GPP2[3]	General Purpose Port	I/O	Open drain	5	8
AGC						
63	AGCIF_1	Channel 1 IF AGC o/p and test input	I/O	Open drain	5	8
62	AGCRF_1/ GPP1[2]	Channel 1 RF AGC o/p or General Purpose Port and test input	I/O	Open drain	5	8
61	AGCIF_2	Channel 2 IF AGC o/p and test input	I/O	Open drain	5	8
60	AGCRF_2/ GPP2[2]	Channel 2 RF AGC o/p or General Purpose Port and test input	I/O	Open drain	5	8
45	RFLEV_1	Tuner 1 RF AGC level input	I	Analog		
46	RFLEV_2	Tuner 2 RF AGC level input	I	Analog		

Pin	Name	Pin description	I/O	Note	V	mA
Control						
50	SLEEP	Complete power down (except ADC)	I	CMOS	5	
51	RESETB	Chip reset active low	I	CMOS	5	
2	IRQB	Interrupt input and test input	I/O	Open drain	5	8
23	STATUS	Status output and test input	I/O	CMOS Tristate	3.3	2
Miscellaneous						
49	TEST	Test pin, should be grounded	I	CMOS	5	
Digital power pins						
29	PLLVDD12	PLL, oscillator and clocking supply	S		1.2	
30	PLLVDD33	PLL supply	S		3.3	
4, 17, 27, 55, 66	CVDD	Core logic power supply	S		1.2	
3, 16, 28, 31, 56, 65, 76	VSS	Core, PLL and I/O ground	S		0	
34	DGND	ADC digital ground supply	S		0	
35	DVDD	ADC digital power supply	S		1.2	
15, 64, 77	IOVDD	I/O ring power supply	S		3.3	
Analogue pins						
38	AIN_1	ADC positive input	I	Analog		
39	AINB_1	ADC negative input	I	Analog		
41	AIN_2	ADC positive input	I	Analog		
42	AINB_2	ADC negative input	I	Analog		
Analogue power pins						
36, 44	AVDD12	ADC analog supply	S		1.2	
48	AVDD33	ADC analog supply	S		3.3	
37, 40, 43, 47	AGND	ADC analog ground	S		0	

4 Demodulator Functional Description

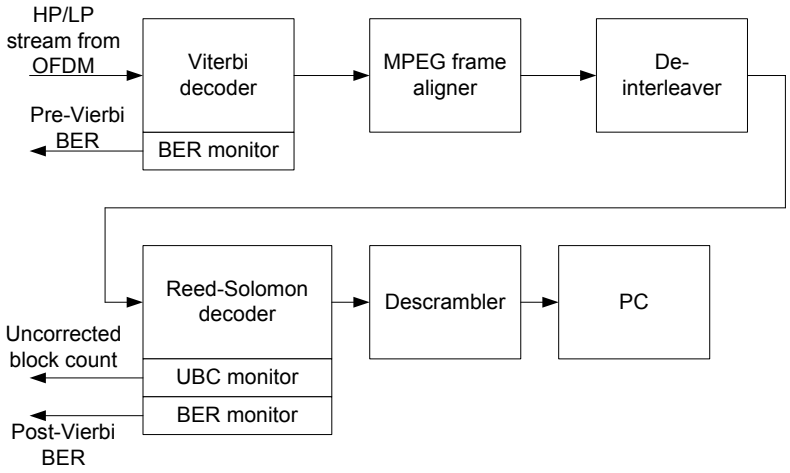
A functional block diagram of the CE6251 OFDM demodulator is shown in Figure 4. This accepts an IF analogue signal and delivers a stream of demodulated soft decision data to the on-chip Viterbi decoder. Clock, timing and frequency synchronization operations are all digital and there are no analogue control loops except the AGC. The frequency capture range is large enough for all practical applications. This demodulator has novel algorithms to combat impulse noise as well as co-channel and adjacent channel interference. If the modulation is hierarchical, the OFDM outputs both high and low priority data streams. Only one of these streams is FEC-decoded, but the FEC can be switched from one stream to another with minimal interruption to the transport stream.

Figure 4 OFDM demodulator diagram



The FEC module shown in Figure 5 consists of a concatenated convolutional (Viterbi) and Reed-Solomon decoder separated by a depth-12 convolutional de-interleaver. The Viterbi decoder operates on 5-bit soft decisions to provide the best performance over a wide range of channel conditions. The trace-back depth of 128 ensures minimum loss of performance due to inevitable survivor truncation, especially at high code rates. Both the Viterbi and Reed-Solomon decoders are equipped with bit-error monitors. The former provides the bit error rate (BER) at the OFDM output. The latter is the more useful measure as it gives the Viterbi output BER. The error collecting intervals of these are programmable over a very wide range.

Figure 5 FEC block diagram



The FSM controller shown in Figure 4 controls both the demodulator and the FEC. The controller facilitates the automated search of all parameters or any sub-set of parameters of the received signal. This mechanism provides the fast channel scan and acquisition performance, whilst requiring minimal software overhead in the host driver.

The algorithms and architectures used in the CE6251 have been optimized to minimize power consumption.

4.1 Analogue-to-Digital Converter

The CE6251 has a high performance 10-bit analogue-to-digital converter (ADC) which can sample a 6, 7 or 8 MHz bandwidth OFDM signal, with its spectrum centred at:

• 36.17 MHz IF

• 43.75 MHz IF

• 5 - 10 MHz near-zero IF

An on-chip programmable phase locked loop (PLL) is used to generate the ADC sampling clock. The PLL is highly programmable allowing a wide choice of sampling frequencies to suit any IF frequency, and all signal bandwidths.

4.2 Automatic Gain Control

An AGC module compares the absolute value of the digitized signal with a programmable reference. The error signal is filtered and is used to control the gain of the amplifier. A sigma-delta modulated output is provided, which has to be RC low-pass filtered to obtain the voltage to control the amplifier.

The bandwidth of the AGC is set to a large value for quick acquisition then reduced to a small value for tracking.

The AGC is free running during OFDM channel changes and locks to the new channel while the tuner lock is being established. This is one of the features of CE6251 used to minimize acquisition time. A robust AGC lock mechanism is provided and the other parts of the CE6251 begin to acquire only after the AGC has locked.

4.3 IF to Baseband Conversion

Sampling a 36.17 MHz IF signal at 45 MHz results in a spectrally inverted OFDM signal centred at approximately 8.9 MHz. The first step of the demodulation process is to convert this signal to a complex (in-phase and quadrature) signal in baseband. A correction for spectral inversion is implemented during this conversion process. Note also that the CE6251 has control mechanisms to search automatically for an unknown spectral inversion status.

4.4 Adjacent Channel Filtering

Adjacent channels, in particular the Nicam digital sound signal associated with analogue channels, are filtered prior to the FFT.

4.5 Interpolation and Clock Synchronisation

CE6251 uses digital timing recovery and this eliminates the need for an external VCXO. The ADC samples the signal at a fixed rate, for example, 45.0 MHz. Conversion of the 45.0 MHz signal to the OFDM sample rate is achieved using the time-varying interpolator. The OFDM sample rate is 64/7 MHz for 8 MHz and this is scaled by factors 6/8 and 7/8 for 6 and 7 MHz channel bandwidths. The nominal ratio of the ADC to OFDM sample rate is programmed in a CE6251 register (defaults are for 45 MHz sampling and 8 MHz OFDM). The clock recovery phase locked loop in the CE6251 compensates for inaccuracies in this ratio due to uncertainties of the frequency of the sampling clock.

4.6 Carrier Frequency Synchronisation

There can be frequency offsets in the signal at the input to OFDM, partly due to tuner step size and partly due to broadcast frequency shifts, typically 1/6 MHz. These are tracked out digitally, up to 1 MHz in 2 K and 8 K modes, without the need for an analogue frequency control (AFC) loop.

The default frequency capture range has been set to ±286 kHz in the 2 K and 8 K mode. However, these values can be increased, if necessary, by programming an on-chip register (CAPT_RANGE). It is recommended that a larger capture range be used for channel scan in order to find channels with broadcast frequency shifts, without having to adjust the tuner. After the OFDM module has locked (the AFC will have been previously disabled), the frequency offset can be read from an on-chip register.

4.7 Symbol Timing Synchronisation

This module computes the optimum sample position to trigger the FFT in order to eliminate or minimize inter-symbol interference in the presence of multi-path distortion. Furthermore, this trigger point is continuously updated to dynamically adapt to time-variations in the transmission channel.

4.8 Fast Fourier Transform

The FFT module uses the trigger information from the timing synchronization module to set the start point for an FFT. It then uses either a 2 K or 8 K FFT to transform the data from the time domain to the frequency domain. An extremely hardware-efficient and highly accurate algorithm has been used for this purpose.

4.9 Common Phase Error Correction

This module subtracts the common phase offset from all the carriers of the OFDM signal to minimize the effect of the tuner phase noise on system performance.

4.10 Channel Equalisation

This consists of two parts. The first part involves estimating the channel frequency response from pilot information.

Efficient algorithms have been used to track time-varying channels with a minimum of hardware.

The second part involves applying a correction to the data carriers based on the estimated frequency response of the channel. This module also generates dynamic channel state information (CSI) for every carrier in every symbol.

4.11 Impulse Filtering

CE6251 contains several mechanisms to reduce the impact of impulse noise on system performance.

4.12 Transmission Parameter Signalling (TPS)

An OFDM frame consists of 68 symbols and a superframe is made up of four such frames. There is a set of TPS carriers in every symbol and all these carry one bit of TPS. These bits, when combined, include information about the transmission mode, guard ratio, constellation, hierarchy and code rate, as defined in ETS 300 744. In addition, the first eight bits of the cell identifier are contained in even frames and the second eight bits of the cell identifier are in odd frames. The TPS module extracts all the TPS data, and presents these to the host processor in a structured manner.

4.13 Diversity Combiner

This CE6251 combines the received diversity data with the channel-corrected data from its own OFDM demodulation process. The resulting data is passed to the FEC logic to generate an MPEG transport stream, refer to Figure 7 Diversity operation.

Two methods are available for diversity combining OFDM data carriers. The default method is Maximum Ratio Combining, in which carriers are summed after being weighted by their SNR. The other method is Switched Combining, in which the carrier with the higher SNR is chosen as output.

4.14 De-Mapper

This module generates soft decisions for demodulated bits using the channel-equalized in-phase and quadrature components of the data carriers as well as per-carrier channel state information (CSI). The de-mapping algorithm depends on the constellation (QPSK, 16 QAM or 64 QAM) and the hierarchy (α = 0, 1, 2 or 4). Soft decisions for both low- and high-priority data streams are generated.

4.15 Symbol and Bit De-Interleaving

The OFDM transmitter interleaves the bits within each carrier and also the carriers within each symbol. The de-interleaver modules consist largely of memory to invert these interleaving functions and present the soft decisions to the FEC in the original order.

4.16 Viterbi Decoder

The Viterbi decoder accepts the soft decision data from the OFDM demodulator and outputs a decoded bit-stream.

The decoder does the de-puncturing of the input data for all code rates other than 1/2. It then evaluates the branch metrics and passes these to a 64-state path-metric updating unit, which in turn outputs a 64-bit word to the survivor memory. The Viterbi decoded bits are obtained by tracing back the survivor paths in this memory. A trace-back depth of 128 is used to minimize any loss in performance, especially at high code rates. The decoder re-encodes the decoded bits and compares these with received data (delayed) to compute bit errors at its input, on the assumption that the Viterbi output BER is significantly lower than its input BER.

4.17 MPEG Frame Aligner

The Viterbi decoded bit stream is aligned into 204-byte frames. A robust synchronization algorithm is used to ensure correct lock and to prevent loss of lock due to noise impulses.

4.18 De-interleaver

Errors at the Viterbi output occur in bursts and the function of the de-interleaver is to spread these errors over a number of 204-byte frames to give the Reed-Solomon decoder a better chance of correcting these. The de-interleaver is a memory unit which implements the inverse of the convolutional interleaving function introduced by the transmitter.

4.19 Reed-Solomon Decoder

Every 188-byte transport packet is encoded by the transmitter into a 204-byte frame, using a truncated version of a systematic (255,239) Reed-Solomon code. The corresponding (204,188) Reed-Solomon decoder is capable of correcting up to eight byte errors in a 204-byte frame. It may also detect frames with more than eight byte errors.

In addition to efficiently performing this decoding function, the Reed-Solomon decoder in CE6251 keeps a count of the number of bit errors corrected over a programmable period and the number of uncorrectable blocks. This information can be used to compute the post-Viterbi BER.

4.20 De-scrambler

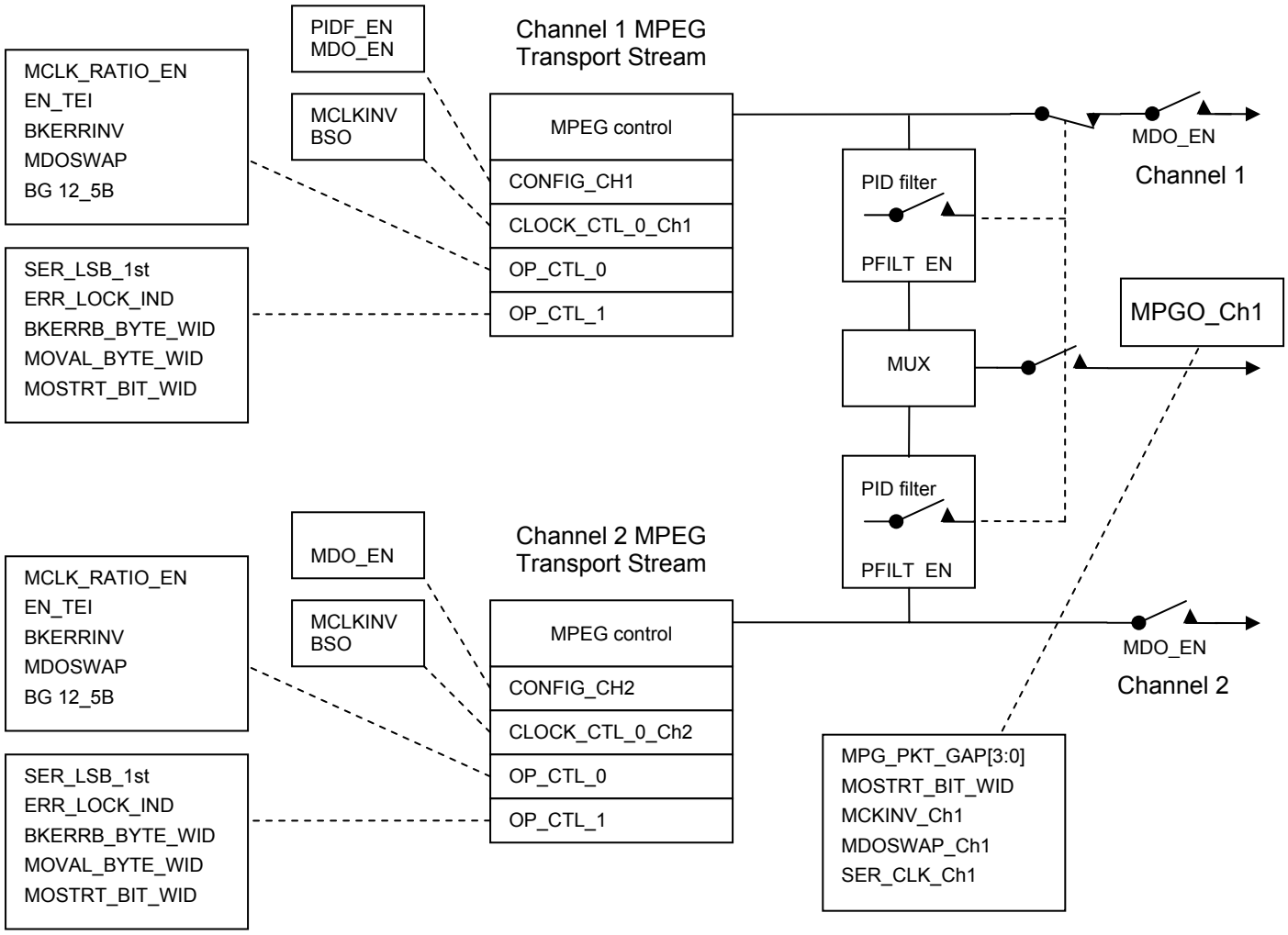
The de-scrambler de-randomizes the Reed-Solomon decoded data by generating the exclusive-OR of this with a pseudo-random bit sequence (PRBS). This outputs 188-byte MPEG transport packets. The TEI bit of the packet header may be set if required to indicate uncorrectable packets.

4.21 MPEG Transport Stream Interface and PID filters

MPEG data can be output in parallel or serial mode. The output clock frequency is automatically chosen to present the MPEG data as uniformly spaced as possible to the transport processor. This frequency depends on the guard ratio, constellation, hierarchy and code rate.

The MPEG output pins MDO(7:0), MOVAL, MOSTRT, MCLK and BKERRB shall be tristated in normal device operation when MDOENB is '1' (the default). The multiplexed output is enabled whenever the PID filters are enabled.

Figure 6 TS output control



4.22 PID Filter

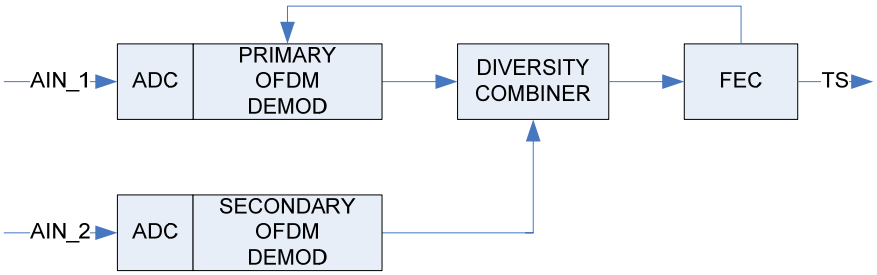
The packet identifier filter has 2 main functions. It filters out unwanted MPEG data by discarding MPEG packets that do not have a valid PID. By reducing the total amount of MPEG data packets, the two channels of the dual demodulator can be output on a single MPEG stream. In order for the MPEG processor to determine which channel the packet has come from, the PID values in each channel may be modified, to ensure they have a unique PID.

Notes:

- The PID filter handles 2 data streams, one for each DVB-T demodulator.
- The PID filter function is controlled from channel 1 only.
- Bit 0 (PF1_EN) and 1 (PF2_EN) of PFILT_EN_Ch1 must both be set to 1 for PID filtering to take place.
- The multiplexed MPEG output is enabled whenever the PID filters are enabled.
- The channel 1 MPEG output is disabled whenever the PID filters are enabled but channel 2 MPEG output will continue to be output unless turned off through MDO_EN.
- The multiplexed MPEG output can be either serial or parallel, set by SER_CLK_Ch1 in MPGO_Ch1 register.
- The normal, non multiplexed, MPEG outputs can also be serial or parallel BUT if the PID filters are to be used the outputs MUST be set to parallel.

4.23 Diversity operation

Figure 7 Diversity operation



Diversity reception is a receiving process that combines more than one received signal to obtain a better result than that obtained from using just one signal. The diversity technique used by the CE6251 is called spatial diversity, and relies on two antennas receiving the same broadcast signal. The two antennas must be spaced apart by a distance that is significant when compared to the wavelength of the RF signal that is being received. This is so that the signals from each antenna suffer different impairments, but the combination can yield acceptable results.

The diversity combining technique used in the CE6251 is called Maximum Ratio Combining (MRC) and is the optimum technique that can be employed. This combination of the signals occurs immediately after the FFT block in the demodulator, before the Viterbi and Reed-Solomon forward error correction (FEC) blocks (see Figure 2). The secondary demodulator supplies the output information from its FFT block to a circuit in the primary demodulator which combines this information with its own FFT data and passes the resulting information to the Viterbi block within the primary demodulator.

The operations of the Intel DVB-T demodulators are internally controlled by a state machine. This significantly reduces the software overhead required by the device driver. During acquisition, first the symbol synchronisation has to be achieved. Then the FFT block is aligned in terms of frequency. Once this is achieved the Viterbi block can start synchronisation. In a diversity application, the state machine in the primary demodulator will start to acquire Viterbi lock when the FFT block in either the primary or secondary channel has achieved symbol lock and frequency lock.

The quality of the signal present at the input to the primary channel necessary to achieve FFT lock does not have to be high. Indeed, a signal with a carrier to noise ratio of 0dB is sufficient, and will also provide TPS information from either the primary or secondary demodulator.

5 Electrical characteristics

Test conditions unless otherwise stated.
Tamb = 0 - 80ºC, Vdd = 3.3V ± 10% and 1.2 ± 5%

5.1.1 Recommended Operating Conditions

Table 5.1 Recommended operating conditions

Symbol	Parameter		Min	Typ	Max	Units
VDD	Power supply voltage:	periphery	3.0	3.3	3.6	V
CVDD		core	1.14	1.2	1.26	V
IDD_P	Power supply current:	periphery[1]		1		mA
IDD_C		core		210		mA
XTI	Crystal frequency		- 100ppm	20.48	+ 100ppm	MHz
T_{amb}	Ambient operating temperature		-10	-	80	ºC
Rja	Theta-JA (θJA), Still Air [3]			38		ºC /W

[1] Current from the 3.3 V supply will be mainly dependent on the external loads.
[2] Current given is for optimum performance, lower current is possible with reduced performance.
[3] Theta-JA (θJA) is the junction-to-ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

5.1.2 Absolute Maximum Ratings

Table 5.2 Absolute maximum ratings

Symbol	Parameter		Min	Max	Units
VDD	Power supply voltage:	periphery	-0.3	3.6	V
CVDD		core	-0.3	1.26	V
V_I	Voltage on input pins (5 V rated)		-0.3	5.5	V
V_I	Voltage on input pins (3.3 V rated)		-0.3	VDD + 0.3	V
V_O	Voltage on input pins (5 V rated)		-0.3	5.5	V
V_O	Voltage on input pins (3.3 V rated)		-0.3	VDD + 0.3	V
T_{STG}	Storage temperature		-55	150	ºC
T_{OP}	Operating ambient temperature		-40	85	ºC
T_J	Junction temperature		-	125	ºC

Note: Stresses exceeding these listed under absolute maximum ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

5.1.3 DC Electrical Characteristics

Table 5.3 DC electrical characteristics

Symbol	Parameter	Conditions	Pins	Min	Typ	Max	Units
VDD	Operating voltage: periphery			3.0	3.3	3.6	V
CVDD	core			1.14	1.2	1.26	V
IDD_C	Supply current	1.14>CVDD>1.26			210		mA
Outputs							
V_{OH}	Output levels	IOH 2mA 3.0>VDD>3.6	MDI(7:0), MIVAL, MISTRT, MCLK, SLEEP	-	-	-	V
V_{OL}		IOIOL 2mA 3.0>VDD>3.6		-	-	0.4	V
V_{OL}		IOL 6mA 3.0>VDD>3.6	GPP(7:0), DATA(1:3), CLK1, CLK2,AGC1, AGC2,	-	-	0.4	V
	Output capacitance	Not including track	MDI(7:0), MIVAL, MISTRT, MCLK,	3.0	3.0	-	pF
			GPP(7:0), DATA(1:3), CLK1, CLK2, AGC1, AGC2,	3.6	3.6	-	pF
I_{LZ}	Output leakage current (tri-state)			-	-	1	µA
Inputs							
V_{IH}	Input levels	3.0>VDD>3.6 -0.5 ≥ Vin ≥ VDD+0.5V	MICLK,	-	-	-	V
V_{IH}	Input levels	3.0>VDD>3.6 -0.5 ≥ Vin ≥ +5.5V	GPP(3:0), CLK3, DATA1, IRDI, SCK, ADFMT, RESETB, SCK	-	-	-	V
V_{IL}	Input levels	3.0>VDD>3.6	All inputs	-	-	0.8	V
	Input leakage current	Capacitances do not include track	SLEEP, MICLK, CLK1, CLK2	-	-	+1	µA
	Input capacitance			1.8	1.8	-	pF
	Input capacitance		DATA(1:3), GPP(7:0)	3.6	3.6	-	pF
T_{RESET}	Reset Time after Valid Power	Vcc MIN = 3.0V			50		ms

5.1.4 Crystal specification

Parallel resonant fundamental frequency (preferred)	20.48 MHz
Tolerance overall, including frequency accuracy and over temperature	± 100ppm
Equivalent series resistance (ESR)	40 Ohms typical
Typical load capacitance (CL)	10 pF Min, 30pF Max
Drive level	100 µW

Value of C1, C2 (parallel capacitors in the application) for an ESR of 40 Ohms – 27pF

6 Dynamic characteristics

Table 6.1 Digital input bus timing

Parameter	Min	Max	Units
Parallel mode TS MCLK frequency		12	MHz
Serial mode TS MCLK frequency		100	MHz
Parallel mode MDI/MIVAL/MISTART to MCLK setup time	5		ns
Parallel mode MDI/MIVAL/MISTART to MCLK hold time	8		ns
Serial mode MDI(0)/MIVAL/MISTART to MCLK setup time	1		ns
Serial mode MDI(0)/MIVAL/MISTART to MCLK hold time	5		ns

7 Mechanical

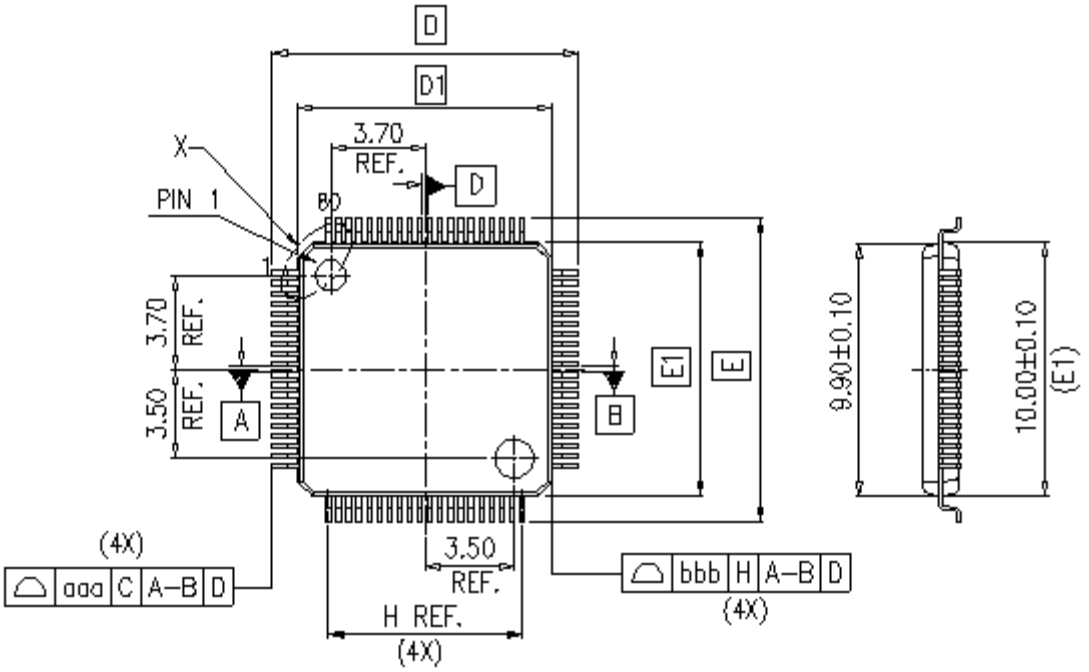
7.1.1 Package Dimensions

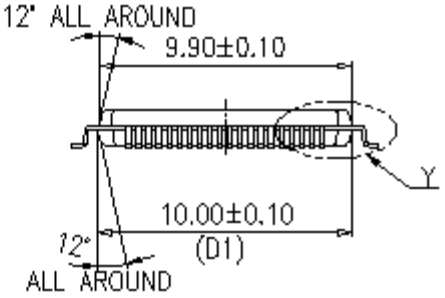
DIMENSION LIST (FOOTPRINT: 2.00)

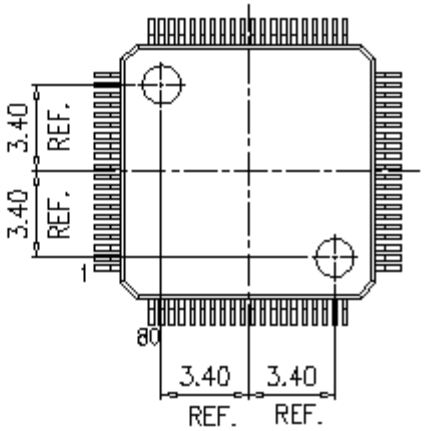
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A1	0.100±0.050	STANDOFF
3	A2	1.400±0.050	PKG THICKNESS
4	D	12.000±0.200	LEAD TIP TO TIP
5	D1	10.000±0.100	PKG LENGTH
6	E	12.000±0.200	LEAD TIP TO TIP
7	E1	10.000±0.100	PKG WIDTH
8	L	0.600±0.150	FOOT LENGTH
9	L1	1.000 REF.	LEAD LENGTH
10	T	$0.150^{+0.05}_{-0.06}$	LEAD THICKNESS
11	T1	0.127±0.030	LEAD BASE METAL THICKNESS
12	α	0°~7°	FOOT ANGLE
13	b	0.180±0.050	LEAD WIDTH
14	b1	0.160±0.030	LEAD BASE METAL WIDTH
15	e	0.400 BASE	LEAD PITCH
16	H (REF.)	(7.600)	CUM. LEAD PITCH
17	aaa	0.200	PROFILE OF LEAD TIPS
18	bbb	0.200	PROFILE OF MOLD SURFACE
19	ccc	0.080	FOOT COPLANARITY
20	ddd	0.080	FOOT POSITION

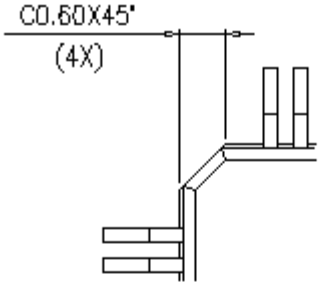
NOTES :

S/N	DESCRIPTION		SPECIFICATION
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXPECT EJECTION AND PIN 1 MARKING.		Ra0.8~2.0um
3	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):		MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):		MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
7	COMPLIANT TO JEDEC STANDARD: MS-026		

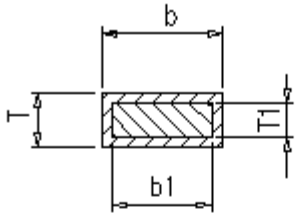

D
D1
3.70
REF.
D
X
PIN 1
80
1
3.70
REF.
3.50
REF.
A
B
E1
E
9.90±0.10
10.00±0.10
(E1)
(4X)
aaa C A–B D
3.50
REF.
H REF.
(4X)
bbb H A–B D
(4X)


12° ALL AROUND
9.90±0.10
Y
10.00±0.10
(D1)
12°
ALL AROUND

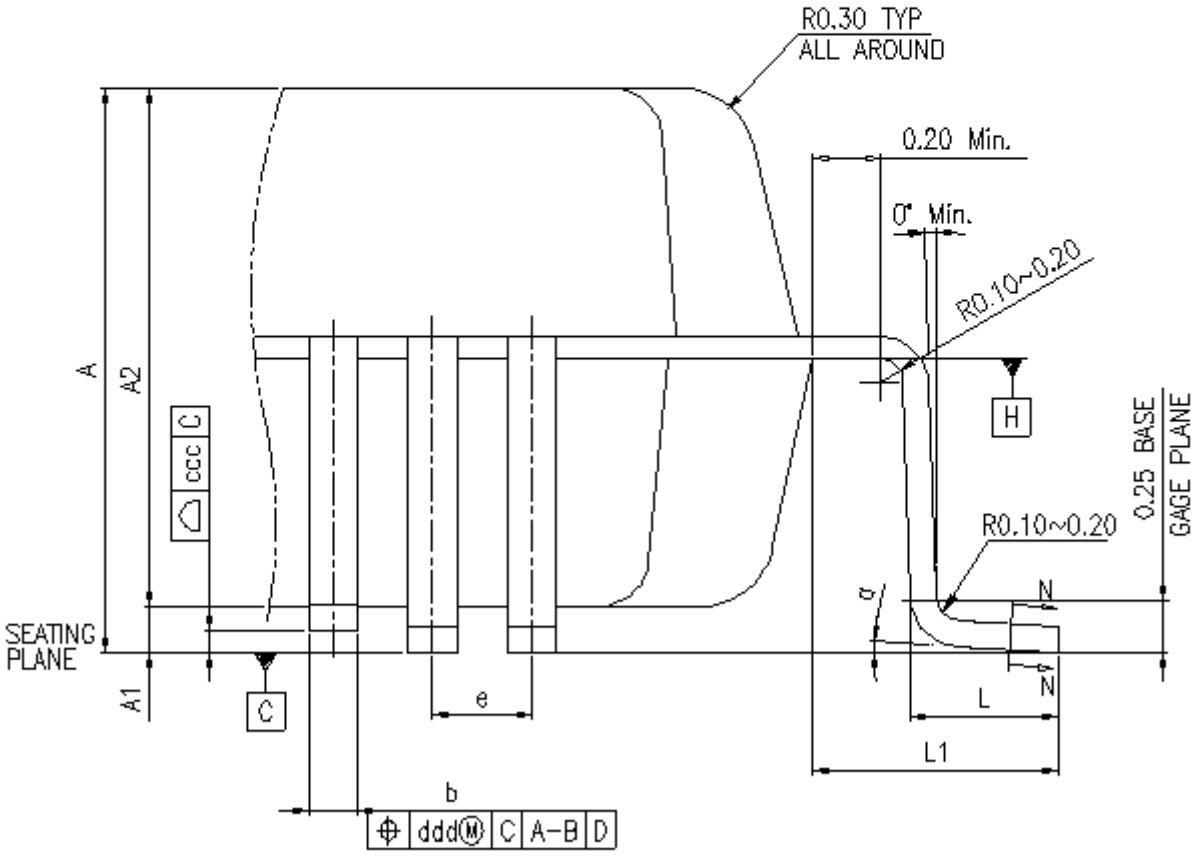

3.40
REF.
3.40
REF.
1
80
3.40
REF.
3.40
REF.



DETAIL X



SECTION N-N



DETAIL Y