How to Measure RDRAM* System Clock Jitter

Application Note AP- 667

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Contents

Revision History

Rev.	Draft/Changes	Date
- 001	• Initial Release	March 1999
- 002	• Section 1, detail 4: Typographical error. "0.1 uF capacitors are better than …" • Section 3, details 1-2: Added information regarding additional LeCroy and Tektronix jitter measurement equipment. • Section 7, table 2: Increased allowable channel jitter to component +/- 50 pS • Section 7, table 2: Added 355.5 MHz component and channel jitter specification • Section 7, detail 3: Changed to reflect +/- 50 pS channel adder.	June 1999

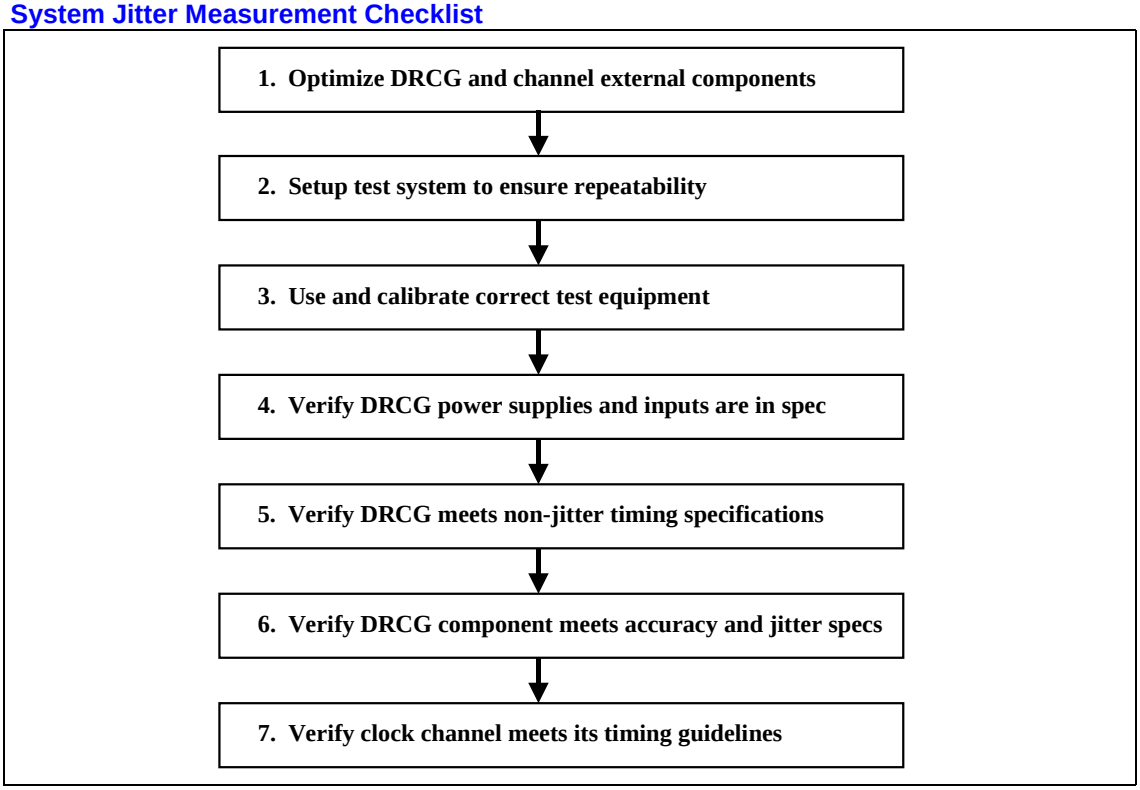
Introduction

Making optimal system level jitter and timing measurements within the RDRAM* channel is difficult. The intent of this applications note is to document a “best known method” (BKM) for making repeatable and accurate timing measurements for the Direct Rambus Clock Generator (DRCG) and derivative devices. This is not the only method to produce satisfactory results, but provides a solid set of guidelines and baseline information to make the measurement and validation task easier.

The flow chart below has been broken into seven specific tasks to simplify the process. It is recommended that the entire process be reviewed before making critical timing measurements. Skipping, or incorrectly completing, any of the steps leads to an apparent loss of critical timing margin for the clocks. The magnitude of induced “operator error” varies from ones of pS to as high as 30 pS in some systems.

Successfully completing steps 1-6 will "validate" the DRCG clock component in your system configuration. However, all system timing is measured within the channel and not at the DRCG component. Step 7 is a required, critical gauge to determine if the clock channel routing implementation is satisfactory.

Figure 1: System Jitter Measurement Checklist



1. Optimize DRCG and Channel External Components

It must be noted that all system boards are different when it comes to clock jitter. The following DRCG decoupling scheme has been shown to be successful on multiple boards. However, it may not be the optimal solution for all system layouts.

Figure 2: External DRCG Components

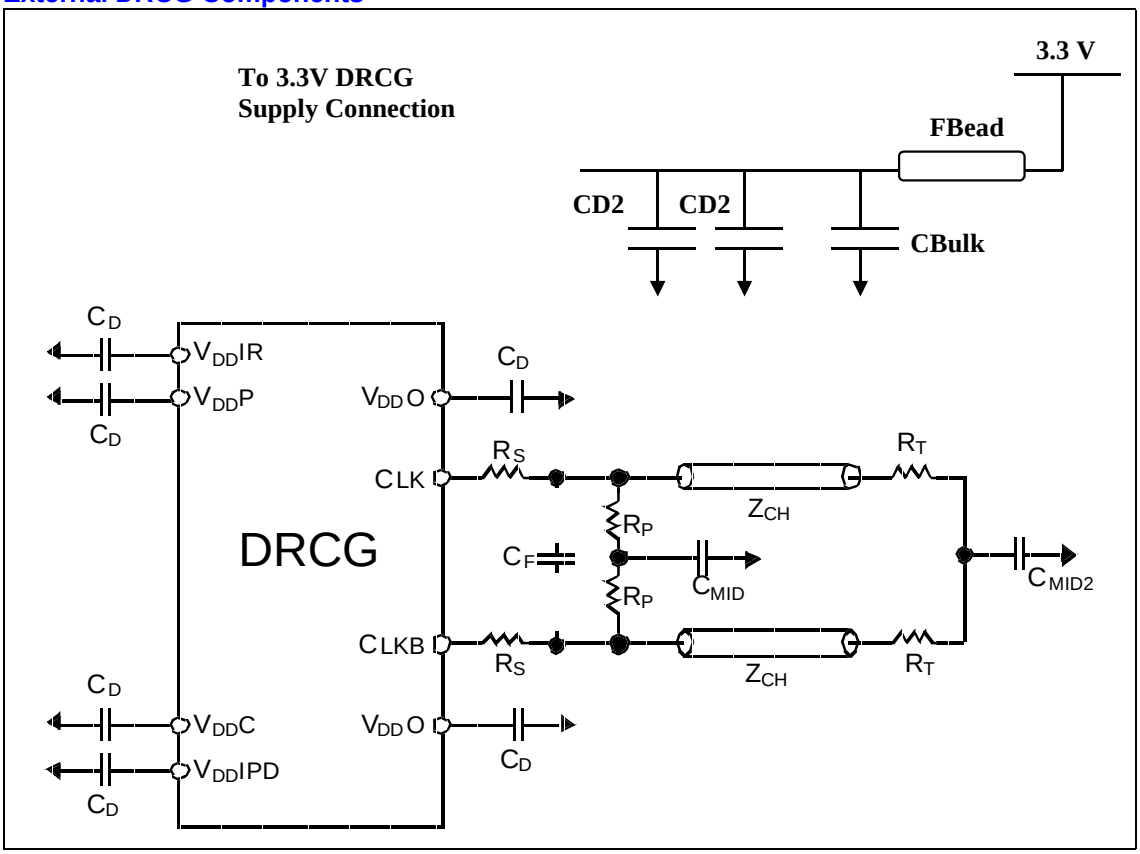


Table 1: External DRCG Components

Component	Nominal Value	Notes
C_D	0.1 uF	Decoupling caps to ground
R_S	39 Ohms	Series termination resistor
R_P	51 Ohms	Parallel termination resistor
C_{MID}, C_{MID2}	0.1 uF	Virtual ground caps
R_T	27 Ohms	End of channel termination
C_F	4 – 15 pF	Do not stuff, leave pads for future use
FBead	50 Ohms @ 100MHz	Ferrite bead
CD2	0.1 uF	Additional 3.3V decoupling caps
CBulk	10 uF	Bulk cap on device side of ferrite bead

Details:

1. Note the removal of the original EMI capacitors between the junctions of R_S, R_P and ground. These capacitors had minimal impact on EMI and increased DRCG output jitter by approximately 2X.

2. The intent of component C_F is to decouple CLK and CLKB outputs to each other, but early data shows this actually increases device jitter. C_F should not be stuffed at this time.

3. The ferrite bead and 10 uF bulk cap combination improves jitter and helps to keep the clock noise away from the rest of the system. The additional 3.3V capacitors (CD2) have a minor positive impact, but the ideal values have not been extensively optimized. There is a possibility that one or both CD2 caps can be removed in future board revisions.

4. 0.1 uF capacitors are better than 0.01 uF or 0.001 uF caps for DRCG decoupling. Most decoupling experiments that replaced 0.1 uF caps with higher frequency caps ended up with the same or worse jitter. Replacing existing 0.1 uF caps with higher frequency caps is not advised.

5. C_{mid} at 0.1 uF has improved jitter versus C_{mid} at 100 pF. However, this will increase the latency coming out of a stopclock or tri-state mode.

6. R_S, R_P, R_T were modified to improve channel signal integrity through increasing CTM/CTMN swing.

2. Setup Test System to Ensure Repeatability

A key issue in clock validation is repeatability. Hardware supplier, software, probe position, and scope calibration are just a few of the system variables which make test repeatability difficult. To properly choose which clock device or decoupling solution is best, one must reduce all system variables to one, take data for both and compare. Careful documentation on all system and software setups for all validation tests is strongly encouraged.

Details:

1. Prepare system validation hardware and software to assure repeatable results. Document all hardware and software variables to remove ambiguity.

2. Verify system BIOS provides adequate time for all system clock devices to stabilize. This time will vary according to system implementation, but should be at least 6 mS to allow the DRCG PLL and the phase aligner to become stable. Record the BIOS version/release date to minimize confusion later.

3. Put board and system components in a metal chassis or similar probe station that approximates a typical system. Make sure power supply ground is not floating and is electrically connected to the board ground. A power supply not electrically grounded to the board will still boot, but will have as much as 7 Ohms between supply and board ground.

4. Document exact configuration specifics such as vendor, device count and location of RIMM and continuity RIMM modules. If possible, number the modules to simplify.

5. Mark appropriate probe points and grounds on the board to avoid confusion later. If possible, mark CLK, CLKB and ground with separate colors. All DRCG and channel probe points were vias on the backside of the system board under test.

6. Use a razor blade to carefully remove soldermask material from all via probe points to expose copper to make a reliable connection.

7. Boot system with a repeatable hardware and software condition for both "quiet" and "noisy" systems. DOS mode is an accepted repeatable software condition to test clocks in a low system noise condition. Many third party software programs (applications or games) will create large system noise conditions, but do not provide repeatable results when system variables (such as memory configuration) are changed. Use a program that directly accesses the memory controller and configure to provide repeatable "worst case" system noise.

8. Double-check that the processor and RIMM modules are firmly placed in sockets before proceeding. Removing and re-seating memory or CPU components eliminates most boot abnormalities.

9. If available, use a BIOS post card to verify completion of post routines.

3. Use and Calibrate Correct Test Equipment

Using incorrect test equipment or failing to calibrate correctly will result in erroneous results. The following test equipment if used properly, should be adequate.

Details:

1. Intel's system level clock validation has been done using a combination of a HP54720D (2 channels @ 4 GSamples/sec), a HP Infinium scope (2 channels @ 8 GSamples/sec) and version 2.06 of Amherst Systems M1 jitter software package. Other sources of clock jitter measurement equipment are available from LeCroy (2 channels @ 4 GSamples/sec , 1 channel @ 8 Gsamples/sec) and Tektronix (4 channels @ 10 GSamples/sec). Each program requires an extra, supplier-provided, "jitter-specific" software package that runs resident on the scope (LeCroy-JTA, Tektronix-TDSJIT1.)

2. Intel has used HP's 2.5 GHz active probes with "walking stick" grounds and the sharpest probe tips available. The 5470D and the Infinium scope use essentially the same probe, but the Infinium probe form factor is different. The LeCroy scope also uses the 54720D probes if the proper HP probe power source is used. . Addtionally, the Tektronix scope has a 1.7 GHz differential probe available which will simplify multi-channel measurements.

3. Use probe-holders that will reduce the physical movement of probes. It is not recommended to make any critical differential measurements without using probe holders. An example of a probe holder is the "EZ-Probe" by Cascade Microtech or Articulating Arm by Tektronix.

4. There has been no effort to investigate the accuracy impact of soldering wires or fixed probe points to the system under test. All measurements were made with active probes only.

5. Turn scope on and let warm up for ≅20 minutes before any measurements or calibrations. If channels can be calibrated (as in HP54720), calibrate using the channel best calibration mode after the warm up period. Do NOT do a frame calibration, as it is a factory-only calibration mode.

6. Voltage calibrate the active probes by using the calibration method for each channel. Once calibrated, do not remove or swap probes.

7. Deskew probes by placing both probes on a known output signal with a greater that 1 V/nS edge-rate and < 250 pS of jitter. A properly terminated CK133 output is acceptable. Do NOT use the calibration signal from the scope as it's edge rate is slow enough to add noise to the calibration. Turn off any interpolation filters within the scope and use only the real data points. Align the data points for both channels by adjusting the relative skew for one channel. Turn all interpolation filters back on after channels are de-skewed.

8. Use highest available sampling rate for measurement.

9. Adjust scope to allow largest signal on display without crossing upper or lower boundary. Center the offset voltage to the middle of the screen for both channels. Make sure both channels use exactly the same vertical scaling per division and same offset. Use infinite persistence mode to verify min/max excursions. Allow at least one half vertical division margin on both top/bottom.

10. When probing differential signals, take care to probe at similar angles for CLK and CLKB to maintain a consistent probe tip connection for both signals. Come in at a 30-60 Degree angle and avoid probing perpendicular to the board.

11. When possible, connect both probe grounds to the SAME ground via for both CLK and CLKB. Ideally, this ground point will be equidistant from both signals. Using this common ground has reduced jitter by 10-20pS on some systems under test.

4. Verify DRCG Power Supplies and Inputs Are In Spec

It is unlikely that the DRCG will meet all of its datasheet specifications unless the board implementation provides "clean" power and inputs. One must verify that the DRCG power supplies, input signals and select pins meet component specifications before proceeding. If using spread spectrum clocking (SSC) additional testing must be done to verify the clock providing the spread spectrum is in specification.

Details:

1. Measure as close to the DRCG pins as possible and make sure to use a low inductance ground probe for all measurements

2. Measure all three different DRCG supply voltages. Specifications are +/- 5% for VddP, VddC, VddO (3.3V), VddIR (2.5V), and VddIPD (1.8V.) Note frequency components and peak-peak values of the spikes. Improve supply decoupling by using additional capacitors and/or ferrite beads until power supply voltages meet component specifications.

3. Characterize the DRCG input reference signal (Refclk) by measuring as close to Pin2 as possible. Measure rise/fall time, min/max period, duty-cycle and cycle-cycle jitter at nominal VddIR/2 (1.25V if using CK133 or similar.) Revise CK133 decoupling capacitors and/or termination scheme until DRCG Refclk meets component specifications.

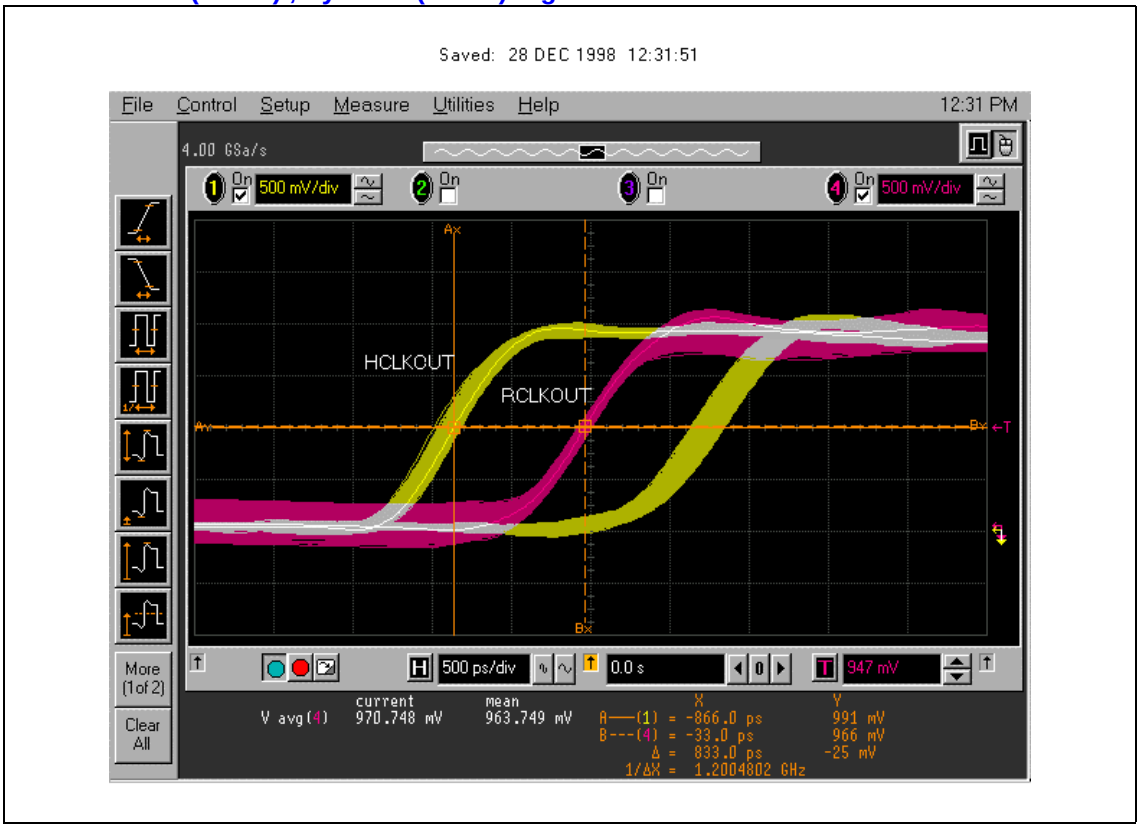
4. Verify spread spectrum clocking is disabled/enabled as desired by looking at min/max period and average period over time using a jitter analysis tool for the Refclk input.

5. Verify that PclkM, SynclkN rise/fall times exceed 1V/nS between 20-80% (of VddiPD nominal voltage) measure points. Measure as close to DRCG input pins as possible. Modify chipset output termination scheme until PclkM, SynclkN rise/fall times meet component specifications.

6. Note that PclkM, Synclk inputs will NOT be <100 pS apart as unclearly defined in DRCG component specification. Put scope on infinite persistence, trigger on RCLKOUT and verify the bimodal distribution of PclkM (HCLKOUT) around SynclkN (RCLKOUT). See Figure 3 below. If triggering on PclkM, the edges will be reversed.

7. Verify remaining DRCG input control voltages are as expected and meet the DRCG component specification.

Figure 3: Correct PclkM (HCLK) , SynclkN (RCLK) Signals



5. Verify DRCG Meets Non-Jitter Timing Specifications

One must verify the DRCG meets all its non-jitter timing specifications before measuring jitter. All measurements are done at the component at the junction of the RS and RP resistors.

Details:

1. Probe at junction of series and parallel termination resistors for both CLK and CLKB. The probes should be on the channel side of the series termination resistor. Connect probe grounds as close to the signals and equidistant to each other. If possible, connect both grounds to the same ground pad or via. Visually verify that probe and ground have good connection and have not moved due to board flex.

2. Verify frequency of operation, VOH, VOL, crossing point, and rise/fall time. Note requirement to validate all clock parameters on BOTH edges of the CLK and CKB.

3. Examine worst case conditions for each parameter. Changing the number of devices in the channel as well as software changes will have an impact on the parameters.

6. Verify DRCG Accuracy and Jitter Timing Specifications

The non-jitter timing specifications in #5 can be measured using only a scope. However, the remaining DRCG parameters must be measured with a jitter/timing analysis tool. Cycle-to-cycle jitter (single and multiple cycles) and short-term duty cycle can't be done accurately any other way. Period accuracy measurements and long-term duty cycle data falls out of the jitter analysis as well.

Details:

1. Verify scope is in real-time mode and measure jitter using jitter analysis package or program. Verify waveform voltage is optimized for horizontal scale as per test equipment discussion above.

2. Note that DRCG jitter is measured at the crossing points for BOTH the rising and falling edge of CLK. Earlier information that stated that only the jitter on the falling edge of CLK was INCORRECT. System level jitter needs to be verified on both crossing points to ensure proper RDRAM DLL operation. Even though all system level timing is referenced to the falling edge of the CLK output, all DRCG timings must be verified on BOTH edges. Figure 4 shows valid falling edge cycles (A1, A2) as well as valid rising edge cycles (B1, B2) for jitter measurements. Version 2.06 of the M1 jitter analysis package has a switch inside the measurement options that allows the user to change the measured edge (rising or falling) without physically swapping the probes.

3. Look at min/max and average periods over a few scope acquisitions to verify spread spectrum functionality is on or off as expected.

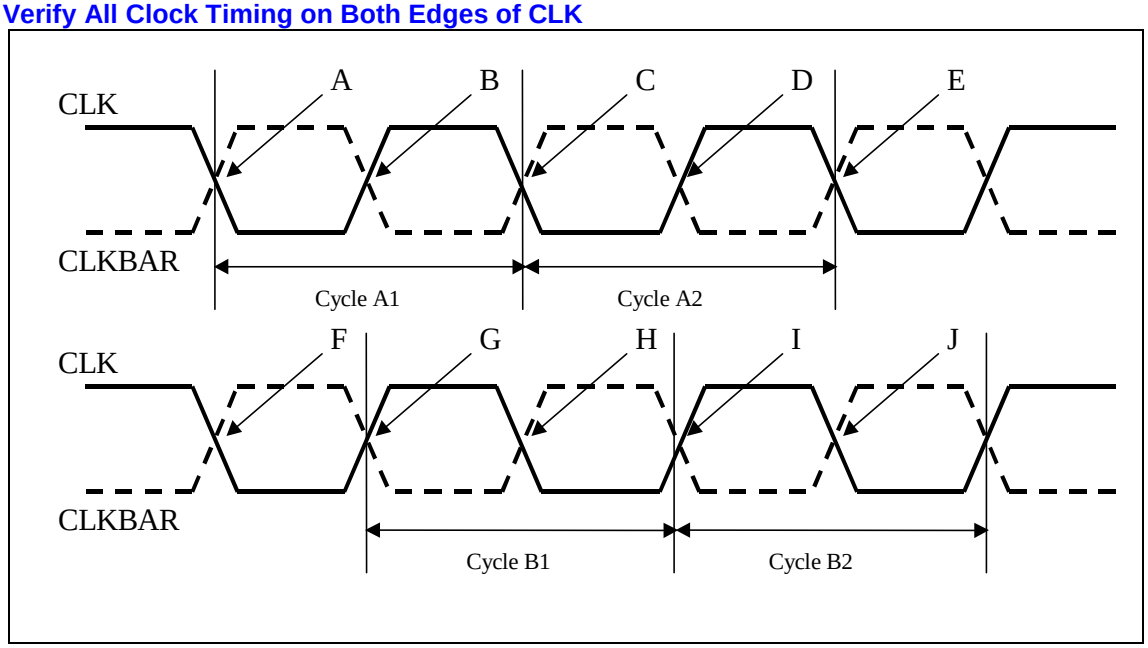
4. Make multiple scope acquisitions to get feel for component performance versus system and software configuration. Focus probe placements and waveform scaling to get minimized, repeatable single cycle data before recording multiple cycle data. Remember that the worst case result is the larger of the + or – maximum displacement values. Don't forget to characterize jitter in a quiet system (DOS) and use acceptable software to run worst case data patterns in the channel.

5. After single cycle data is acceptable and repeatable, verify multiple cycle jitter for the same system variables. Note that worst case single cycle data does NOT guarantee worst case multiple cycle data.

6. Change system variables such as frequency, memory configuration and software.

7. Short-term duty cycle is measured on M1 system by using Pulsewidth + feature.

Figure 4:Verify All Clock Timing on Both Edges of CLK



7. Verify Clock Channel Meets Its Timing Guidelines

After completing steps 1-6, the DRCG component has been "validated" in the system. However, all the channel timing parameters are measured in the channel itself and not at the DRCG output. A guideline de-rating for critical channel clock measurement points allows a small increase over jitter measured at the output of the DRCG. If the DRCG in the system (steps 1-6) passes its specs, but fails within the channel, there is a high possibility that the channel routing is not optimal. The clock channel validation (figure 5) can be minimized by looking at the CFM closest to the chipset (point "B") and the CFM after it exits the last RIMM at the end of the channel (point "C3"). However, point "C3"is the worst case channel measure point and, in reality, jitter is only meaningful at the end of the last RIMM that contains memory devices. Figure 5 shows alternate measure points "C2" and "C1" for various memory and continuity module positions. Information from these two measure points provides enough information to validate clock jitter performance through the channel.

Figure 5: Clock Channel Characterization Measure Points and Specifications

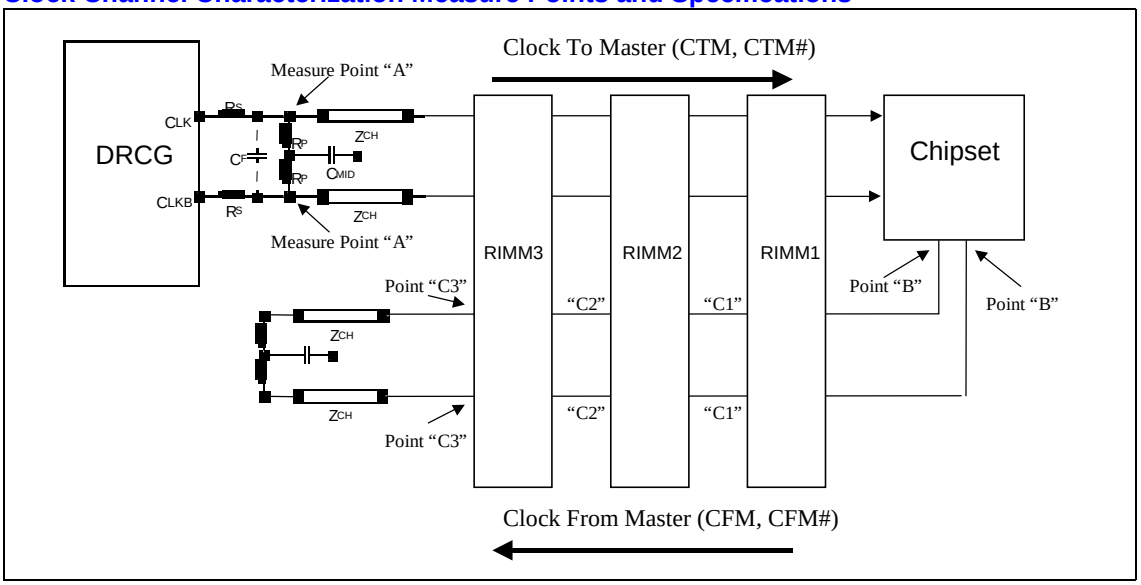


Table 2. Clock Channel Characterization Measure Points and Specifications

Measure Point	Jitter Specification and Channel Guidelines
DRCG Output ("A")	Same as component datasheet: +/- 50 pS @ 400 MHz +/- 60 pS @ 355.5 MHz +/- 70 pS @ 300 MHz
CFM @ Chipset ("B")	Add +/- 50 pS to component spec: +/- 100 pS @ 400 MHz +/- 110 pS @ 355.5 MHz +/- 120 pS @ 300 MHz
CFM @ Last RIMM ("C")	Add +/- 50 pS to component spec: +/- 100 pS @ 400 MHz +/- 110 pS @ 355.5 MHz +/- 120 pS @ 300 MHz

Details:

1. All measurement, probing and system issues are the same whether probing the output of the DRCG or measuring in the channel. Jitter measurements should be with respect to BOTH rising and falling edges of CLK.

2. It is recommended to measure "end of channel" jitter at the end of the last populated RIMM; rather than at point "C3", if continuity modules are placed in RIMM3 (or RIMMs 2 and 3.) Measurements have shown as high as 50 pS jitter adder measured at "C3" versus "C1" when RIMMs 2 and 3 contain continuity modules.

3. The additional 50 pS jitter guideline in the channel is frequency independent.

Summary

One can successfully characterize and validate a DRCG clock driver, or equivalent, by using the seven-step documented test procedure. The measurement guidelines and details are not new, but are best measurement practices that should be followed for all high precision measurements. Neglecting, or incorrectly following, these best known methods will add "operator error" to the jitter measurements, and will result in a significantly degraded, or failing clock design.