Intel® 810/810E Chipsets: GMCH Electrical and Thermal Specifications

Datasheet Addendum

January 31, 2000

Order Number: 298180 - 001

Contents

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Revision History

Rev.	Description	Date
-001	• Initial Release	January 31, 2000

1. Overview

This document covers the Electrical and Thermal Specifications (ETS) for the Graphics and Memory Controller Hub (GMCH) components for the Intel® 810 chipset and Intel® 810E chipset. The components covered are:

- Intel® 810 chipset: Intel® 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH)
- Intel® 810E chipset: Intel® 82810E Graphics and Memory Controller Hub (GMCH)

Information in this document that is not shaded applies to both devices.

Information that is shaded, as is shown here, indicates differences between the two devices.

1.1. Related Documents and References

- Intel® 810 Chipset: Intel® 82810/82810-DC100 Graphics and Memory Controller Hub (GMCH) Datasheet
- Intel® 810E Chipset: Intel® 82810E Graphics and Memory Controller Hub (GMCH) Datasheet
- Intel® Celeron™ Processor – Datasheets
- Intel® Pentium® II Processor Developer's Manual
- Intel® Pentium® III Processor Datasheets
- Intel® 810 Chipset Design Guide
- CK Whitney Clock Synthesizer / Driver Specification
- Intel® Celeron™ Processor I/O Buffer Models
- Whitney I/O Buffer Models rev 1.3 (IBIS Format)

2. Electrical Characteristics

Unused active low 3.3V tolerant inputs should be connected to 3.3V. Unused active high inputs should be connected to ground (VSS).

2.1. Absolute Maximum DC Ratings

Case Temperature under Bias ..... 0^{o}C to +105^{o}C
Storage Temperature ..... -55^{o}C to +150^{o}C
3.3V Supply Voltage with Respect to Vss (VCC) ..... -0.3 to + 4.3 V
1.8V Supply Voltage with Respect to Vss ..... -0.3 to + 2.5V

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "Operating Conditions" is not recommended and extended exposure beyond "Operating Conditions" may affect reliability.

2.2. Thermal Characteristics

The GMCH is designed for operation at case temperatures between 0^{o}C and 105^{o}C. For thermal considerations and guidelines, refer to the Intel® 810 Chipset Application Note #1, *Thermal Design and Considerations.*

2.3. Power Characteristics

Table 1. Power Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
P_{GMCH}	Total Chip Power Dissipation		4.0	W	
$V_{CC\_1.8}$	1.8V Supply Voltage	1.71	1.89	V	
$V_{CC\_3.3}$	3.3V Supply Voltage	3.14	3.46	V	
$V_{sus\_3.3}$	3.3V Standby Supply Voltage	3.14	3.46	V	
$I_{CC\_1.8}$	1.8V Power Supply Current		1.40	A	
$I_{CC\_3.3\_SM}$	3.3V Power Supply Current for System Memory		950	mA	
$I_{CC\_3.3\_DC}$	3.3V Power Supply Current for Display Cache		250	mA	
$I_{CC\_3.3\_DAC}$	3.3V Power Supply Current for RAMDAC		200	mA	
$I_{sus\_3.3}$	3.3V Standby Supply Current		110	mA	

NOTES:
1. The maximum values of the currents should not be used to calculate the maximum power consumption, since they may not occur at the same time. The P_{GMCH} listed above is the maximum power consumption.

2.4. Signal Groups

To ease discussion of the AC and DC characteristics, the signals on the GMCH have been combined into groups with similar characteristics. These signal groups are referenced throughout this document.

Table 2. GMCH Signal Groups

Signal Group	Signal Type	Signals
(a)	GTL+ I/O	HA[31:3]#, HD[63:0]#, ADS#, BNR#, DBSY#, DRDY#, HIT#, HITM#, HREQ[4:0]#, HTRDY#, RS[2:0]#
(b)	GTL+ Input	HLOCK#
(c)	GTL+ Output	CPURST#, BPRI#, DEFER#
(d)	GTL+ Termination Voltage	GTLREF[B:A]
(e)	CMOS (2.5V) Input	HCLK
(f)	CMOS I/O	SDQM[7:0], SMD[63:0], LMD[31:0], LDQM[3:0]
(g)	CMOS Input	SCLK, RESET#, DCLKREF, LRCLK
(h)	CMOS Output	SCS[3:0]#, SRAS#, SCAS#, SMAA[11:0], SBS[1:0], SMAB[7:4]#, SWE#, SCKE[1:0], LCS#, LSRAS#, LSCAS#, LMA [11:0], LWE#, LOCLK, LTCLK
(k)	CMOS (1.8V) Input	TVCLKIN/INT#
(l)	CMOS (1.8V) Output	CLKOUT[1:0], BLANK#, LTVDATA[11:0], TVVSYNC, TVHSYNC
(m)	CMOS I/OD	DDCSCL*, DDCSDA*, LTVCL, LTVDA
(n)	RAMDAC output	RED, GREEN, BLUE
(o)	Display Sync output	VSYNC, HSYNC
(p)	Display Reference	IREF, IWASTE

NOTES:
1. DDC inputs are not 5V tolerant.

2.5. DC Characteristics

Table 3. DC Characteristics

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Symbol	Signal Group	Parameter	Min	Max	Unit	Notes
GTL+ I/O DC Characteristics						
VIL_GTL	(a,b)	GTL+ Input Low Voltage	-0.3	GTLREF –0.2	V	
VIH_GTL	(a,b)	GTL+ Input High Voltage	GTLREF +0.2	1.835	V	
VOL_GTL	(a,c)	GTL+ Output Low Voltage		0.6	V	
IOL_GTL	(a,c)	GTL+ Output Low Current	36	48	mA	
GTL_REF	(d)	GTL+ Reference Voltage	2/3(1.5V)-2%	2/3(1.5V)+2%	V	
I_{LEAK_GTL}	(a,b)	Leakage Current		±10	µA	
3.3V CMOS I/O Signal DC Characteristics						
VIL_3.3	(f,g)	CMOS Input Low Voltage	-0.3	0.8	V	
VIH_3.3	(f,g)	CMOS Input High Voltage	2.0	VCC_3.3 +0.3	V	
VOL_3.3	(f,h)	CMOS Output Low Voltage		0.4	V	
VOH_3.3	(f,h)	CMOS Output High Voltage	2.4		V	
IOL_3.3	(f,h)	CMOS Output Low Current		3	mA	
IOH_3.3	(f,h)	CMOS Output High Current	-2.0		mA	
$I_{LEAK\_3.3}$	(f,g)	Leakage Current		±100	µA	
1.8V CMOS I/O DC Characteristics						
VIL_1.8	(j,k)	CMOS Input Low Voltage	-0.3	0.4(Vcc1.8max)	V	
VIH_1.8	(j,k)	CMOS Input High Voltage	0.6(Vcc1.8min)	0.3 + (Vcc1.8max)	V	
VOL_1.8	(j,l)	CMOS Output Low Voltage		0.1(Vcc1.8max)	V	
VOH_1.8	(j,l)	CMOS Output High Voltage	0.9(Vcc1.8min)		V	
IOL_1.8	(j,l)	CMOS Output Low Current		1.0	mA	
IOH_1.8	(j,l)	CMOS Output High Current	-1.0		mA	
$I_{LEAK\_1.8}$	(j,k)	Leakage Current		±10	µA	

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Symbol	Signal Group	Parameter	Min	Max	Unit	Notes
CMOS I/OD Signal DC Characteristics						
VIL_I/OD	(m)	CMOS I/OD Input Low Voltage	0.1	0.8	V	
VIH_I/OD	(m)	CMOS I/OD Input High Voltage	2.0	$V_{CC\_3.3}$ + 0.1	V	
VOL_I/OD	(m)	CMOS I/OD Output Low Voltage		0.4	V	
VOH_I/OD	(m)	CMOS I/OD Output High Voltage	2.4		V	
IOL_I/OD	(m)	CMOS I/OD Output Low Current	4		mA	
$I_{LEAK\_I/OD}$	(m)	Leakage Current		±100	µA	
Display Sync Output DC Characteristics						
VOL_DIS	(o)	Display Sync Output Low Voltage		0.4	V	
VOH_DIS	(o)	Display Sync Output High Voltage	2.4		V	
IOL_DIS	(o)	Display Sync Output Low Current	4		mA	
Input/Output Capacitance						
CIN1	(g)	Input Capacitance	7.5	11.3	pF	F_C = 1 MHz
CIN2	(k)	Input Capacitance	6.4	9.8	pF	F_C = 1 MHz
COUT1	(h)	Output Capacitance	3.54	6.6	pF	F_C = 1 MHz
COUT2	(i)	Output Capacitance	6.4	9.8	pF	F_C = 1 MHz
CI/O1	(f)	I/O Capacitance	3.54	6.6	pF	F_C = 1 MHz
CI/O2	(j)	I/O Capacitance	6.4	9.8	pF	F_C = 1 MHz

2.6. AC Characteristics

All timings are in nanoseconds (ns), unless otherwise specified. In addition, all the clock-to-output values are specified into 0 pF load, unless otherwise specified.

Table 4. Clock Timings (66/100 MHz)

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Sym	Parameter	66 MHz		100 MHz		133 MHz (810E only)		Fig	Unit	Notes
		Min	Max	Min	Max	Min	Max			
HCLK (Host Clock)										
t1a	HCLK Period	15	15.5	10.0	10.5	7.5	8.0	1	ns	
t1b	HCLK Jitter		± 250		± 250		± 250	1	ps	
t1c	HCLK High Time	5.2		3.0		1.87		1	ns	
t1d	HCLK Low Time	5.0		2.8		1.87		1	ns	
t1e	HCLK Slew Rate	1.0	4.0	1.0	4.0	1.0	4.0	1	V/ns	
SCLK (System Memory Clock)										
t2a	SCLK Period	N/A	N/A	10	10.5	N/A	N/A	1	ns	
t2b	SCLK Jitter	N/A	N/A		± 250	N/A	N/A	1	ps	
t2c	SCLK High Time	N/A	N/A	3.0		N/A	N/A	1	ns	
t2d	SCLK Low Time	N/A	N/A	3.0		N/A	N/A	1	ns	
t2e	SCLK Slew Rate	N/A	N/A	1.0	4.0	N/A	N/A	1	V/ns	
t2f	SCLK Duty Cycle	N/A	N/A	45%	55%	N/A	N/A	1		
LRCLK (Display Cache Receive Clock)										
t3a	LRCLK Period	N/A	N/A	10	10.5	7.5	8.0	1	ns	
t3b	LRCLK Jitter	N/A	N/A		± 250		± 250	1	ps	
t3c	LRCLK High Time	N/A	N/A	3.0		2.0		1	ns	
t3d	LRCLK Low Time	N/A	N/A	3.0		2.0		1	ns	
t3e	LRCLK Slew Rate	N/A	N/A	1.0	4.0	1.0	4.0	1	V/ns	
t3f	LRCLK Duty Cycle	N/A	N/A	45%	55%	45%	55%	1		
LTCLK (Display Cache Transmit Clock)										
t4	LTCLK Period	N/A	N/A	10	10.5	7.5	8.0	1	ns	
t5	LOCLK Period	N/A	N/A	10	10.5	7.5	8.0	1	ns	

NOTES:

1. AC specifications are measured at the GMCH.

Table 5. Display Interface Clock Timing

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Symbol	Parameter	48 MHz		Fig	Unit	Notes
		Min	Max			
DCLKREF (display interface clock) (Must be non-spread spectrum modulated)						
t6a	DCLKREF Period	20.83	24.31	2	ns	
t6b	DCLKREF Jitter		± 500	2	ps	
t6c	DCLKREF High Time	9.2		2	ns	
t6d	DCLKREF Low Time	9.2		2	ns	
t6e	DCLKREF Slew Rate	1.0	4.0	2	V/ns	
t6f	DCLKREF Duty Cycle	45%	55%	2		

Table 6. CPU Interface Timings for 370-pin Socket (Intel® 810 Chipset)

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Symbol	Parameter	66 MHz		100 MHz		Fig	Unit	Notes
		Min	Max	Min	Max			
t7	Valid Delay from HCLK Rising (tco)	1.27	7.0	1.27	5.35	4	ns	
t8	Input Setup Time to HCLK Rising (tsu)	2.72		2.72		5	ns	
t9	Input Hold Time from HCLK Rising (thld)	0.10		0.10		5	ns	

Table 7. CPU Interface Timings for 370-Pin Socket (Intel® 810E Chipset)

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Sym	Parameter	66 MHz		100MHz		133MHz		Fig	Unit	Notes
		Min	Max	Min	Max	Min	Max			
t7	Valid Delay from HCLK Rising (tco)	1.05	4.10	1.05	4.10	1.05	4.10	4	ns	
t8	Input Setup Time to HCLK Rising (tsu)	2.65		2.65		2.65		5	ns	
t9	Input Hold Time from HCLK Rising (thld)	0.10		0.10		0.10		5	ns	

Table 8. CPU Interface Timings for SC242 Connector (Intel® 810 Chipset)

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Sym	Parameter	66 MHz		100 MHz		Fig	Unit	Notes
		Min	Max	Min	Max			
t7_s	Valid Delay from HCLK Rising (tco)	N/A	N/A	0.50	4.50	4	ns	
t8_s	Input Setup Time to HCLK Rising (tsu)	N/A	N/A	2.27		5	ns	
t9_s	Input Hold Time from HCLK Rising (thld)	N/A	N/A	0.28		5	ns	

Table 9. CPU Interface Timings for SC242 (Intel® 810E Chipset)

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Sym	Parameter	66 MHz		100MHz		133MHz		Fig	Unit	Notes
		Min	Max	Min	Max	Min	Max			
t7_s	Valid Delay from HCLK Rising (tco)	0.50	3.63	0.50	3.63	0.50	3.63	4	ns	
t8_s	Input Setup Time to HCLK Rising (tsu)	2.27		2.27		2.27		5	ns	
t9_s	Input Hold Time from HCLK Rising (thld)	0.28		0.28		0.28		5	ns	

Table 10. System Memory Timings (100MHz)

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Sym	Parameter	1x Buffer		2x Buffer		3x Buffer		4x Buffer		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
t10	WE# Valid Delay from SCLK Rising	1.15	4.70	1.05	4.30	1.05	4.30	N/A	N/A	ns	0pF
t11	SRAS# Valid Delay from SCLK Rising	1.15	4.70	1.05	4.30	1.05	4.30	N/A	N/A	ns	0pF
t12	SCAS# Valid Delay from SCLK Rising	1.15	4.70	1.05	4.30	1.05	4.30	N/A	N/A	ns	0pF
t13	CS[3:0]# Valid Delay from SCLK Rising	N/A	N/A	1.05	4.30	1.05	4.30	N/A	N/A	ns	0pF
t14	MAA[11:8, 3:0], BS[1:0], Valid Delay from SCLK Rising	1.15	4.70	1.05	4.30	1.05	4.30	N/A	N/A	ns	0pF
t15	CKE[1:0] Valid Delay from SCLK Rising	N/A	N/A	0.95	3.60	0.96	3.55	0.91	3.52	ns	0pF
t16	MAA/B[7:4]# Valid Delay from SCLK Rising	1.15	4.00	0.95	3.55	0.96	3.55	0.91	3.51	ns	0pF

Sym	Parameter	1.0x Buffer		1.5x Buffer		2.5x Buffer		Units	Notes
		Min	Max	Min	Max	Min	Max		
t17	DQM[7:0] Valid Delay from SCLK Rising	1.24	4.60	1.38	4.95	1.17	4.40	ns	0pF
t18	MD[63:0] Valid Delay from SCLK Rising	1.24	4.60	1.38	4.95	1.17	4.40	ns	0pF

Sym	Parameter	Min	Max	Units	Notes
t19	MD[63:0] Setup Time to SCLK Rising	0.50		ns	0pF
t20	MD[63:0] Hold Time from SCLK Rising	1.10		ns	0pF

Table 11. Display Cache Memory Timings (100 MHz)

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Symbol	Parameter	100 MHz		133 MHz (810E only)		Units	Figure	Notes
		Min	Max	Min	Max			
t21	LCS[1:0]# Valid Delay from LTCLK Rising	3.10	4.60	1.90	3.30	ns	4	0pF
t22	LDQM Valid Delay from LTCLK Rising	3.10	4.60	1.90	3.30	ns	4	0pF
t23	LSRAS# Valid Delay from LTCLK Rising	3.10	4.60	1.90	3.30	ns	4	0pF
t24	LSCAS# Valid Delay from LTCLK Rising	3.10	4.60	1.90	3.30	ns	4	0pF
t25	LMA[11:0] Valid Delay from LTCLK Rising	3.10	4.60	1.90	3.30	ns	4	0pF
t26	LWE# Valid Delay from LTCLK Rising	3.10	4.60	1.9	3.30	ns	4	0pF
t27	LMD[31:0] Valid Delay from LTCLK Rising	3.10	4.60	1.9	3.30	ns	4	0pF
t28	LMD[31:0] Setup Time to LRCLK Rising	0.5		0.5		ns	5	0pF
t29	LMD[31:0] Hold Time to LRCLK Rising	1.0		1.0		ns	5	0pF

Table 12. Digital Video Out: Flat Panel Timings

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t42	LTVDATA[11:0], BLANK#, TVVSYNC, TVHSYNC valid before CLKOUT[1:0], tTDVb	See Table 11		ns	9	1
t43	LTVDATA[11:0], BLANK#, TVVSYNC, TVHSYNC valid after CLKOUT[1:0], tTDVa	See Table 11		ns	9	1
Receiver Timing						
N/A	INT# Asynchronous	N/A		ns		

NOTES:

1. The output valid delay is measured into a 60 ohm transmission line load and is frequency dependent.

Table 13. Flat Panel Data Setup and Hold Times from CLKOUT

CLKOUT (MHz)	tTDVb (min) (ns)	tTDVa (min) (ns)
20	10.75	10.95
25	8.40	8.60
30	6.85	7.05
35	5.74	5.94
40	4.90	5.10
45	4.25	4.45
50	3.73	3.93
55	3.30	3.50
60	2.95	3.15
65	2.65	2.85
70	2.39	2.59
75	2.16	2.36
80	2.01	2.21
85	1.80	2.00

Table 14. Digital Video Out: TV Out Timings

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t44	LTVDATA[11:0], BLANK#, TVVSYNC, TVHSYNC valid before CLKOUT[1:0], tTDVb	See Table 15		ns	9	1
t45	LTVDATA[11:0], BLANK#, TVVSYNC, TVHSYNC valid after CLKOUT[1:0], tTDVa	See Table 15		ns	9	1
Receiver Timing						
	TVCLKIN @ 20-40 MHz					
t46a	TVCLKIN Period	11.75	50	ns		
t46b	TVCLKIN Jitter		±300	ps		
t46c	TVCLKIN High Time	3.0		ns		
t46d	TVCLKIN Low Time	3.0		ns		
t46e	TVCLKIN Rise Time	0.4	2.0	ns		
t46f	TVCLKIN Fall Time	0.4	2.0	ns		

NOTES:

1. The output valid delay is measured into a 60 ohm transmission line load and frequency dependent.

Table 15. TV Out Data Setup and Hold Times from CLKOUT

CLKOUT (MHz)	tTDVb (min) (ns)	tTDVa (min) (ns)
20	10.75	10.95
25	8.40	8.60
30	6.85	7.05
35	5.74	5.94
40	4.90	5.10

2.7. GMCH Timing Diagrams

Figure 1. 2.5V Clocking Interface

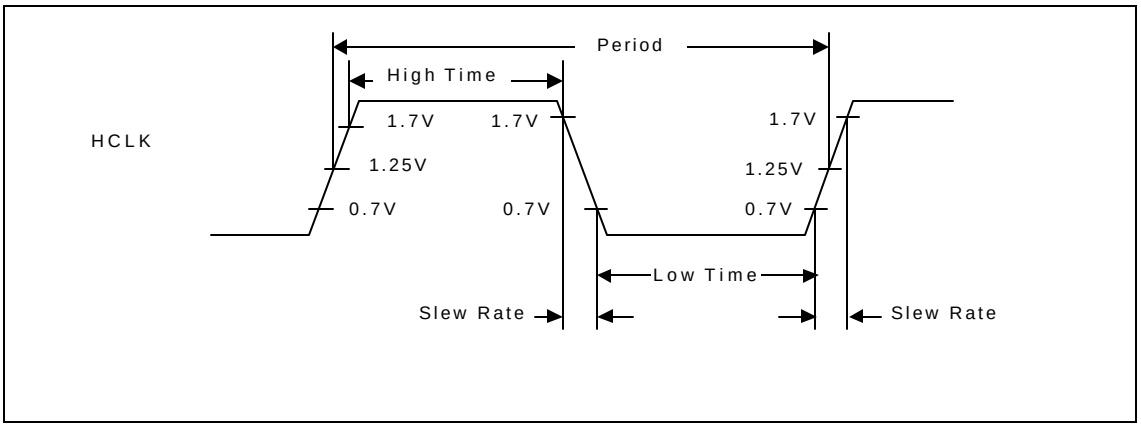


Figure 2. 3.3V Clocking Interface

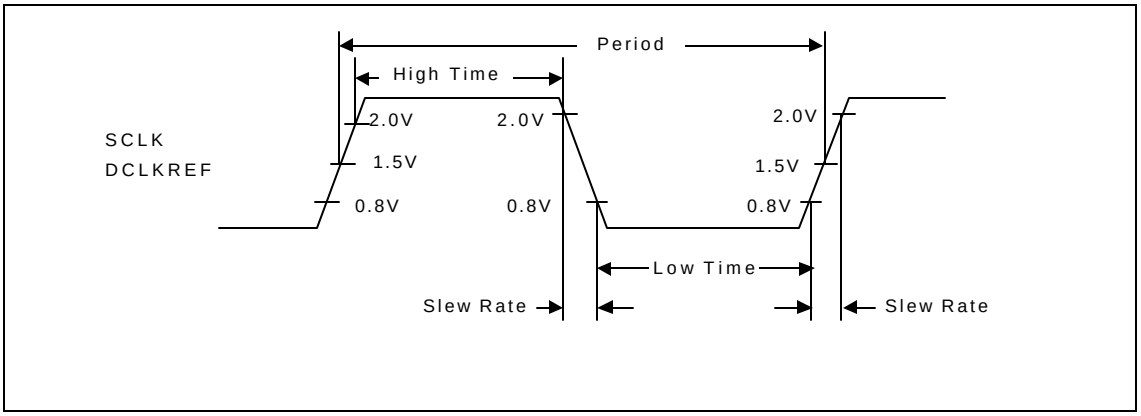
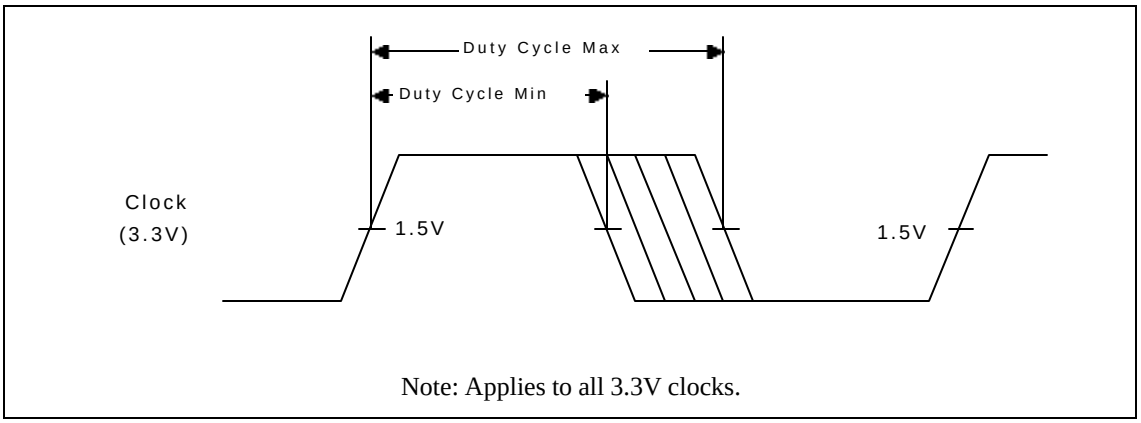


Figure 3. 3.3V Clock Duty Cycle



Note: Applies to all 3.3V clocks.

Figure 4. Valid Delay From Rising Clock Edge

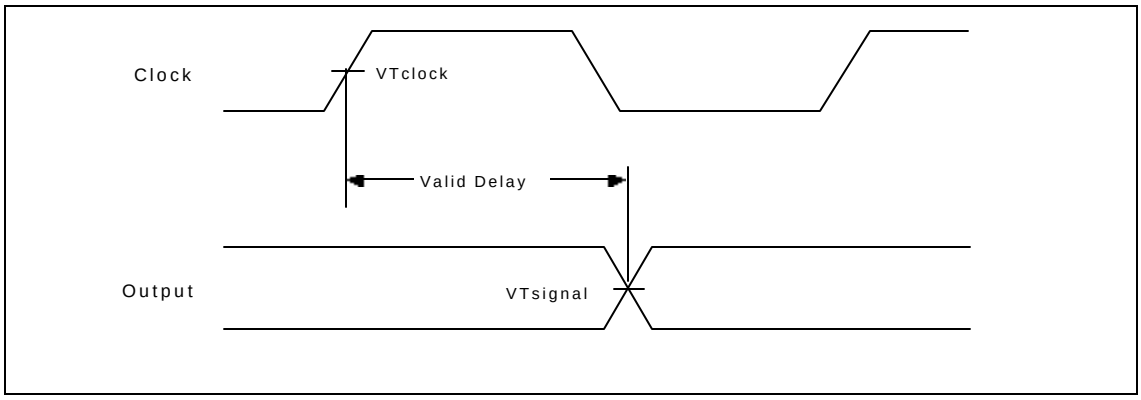


Figure 5. Setup and Hold Time to Clock

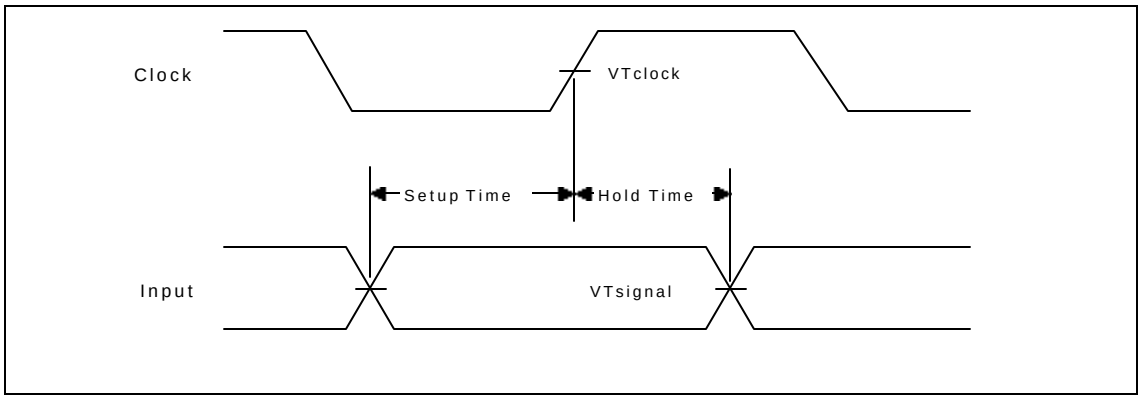


Figure 6. Float Delay

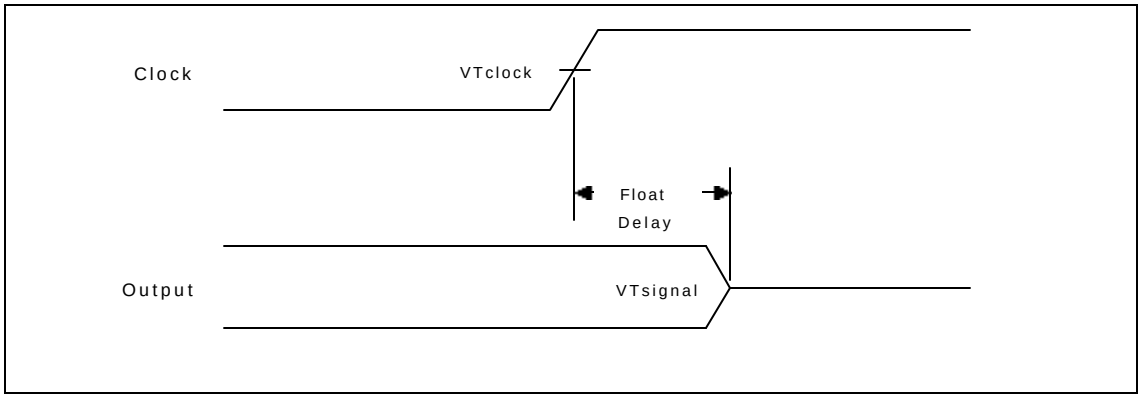


Figure 7. Pulse Width

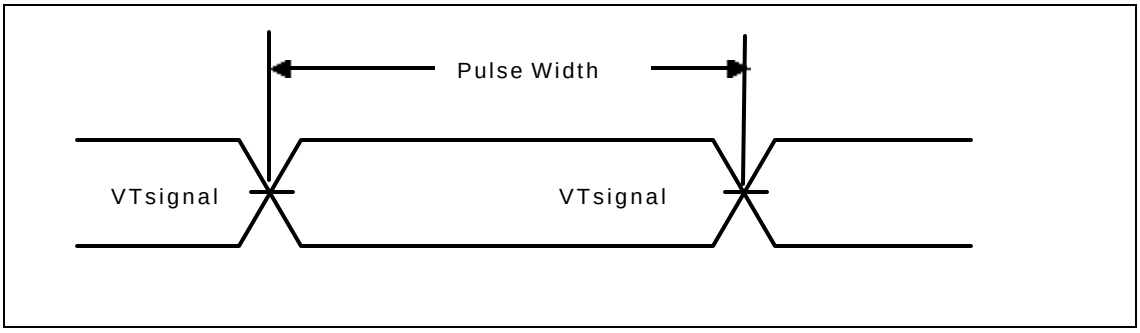
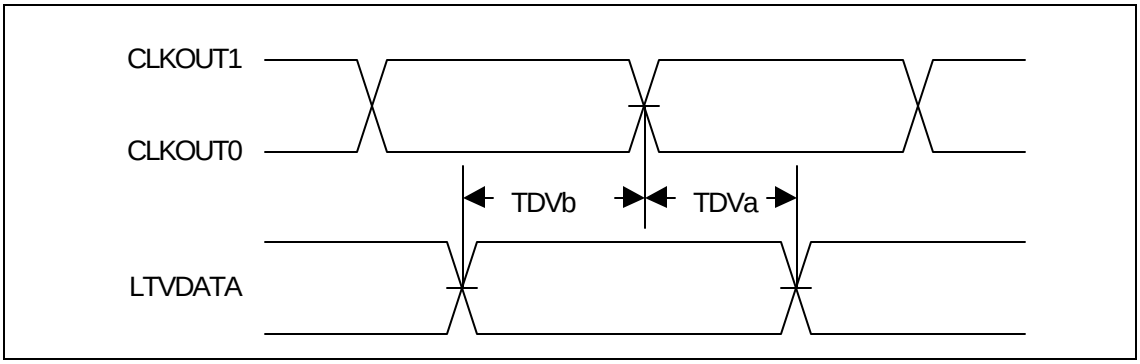


Figure 8. Source Synchronous Digital Video Out timings



3. GMCH DAC

The GMCH DAC (digital-to-analog converter) consists of three identical 8-bit DACs to provide red, green and blue color components. Each DAC can output a current from 0 to 255 units of current, where one unit of current (LSB) is defined based on the VESA video signal standard.

3.1. DAC DC Characteristics

Table 16. DAC DC Characteristics

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Parameter	Min	Typical	Max	Unit	Notes
DAC Resolution			8	Bits	
ILE (Integral Linearity Error)	-1.0		+1.0	LSB	
DLE (Differential Linearity Error)	-1.0		+1.0	LSB	1
Full Scale (gain) Error	-5.0		+10.0	%	Of Full Scale
DAC Full Scale Voltage	665	700	770	mV	VESA Video Level
LSB Current		73.2		uA	
Monotonicity	Guaranteed				

NOTES:
1. Guaranteed by design characterization

3.2. DAC Reference and Output Specifications

Table 17. DAC Reference and output Specifications

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Parameter	Description	Note
Reference Resistor (Connected to IREF pad)	174 Ω for VESA Standard	
Output Load	Double termination required with 75Ω (effective resistance 37.5 Ω)	
Video Filter	PI Filter: Ferrite bead (75 Ω @ 100 MHz) and two 3.3 pF capacitors	Apply to each RAMDAC output

3.3. DAC AC Characteristics

Table 18. DAC AC Characteristics

Functional Operating Range ($V_{CC\_1.8}$ = 1.8V ±5%, $V_{CC\_3.3}$ / $V_{SUS\_3.3}$ = 3.3V ±5%; T_{CASE} = 0°C to +105°C)

Parameter	Min	Typical	Max	Unit	Notes
Pixel Clock Rate			250	MHz	
RGB Video Output Rise Time (10-90% of full-scale) no load		0.23	0.52	ns	
RGB Video Output Rise Time (10-90% of full-scale)		0.8	3.0	ns	1
RGB video Output Fall Time (10-90% of full-scale) no load		0.57	1.55	ns	
RGB Video Output Fall Time (10-90% of full-scale)		1.35	2.5	ns	1
Glitch Energy/Clock Feed Through			200	pV-s	2

NOTES:

1. As measured at the VGA connector
2. Black to White level transition with 37.5 Ω load. Spec guaranteed by design characterization

4. Signal Quality Specifications

4.1. 3.3V Signal Overshoot/Undershoot Specification

Table 19. 3.3V Signal Quality Specification

Symbol	Parameter	Max	Time Duration	Note
VOS_MAX	Absolute Maximum Overshoot	Vcc_3.3 + 1.5V	N/A	1
VUS_MAX	Absolute Maximum Undershoot	– 1.5V	N/A	1
VOS	Overshoot Voltage Magnitude	Vcc_3.3 + 1V	2ns	
VUS	Undershoot Voltage Magnitude	–1V	2ns	

NOTES:
1. The signal voltage must not exceed the absolute maximum overshoot/undershoot voltage

4.2. GTL+ Signal Overshoot/Undershoot Specification

Table 20. GTL+ Signal Quality Specification

Symbol	Parameter	Max	Time Duration	Note
VOS_MAX	Absolute Maximum Overshoot	Vcc_1.8 + 1V	N/A	1
VUS_MAX	Absolute Maximum Undershoot	– 1V	N/A	1

NOTES:
1. The signal voltage must not exceed the absolute maximum overshoot/undershoot voltage

4.3. 1.8V Signal Overshoot/Undershoot Specification

Table 21. 1.8V Signal Quality Specification

Symbol	Parameter	Max	Time Duration	Note
VOS_MAX	Absolute Maximum Overshoot	Vcc_1.8 + 1V	N/A	1
VUS_MAX	Absolute Maximum Undershoot	– 1V	N/A	1

NOTES:
1. The signal voltage must not exceed the absolute maximum overshoot/undershoot voltage