



Mobile Intel[®] Pentium[®] III Processor/440MX Chipset Platform Design Guide

May 2002

Order Number: 273504-002





Information in this document is provided in connection with Intel® products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The 440MX chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

AlertVIEW, i960, AnyPoint, AppChoice, BoardWatch, BunnyPeople, CablePort, Celeron, Chips, Commerce Cart, CT Connect, CT Media, Dialogic, DM3, EtherExpress, ETOX, FlashFile, GatherRound, i386, i486, iCat, iCOMP, Insight960, InstantIP, Intel, Intel logo, Intel386, Intel486, Intel740, IntelDX2, IntelDX4, IntelSX2, Intel ChatPad, Intel Create&Share, Intel Dot.Station, Intel GigaBlade, Intel InBusiness, Intel Inside, Intel Inside logo, Intel NetBurst, Intel NetStructure, Intel Play, Intel Play logo, Intel Pocket Concert, Intel SingleDriver, Intel SpeedStep, Intel StrataFlash, Intel TeamStation, Intel WebOutfitter, Intel Xeon, Intel XScale, Itanium, JobAnalyst, LANDesk, LanRover, MCS, MMX, MMX logo, NetPort, NetportExpress, Optimizer logo, OverDrive, Paragon, PC Dads, PC Parents, Pentium, Pentium II Xeon, Pentium III Xeon, Performance at Your Command, ProShare, RemoteExpress, Screamline, Shiva, SmartDie, Solutions960, Sound Mark, StorageExpress, The Computer Inside, The Journey Inside, This Way In, TokenExpress, Trillium, Vivonic, and VTune are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

Copyright © Intel Corporation, 2002

*Other names and brands may be claimed as the property of others.

Contents

1.0	Introduction	7
1.1	Overview	7
1.2	References	9
2.0	Design Features	10
2.1	Processor.....	10
2.2	Intel® 440MX Chipset	10
2.2.1	Processor System Bus Interface	11
2.2.2	DRAM Interface	11
2.2.3	PCI Interface	11
2.2.4	System Clocking	11
2.2.5	PCI-to-X-Bus.....	11
2.2.6	USB Controller	11
2.2.7	IDE Controller	12
2.2.8	AC'97 Controller	12
2.2.9	Power Management.....	12
3.0	Clocking Guidelines	12
3.1	Clocking Guidelines with CK100 Clock Generator	12
3.1.1	Clocking System Overview Option 1: CK100 Clock Generator With Integrated SDRAM Clock Buffer	12
3.1.2	Specifications.....	14
3.2	Clocking System Overview Option 2: Clocking Guidelines With CK100 Clock Generator and CKBF (Discrete SDRAM Clock Buffer)	15
3.2.1	Clocking System Overview With CK100-M Clock Generator.....	15
3.2.2	CK100 Clock Synthesizer Pinout and Specifications.....	16
3.3	Clock Layout Guidelines for CK100 Clock Generators.....	18
3.4	Optional Clock Layout.....	20
3.5	Clock Vendors	20
4.0	Memory Guidelines	21
4.1	Mobile DRAM Interface Overview.....	21
4.2	DRAM Interface Signals	22
4.3	Mobile DRAM Layout Guidelines.....	22
4.3.1	100-MHz Memory Trace Lengths (With CK100 Clock Generator).....	24
5.0	Design Checklists	25
5.1	Mobile Pentium® III Processor.....	25
5.1.1	Mobile Pentium® III Processor Errata	25
5.1.2	Power and Ground Pins.....	26
5.1.3	Decoupling Requirements	27
5.1.4	Clock and Test Signals	27
5.1.5	Processor Signals.....	27
5.2	440MX Chipset Design Checklist	29
5.2.1	440MX Chipset Errata	29
5.2.2	440MX Chipset Power and Ground Pins	29
5.2.3	440MX Chipset Decoupling Guidelines	30



5.2.4	440MX Chipset Strapping Options	30
5.2.5	440MX Chipset Clock and Test Signals.....	31
5.2.6	Processor System Bus (PSB).....	31
5.2.7	Processor Sideband Signals.....	31
5.2.8	440MX Chipset SDRAM Memory Interface Signals.....	32
5.2.9	440MX Chipset PCI Bus Signals	32
5.2.10	440MX Chipset IDE Interface	34
5.2.11	USB Interface	34
5.2.12	AC'97 Interface	35
5.2.13	440MX Chipset X-bus Signals	35
5.2.14	Power Management Signals.....	36
5.2.15	General Purpose I/O Signals	37
5.3	Transitioning from a 440BX AGPset to a 440MX Chipset Design	37

Figures

1	System Block Diagram	8
2	CK100 With Integrated SDRAM Clock Buffer - Clocking Block Diagram	13
3	CK100 With Integrated SDRAM Clock Buffer - Clock Layout Guidelines.....	14
4	CK100 With Discrete SDRAM Clock Buffer - Clocking Block Diagram	15
5	CK100 With Discrete SDRAM Clock Buffer - Clock Layout Guidelines.....	16
6	Pinout for CK100 Clock Synthesizer (With No Clock Buffer).....	17
7	Pinout for CKBF Clock Buffer	17
8	General Clock Layout	20
9	440MX Chipset Memory Interface Routed to One or Two On-Board Memory Banks, One SO-DIMM Connector	23
10	440MX Chipset Memory Interface Routed to Two SO-DIMM Connectors	23
11	Pull-up Resistor Example	25
12	Circuit for Generating Reference Voltages	26
13	440MX Chipset Decoupling	30
14	Voltage Translation of FERR#	31
15	SUSA# Connected to PWR_DWN# of Clock Synthesizer.....	36



Tables

1	Related Documents	9
2	Mobile Intel® Pentium® III Processor/440MX Chipset Based System: Clock Trace Length and Width Specifications	19
3	SDRAM Interface Trace Lengths With CK100 Clock Generator	24
4	Values for Reference Voltages	27
5	440MX Chipset Strapping Options	30
6	Processor Sideband Signals.....	32
7	440MX Chipset PCI Bus Signals	33
8	440MX Chipset IDE Signals	34
9	440MX Chipset X-bus Signals	35



Revision History

Date	Revision	Description
April 2002	002	Removed two sections.
July 2001	001	First publication of this document.

1.0 Introduction

The Intel[®] 440MX chipset is a single device that integrates the two components of Intel's 440BX chipset – the 82443BX north bridge and the 82371EB (PIIX4E) south bridge. This document provides special design recommendations to facilitate the development of a system based on the 440MX chipset and these Intel Pentium[®] III processors:

- Mobile Intel Pentium III processor
- Low voltage Mobile Intel Pentium III processor
- Ultra low voltage Mobile Intel Pentium III processor
- Intel Pentium III Processor – Low Power (for applied computing applications)

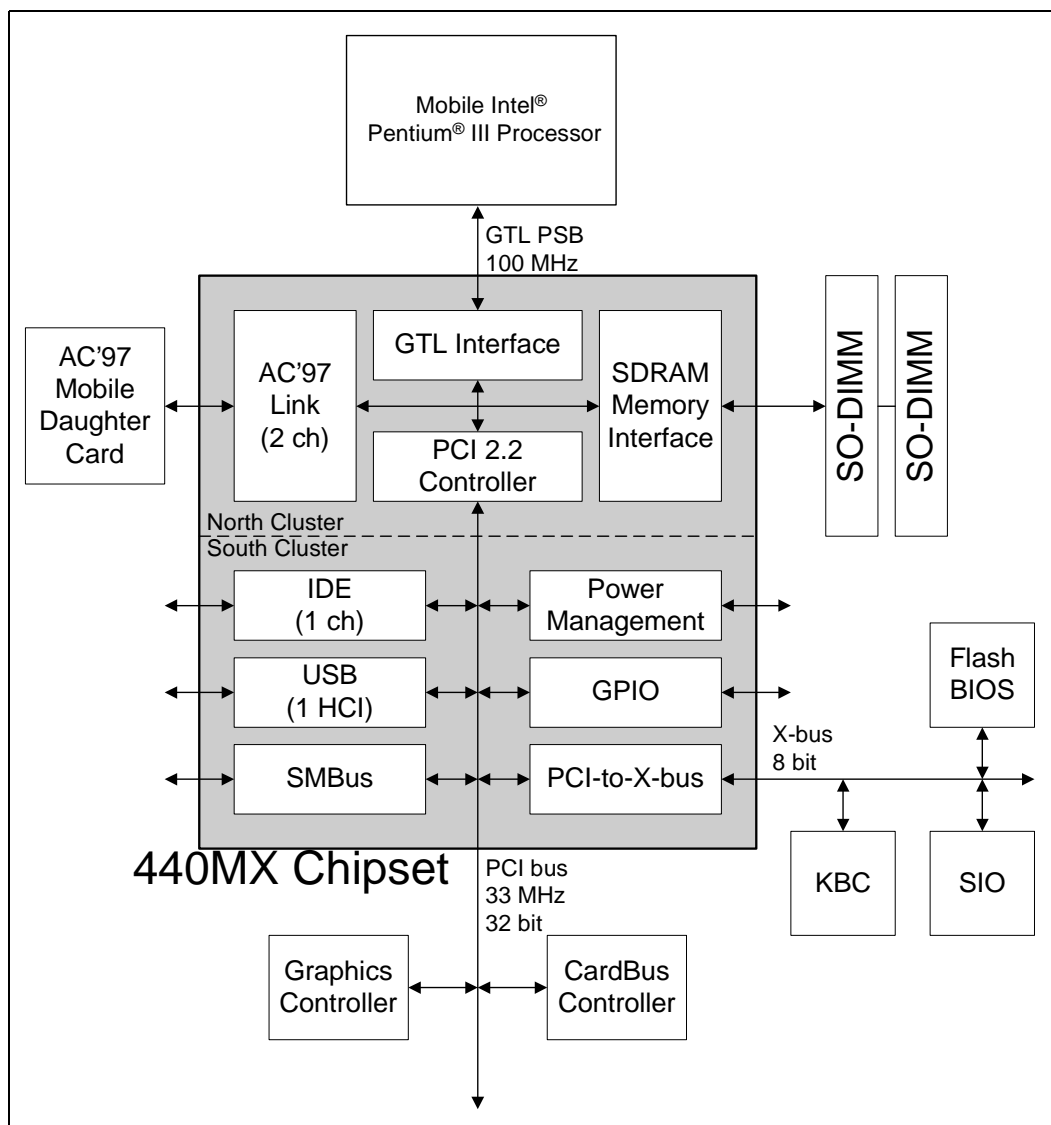
These processors will be referred to in this document as the Mobile Pentium III processor. See Figure 1 for a block diagram. To minimize problems during the debug phase, likely design errors have been identified and included in a checklist format in Section 5.0.

Note: This document describes design and debug practices applicable to a 440MX chipset design operating at a 100 MHz processor system bus and memory interface.

1.1 Overview

- 82443MX PCIset single-component chipset
- Full support for the Mobile Intel Pentium III processor, the low voltage Mobile Intel Pentium III processor, the ultra low voltage Mobile Intel Pentium III processor and the Pentium III Processor – Low Power with system bus frequency of 100 MHz
- Intel[®] SpeedStep[®] Technology support for multiple processor performance states
- 100-MHz memory interface
 - 64-bit memory data interface (without ECC support)
 - SDRAM support only (no EDO support)
 - 16-Mbit, 64-Mbit, and 128-Mbit DRAM technologies support
- AC'97 host controller with soft modem and soft audio support
- PCI rev 2.2 compliant bridge
 - Supports four PCI masters
 - Fourth PCI master is muxed with GPIO signals
- Integrated IDE controller with Ultra DMA/33 support
 - PIO Mode 4 transfers
 - PCI IDE bus master support
 - Single channel IDE only
- Integrated Universal Serial Bus (USB) controller with two USB ports
- Integrated system power management support
- PCI-to-X-bus bridge
- System Management Bus (SMBus) controller
- General purpose inputs and outputs

Figure 1. System Block Diagram





1.2 References

Table 1. Related Documents

Document	Intel Order Number (or other locator)
Mobile Intel® Pentium® III Processor in BGA2 and Micro-PGA2 Packages Featuring Intel SpeedStep® Technology at 1 GHz, 900 MHz, 850 MHz, 800 MHz, 750 MHz, 700 MHz, Low-voltage 700MHz, Low-voltage 600 MHz, and Ultra Low-voltage 500 MHz datasheet	249562
Intel® 440MX-100 PCIset Datasheet	245292
Intel® 440MX Chipset AC'97 Power/Performance Application Note	245212
Intel® 82443MX PCIset Specification Update	245051
Intel® 440BX AGPset: 82443BX Host Bridge/Controller Datasheet	290633
Intel® 440BX AGPset: 82443BX Host Bridge/Controller Specification Update	290639
Intel® 82371AB PCI-to-ISA/IDE Xcelerator (PIIX4) Datasheet	290562
Intel® 82371EB PIIX4E Specification Update	290635
CK97 Clock Synthesizer Design Guidelines NOTE: This document includes CK100 clock specifications.	243867
Intel® Architecture Software Developer's Manual, Volume 1; Basic Architecture	243190
Intel® Architecture Software Developer's Manual, Volume 2; Instruction Set Reference	243191
Intel® Architecture Software Developer's Manual, Volume 3; System Programming Guide	243192
Intel® Architecture MMX™ Technology Developer's Guide	243006
AP-485 Intel Processor Identification and CPUID Instruction application note	241618
AP-585 Layout Application Note	243330
AP-586 Thermal Application Note	243331
AP-587 Power Application Note	243332
AP-589 Design for EMI	243334
AP-524 Pentium® Pro Processor GTL+ Layout Guidelines application note	242765
66/100 MHz PC SDRAM 64-bit Non-ECC/Parity 144-pin Unbuffered SO-DIMM Specification Revision 1.0	www.intel.com/technology/memory/
PCI Local Bus Specification, Revision 2.1	www.pcisig.org
Universal Serial Bus Specification, Revision 1.0	www.usb.org
System Management Bus Specification	www.smbus.org/specs
Intel® Mobile EMI Design Guide	†
82371AB PIIX4 Application Note #1 USB Design Guide And Checklist	†
For Intel SpeedStep® Technology design information, contact your Intel field sales representative.	†

† This material is available through an Intel field sales representative.

2.0 Design Features

2.1 Processor

The 440MX chipset supports the Mobile Pentium III processor operating at a 100 MHz bus frequency. The Mobile Pentium III processor integrates the processor core, 256 Kbytes of second-level cache memory, and a 100-MHz 64-bit wide low power GTL+ processor system bus (PSB) in a BGA2 or μ PGA package.

2.2 Intel® 440MX Chipset

The 440MX chipset is a single-component chipset based on the Intel 440BX AGPset. Refer to Figure 1 for a block diagram of a typical platform based on the 440MX chipset with a Mobile Intel Pentium III processor, low voltage Mobile Intel Pentium III processor, ultra-low voltage Mobile Intel Pentium III processor, Pentium III Processor – Low Power, Mobile Intel Pentium II processor, or Mobile Intel® Celeron® processor.

The north cluster of the 440MX chipset component is designed with a low power GTL+ processor system bus to interface with the processor operating at 100 MHz. The north cluster, in addition to the processor system bus, includes a PCI revision 2.2-compliant host-to-PCI bridge interface, is optimized for high-speed memory operation with a 100 MHz 3.3 V SDRAM memory controller and data path, and integrates an AC'97 host controller.

The south cluster of the 440MX chipset component integrates a PCI-to-X-bus bridge function, a high-performance bus-master capable PCI IDE function, a Universal Serial Bus host/hub function, and an enhanced power management function including chip select controls and general purpose input and output pins.

The 440MX chipset component includes the following functions and capabilities:

- 64-bit Low Power GTL+ based system data bus interface
- 32-bit system address bus support
- 64-bit SDRAM main memory interface
- 32-bit PCI bus interface with integrated PCI arbiter
- PCI Revision 2.2-compliant PCI host controller
- PCI-to-X-bus bridge with support for 33 MHz PCI operations
- ACPI power management support
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated IDE controller supporting a single Ultra DMA/33 IDE channel
- USB host interface with support for two USB ports
- AC'97.2 host interface
- System Management Bus (SMBus) host controller, supports DRAM SO-DIMM serial presence detect
- General purpose input and outputs

2.2.1 Processor System Bus Interface

The 440MX chipset supports a maximum 32-bit (4 Gbytes) system address space and provides a four-deep in-order queue (i.e., it provides pipelining support for up to four outstanding transaction requests on the system bus). The Mobile Pentium III processor includes an integrated L2 cache; all cache control logic is provided on the processor.

For system bus-to-PCI transfers, the addresses are either translated or directly forwarded to the PCI bus, depending on the PCI address space being accessed. When accessing a PCI configuration space, the processor I/O cycle is mapped to a PCI configuration space cycle. When accessing a PCI I/O or a memory space, the processor address is passed without modification to the PCI bus. Certain memory address ranges are dedicated for a graphics memory address space.

2.2.2 DRAM Interface

The 440MX chipset integrates a main memory controller that supports a 100 MHz, 64-bit synchronous DRAM interface. The integrated DRAM controller drives a total of four rows of memory (two double-sided SO-DIMMs) and supports 16-Mbit, 64-Mbit, and 128-Mbit DRAM technology, and provides up to 256 Mbytes of total system memory.

2.2.3 PCI Interface

The 33-MHz PCI interface is Revision 2.2 compliant and supports up to four external PCI bus masters in addition to the internal south cluster functions, which are logically present on the PCI bus at IDSEL 18 (device 07).

2.2.4 System Clocking

The 440MX chipset operates the processor system bus and the memory interface at 100 MHz, and the PCI interface at 33 MHz. The 440MX chipset clocking scheme uses an external clock synthesizer that produces reference clocks for the system bus and PCI interfaces. For details, refer to the *CK97 Clock Synthesizer Design Guidelines* (order number 243867).

2.2.5 PCI-to-X-Bus

The 440MX chipset provides a PCI-to-X-bus bridge, integrating many common I/O functions found in ISA-based PC systems, including a seven-channel DMA controller, two 82C59 interrupt controllers, an 8254 timer/counter, and a real time clock. In addition to compatible transfers, each DMA channel supports type F transfers. The 440MX chipset fully supports both PC/PCI and distributed DMA protocols implementing PCI-based DMA. The interrupt controller has edge or level-sensitive programmable inputs. Chip select decoding is provided for the BIOS, a keyboard controller, a second external micro-controller, and two programmable address ranges for additional devices. The 440MX chipset provides full plug-and-play compatibility, and can be configured as a subtractive decode bridge or as a positive decode bridge.

2.2.6 USB Controller

The 440MX chipset contains a Universal Serial Bus (USB) host controller that is Universal Host Controller Interface (UHCI) compatible. The host controller's root hub has two programmable USB ports.

2.2.7 IDE Controller

The 440MX chipset supports a single IDE channel for one or two IDE devices providing an interface for IDE/EIDE hard disks and CD ROMs. The 440MX chipset provides support for Ultra DMA/33 synchronous DMA-compatible devices.

2.2.8 AC'97 Controller

The 440MX chipset integrates an AC'97.2 codec interface, supporting modem codecs and audio codecs. The AC'97 interface is logically located within the north cluster of the 440MX chipset to maximize performance and minimize latency.

2.2.9 Power Management

The 440MX chipset supports enhanced power management, including full clock control, device management to monitor device activity states, and suspend and resume logic with Power-On-Suspend, Suspend-to-RAM or Suspend-to-Disk. It fully supports operating system-directed power management via the Advanced Configuration and Power Interface (ACPI) specification. The 440MX chipset includes a System Management Bus (SMBus) host and slave interface for serial communication with other devices.

3.0 Clocking Guidelines

This section provides clocking guidelines to be followed when routing signal traces for the board design. These guidelines are based on the HCLK, PCLK, and SDRAMCLK requirements and should be implemented along with the application instructions supplied by the clock vendor.

Signal routing order will vary from designer to designer. Some designers prefer routing all of the clock signals first, while others prefer routing all of the high-speed bus signals first. Either routing methodology can be used, provided the guidelines in this section are followed. If these guidelines are not followed, it is very important to simulate your design. Even when the guidelines are followed, it is still a good idea to simulate as many signals as possible for proper signal integrity, flight time and cross talk.

3.1 Clocking Guidelines with CK100 Clock Generator

A CK100-compliant clock generator should be used to generate the system clocks for systems using a 100 MHz processor system bus and memory interface.

3.1.1 Clocking System Overview Option 1: CK100 Clock Generator With Integrated SDRAM Clock Buffer

Figure 2 shows the connections between the CK100 clock generator with integrated SDRAM buffer and the processor, chipset, and SDRAM memory devices.

Figure 2. CK100 With Integrated SDRAM Clock Buffer - Clocking Block Diagram

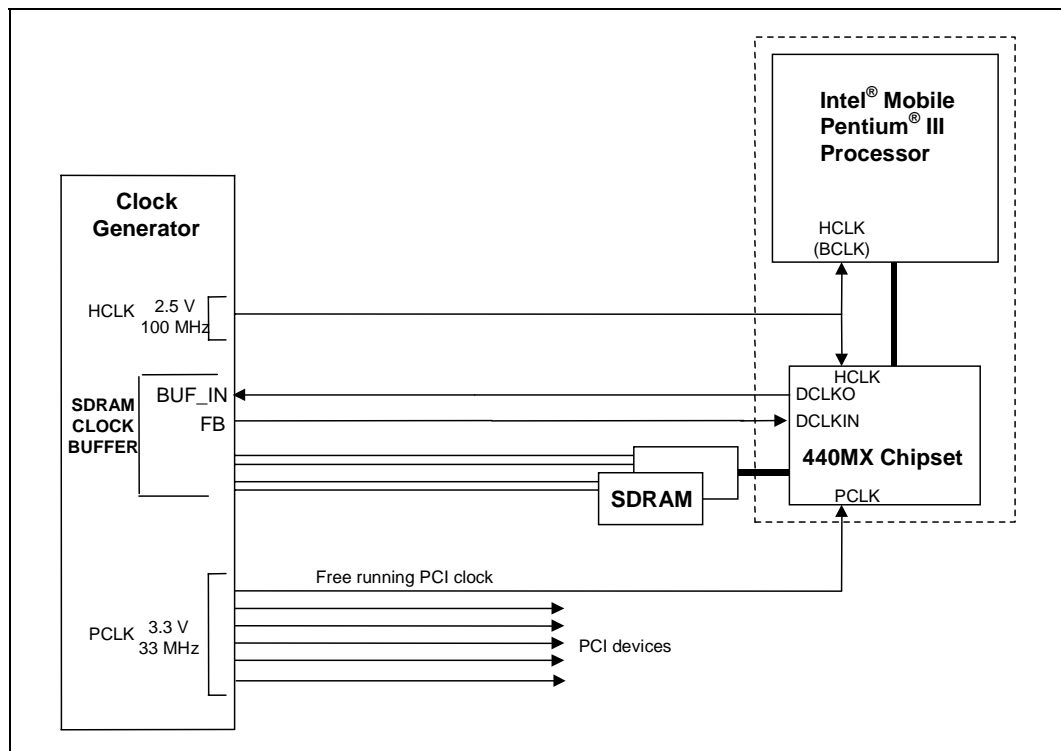
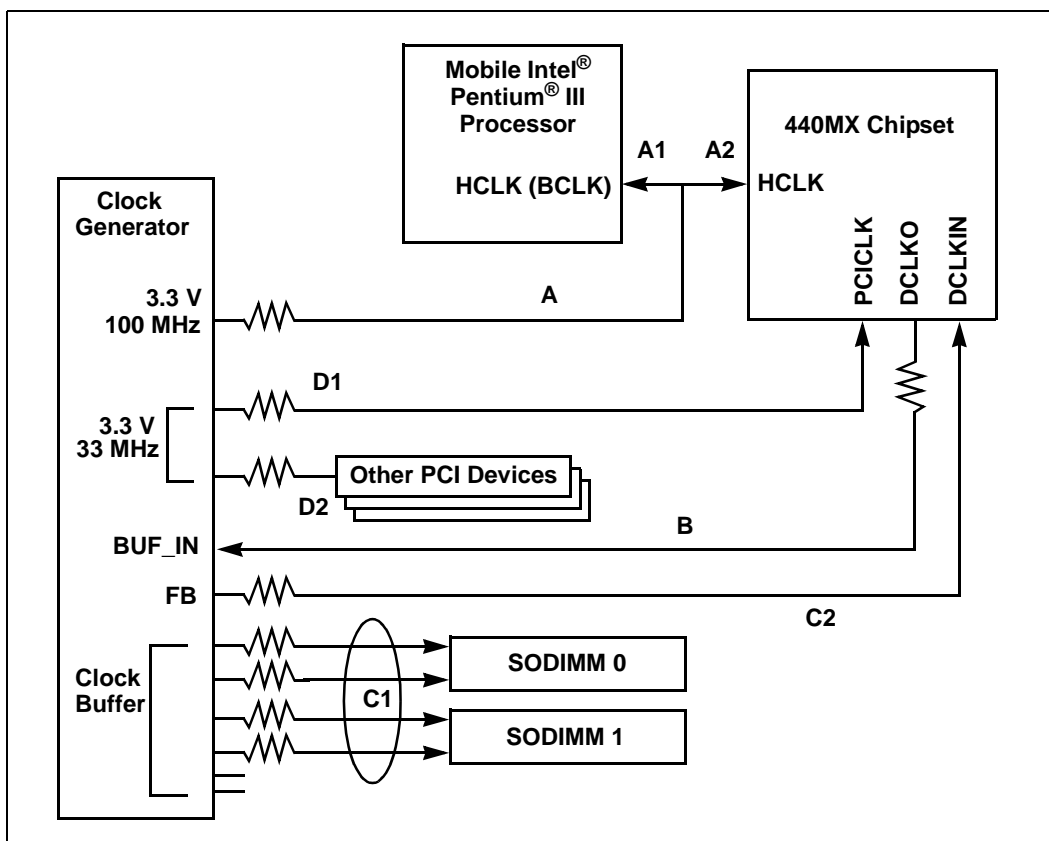


Figure 3. CK100 With Integrated SDRAM Clock Buffer - Clock Layout Guidelines



For more information, refer to “Clock Layout Guidelines for CK100 Clock Generators” on page 18.

3.1.2 Specifications

A clock generator that meets the CK100 clock specification will meet the requirements for a 440MX chipset-based system. “Clock Vendors” on page 20 is a list of vendors that provide clock synthesizers that meet CK100 clocking solution guidelines. The CK100 clock specification is available at:

<http://developer.intel.com>

Note: The CK100 specifications are included in the CK97 Clock Synthesizer Design Guidelines (order number 243867).

To comply with the CK100 specification, processor clocks operate at 100 MHz at 2.5 V, and the PCI clocks operate at 33 MHz at 3.3 V. CK100 also provides an integrated SDRAM clock buffer that provides clocks for SDRAM operating at 100 MHz at 3.3 V. Contact the clock device vendor for clock device pinout information.

3.2 Clocking System Overview Option 2: Clocking Guidelines With CK100 Clock Generator and CKBF (Discrete SDRAM Clock Buffer)

A CK100 compliant clock generator should be used to generate the system clocks for systems using a 100-MHz processor system bus and memory interface.

3.2.1 Clocking System Overview With CK100-M Clock Generator

Figure 4 shows the connections between a CK100 clock synthesizer and the processor, chipset, and SDRAM devices and/or slots.

Figure 4. CK100 With Discrete SDRAM Clock Buffer - Clocking Block Diagram

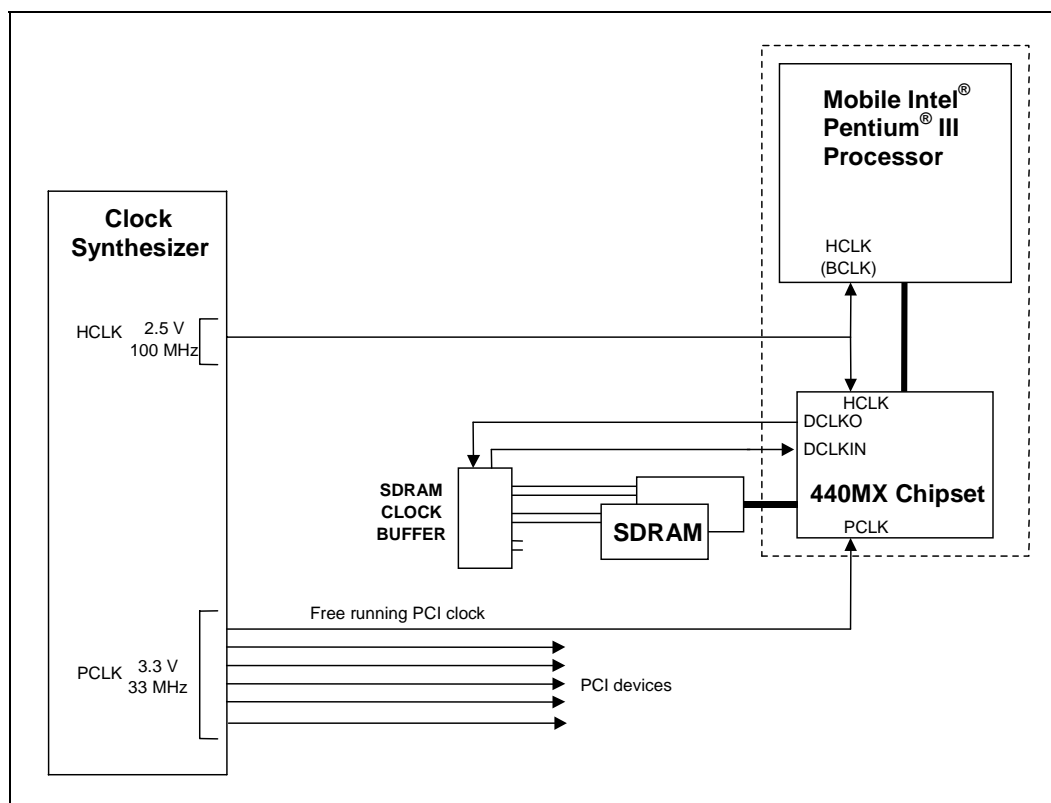
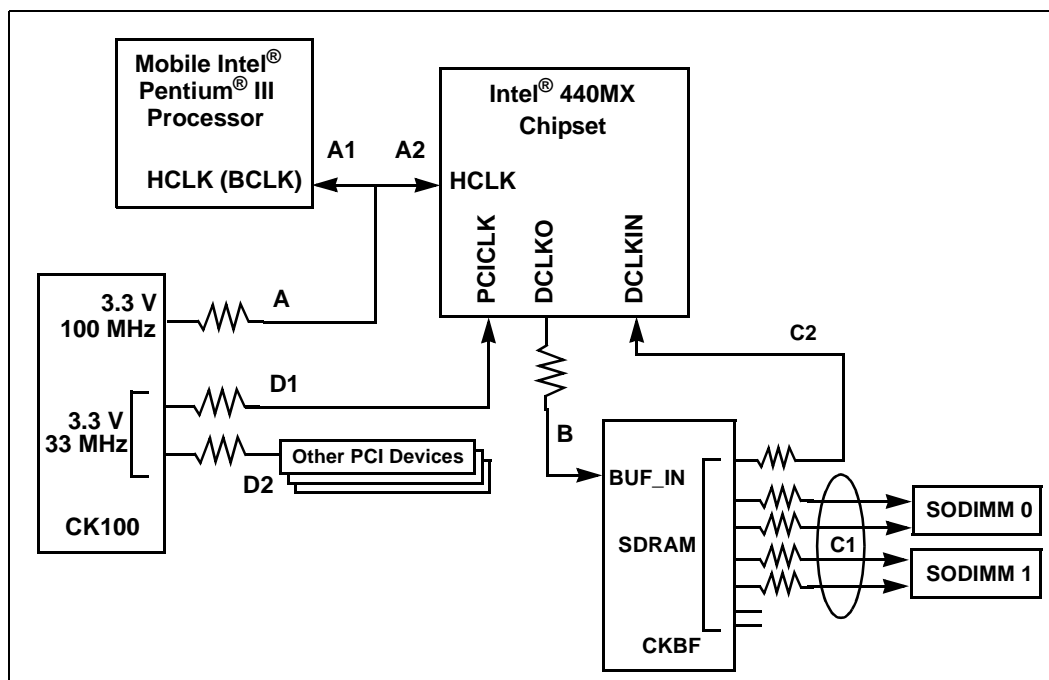


Figure 5. CK100 With Discrete SDRAM Clock Buffer - Clock Layout Guidelines



For more information, refer to “Clock Layout Guidelines for CK100 Clock Generators” on page 18.

3.2.2 CK100 Clock Synthesizer Pinout and Specifications

A clock generator that meets the CK100 clock specification will meet the requirements for a 440MX chipset-based system. “Clock Vendors” on page 20 is a list of vendors that provide clock synthesizers that meet CK100 clocking solution guidelines. The CK100 clock specification is available at:

<http://developer.intel.com>

Note: The CK100 specifications are included in the CK97 Clock Synthesizer Design Guidelines (order number 243867).

Note: The CK100 is running in the multi-voltage mode. The processor clocks operate at 100 MHz at 2.5 V, and the PCI clocks operate at 33 MHz at 3.3 V. The CKBF provides clocks for SDRAM operating at 100 MHz at 3.3 V.

Figure 6. Pinout for CK100 Clock Synthesizer (With No Clock Buffer)

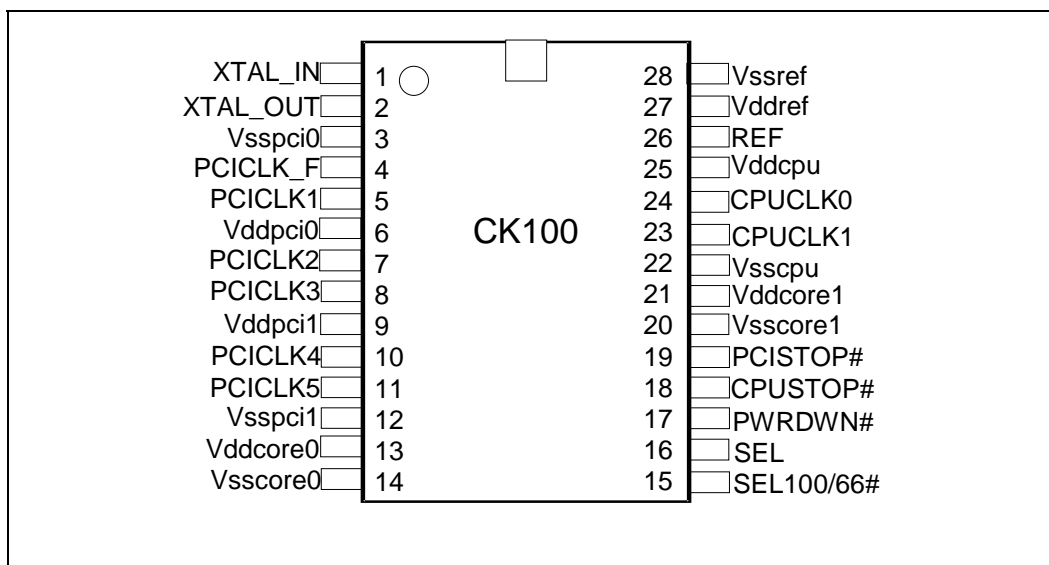
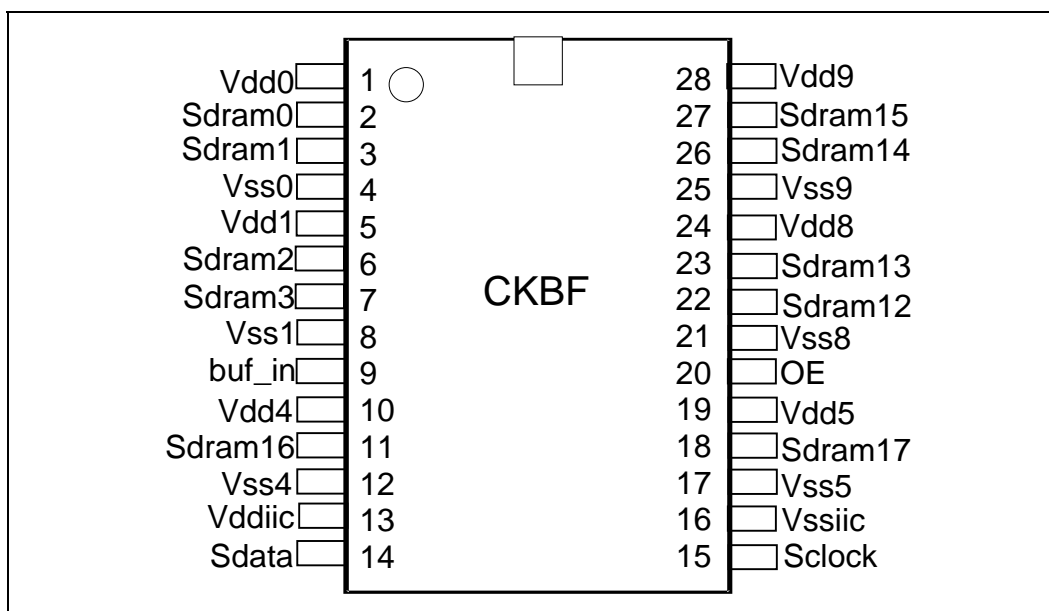


Figure 7. Pinout for CKBF Clock Buffer



3.3 Clock Layout Guidelines for CK100 Clock Generators

These guidelines are for illustration purposes; it is up to an individual designer to ensure that all timing and signal quality requirements for the chipset, processor, and memory devices are met.

1. For each clock signal trace that transitions from the surface layer to an internal layer, place a ground via stitching the two ground planes together.
2. General guidelines:
 - All clocks except CPUCLKs should be routed with 1:2 spacing and an impedance of $55 \Omega \pm 10\%$
 - Route all clocks on internal layers to provide better trace delay consistency and better EMI containment.
 - Minimize the use of vias on clock signals.
3. To minimize cross-talk:
 - Clock trace spacing is recommended to be at least 14 mil.
 - Serpentine trace separation should be a minimum of 18 mil.
4. Series matching resistors are required as near to the driver pin as possible (less than 1"). See Table 5, "440MX Chipset Strapping Options" on page 30 for values.
5. A PCICLK that is used for a PCI socket or is sent to a docking station should be implemented as a point-to-point connection and should not be shared with another load.
6. When designing with a docking connector, remember to account for the PCICLK trace length in the docking station.
7. Place all damping resistors and filter capacitors within 0.5" of the clock generator.
8. Place all decoupling capacitors close to the clock generator.
9. Board impedance should be $55 \Omega \pm 15\%$
10. Use discrete resistors on HCLK signals coming from the clock generator.
11. For CK100 with CKBF: the CKBF should be on the V3 rail and the CK100-M should be on the V3S rail.

Table 2. Mobile Intel® Pentium® III Processor/440MX Chipset Based System: Clock Trace Length and Width Specifications

Variable	Trace Length (min)	Trace Length (max)	Tolerance ^{Note 2}	Trace Width	Resistor
A	2.0 inches (50.8 mm)	4.5 inches (114.3 mm)		8 mil	22 Ω ±5%
A1	A2 + 0.876 inches (A2 + 22.25 mm)	A2 + 0.878 inches (A2 + 22.30)		4 mil	NONE
A2	1.25 inches (31.8 mm)	1.35 inches (34.3 mm)		4 mil	NONE
B	0	4.0 inches (101.6 mm)		5 mil	18 Ω ±5%
C1	0	4.0 inches (101.6 mm)	+/- 0.1 inch (+/- 2.54 mm)	5 mil	18 Ω ±5%
C2 ^{Note 1}	C1 + 2.4 inches (C1 + 60.9 mm)	C1 + 2.6 inches (C1 + 66 mm)		5 mil	18 Ω ±5%
D1	A + A2	A + A2 + 4.0 inches (A + A2 + 101.6 mm)		5 mil	33 Ω ±5%
D2	D1	D1	+/- 4.0 inches (+/- 101.6 mm)	5 mil	33 Ω ±5%

NOTES:

1. For platforms with on-board memory devices, clock traces should be routed as if there were a “phantom” connector on the board. The designer should follow the routing guidelines in the *66/100 MHz Unbuffered SDRAM 64-bit Non-ECC/Parity 144-pin SO-DIMM Specification* for the clock signals from the “phantom” connector to the on-board memory devices. In other words, route the clock trace to the position that SODIMM0 would occupy following the constraints given above, and route from that point onward according to the *66/100 MHz Unbuffered SDRAM 64-bit Non-ECC/Parity 144-pin SO-DIMM Specification*.
2. “Tolerance” refers to the allowed difference in length between multiple traces sharing the same variable name.

3.4 Optional Clock Layout

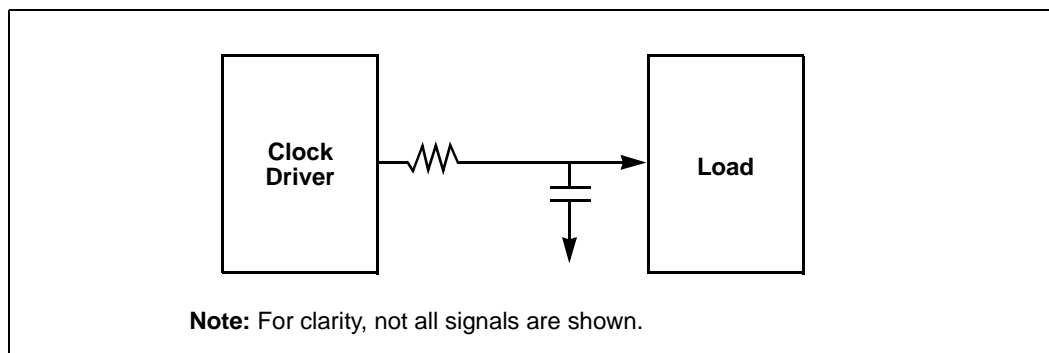
Figure 8 illustrates an optional clock layout implementation to accommodate tuning the HCLK, SDRAMCLK, and PCLK clocks from CK100 generators. Individual clock signals can be tuned to minimize EMI and to allow for variations in impedance, skew and loading. Refer to the *Intel® Mobile EMI Design Guide*.

The variables to be considered include:

- Variation in actual device load
- Line and load impedance variation
- Driver output impedance
- Vendor variation

Minimize the stub to the capacitor. The maximum stub length on a clock trace is < 0.5 inches. The capacitor should be placed as close as possible to the load. Refer to the clock vendor specifications for layout and termination guidelines.

Figure 8. General Clock Layout



3.5 Clock Vendors

- International Microcircuits, Inc.
525 Los Coches Street
Milpitas, CA. 95035
(408) 263-6300
- Integrated Circuit Systems, Inc.
1271 Parkmoor Avenue
San Jose, CA. 95126-3448
(408) 925-9460
- Cypress Semiconductor Corporation
3901 North First Street
San Jose, CA 95134
(408) 943-2600

Note: Companies and products are listed by Intel as a convenience to Intel's general customer base; Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality or compatibility of these companies and products. This list may be subject to change without notice. Listed companies and products in no way constitute a recommendation of products

or companies by Intel, but rather indicate a potential source for products. Other companies may offer additional products of interest.

4.0 Memory Guidelines

4.1 Mobile DRAM Interface Overview

The 440MX chipset integrates a main memory DRAM controller that supports a 64-bit DRAM array for mobile environments. Synchronous DRAM is the only memory type supported; Extended Data Out (EDO) memory is NOT supported. The DRAM interface operates at 100 MHz. The DRAM controller interface is fully configurable through a set of control registers. Complete descriptions of these registers are given in the 440MX chipset BIOS specification.

The 440MX chipset supports industry-standard 64-bit wide, 144-pin SO-DIMM modules with SDRAM devices. Both symmetric and asymmetric addressing are supported. For write operations of less than a Qword in size, the 440MX chipset performs byte-wide writes. The 440MX chipset supports 100 MHz SDRAM with a CAS Latency of two or three, and supports one- and two- row SO-DIMMs. The 440MX chipset supports only self-refresh SDRAM and can be configured via the paging policy register to keep multiple pages open within the memory array. Pages can be kept open in all rows of memory. When using two-bank SDRAM devices in a particular row, up to two pages can remain open within that row. The chipset supports up to 256 Mbytes of memory.

The 440MX chipset's DRAM interface is configured by the DRAM control registers, DRAM timing register, SDRAM control register, bits in the NBXCFG and four DRAM row boundary (DRB) registers. The DRAM configuration registers noted above control the DRAM interface to select RAS timing and CAS rates. The four DRB registers define the size of each row in the memory array, enabling the 440MX chipset to assert the proper CS# for accesses to the array.

4.2 DRAM Interface Signals

The 440MX chipset's memory interface consists of the following signals:

MA[13:0]	Memory address signals
MD[63:0]	Memory data signals
CS[3:0]#	Chip select control signals
DQM[7:0]	Byte enable signals
CKE[3:0]	Clock enable signals
SRAS#	Row control signal
SCAS#	Column control signal
WE#	Write enable control signal

4.3 Mobile DRAM Layout Guidelines

- The DRAM expansion socket for mobile platforms is the 144-pin SO-DIMM.
 - MA[11] should be connected to pin 106 of the SO-DIMM connector.
 - MA[12] should be connected to pin 70 and pin 110 of the SO-DIMM connector.
 - MA[13] should be connected to pin 72 and pin 112 of the SO-DIMM connector.
- For on-board 64 Mbit SDRAM devices on the motherboard, MA[11] should be connected to A13/BA0 and MA[13] should be connected to A11 on the SDRAM device.
- The memory data byte lanes may be swapped to simplify board routing and minimize trace lengths (be sure to also swap the appropriate DQM signals). This can also be done for the data bits within a byte lane.
- Board impedance should be $55 \Omega \pm 15\%$.
- All resistors should be maximum 5% tolerance.
- Trace widths for memory signals should be 5 mil.
- Populate farther SO-DIMM first to avoid stub reflections.
- Any on-board memory should be located farther away from 440MX chipset than a SO-DIMM connector.
- Place on-board DRAM and SO-DIMM connectors as near as possible to each other.

Figure 9 and Figure 10 provide two examples of routing the 440MX chipset memory interface to on-board memory and SO-DIMM memory modules.

Figure 9. 440MX Chipset Memory Interface Routed to One or Two On-Board Memory Banks, One SO-DIMM Connector

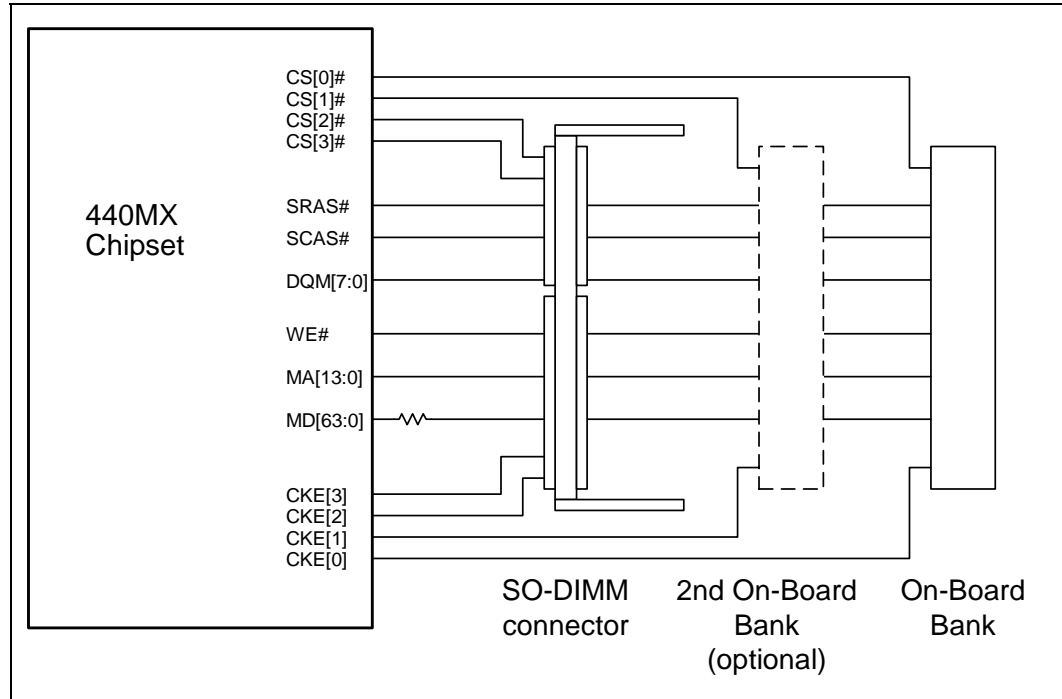
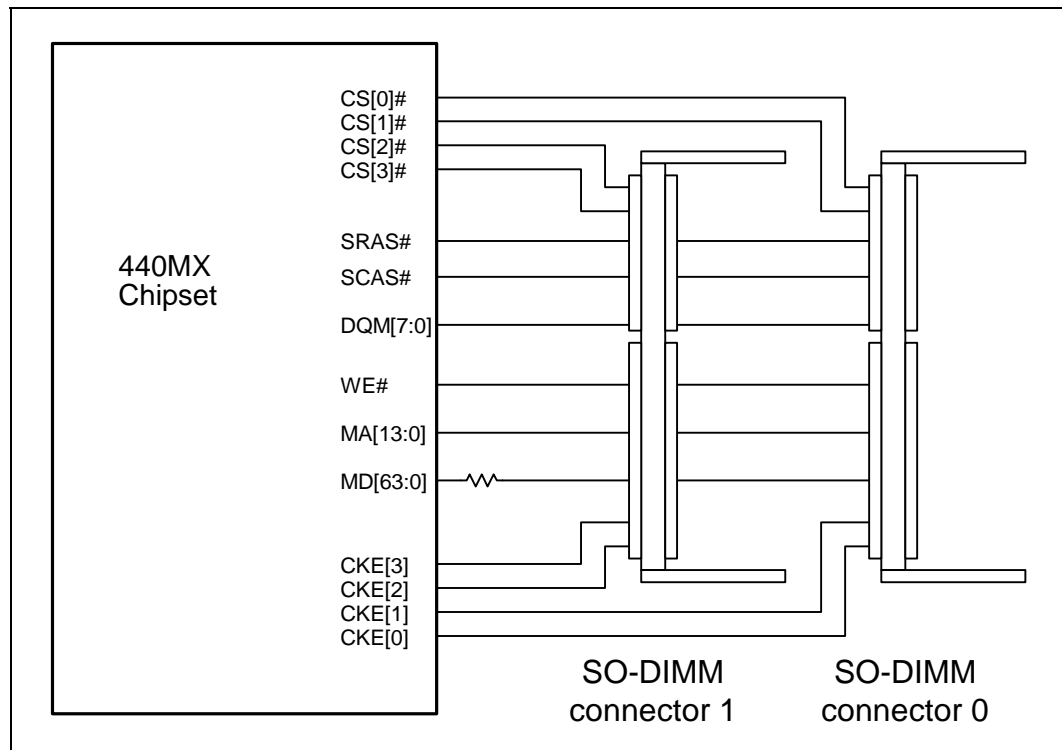


Figure 10. 440MX Chipset Memory Interface Routed to Two SO-DIMM Connectors





4.3.1 100-MHz Memory Trace Lengths (With CK100 Clock Generator)

Memory traces should follow the guidelines set in the *Low-Power Module SDRAM DIMM Routing Guidelines Application Note* (order number 273317), which are summarized in this section. Table 3 provides the minimum and maximum trace lengths to the SO-DIMM connector for each signal group (excluding clocks) for a CK100 design. Traces should have 1:2 spacing on inner layers and an impedance of $55 \Omega \pm 10\%$. Trace widths should be 5 mils. For memory clock routing guidelines, see “Clocking Guidelines” on page 12. Note that these guidelines are based on signal integrity and signal edge rates. A designer should evaluate whether resistors on additional signal(s) would be required for EMI or other concerns.

Table 3. SDRAM Interface Trace Lengths With CK100 Clock Generator

Signal	Min. Length		Max. Length		Damping Resistor
	(inches)	(mm)	(inches)	(mm)	
MA[13:0], WE#, SRAS#, SCAS#					
440MX chipset to first slot	1.0	25.4	3.6	91.4	none required
between slots	0.0	0.0	0.6	15.2	none required
total length	1.0	25.4	3.6	91.4	none required
CKE[3:0]	1.0	25.4	3.25	82.5	none required
CS[3:0]#	1.0	25.4	4.0	101.6	none required
DQM[7:0]# (440MX chipset to first slot)	1.0	25.4	4.0	101.6	none required
DQM[7:0]# (between slots)	0.0	0.0	1.0	25.4	none required
DQM[7:0]# (total length)	1.0	25.4	4.0	101.6	none required
MD[63:0] (440MX chipset to damping resistor)	0.0	27.9	1.0	25.4	10 Ω \pm 5%
MD[63:0] (from damping resistor to first slot)	1.0	25.4	4.0	101.6	
MD[63:0] (total length)	0.0	0.0	4.0	101.6	

The 440MX chipset supports setting some options on power-up reset by strapping resistors on some MA lines (see “440MX Chipset Strapping Options” on page 30 for details). Stubs created by routing to these pullup or pulldown resistors should be less than 0.1 inches (2.54 mm) in length.

5.0 Design Checklists

The checklists in this section are intended for schematic reviews of 440MX chipset and Mobile Pentium III processor-based platform designs. It does not represent the only way to design the system, but does provide Intel’s recommendations. The system designer should examine the checklist items for accuracy.

Pull-up and pull-down resistor values are system dependent. The appropriate value for a specific system can be determined from an AC/DC analysis of the pull-up voltage, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the input high/low voltage specifications, the input timing specifications (RC rise time), etc. Analysis should be done to determine the minimum/maximum values that may be used on an individual signal. Cost concerns, commonality considerations, manufacturing issues, specifications and other considerations must be evaluated to determine the optimal value.

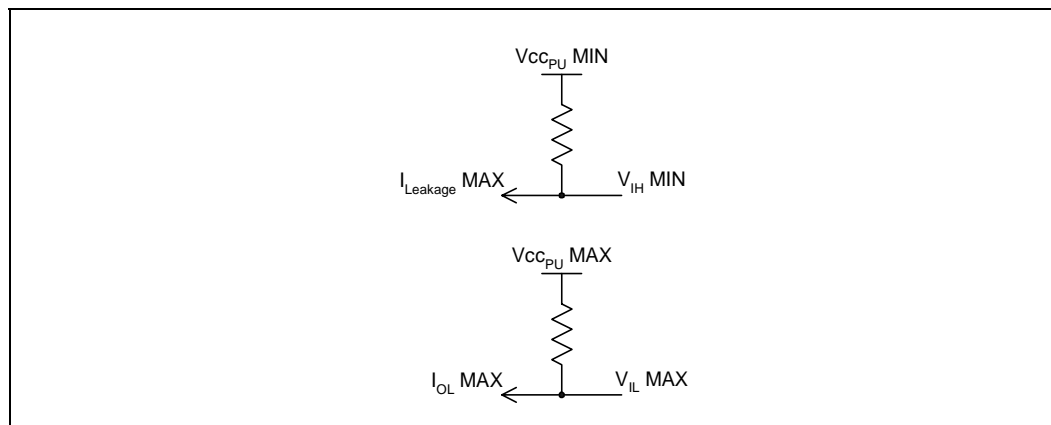
Simplistic DC calculations for pull-up values can be performed using the following equations:

$$R_{MAX} = (V_{CCPU\ MIN} - V_{IH\ MIN}) / I_{Leakage\ MAX}$$

$$R_{MIN} = (V_{CCPU\ MAX} - V_{IL\ MAX}) / I_{OL\ MAX}$$

Figure 11 shows an example of the minimum and maximum pull-up resistor configurations.

Figure 11. Pull-up Resistor Example



5.1 Mobile Pentium® III Processor

This section provides design requirements specific to the 440MX chipset and the Mobile Pentium III processor. Refer to Section 5.2 for information about the interfaces between the 440MX chipset and the processor.

5.1.1 Mobile Pentium® III Processor Errata

Please see the *Mobile Pentium® III Processor Specification Update* (order number 245306) for workarounds of any errata that may be present for a particular stepping.

5.1.2 Power and Ground Pins

The following voltage planes supply power to the Mobile Pentium III processor or its interfaces:

- V_{CC} pins supply power to the processor core logic.
- V_{CCT} supplies voltage for the processor GTL+ interface including the internal pull-up resistors.
- V_{CCT_IO} supplies power to the processor sideband signals, though this voltage is not supplied directly to the processor core.
- V_{REF} pins provide a reference voltage for the processor GTL+ interface. V_{REF} is also supplied to the 440MX chipset. See Figure 12 and Table 4 for reference voltages.
- CMOSREF provides a reference voltage for CMOS input buffers.
- CLKREF provides a reference voltage to define the trip point for the BCLK signal.
- The voltage ID signals (VID[4:0]) should have pull-up resistors that are connected to a power supply which is guaranteed to be stable when power to the core is stable.
- The Mobile Pentium III processor does not require a 3.3 V supply.

Refer to the *Mobile Intel® Pentium® III Processor in BGA2 and Micro-PGA2 Packages Featuring Intel SpeedStep® Technology at 1 GHz, 900 MHz, 850 MHz, 800 MHz, 750 MHz, 700 MHz, Low-voltage 700 MHz, Low-voltage 600 MHz, and Ultra Low-voltage 500 MHz* datasheet for a list of power, ground, test, and reserved/no connect pins as well as precise values and tolerances for these voltage planes.

Figure 12. Circuit for Generating Reference Voltages

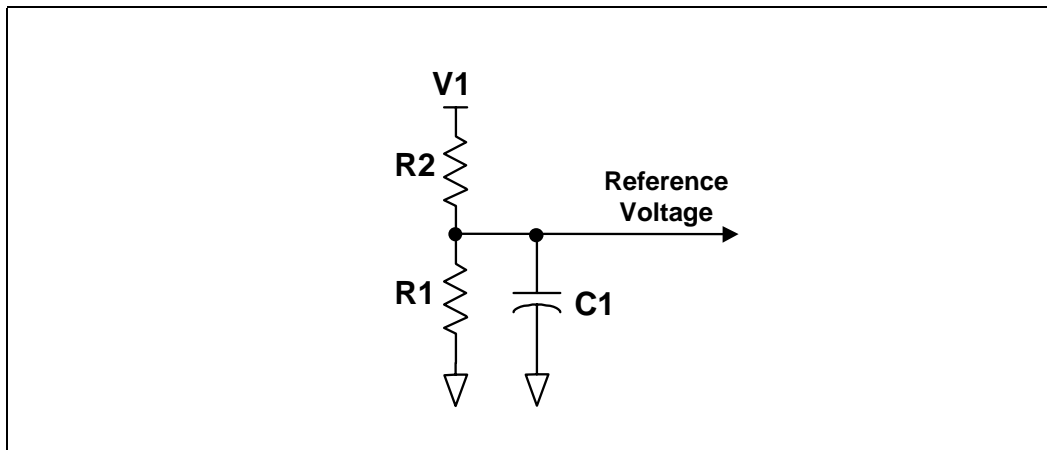


Table 4. Values for Reference Voltages

Reference Voltage	Target Voltage (V)	V1 (V)	R1 (KΩ) (recommended)	R2 (KΩ) (recommended)	Tolerance (each resistor)	C1
V _{REF}	2/3 V _{CCT}	V _{CCT_IO}	2.0	1.0	1%	At least seven 0.1 μF high frequency decoupling capacitors
CMOS _{REF}	1.0	V _{CLK}	1.0	1.5	1%	At least two 0.1 μF high frequency decoupling capacitors
CLK _{REF}	1.25	V _{CLK}	2.0	2.0	1%	At least one 0.1 μF high frequency decoupling capacitor

5.1.3 Decoupling Requirements

1. The amount of bulk decoupling required to meet the voltage tolerance requirements for the Mobile Pentium III processor is a strong function of the power supply design. Contact your Intel Field Sales Representative for tools to help determine how much decoupling is required. The processor core power plane (V_{CC}) should have at least forty 0.1 μF high frequency decoupling capacitors. The GTL+ power plane (V_{CCT}) requires 300 μF of bulk decoupling and at least twenty 0.1 μF high frequency decoupling capacitors.
2. The low power GTL+ voltage reference power plane (V_{REF}) should have at least seven 0.1 μF high frequency decoupling capacitors.
3. The low power CMOS reference power plane (CMOS_{REF}) should have at least two 0.1 μF high frequency decoupling capacitors.
4. The low power 2.5 V reference power plane (CLK_{REF}) should have at least one 0.1 μF high frequency decoupling capacitor.

5.1.4 Clock and Test Signals

1. See Section 3.0 for clocking guidelines.
2. Ensure that the clock generation logic to the Mobile Pentium III processor is at 2.5 V (BCLK, PICCLK (if used), and TCK (if used)).
3. All signals named NC and RSVD must be left unconnected.
4. TESTHI is for testing only; pull up to V_{CCT} with a 1.5 KΩ resistor.
5. TESTLO signals are for testing only; tie these signals to V_{SS} (1 KΩ resistor is not required).

5.1.5 Processor Signals

1. Refer to “Processor System Bus (PSB)” on page 31 and “Processor Sideband Signals” on page 31 for design information on the processor system bus interface and the processor side-band signals.
2. Ensure that the Mobile Pentium III processor inputs are not being driven by 3.3 V or 5 V logic. Logic translation of 3.3 V or 5 V signals may be accomplished using open-drain drivers pulled up to the appropriate voltage.

3. All reserved pins must be unconnected.
4. Unused CMOS active low inputs should be connected to V_{CCT_IO} through 1.5 K Ω resistors and unused active high inputs should be connected to V_{SS} through 1 K Ω resistors. Unused CMOS outputs may be left unconnected.
5. The Mobile Pentium III processor includes a new signal, EDGCTRLP, to configure the edge rate of the low power GTL+ output buffers. Connect EDGCTRLP to V_{SS} with a 110 Ω , 1% resistor.
6. The Mobile Pentium III processor includes two pins, BSEL[1:0], to set the processor system bus speed. Tie BSEL1 directly to V_{SS} and BSEL0 to V_{CCT_IO} with a 1.5 K Ω resistor.
7. The Mobile Pentium III processor implements an ITP port supporting the IEEE JTAG specification. TDI should have only one 150 Ω pull-up to V_{CCT_IO} if it is being used. If it is not used then it should have a 1 K Ω pull-down resistor. TCK and TMS should each have only one 1 K Ω pull-up to V_{CCT_IO} if they are being used. If they are not used, then they should have a 1 K Ω pull-down resistor. TRST# should have only one 680 — 1 K Ω pull-down whether or not it is being used. For further information about ITP or the Debug Port, refer to the *Mobile Intel® Pentium® III Processor in BGA2 and Micro-PGA2 Packages Featuring Intel® SpeedStep® Technology at 1 GHz, 900 MHz, 850 MHz, 800 MHz, 750 MHz, 700 MHz, Low-voltage 750MHz, Low-voltage 700MHz, Low-voltage 600 MHz, Ultra Low-voltage 600 MHz and Ultra Low-voltage 500 MHz* datasheet.
8. PWRGOOD is a 2.5 V tolerant input. It is expected that this signal will be a clear indication that clocks and the power supplies (V_{CC} , V_{CCT} , V_{CCT_IO} , etc.) are stable and within their specifications. It is highly recommended that the PWRGOOD signal from the power supply *not* be connected directly to logic on the board without first going through Schmitt trigger type circuitry to square-off and maintain the signal integrity of PWROK.
9. If the local APIC is hardware disabled, PICCLK and PICD[1:0] should be tied to V_{SS} with a 1-K Ω resistor. One resistor can be used for the three signals. Otherwise PICCLK must be driven with a clock that meets specification and the PICD[1:0] signals must be pulled up to V_{CCT} with 150- Ω resistors, even if the local APIC is not used.
10. At reset, the state of the A15# signal configures the processor for quick start state or stop grant state. The 440MX chipset will drive this signal to the correct value.
11. The GHI# signal tells the processor which Intel SpeedStep Technology-enabled mode to operate in. This signal has an internal pull-up and can be left disconnected in a non-Intel SpeedStep Technology enabled system. In an Intel SpeedStep Technology-enabled system, connect this to the control logic. Note the processor will always boot in the battery optimized mode regardless of the level of this signal at startup.
12. PRDY# and RESET# may not meet the layout requirements for Low Power GTL+. If they do not then they must be terminated using dual termination, which is 120 Ω termination at each end. (Refer to the *Mobile Intel® Pentium® III Processor in BGA2 and Micro-PGA2 Packages Featuring Intel® SpeedStep® Technology at 1 GHz, 900 MHz, 850 MHz, 800 MHz, 750 MHz, 700 MHz, Low-voltage 750MHz, Low-voltage 700MHz, Low-voltage 600 MHz, Ultra Low-voltage 600 MHz and Ultra Low-voltage 500 MHz* datasheet.)
13. The Mobile Pentium III processor has no power sequencing requirements. It is recommended that all of the processor power planes rise to their specified values within one second of each other.

5.2 440MX Chipset Design Checklist

This section provides 440MX chipset design information.

5.2.1 440MX Chipset Errata

Please see the *Intel® 82443MX PCIsset Specification Update* (order number 245051) for workarounds of any errata that may be present for a particular stepping.

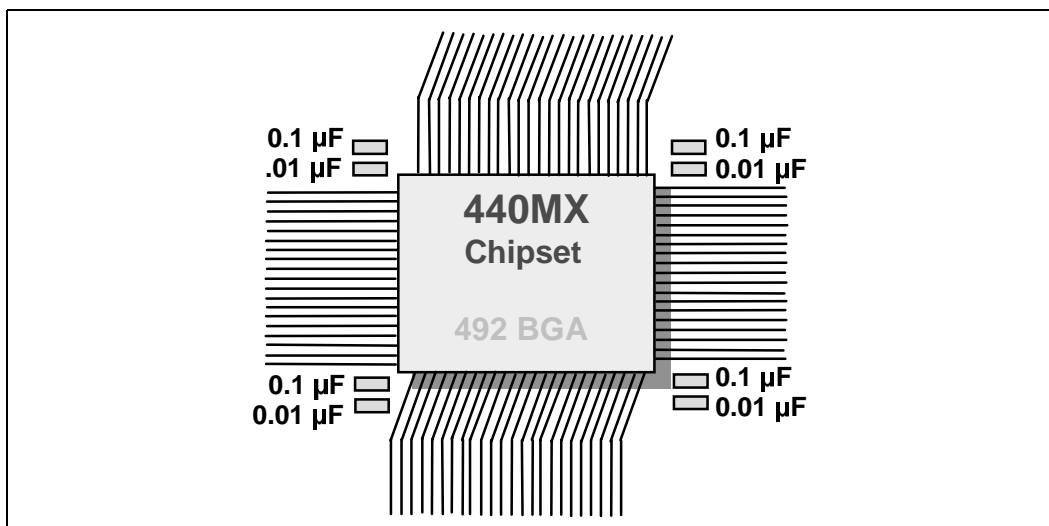
5.2.2 440MX Chipset Power and Ground Pins

1. Power plane terminology is included here for use with the recommendations provided in this section.
 - V3 is a 3.3 V power plane controlled by SUSC#. It is on during power-on suspend (POS, ACPI S1 or S2), suspend-to-RAM (STR, ACPI S3), and off in suspend-to-disk (STD, ACPI S4) and soft-off (SOFF, ACPI S5).
 - V3S is a 3.3 V power plane controlled by SUSB#. It is on during POS and off in STR, STD, and SOFF.
 - V5 is a 5 V power plane controlled by SUSC#. It is on during POS and STR, off in STD and SOFF.
 - V5S is a 5 V power plane controlled by SUSB#. It is on during POS and off in STR, STD, and SOFF.
 - V3RSM is a 3.3 V power plane that is on whenever 440MX chipset's resume logic is active.
 - V3RTC is a power plane that supplies power to 440MX chipset's real time clock and CMOS RAM. It should always be on to maintain power to the RTC and CMOS RAM.
 - V_{CCT_IO} supplies power to the processor sideband signals; it is not directly supplied to 440MX chipset.
2. The 440MX chipset's V_{CC}(CORE) pins provide power to the core logic; supply these pins with V3.
3. The 440MX chipset's V_{CC}(USB) pins supply power to the USB host controller; supply these pins with V3RSM. Can also use V3, but ensure the power supplied to V_{CC}(USB) is clean.
4. The 440MX chipset's V_{CC}(RSM) pins supply power to the resume logic; supply these pins with V3RSM.
5. The 440MX chipset's V_{CC}(RTC) pins supply power to the RTC and CMOS RAM circuitry; supply these pins with V3RTC.
6. The 440MX chipset's V_{5REF} pin is a 5 V reference voltage. V_{5REF} must be tied to 5 V in a 5 V tolerant system. This signal must be powered up before or simultaneous to V_{CC}(CORE), and it must be powered down after or simultaneous to V_{CC}(CORE). Note that since V_{CC}(CORE) is powered by V3, V_{5REF} should be powered by V5 and not V5S. V_{5REF} can be tied to V_{CC}(CORE) in a non-5 V tolerant system; however, note that most IDE drives are 5 V only.
7. If additional GTL+ termination is required (i.e., a logic analyzer connector is used), supply with V_{CCT} (same as processor GTL+ voltage).
8. V_{REF} is a reference voltage for the GTL+ interface and can be shared with the V_{REF} for the processor.

5.2.3 440MX Chipset Decoupling Guidelines

Decoupling capacitors should be placed at the corners of the 440MX chipset μ BGA package (see Figure 13). A minimum of four to eight 0.1 μ F capacitors with four to eight 0.01 μ F or 0.001 μ F capacitors should be used, depending on how quiet the system's power planes are and other specific EMI considerations.

Figure 13. 440MX Chipset Decoupling



Note: There are other discrete components for V_{CCT} , I_{O} , GTL reference voltages that must be also considered when routing around the 440MX chipset.

5.2.4 440MX Chipset Strapping Options

Table 5. 440MX Chipset Strapping Options

Pin Name	Function	Low	High	Internal Resistor	Status Register
MA12#	System frequency select	66 MHz	100 MHz	pull-down	NBXCFCG[13]
MA11#	In-Order Queue Depth Enable	1 (no pipelining)	4 (max)	pull-up	NBXCFCG[2]
MA10	Quick Start Select	Stop Clock Mode	Quick Start Mode	pull-up	PMCR[3]
MA8#	Reserved			pull-down	
MA13#	CPU clock ratio: sets NMI	NMI low	NMI high	pull-down	
MA9#	CPU clock ratio: sets INTR	INTR low	INTR high	pull-down	
MA7#	CPU clock ratio: sets IGNNE#	IGNNE# low	IGNNE# high	pull-down	
MA1#	CPU clock ratio: sets A20M#	A20M# low	A20M# high	pull-down	

NOTES:

1. Internal resistors are 50 K Ω pull-up or pull-down.
2. Use external resistors of 10 K Ω to configure modes.
3. Strapping option pull-ups should be to V3.
4. This document assumes MA12# has a pull-up enabling 100 MHz operation.

The bus ratio is programmed into the processor during manufacturing and cannot be overridden.

5.2.5 440MX Chipset Clock and Test Signals

1. See Section 3.0 for clocking guidelines.
2. Do not mix HCLK, PCICLK, and SDRAMCLK signals coming from the CK100 devices in R-packs; use discrete resistors.
3. USB Clock - 48 MHz with a duty cycle of better than 40%/60% should be fed into 440MX chipset's USB clock input.
4. TEST# is in the resume well (not RTC well). Pull high to V3RSM with a 10 KΩ resistor.

5.2.6 Processor System Bus (PSB)

1. Termination of the Low Power GTL+ bus is not necessary for the Mobile Pentium III processor unless a logic analyzer connector is present.
2. All unused low power GTL+ signals should be left unconnected.
3. Note that processor address and data bus signals are logically inverted signals. The actual values are inverted from what appears on the CPU bus.

5.2.7 Processor Sideband Signals

The processor sideband signals require pull-up resistors as indicated in Table 6. Note that unused inputs should be pulled to their inactive values. Unused outputs may be left unconnected.

Since the side-band signal FERR# is an input to the 440MX chipset, it needs to be voltage translated using a FET or PNP transistor. One method of this is shown in Figure 14.

Figure 14. Voltage Translation of FERR#

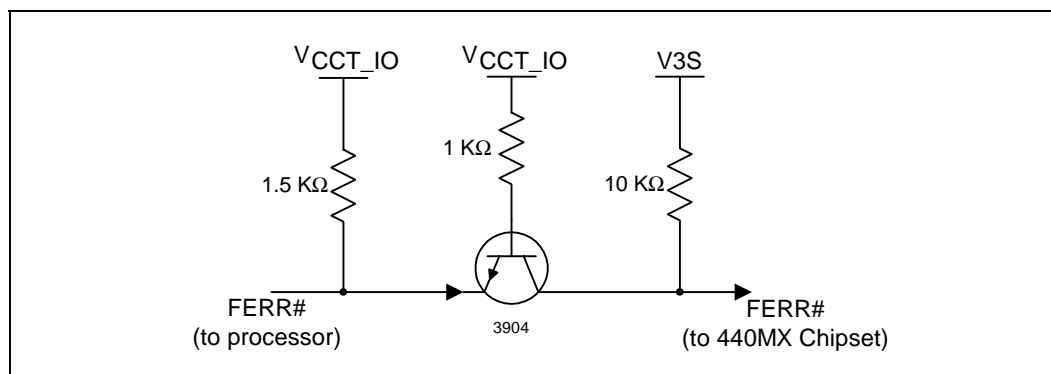


Table 6. Processor Sideband Signals

Signal	Function	Pull-up/Pull-down Resistor	Notes
A20M#	Address 20 Mask	1.5 K Ω pull-up to V _{CCT_IO}	
FERR#	Floating Point Error	1.5 K Ω pull-up to V _{CCT_IO}	
FLUSH#	Flush	1.5 K Ω pull-up to V _{CCT_IO}	Not supported by 440MX chipset
GHI#	SpeedStep Technology	None	Pull-up internal to processor
IERR#	Internal Error	1.5 K Ω pull-up to V _{CCT_IO}	Not supported by 440MX chipset; pull-up resistor is optional
IGNNE#	Ignore Numeric Error	1.5 K Ω pull-up to V _{CCT_IO}	
INIT#	Initialization	1.5 K Ω pull-up to V _{CCT_IO}	
INTR	Interrupt	1.5 K Ω pull-up to V _{CCT_IO}	
NMI	Non Maskable Interrupt	1.5 K Ω pull-up to V _{CCT_IO}	
SLP#	Sleep	1.5 K Ω pull-up to V _{CCT_IO}	Not supported by 440MX chipset
SMI#	System Management Interrupt	1.5 K Ω pull-up to V _{CCT_IO}	
STPCLK#	Stop Clock	680 Ω pull-up to V _{CCT_IO}	

5.2.8 440MX Chipset SDRAM Memory Interface Signals

1. See Section 4.0 for memory guideline details.
2. All unused output memory signals should be left unconnected.
3. MD[63:0] should have series termination resistors. Resistor packs are recommended. See Section 4.0.
4. SDRAM control signals drive the memory array directly without any external buffers.
5. All the memory interface signals have a programmable buffer strength to optimize for different signal loading conditions.

5.2.9 440MX Chipset PCI Bus Signals

1. The south cluster of the 440MX chipset is logically hard-wired to IDSEL 18 (device 7). Do not use this IDSEL for other PCI devices. As with the 440BX AGPset, the host-to-PCI bridge is hard-wired to IDSEL 11 (device 0). Even though the 440MX chipset does not support AGP, a design should probably avoid IDSEL 12 (device 1), which is typically the IDSEL for an AGP bridge.
2. All IDSEL signals for motherboard PCI devices should have a 100 Ω series resistor at each device.
3. 440MX chipset's PCI interface is 5 V-tolerant but drives at only 3 V. The following pull-up recommendations assume the PCI bus is 3 V. Refer to the 440MX chipset datasheet or the PCI specification for pull-up values for a 5 V PCI bus.
4. In a 3.3 V PCI environment, provide 10 K Ω pull-ups resistors to V3S on FRAME#, TRDY#, STOP#, IRDY#, DEVSEL#, PLOCK#, and SERR# on the PCI bus.
5. 440MX chipset does not implement the PERR# pin. However, data parity errors are still detected and reported on SERR# (if enabled by SERRE).

6. The fourth PCI master REQ/GNT pair, PREQ[3]# and PGNT[3]#, are muxed with GPIO[29] and GPIO[30], respectively. If used as a PCI REQ/GNT pair, PREQ[3]# and PGNT[3]# should both have 10 KΩ pull-up resistors to V3S.
7. PC/PCI REQ/GNT pair REQA#/GNTA# are muxed with GPIO[2] and GPIO[3], respectively. If used as a PC/PCI REQ/GNT pair, pull up both of these signals to V3S with 10 KΩ resistors.
8. PCI interrupt C and D channels are muxed with GPIO[22] and GPIO[23], respectively. If used as PIRQ[C]# and PIRQ[D]#, they must be pulled up.
9. Serial IRQ signal SERIRQ is muxed with GPIO7. Pull up to V3S with a 10 KΩ resistor if used as SERIRQ.
10. CLKRUN#: An (8.2 K-10 KΩ) pull-up to V3S should be placed on the CLKRUN# signal.

Table 7. 440MX Chipset PCI Bus Signals

Signal	Termination Resistor	Pull-up or Pull-down Resistor
AD[31:0]	None	None
C/BE[3:0]#	None	None
FRAME#	None	10 KΩ pull-up to V3S
DEVSEL#	None	10 KΩ pull-up to V3S
IRDY#	None	10 KΩ pull-up to V3S
TRDY#	None	10 KΩ pull-up to V3S
STOP#	None	10 KΩ pull-up to V3S
LOCK#	None	10 KΩ pull-up to V3S
REQ[2:0]#	None	10 KΩ pull-up to V3S
GNT[2:0]#	None	10 KΩ pull-up to V3S if used
REQ3#/GNT3#	None	10 KΩ pull-up to V3S if used as PCI REQ/GNT (signals muxed with GPIO[29,30])
PAR	None	None
SERR#	None	10 KΩ pull-up to V3S
CLKRUN#	None	8.2 K - 10 KΩ pull-up to V3S
PCIRST#	None	None
REQA/GNTA	None	10 KΩ pull-up to V3S if used as REQA/GNTA (signals muxed with GPIO[2,3])
PIRQ[B:A]#	None	10 KΩ pull-up to V3S
PIRQ[D:C]#	None	10 KΩ pull-up to V3S if used as PCI interrupts (signals muxed with GPIO[22,23])
SERIRQ	None	10 KΩ pull-up to V3S if used as SERIRQ (signal muxed with GPIO[7])

5.2.10 440MX Chipset IDE Interface

1. 470 Ω pull-down resistor on pin 28 (CSEL) of the IDE connector. Support of Cable Select (CSEL) is a PC97 requirement. The state of the cable select pin determines the master/slave configuration of the hard drive at the end of the cable.
2. The primary IDE channel (the only channel supported by the 440MX chipset) uses IRQ14.
3. All signals running to IDE connectors must have series terminating resistors (33 Ω). These series termination resistors should be placed as close as possible to the 440MX chipset. If the distance between the 440MX chipset and the connector is greater than 4 inches, the terminating resistor should be placed within 1 inch of the 440MX chipset.
4. Series resistors may or may not be necessary on PIORDY. A system designer should perform simulations in order to determine if series resistors are required.
5. If using ISA reset signal RSTDRV from the 440MX chipset, it should be routed through a Schmitt trigger for RESET# signals to the IDE channel.
6. Ground pins 2, 19, 22, 24, 26, 30 and 40 of ATA connectors.
7. Do not connect pin 20 of the ATA connector.
8. Pin 34 of the ATA connector is PDIAG for the IDE interface; if multiple IDE connectors are used, connect each pin 34 together. If a single IDE connector is used, pin 34 can be left unconnected.
9. According to ATA-4 spec, a 10 K Ω pull-down resistor is required on PD7 to allow a host to recognize the absence of a device at power-up.

Table 8. 440MX Chipset IDE Signals

Name	Termination Resistor	Pull-up or Pull-down Resistor
PDCS1#	33 Ω	None
PDCS3#	33 Ω	None
PDA[2:0]	33 Ω	None
PDD[15:0]	33 Ω	10 K Ω pull-down resistor on PDD[7] only.
PDDACK#	33 Ω	None
PDDRQ	33 Ω	5.6 K Ω pull-down resistor
PDIOR#	33 Ω	None
PDIOW#	33 Ω	None
PIORDY	33 Ω (may not need)	1 K Ω pull-up resistor to V3S
CSEL (does not connect to the 440MX chipset)	None	470 Ω pull-down resistor

5.2.11 USB Interface

Refer to the *82371AB PIIX4 Application Note #1 USB Design Guide And Checklist* for the layout recommendations for USB, clock, over current detection circuit and general board layout recommendations.

5.2.12 AC'97 Interface

If the AC'97 interface is not used, leave these signals unconnected. Internal pull-up and pull-down resistors will ensure the unused AC'97 interface is not floating.

5.2.13 440MX Chipset X-bus Signals

1. The 440MX chipset implements a 5 V-tolerant, 3 V-drive X-bus interface. During Power-On-Suspend (POS), many X-bus signals are actively driven by the chipset. For this reason, if a design implements POS, X-bus signals should be pulled up to V3S to avoid unnecessary leakage. If POS is not supported, V5S is acceptable.
2. GPIO[6]/IRQ8# defaults to a GPIO; the IRQ8# function is in the resume well, but the GPIO[6] function is in the core well (see Section 5.2.15 for details). If used as IRQ8#, an external 10 KΩ pullup to V3RSM is required. If used as GPIO[6], an external pullup to V3 may be required to ensure a valid logic level.
3. DMA channel 3 signals, DREQ3 and DACK3#, are muxed with GPIO[27] and GPIO[28], respectively. If the DMA channel is used, pull DREQ3 down with a 4.7 KΩ resistor.
4. The 440MX chipset does not support an address enable signal AEN; instead, the chipset drives 0x00000 on the X-Bus address bus for DMA transactions, and there is no danger of address confusion. Tie AEN inactive low to devices that have AEN inputs. Alternatively, AEN can be generated externally using glue logic on the board to drive AEN when a DMA acknowledge signal is asserted.
5. ZEROWS# is muxed with GPIO[21]. If used as ZEROWS#, pull up with a 1 KΩ resistor to V3S.

Table 9. 440MX Chipset X-bus Signals

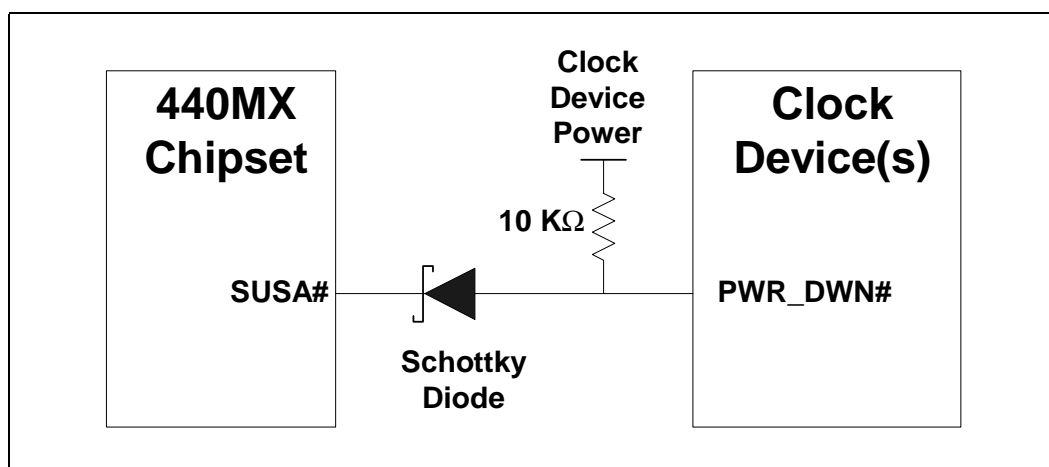
Name	Termination Resistor	Pull-up or Pull-down Resistor
IOCHRDY	None	1 KΩ pull-up resistor to V3S
IOR#/IOW#/MEMR#/MEMW#	None	4.7 KΩ pull-up resistors to V3S
RSTDRV	None	Pull-up
SA[18:0]	None	None
SD[7:0]	None	4.7 KΩ pull-up resistors to V3S
SYSCLK	None	None
ZEROWS#	None	1 KΩ pull-up resistor to V3S if used as ZEROWS# (signal is muxed with GPIO[21])
DRQ[2:0]	None	4.7 KΩ pull-down resistors.
DACK[2:0]#	None	None
DRQ3	None	4.7 KΩ pull-down resistor if used as DRQ3 (signal is muxed with GPIO[27])
DACK3#	None	None if used as DACK[3]# (signal is muxed with GPIO[28])
TC	None	None
IRQ[14,12,7:3,1]	None	10 KΩ pull-up resistor to V3S

5.2.14 Power Management Signals

1. Power management signals that reside in the suspend well requiring pull-up resistors must be pulled up to V3RSM. Note that these signals do not support 5 V input levels.
2. EXTSMI# is an input at reset and an open drain output if activating an SMI# within the Serial IRQ function. Designers may need an 8.2 K Ω pull-up to V3RSM if it is not always being driven to a valid state.
3. CLKRUN# requires a (8.2K -10 K Ω) pull-up to V3S.
4. PCI_STP# should be connected to the clock synthesizer to stop the PCI clocks.
5. CPU_STP# should be connected to the clock synthesizer to stop the processor clock.

SUSA# is connected to the clock synthesizer's PWR_DWN# pin through a Schottky diode with a 10 K Ω pull-up. Alternatively, SUSA# may be used to control the clock synthesizer's power plane.

Figure 15. SUSA# Connected to PWR_DWN# of Clock Synthesizer



6. SUSB#, SUSC# can be connected to control the power planes.
7. THERM# should be connected to the thermal protection logic.
8. RI# should be connected to the modem if this feature is used.
9. BATLOW# should be connected to the battery monitoring logic if the feature is implemented.
10. LID is connected to the lid monitoring logic of the system.
11. PWRBTN# should be connected to logic that allows the user to switch to and from suspend.
12. RSMRST# should be connected to a switch to allow a complete system reset. Note that this signal resides in the V_{CC}(RTC) well, hence its potential must not exceed that of V_{CC}(RTC).
13. SMBCLK and SMBDATA can be used as SMBus signals or I²C signals. When used in an SMBus environment, there are restrictions on the maximum capacitance and pull-up current on these signals. Refer to the *System Management Bus Specification* at www.smbus.org/specs.

5.2.15 General Purpose I/O Signals

The following are the rules that govern the functionality of the 440MX chipset's GPIOs:

1. GPIOs that are MUXed with functions default to the functional use EXCEPT for GPIOs that have the same alternate function as the PIIX4E (REQA#, GNTA#, SERIRQ, and IRQ8#), in which case they follow the PIIX4E programming model.
2. Some GPIOs are powered by the resume well (see #3 below). The rest are powered by the core well. GPIOs that are powered by the resume well can be programmed to retain their programming during STR and STD/SOFF (these GPIOs are reset by the assertion of RSMRST# and not PCIRST#) – i.e., inputs can be used to wake the system, and outputs can be programmed to retain their state. GPIOs that are powered by the core well will be three-stated during STR and are not powered during STD/SOFF.
3. GPIOs that default to functions powered by the resume well are only powered by the resume well when used as that default function. If used as a GPIO, those pins do not behave as if powered by the resume well (i.e., they do not retain their programming through STR and STD/SOFF).
4. GPIOs that default to GPIOs (not functional signals), default to inputs.
5. All unused GPIO signals should be pulled to a valid logic level with 10 K Ω resistors. If pulled high, they should be pulled to V3S except for the GPIOs that are in the resume well, which should be pulled to V3RSM.
6. All unused outputs can be left as no-connects.

Consider the default functional use of GPIOs when assigning active low and active high outputs to these pins. Note the power wells that supply the GPIOs and also consider this for assigning GPIOs that need to stay active through suspend. As noted above, GPIOs powered by the resume well can retain their values during STR and also STD/SOFF.

5.3 Transitioning from a 440BX AGPset to a 440MX Chipset Design

Logically, the 440MX chipset is similar to the 440BX AGPset with the following changes:

- The 440BX AGPset supports AGP; the 440MX chipset does not
- The 440BX AGPset supports EDO and SDRAM memory (not simultaneously); the 440MX chipset supports SDRAM only
- The 440BX AGPset supports six rows of memory; the 440MX chipset supports four rows of memory
- The 440BX AGPset supports two IDE channels; the 440MX chipset supports one IDE channel
- The 440MX chipset includes support for AC'97; the 440BX AGPset does not
- The 440MX chipset includes improved power management, especially with USB and GPIOs

Almost everything else is the same as for the 440BX AGPset, minimizing the changes required in transitioning a 440BX AGPset design to a 440MX chipset design. For complete details on the difference between the two chipsets, contact an Intel field sales representative.

