Intel® Celeron®/Intel® Pentium® III Processor - Low Power/Ultra Low Power (BGA2) and Intel® 815E Chipset

Design Guide

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1 Introduction

This document provides design guidelines for developing systems based on the Intel® Celeron® Processor – Low Power or Ultra Low Power or Intel® Pentium® III - Low Power in a BGA2 package and the Intel® 815E chipset. Special design recommendations and concerns are presented. Likely design errors have been listed here in a checklist format. These are recommendations only.

These design guidelines and recommendations have been simulated and validated and strongly recommended to meet the timing and signal quality specifications. It is recommended that simulations be performed to meet design-specific requirements.

Note: The system bus speed supported by the design is based on the capabilities of the processor, chipset, and clock driver.

1.1 Audience

This document is intended to be used by Intel® Celeron® or Intel® Pentium® III – LP/ULP/815E system developers.

1.2 Notation and Terminology

This section describes some of the terms used in this document.

Term	Description
AGP	Accelerated Graphics Port
GTL+	Refers to processor bus signals that are implemented open drain GTL+ interface signal.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL bus.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk–coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor signal. • Forward Crosstalk–coupling that creates a signal in a victim network that travels in the same direction as the aggressor signal. • Even Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk–coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
GMCH	Graphics and Memory Controller Hub. A component of the Intel® 815 chipset platform for use with Intel® Pentium III-Low Power and Intel® Celeron-Ultra Low Power/Low Power
ICH2	Intel® 82801BA I/O Controller Hub component.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network Length	The distance between agent 0 pins and the agent pins at the far end of the bus.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
Pin	The contact point of a component package to the traces on a substrate such as the motherboard. Signal quality and timings can be measured at the pin.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.

Term	Description
SSO	Simultaneous Switching Output (SSO) Effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "push-out"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets need to include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
System Bus	The system bus is the processor bus.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below V_{SS} at the device pad.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.

In this document, a '#' symbol after a signal name identifies the signal as active low; that is, a signal that is in the active state, based on the name of the signal, when driven to a low level. For example, when FLUSH# is low, a flush has been requested. When NMI is high, a non-maskable interrupt has occurred. When a signal name does not imply an active state, a # symbol indicates that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

The term "BGA2-based processor(s)" refers to the Intel® Celeron® processor-Ultra Low Power and Low Power in a BGA2 package and the Intel® Pentium® III processor-Low Power in a BGA2 package.

1.3 Reference Documents

The reader of this document needs to be familiar with the material and concepts presented in the following documents.

Document	Document Number / Location
Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) for use with the Universal Socket 370 Datasheet	298351
Intel® 82802AB/82802AC Firmware Hub (FWH) Datasheet	290658
Intel® 82801BA I/O Controller Hub (ICH2) *and Intel® 82801BAM I/O Controller Hub (ICH2-M) Datasheet*	290687
Intel® Pentium® III Processor-Low Power Datasheet	273500
Intel® Celeron® Processor-Ultra Low Power/Low Power Datasheet	273509
Intel® 815EM Chipset: 82815EM Graphics and Memory Controller Hub (GMCH2-M)	290689
Intel® 815EM Chipset Platform Design Guide	298241
Intel® 815E Chipset Platform Design Guide	298234
Intel® 815E Chipset Platform For Use With Universal Socket 370 Design Guide	298350
Accelerated Graphics Port Interface Specification, Revision 2.0	
PCI Local Bus Specification, Revision 2.2	
AC'97 2.1 Specification	http://developer.intel.com/pc-supp/platform/ac97/index.htm.
82562EH HomePNA 1 Mb/s Physical Layer Interface Datasheet	(Doc # 278313) http://developer.intel.com
82562EH HomePNA 1 Mb/s Physical Layer Interface Brief Datasheet	(Doc # 278314) http://developer.intel.com
Communication Network Riser Specification, Revision 1.1	http://developer.intel.com/technology/cnr/
Universal Serial Bus, Revision 1.0 Specification	

2 General Design Considerations

This section documents the example of a nominal board stack up for BGA2-based processor with the 815E platform.

Make sure the impedance for all signal layers is 60 Ω ± 15%. That is, the impedance of the trace when not subjected to fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace, based on the switching of neighboring traces. The use of wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

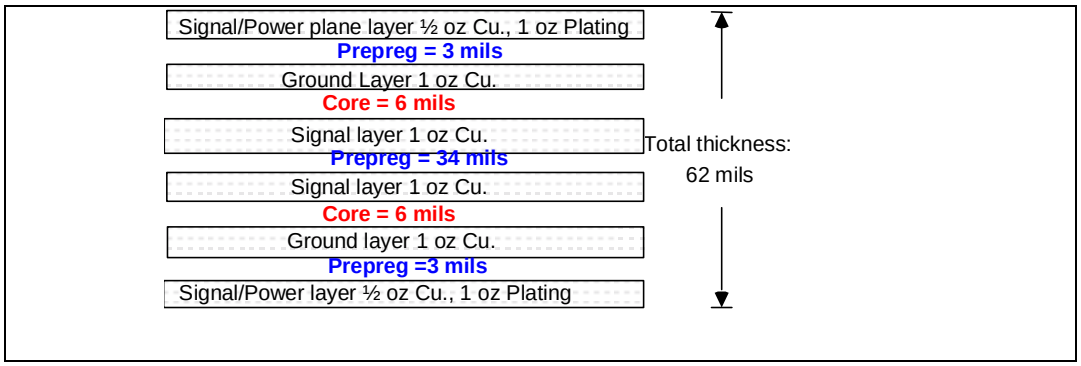
Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, follow the routing guidelines documented in this section.

The routing guidelines in this design guide have been created using a PCB *stack-up* similar to that in Figure 1. When this stack-up is **not** used, thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) makes routing very difficult or impossible.

2.1 Nominal Board Stack-up

The BGA2-based processor/815E platform requires a board stack-up yielding a target impedance of 60 Ω ± 15% with a 5 mil nominal trace width. Figure 1 shows an example stack-up achieving this. It is a 6-layer printed circuit board (PCB) construction using 53%-resin FR4 material.

Figure 1. Board Construction Example for 60 Ω Nominal Stack-up



Dieletric Constant for FR4 = 4.2
4 mils trace width for outer layers gives a 50 Ω signal impedance.
5 mils trace width for inner layers gives a 60 Ω signal impedance

Additional guidelines on board stack-up, placement, and layout include the following.

- The board impedance (Z) is 60 Ω ± 15%.
- The dielectric process variation in the PCB fabrication is minimized.
- The ground plane is not split on the ground plane layer.
- Keep vias for decoupling capacitors as close to the capacitor pads as possible.

3 Processor Host Bus Design

This section documents the layout and routing guidelines using the BGA2-based processor with the Intel® 815E chipset platform. The solution covers system bus speeds of 100 MHz only. The processor must also be configured to 56.2 Ω ± 1% on-die termination. The document does not discuss the functional aspect of any bus or the layout guideline for an add-in device.

When the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations be completed for each design. Even when the guidelines are followed, simulate critical signals to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely. Simulate any deviation from these guidelines.

3.1 Initial Timing Analysis

To determine the available flight time window, perform an initial timing analysis. Analysis of setup and hold conditions determine the minimum and maximum flight time bounds for the system bus. Use the following equations to establish the system flight time limits.

Table 1. System Timing Equations

Equation
$T_{flight,min} >= T_{hold} - T_{co,min} + T_{skew}$
$T_{flight,max} <= T_{cycle} - T_{co,max} - T_{su} - T_{skew} - T_{jit} - T_{adj}$

Table 2. System Timing Terms

Term	Description
T_{cycle}	System cycle time, defined as the reciprocal of the frequency.
$T_{flight,min}$	Minimum system flight time.
$T_{flight,max}$	Maximum system flight time.
$T_{co,max}$	Maximum driver delay from input clock to output data.
$T_{co,min}$	Minimum driver delay from input clock to output data.
T_{su}	Minimum setup time. Defined as the time for which the input data must be valid prior to the input clock.
T_{hold}	Minimum hold time. Defined as the time for which the input data must remain valid after the input clock.
T_{skew}	Clock generator skew. Defined as the maximum delay variation between output clock signals from the system clock generator, the maximum delay variation between clock signals due to system board variation and chipset loading variation.
T_{jit}	Clock jitter. Defined as maximum edge to edge variation in a given clock signal.
T_{adj}	Multi-bit timing adjustment factor. This term accounts for the additional delay that occurs in the network when multiple data bits switch in the same cycle. The adjustment factor includes such mechanisms as package and PCB crosstalk, high inductance current return paths, and simultaneous switching noise.

Table 3 lists the GTL+ component timings of the processors and GMCH defined at the pins for the Intel® 815E platform.

Note: These timings are for reference only. Obtain the processor specifications from respective processor datasheet and chipset values from the appropriate Intel® 815E chipset datasheet.

Table 3. Intel® Celeron® - Ultra Low Power and 82815E GMCH GTL+ Parameters for Example Calculations

IC Parameters	Intel® Celeron®-Ultra Low Power processor core at 100 MHz System Bus	82815E GMCH	Notes
Clock to Output maximum (T_{CO_MAX})	3.40	4.10	1,2
Clock to Output minimum (T_{CO_MIN})	0.20	1.05	1,2
Setup time (T_{SU_MIN})	1.20	2.65	1,2
Hold time (T_{HOLD})	1.20	0.10	1

NOTES:
1. All time in nanoseconds
2. **Numbers in table are for reference only.** These timing parameters are subject to change. Check the appropriate component documentation for valid timing parameter values.

Table 4 provides an example GTL+ initial maximum flight time and Table 5 is an example minimum flight time calculation for a 100 MHz, uni-processor system using the Intel® Celeron® -Ultra Low Power processor/Intel® 815E chipset system bus. Note that assumed values for clock skew and clock jitter were used. **Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.**

Table 4 and Table 5 are derived assuming:

- CLKSKEW = 0.20 ns (Note: Assumes clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together (“ganging”) at clock driver output pins, and the PCB clock routing skew is 150 ps. System timing budget must assume 0.175 ns of clock driver skew and 150 ps PCB clock routing skew if outputs are not tied together and a clock driver that meets the *CK815E Clock Synthesizer/ Driver Specification* is being used.)
- CLKJITTER = 0.250 ns

See the appropriate Intel® 815E chipset documentation, and *CK815E Clock Synthesizer/Driver Specification* for details on clock skew and jitter specifications. Exact details of host clock routing topology are provided with the platform design guideline.

Table 4. Example T_{FLT_MAX} Calculations For 100 MHz Bus

Driver	Receiver	Clk Period[2]	TCO_MAX	TSU_MIN	ClkSKEW	ClkJITTER	TADJ	Recommended TFLT_MAX
Processor	GMCH	10.00	3.40	2.65	0.20	0.25	0.50	3.000
GMCH	Processor	10.00	4.10	1.20	0.20	0.25	0.50	3.750

NOTES:
1. All times in nanoseconds
2. BCLK period = 10.00ns @ 100MHz

Table 5. Example T_{FLT_MIN} Calculations (Frequency Independent)

Driver	Receiver	THOLD	ClkSKEW	TCO_MIN	Recommended TFLT_MIN
Processor	GMCH	0.10	0.20	0.200	0.100
GMCH	Processor	1.20	0.20	1.050	0.350

The flight times in Table 4 include margin to account for the following phenomena that Intel observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect the flight time and signal quality and sometimes are not accounted for during simulation. Accordingly, the maximum flight times depend on the baseboard design, and additional adjustment factors or margins are recommended.

- SSO push-out or pull-in
- Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay
- Crosstalk on the PCB and inside the package which can cause variation in the signals

Additional effects exist that **may not necessarily** be covered by the multi-bit adjustment factor and need to be budgeted as appropriate to the baseboard design. These effects are included as T_{ADJ} in the example calculations in Table 4. Examples include:

- The effective board propagation constant (SEFF), which is a function of:
  - Dielectric constant (ε_r) of the PCB material
  - Type of trace connecting the components (stripline or microstrip)
  - Length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a component of the flight time, **but not necessarily equal to** the flight time.

3.2 General Topology and Layout Guidelines

Figure 2. Topology for BGA2 Designs with Single-Ended Termination (SET)

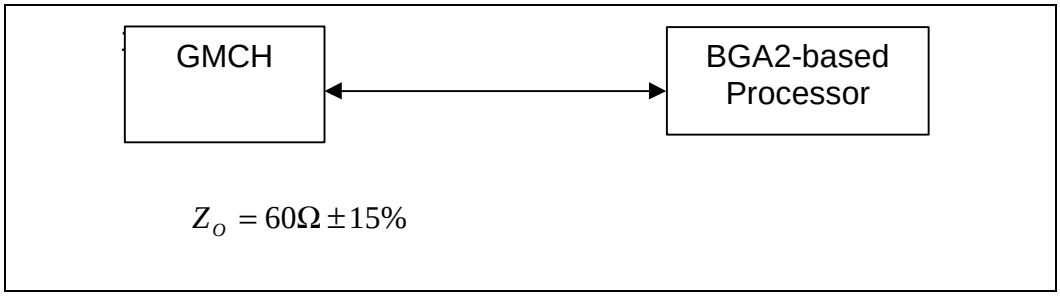


Table 6. Trace Guidelines Recommedation[1, 2, 3]

Description	Min. Length (inches)	Max. Length (inches)
GMCH to BGA2-based processor trace	3.50	5.00

NOTES:
1. Reference all GTL+ bus signals to the ground plane for the entire route.
2. Use an intragroup GTL+ spacing : line width : dielectric thickness ratio of at least 2:1:1 for microstrip geometry. If ε_r = 4.5, this limits coupling to 3.4%. For example, intragroup GTL+ routing could use 10 mils spacing, 5 mils trace width, and a 5 mils prepreg between the signal layer and the plane it references (assuming a 6-layer board design)
3. The recommended trace width is 5 mils, but not greater than 6 mils.

3.3 Simulation Methodology

3.3.1 Pre-Layout Simulation

Analog simulations are recommended for high-speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working “solution space” that meets flight time and signal quality requirements. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulations can be reduced.

Intel recommends running simulations at the device pads for signal quality and at the device pins for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

The BGA2-based processor and 815E I/O buffer models are available from Intel through your Intel representative.

3.3.2 Post-Layout Simulation

From the following layout, extract the traces and run simulations to verify that the layout meets timing and noise requirements. A small amount of trace “tuning” may be required, but experience at Intel has shown that a sensitivity analysis significantly reduces the amount of tuning required.

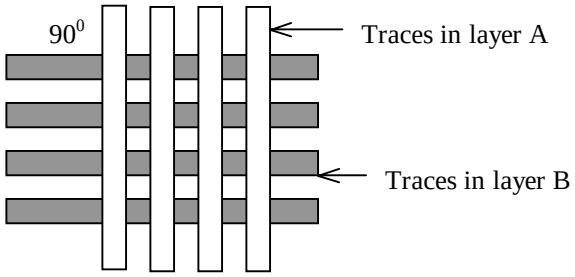
Take into account the expected variation for all interconnect parameters for the post layout simulations. Intel recommends running simulations at the device pads for signal quality and at the device pins for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

3.4 Layout Rules for GTL+ Signals

Ground Reference

It is strongly recommended that GTL+ signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide an effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane. Routing signals between two signals layers not separated by ground plan need to be implemented as shown in Figure 3.

Figure 3. Top view of a PCB layout



When a signal has to go through routing layers, the recommendations are:

Note: Following these layout rules is critical for GTL+ signal integrity, particularly for 0.18 micron and smaller process technology.

- For signals going from a ground reference to a power reference, add capacitors between ground and power near the vias to provide an AC return path. Use one capacitor for every three signal lines that change reference layers. Capacitor requirements are as follows: C=100nF, ESR=80mΩ, ESL=0.6nH.
- For signals going from one ground reference to another, separate ground reference, add vias between the two ground planes to provide a better return path.

Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance. Eliminate routing signal across split/cut plane. When a signal has to route across split plane, add capacitors between the split planes to ground.

Important note: It is strongly recommended **NOT** to route GTL+ signals across split/cut plane or changing reference plane resulted by traversing layers.

Processor Breakout

It is strongly recommended that GTL+ signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the processor on the same layer. When routing is tight, break out from the processor on the opposite routing layer over a ground reference and cross over to main signal layer near the processor.

Minimizing Crosstalk

The following general rules minimize the impact of crosstalk in a high-speed GTL+ bus design:

- Maximize the space between traces. Where possible, maintain a minimum of 10 mils (assuming a 5 mil trace) between trace edges. It may be necessary to use tighter spacing when routing between component pins. When traces must be close and parallel to each other, minimize the distance that they are close together and maximize the distance between the sections when the spacing restrictions are relaxed.
- Avoid parallelism between signals on adjacent layers, when there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since GTL+ is a low-signal-swing technology, it is important to isolate GTL+ signals from other signals by at least 25 mils. This avoids coupling from signals that have larger voltage swings (e.g., 5 V PCI).
- GTL+ signals must be well isolated from system memory signals. GTL+ signal trace edges must be at least 30 mils from system memory trace edges within 100 mils of the ball of the Intel® 82815 GMCH.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the GTL+ specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes crosstalk.
- Route GTL+ address, data, and control signals in separate groups to minimize crosstalk between groups. Keep at least 15 mils between each group of signals.
- Minimize the dielectric used in the system. This makes the traces closer to their reference plane and thus reduces the crosstalk magnitude.
- Minimize the dielectric process variation used in the PCB fabrication.
- Minimize the cross-sectional area of the traces. This can be done by means of narrower traces and/or by using thinner copper, but the trade-off for this smaller cross-sectional area is higher trace resistivity, which can reduce the falling-edge noise margin because of the I*R loss along the trace.

3.5 Layout Rules for Non-GTL+ (CMOS) Signals

Table 7. Routing Guidelines for Non-GTL+ Signals

Signal	Trace Width	Spacing to Other Traces	Trace Length
A20M#	5 mils	10 mils	1” to 9”
FERR#	5 mils	10 mils	1” to 9”
FLUSH#	5 mils	10 mils	1” to 9”
IERR#	5 mils	10 mils	1” to 9”
IGNNE#	5 mils	10 mils	1” to 9”
INIT#	5 mils	10 mils	1” to 9”
LINT[0] (INTR)	5 mils	10 mils	1” to 9”
LINT[1] (NMI)	5 mils	10 mils	1” to 9”
PICD[1:0]	5 mils	10 mils	1” to 9”
PREQ#	5 mils	10 mils	1” to 9”
PWRGOOD	5 mils	10 mils	1” to 9”
SLP#	5 mils	10 mils	1” to 9”
SMI#	5 mils	10 mils	1” to 9”
STPCLK	5 mils	10 mils	1” to 9”

NOTE: Route these signals on any layer or combination of layers.

3.5.1 Additional Routing and Placement Considerations

- Distribute V_{TT} with a wide trace. A 0.050 inch minimum trace is recommended to minimize DC losses. Route the V_{TT} trace to all components on the host bus. Be sure to include decoupling capacitors.
- The V_{TT} voltage need to be 1.25 V ± 3% for static conditions, and 1.25 V ± 9% for worst-case transient conditions.
- Place resistor divider pair for V_{REF} generation at the GMCH component. V_{REF} also is delivered to the processor.

3.6 Undershoot/Overshoot Requirements

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below V_{SS}. The overshoot guideline limits transitions beyond V_{CC} or V_{SS} due to the fast signal edge rates. The processor can be damaged by repeated overshoot events on buffers when the charge is large enough (i.e. when the overshoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline also makes satisfying the ringback specification difficult.

When performing simulations to determine impact of overshoot and undershoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and do not provide overshoot or undershoot protection. Refer to Intel® Celeron® Processor Low Power/Ultra Low Power and Intel® Pentium® III – Low Power datasheet for detailed undershoot/overshoot requirements.

3.7 Processor Reset Requirements

The BGA2-based processor designs must route the GTL+ reset signal from the chipset to the processor as well as to the debug port connector. The A6 (RESET) signal is connected to this pin for the Intel® Pentium® III processor (CPUID=068xh), Intel® Celeron® processor (CPUID=068xh)

Note: The GTL+ reset signal must always terminate to VTT on the motherboard.

Designs that do not support the debug port will not utilize the 240 Ω series resistor or the connection of RESET# to the debug port connector**.**

The routing rules for the GTL+ reset signal are shown in Figure 4.

Figure 4. RESET# Routing Guidelines

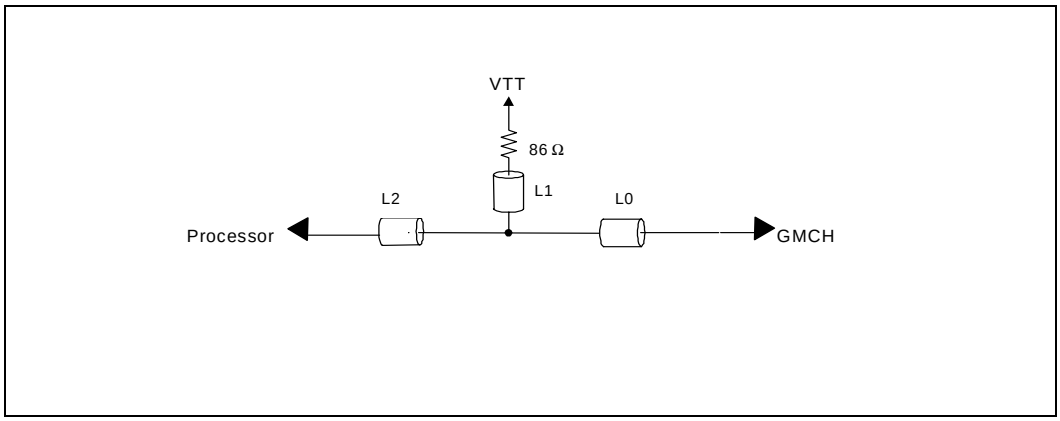


Table 8. RESET# Routing Guidelines (see Figure 4)

Parameter	Minimum (in)	Maximum (in)
L0	2.0	4.1
L1	0.5	1.5
L2	0.9	1.5
L0+L2	3.5	5.0

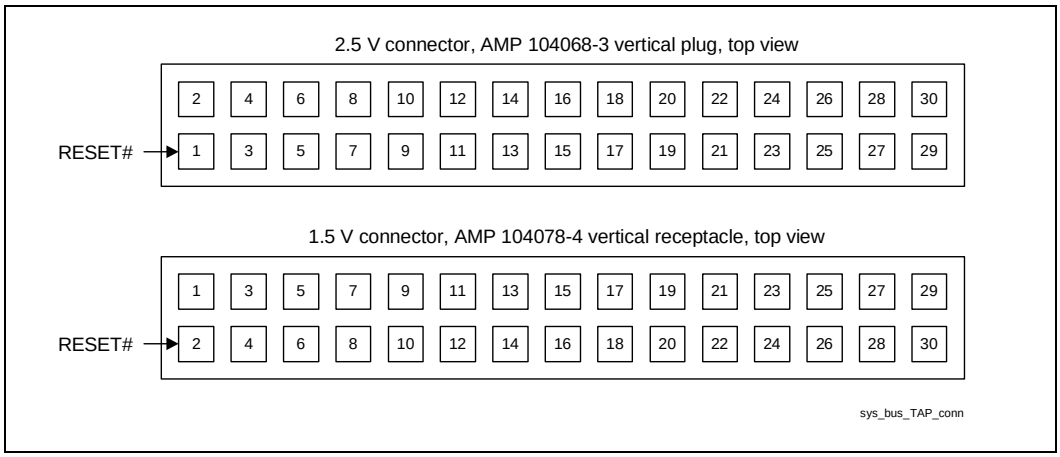
3.8 Debug Port Routing Guidelines

The Test Access Port (TAP) interface is an implementation of the IEEE 1149.1 ("JTAG") standard. Due to voltage levels supported by the TAP interface, Intel recommends that the Intel® Celeron® Processor-LP/ULP and Intel® Pentium® III Processor-LP and the other 1.5V JTAG specification compliant devices be last in the JTAG chain after any devices with 3.3 V or 5 V JTAG interfaces within the system. A translation buffer needs to be used to reduce the TDO output voltage of the last 3.3/5 V device down to the 1.5 V range that the processors can tolerate. Multiple copies of TMS and TRST# must be provided, one for each voltage level.

A Debug Port and connector may be placed at the start and end of the JTAG chain containing the processor, with TDI to the first component coming from the Debug Port and TDO from the last component going to the Debug Port. There are no requirements for placing the Intel® Celeron® Processor-ULP/LP and Intel® Pentium® III Processor-LP in the JTAG chain, except for those that are dictated by voltage requirements of the TAP signals.

The 1.5 V connector is a mirror image of the older 2.5 V connector. Either connector will fit into the same printed circuit board layout. Only the pin numbers change (Figure 5). Also required, along with the new connector, is an In-Target Probe* (ITP) that is capable of communicating with the TAP at the appropriate logic levels.

Figure 5. TAP Connector Comparison



Caution: The Intel® Pentium® III processor (CPUID=068xh) and Intel® Celeron® processor (CPUID=068xh) require an in-target probe (ITP) compatible with 1.5 V signal levels on the TAP. Previous ITPs were designed to work with higher voltages and may damage the processor when connected to any of these specified processors.

See the processor datasheet for more information regarding the debug port.

3.9 PLL Filter Recommendations

It is highly critical that phase lock loop power delivery to the processor meets Intel requirements. A low pass filter is required for power delivery to pins PLL1 and PLL2. This serves as an isolated, decoupled power source for the internal PLL.

3.9.1 Topology

The general desired topology for these PLLs is shown in Figure 6. Not shown are the parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitic associated with each component.

The following tables contain examples of components that meet Intel recommendations when configured in the topology of Figure6.

Table 9. Component Recommendations – Inductor

Part Number	Value	Tolerance	SRF	Rated Current	DCR (Typical)
TDK MLF2012A4R7KT	4.7 µH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max.)
Murata LQG21N4R7K00T1	4.7 µH	10%	47 MHz	30 mA	0.7 Ω (±50%)
Murata LQG21C4R7N00	4.7 µH	30%	35 MHz	30 mA	0.3 Ω max.

Table 10. Component Recommendations – Capacitor

Part Number	Value	Tolerance	ESL	ESR
Kemet T495D336M016AS	33 µF	20%	2.5 nH	0.225 Ω
AVX TPSD336M020S0200	33 µF	20%	2.5 nH	0.2 Ω

Table 21. Component Recommendation – Resistor

Value	Tolerance	Power	Note
1 Ω	10%	1/16 W	Resistor may be implemented with trace resistance, in which case a discrete R is not needed. See Figure.

To satisfy damping requirements, total series resistance in the filter (from V_{TT} to the top plate of the capacitor) must be at least 0.35 Ω. This resistor can be in the form of a discrete component or routing or both. For example, if the chosen inductor has minimum DCR of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance rule (2 Ω). For example, if using discrete R1 (1 Ω ± 1%), the maximum DCR of the L (trace plus inductor) is less than 2.0 – 1.1 = 0.9 Ω, which precludes the use of some inductors and sets a max. trace length.

Other routing requirements:

- The capacitor (C) is close to the PLL1 and PLL2 pins, < 0.1 Ω per route. These routes do not count towards the minimum damping R requirement.
- The PLL2 route is parallel and next to the PLL1 route (i.e., minimize loop area).
- The inductor (L) is close to C. Any routing resistance is inserted between V_{TT} and L.
- Any discrete resistor (R) is inserted between V_{TT} and L.

Figure 6. Example PLL Filter Using a Discrete Resistor

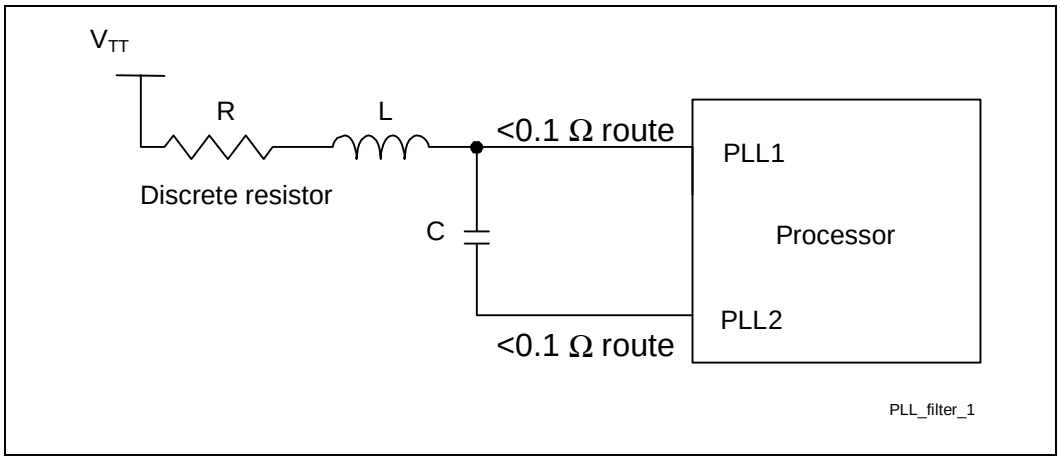
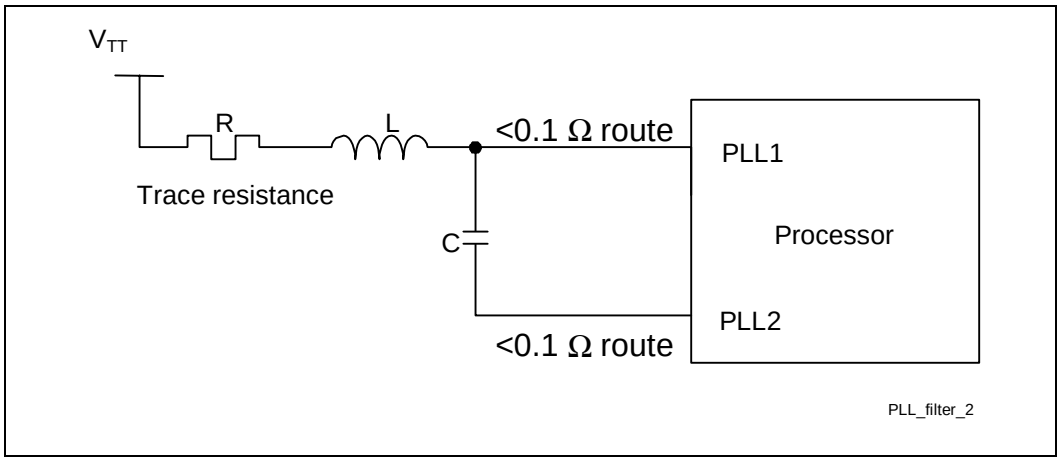


Figure 7. Example PLL Filter Using a Buried Resistor



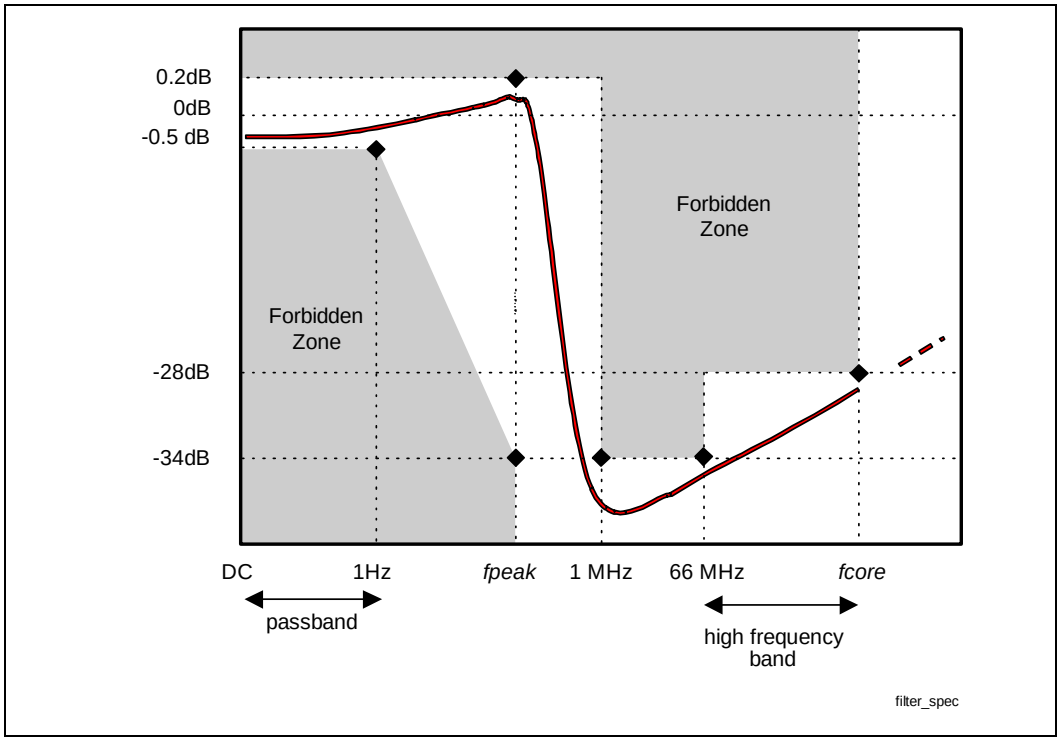
3.9.2 Filter Specification

The function of the filter is to protect the PLL from external noise through low-pass attenuation. The low-pass specification, with input at VCC_{CORE} and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter specification is graphically shown in Figure 8.

Figure 8. Filter Specification



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore*.
3. *fpeak* is less than 0.05 MHz.

Other requirements:

- Use shielded-type inductor to minimize magnetic pickup.
- Filter supports DC current > 30 mA.
- DC voltage drop from VCC to PLL1 is < 60 mV, which in practice implies series R < 2 Ω. This also means pass-band (from DC to 1 Hz) attenuation < 0.5 dB for V_{CC} = 1.1 V, and < 0.35 dB for V_{CC} = 1.5 V.

3.10 Decoupling Guidelines for BGA2-based Processors

The amount of bulk decoupling required on the V_{CC} and V_{CCT} planes to met the voltage tolerance requirements for the Intel® Celeron® Processor – Low Power or Ultra Low Power and Intel® Pentium® III Processor – Low Power are a strong function of the power supply design. Contact your Intel Field Sales Representative for tools to help determine how much bulk decoupling is required.

For 700 MHz processors, the following decoupling is recommended. The processor core power plane (V_{CC}) has fifteen 0.68µF 0603 ceramic capacitors (using X7R dielectric for thermal reasons) placed directly under the package using two vias for power and two vias for ground to reduce the trace inductance. Also to minimize inductance, traces to those vias are 22 mils (in width) from the capacitor pads to match the via-pad size (assuming 22-mil pad size). Twenty-four 2.2µF 0805, X5R mid-frequency decoupling capacitors placed around the die as close to the die as flex solution allows. The system bus buffer power plane (V_{CCT}) has twenty 0.1µF high-frequency decoupling capacitors around the die.

For 500 and 400 MHz processors, the processor core power plane (V_{CC}) has eight 0.1µF high-frequency decoupling capacitors placed underneath the die and twenty 0.1µF mid-frequency decoupling capacitors placed around the die as close to the die as flex solution allows. The system bus buffer power plane (V_{CCT}) has twenty 0.1µF high-frequency decoupling capacitors around the die.

For 300 MHz processors, the processor core power plane (V_{CC}) has eight 0.1µF high-frequency decoupling capacitors placed underneath the die and twenty 0.1µF mid-frequency decoupling capacitors placed around the die as close to the die as flex solution allows. The system bus buffer power plane (V_{CCT}) has twenty 0.1µF high-frequency decoupling capacitors around the die.

3.11 Catastrophic Thermal Protection

The Intel® Celeron® Processor – Low Power / Ultra Low Power and Intel® Pentium® III Processor – Low Power does not support catastrophic thermal protection or the THERMTRIP# signal. An external thermal sensor must be used to protect the processor and the system against excessive temperatures.

4 Clocking

4.1 General Clocking Considerations

The host bus clock signals are critical signals for the BGA2-based processor and 815E platform. The signal integrity and timing of these signals needs to be carefully evaluated and simulated.

In general, the following layout recommendation needs to be followed for the host bus clocks:

- It is recommended that system bus clocks be routed on the signal layer next to the ground layer (referenced to ground)
- It is strongly recommended that system bus clocks do not traverse multiple signal layers.
- System clock routing over power plane splits need to be eliminated.
- When necessary, grounded guard band traces can be routed next to clock traces to reduce cross talk to other signals.

4.2 Single-Ended Host Bus Clocking Routing

The BGA2-based processor and 815E platforms have support for using single-ended host bus clock driver. When using this clocking method, the BCLK signal is used as the single-ended clock input to the BGA2-based processor. The CLKREF signal is used as a reference voltage and must be connected to the appropriate filter circuit described in section 4.2.1

Figure 9 shows the topology recommended for the BGA2-based processor and 815E clock traces. Please note that section 1, section 2 and section 3 refer to trace length between the illustrated components. Table 12 contains the recommended length and component values for this topology.

Figure 9 Single-Ended Clocking Topology

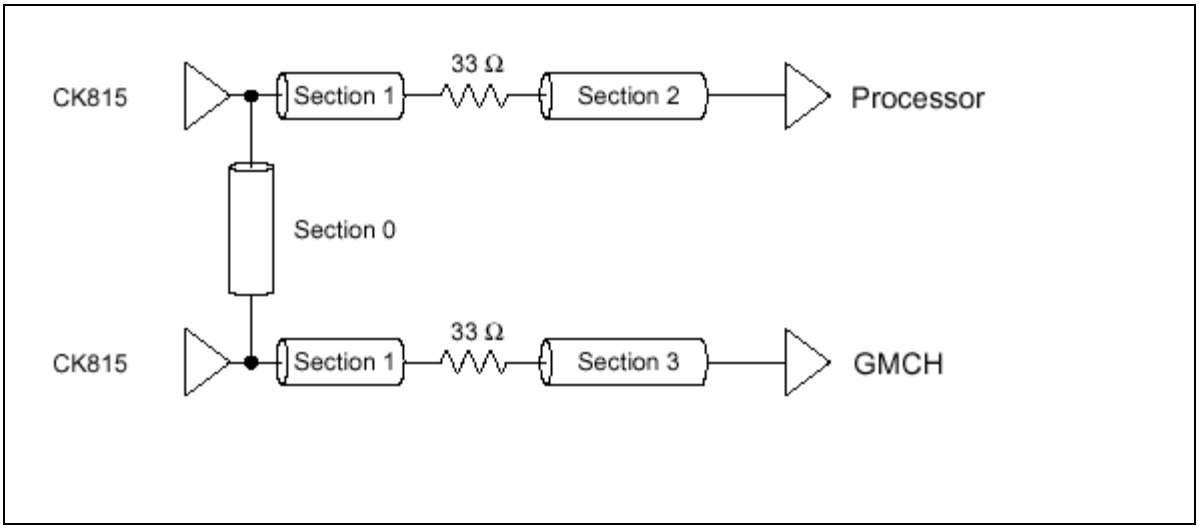


Table 12 Recommended Length for Single-Ended Clocking Topology

Destination	Section 0 Length	Section 1 Length	Section 2 Length	Section 3 Length
Processor BCLK	<0.1”	<0.5”	A + 5.2”	N.A.
GMCH HCLK	N.A.	<0.5”	N.A.	A + 8”

NOTES:
1. Length “A” has been simulated up to 6 inches. The length must be matched between SDRAM MCLK lines by ± 100 mils.
2. All length specific in inches

Clock Decoupling

Several general layout guidelines need to be followed when laying out the power planes for the CK815 clock generator, as follows:

- Isolate power planes to each of the clock groups.
- Place local decoupling as close as possible to power pins, and connect with short, wide traces and copper.
- Connect pins to appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling needs to be connected to a plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14 mils finished hole with a 24 mils to 26 mils pad. An example power via is an 18 mils finished hole with a 33 mils to 38 mils pad. For large decoupling or power planes with large current transients, a larger power via is recommended

4.2.1 CLKREF Filter Implementation

When using single-ended clocking mode, the CLKREF signal on the BGA2-based processor serves as a reference voltage to the clock input. To provide a steady reference voltage, a filter circuit must be implemented and attached to this pin. Figure 10 shows the recommended CLKREF filter implementation. The CLKREF filter need to be placed as close as possible (less than 1.0 inch) to the processor CLKREF pin.

Figure 10. Examples for CLKREF Divider Circuit

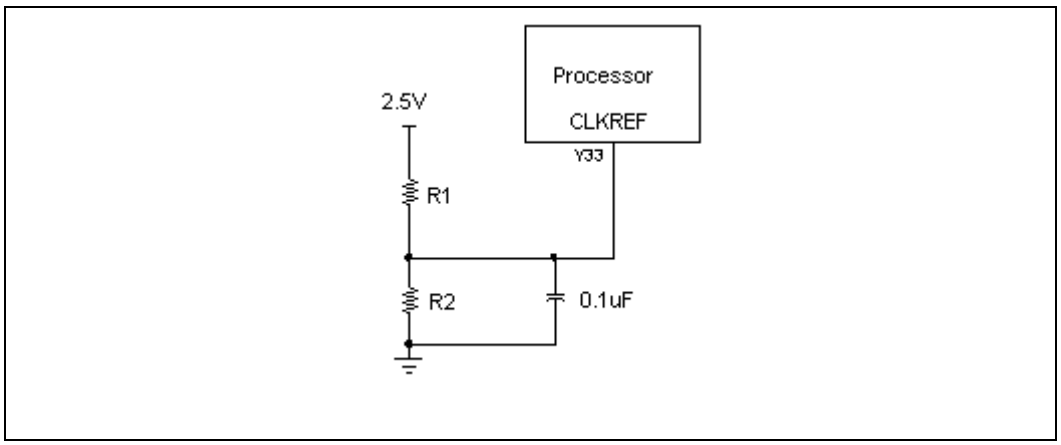


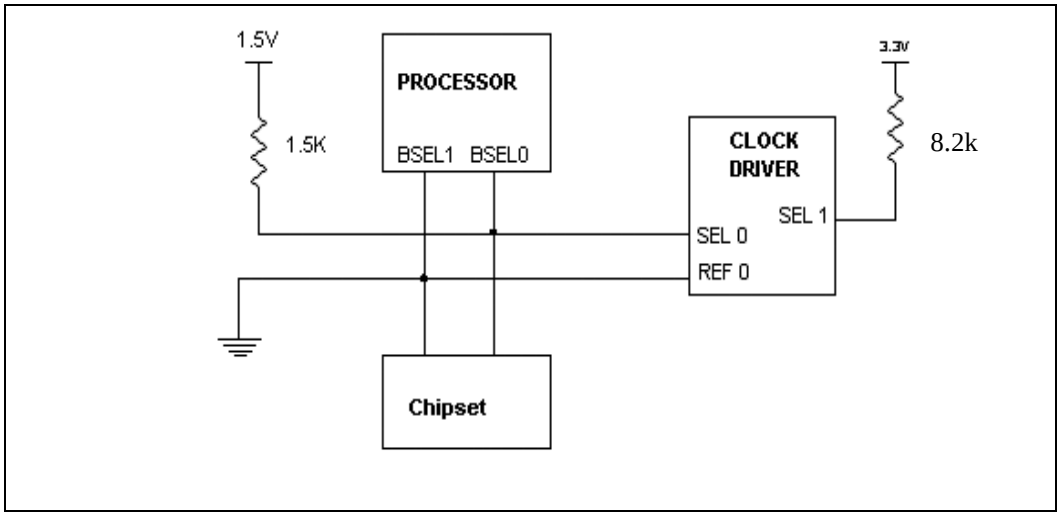
Table 13. CLKREF Component Values

R1 (Ω) ± 1%	R2 (Ω) ± 1%	CLKREF Voltage (V)
1k	1k	1.25

4.2.2 Single-Ended Clocking BSEL[1:0] Implementation

The BGA2-based processor and 815E platform is using single-ended clocking that only support 100 MHz system bus. In order to implement the 100 MHz system bus, BSEL0 needs to be pulled up to 1.5 V through a 1.5 KΩ 5% resistor and BSEL1 needs to be pulled down to GND. This strapping configures the clock generator to output 100 MHz clock to support a 100 MHz capable processor. Figure 11 shows a diagram of this implementation.

Figure 11. BSEL[1:0] Circuit Implementation for LP CopperMine processor Designs



4.2.3 Clock Driver Decoupling and Power Delivery

The decoupling and power delivery requirements of the system clock driver are dependent on the clock driver and chipset used in the system implementation. Because of this, no specific information can be provided in this document. However, since proper decoupling and noise-free power delivery are critical to the clock driver operation, Intel encourages system implementers to carefully follow the chipset and clock driver vendor recommendations in these areas. An incorrect implementation of these circuits can easily cripple clock driver recommendations in these areas and its ability to produce reliable clock signals and lead to system instability. Please refer to the appropriate clock driver and chipset vendor information for more details.

5 Processor Host Bus Design Checklist

5.1 Introduction

This checklist highlights design considerations that need to be reviewed prior to manufacturing a motherboard. This design checklist only provides the processor host bus signals design recommendation. It is not a complete list and does not guarantee that a design functions properly. Besides the items in the following text, refer to most recent version of the *Intel® 815E Chipset Platform For Use with Universal Socket 370 Design Guide* for more detailed instruction. This checklist is to be revised, as new information is available.

5.2 GTL+ Checklist

Table 14. GTL+ signals checklist

Checklist items	Recommendations
A[35:3]#	Connect to A[31:3]# to 815 GMCH. Leave A[35:32]# as N/C.
BNR#, BPRI#, D[63:0]#, DBSY#, DEFER#, DRDY#, HIT#, HITM#, LOCK#, REQ#[4:0], RS[2:0], TRDY#	Connect to 815 GMCH.
ADS#	Connect to 815 GMCH. For debug purpose, pull-up to VCCT through 56 Ω resistor, and placed within 150 mils of 815 GMCH
AERR#, AP[1:0]#, BERR#, BINIT#, BP[3:2]#, BPM[1:0]#, DEP[7:0]#, RP#, RSP#	Leave as N/C.
BREQ0#	10 Ω pull down to ground.
RESET#	Connect to 815 GMCH. Pull up to VCCT with an 86 Ω 1% resistor. Connect to ITP with 240 Ω series resistor near to ITP if ITP is used.

5.2.1 CMOS (Non-GTL+) Checklist

Table 15. CMOS (Non-GTL+) signals checklist

Checklist items	Recommendations
A20M#, IGNNE#, INTR, INIT#, NMI, SMI#, STPCLK#	Connect to ICH2.
FERR#, SLP#,	Connect to ICH2. Pull up to VCCT with a 1.5 KΩ resistor.
FLUSH#, IERR#, PREQ#	Pull up to VCCT with 1.5 K Ω resistor.
PWRGOOD	Pull up to 2.5V with 1.5 K Ω resistor.
PICD[1:0]	Connect to ICH2. Pull up to VCCT with a 150 Ω resistor.

5.3 TAP Checklist

Table 16. TAP signals checklist

Checklist items	Recommendations
TCK, TMS	Connect to ITP with 47 Ω series resistor. Pull up to VCCT with 1 KΩ resistor
TDI, TDO	Connect to ITP. Pull up to VCCT with a 150 Ω resistor.
TRST#	Connect to ITP. Pull down with 1 KΩ resistor to ground.
PRDY#	Connect to ITP with 240 Ω series resistor. Pull up to VCCT with 56.2 Ω resistor.
PRDY1#, PRDY2#, PRDY3#	Pull up to 1.5 V VCCT through 1 KΩ resistor.

5.3.1 Miscellaneous Checklist

Table 17. Miscellaneous signal checklist

BCLK	Connect to CK815 clock generator with 33 Ω series resistor (may vary depends on simulation). Tie both host clock outputs (to the processor and to the chipset) at the clock generator before routing out to processor and GMCH.
BSEL0	Pull up to VCCT with 1.5 KΩ 5% resistor (100 MHz PSB only).
BSEL1	Tie to ground (100 MHz PSB only).
CLKREF	Connect to voltage divider circuitry on 2.5 V to create 1.25 V reference. Decouple using 0.1 µF capacitor
EDGECTRLP	Pull down with 110 Ω resistor 1% to ground.
PICCLK	Connect to CK815E clock generator with 33 Ω series resistor (may vary depends on simulation).
PLL1, PLL2	Connect to PLL low pass filter circuit.
RTTIMPEDP	Pull down with 56.2 Ω resistor 1% to ground.
THERMDA, THERMDC	If thermal sensor is used, connect to thermal sensor. Else, leave as NC.
CMOSREF	Connect to voltage divider circuitry on 2.5 V to create 1V reference. Decouple using two 0.1 µF capacitors.
VID[4:0]	Connect 100 Ω resistor to GND.
VREF[7:0]	Connect to voltage divider circuit to VCCT with 2/3 ratio (75 Ω and 150 Ω, 1% resistors). Decouple with four 0.1 µF capacitors near processor. Also connect to 815 GMCH GTLREF[A,B] with two 0.1 µF decoupling capacitors at GMCH.
VCC_CORE	Processor core supply. See notes 1 and 2
VCCT	1.5 V supply.
VSS	Ground.
A15, A16, A17, C14, D8, D14, D16, E15, G2, G5, G18, H3, H5, J5, M4, M5, P3, P4, AA5, AA19, AC3, AC17, AC20, AD15, R2	No connect.

NOTES:

1. Refer to *Intel® Pentium® III Processor – Low Power 700Mhz, 500Mhz and 400Mhz Processors in BGA2 Package* for power supply decoupling requirement.
2. Refer to *Intel® Celeron® Processor – Low Power/Ultra Low Power 300MHz (ULP) and 400AMHz (LP) Processor in a BGA2 Package* for power supply decoupling requirement.

6 Reference Schematic

This section provide the reference schematic for Intel ® Celeron® Processor – Low Power or Ultra Low Power or Intel ® Pentium® III - Low Power in a BGA2 package and the Intel ® 815E chipset platform.

INTEL® PENTIUM® III LOW POWER & INTEL® CELERON (TM) ULTRA-LOW POWER PROCESSOR (BGA2) / INTEL® 815E CHIPSET

UNIPROCESSOR CUSTOMER REFERENCE SCHEMATICS

REVISION 0.5

** Please note these schematics are subject to change.

THESE SCHEMATICS ARE PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF PROPOSAL, SPECIFICATION OR SAMPLES.

	COVER SHEET		
Title	Low Power Intel® Celeron®/Pemtium® III with 815E		
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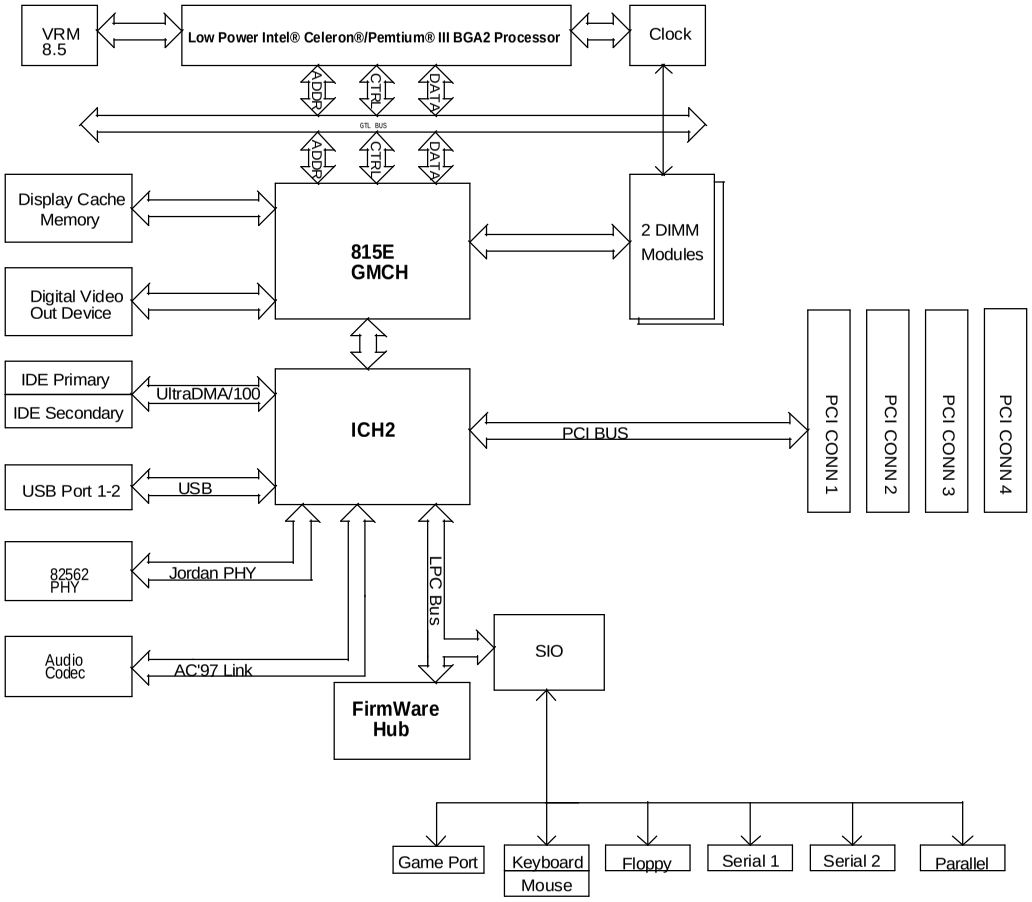
Block Diagram



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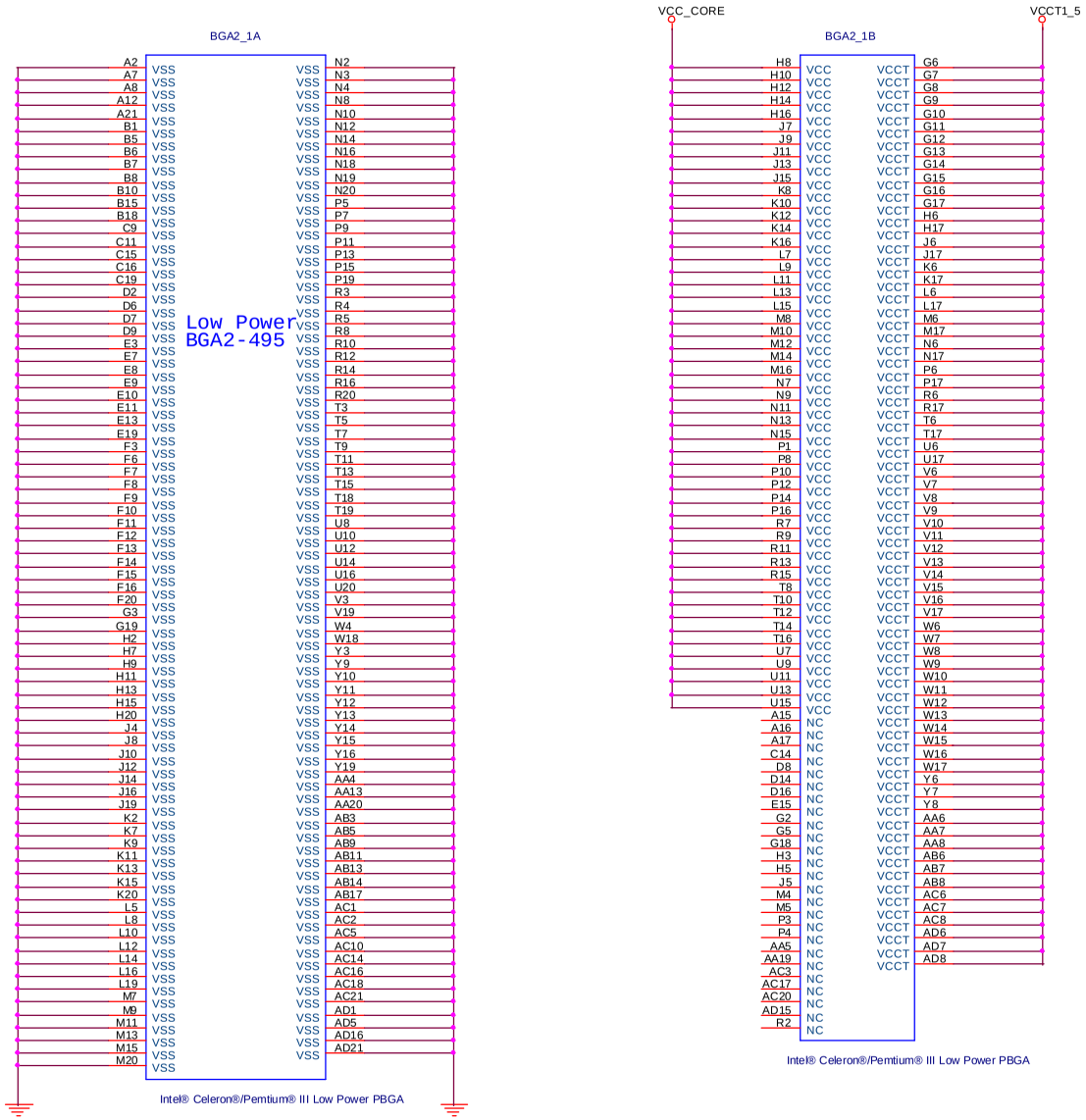

PROCESSOR PART 1

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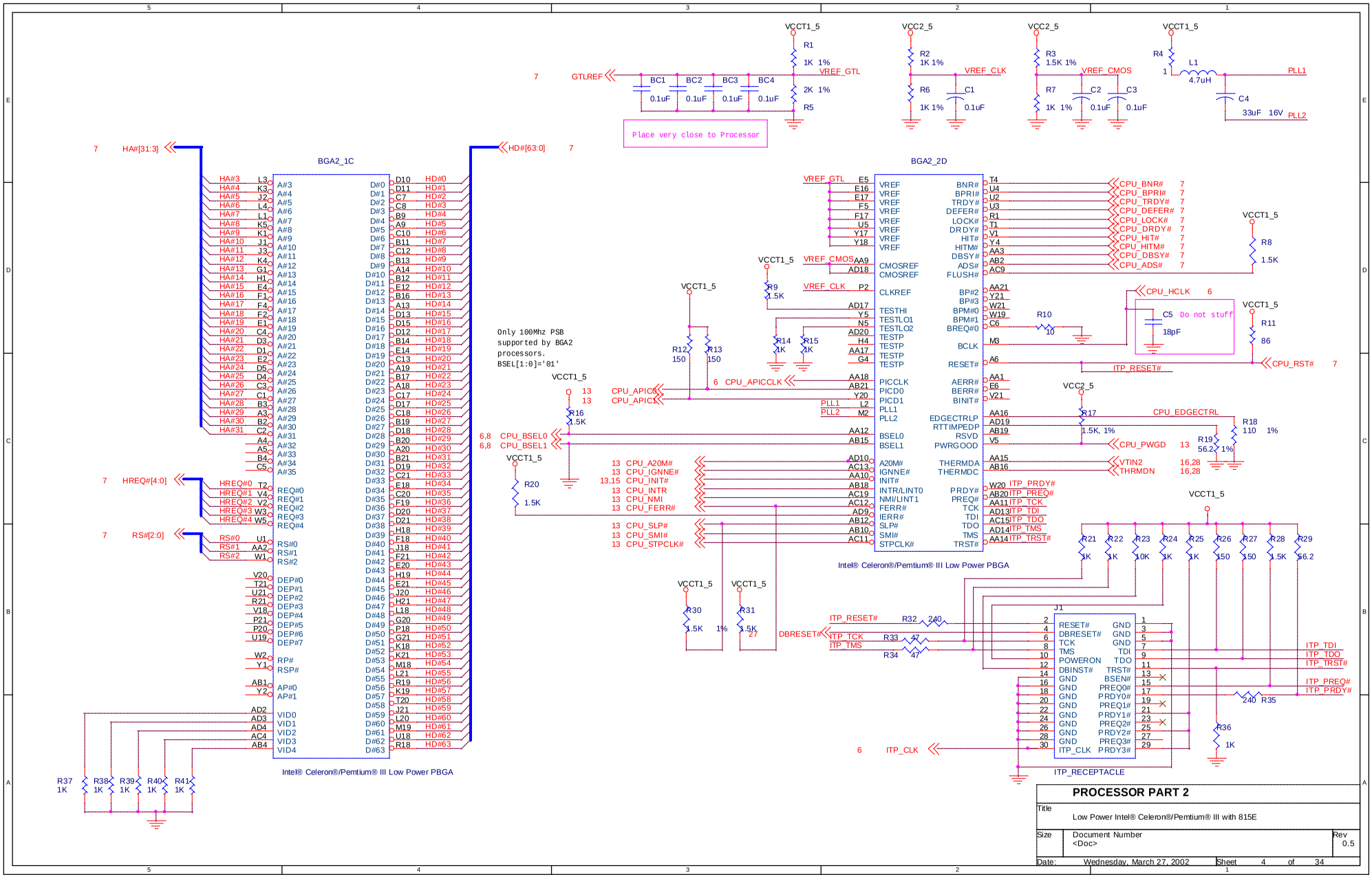
BGA2_1C
BGA2_2D
Intel® Celeron®/Pemtium® III Low Power PBGA
Intel® Celeron®/Pemtium® III Low Power PBGA
Only 100Mhz PSB supported by BGA2 processors.
BSEL[1:0]='01'
Place very close to Processor
ITP_RECEPTACLE
PROCESSOR PART 2
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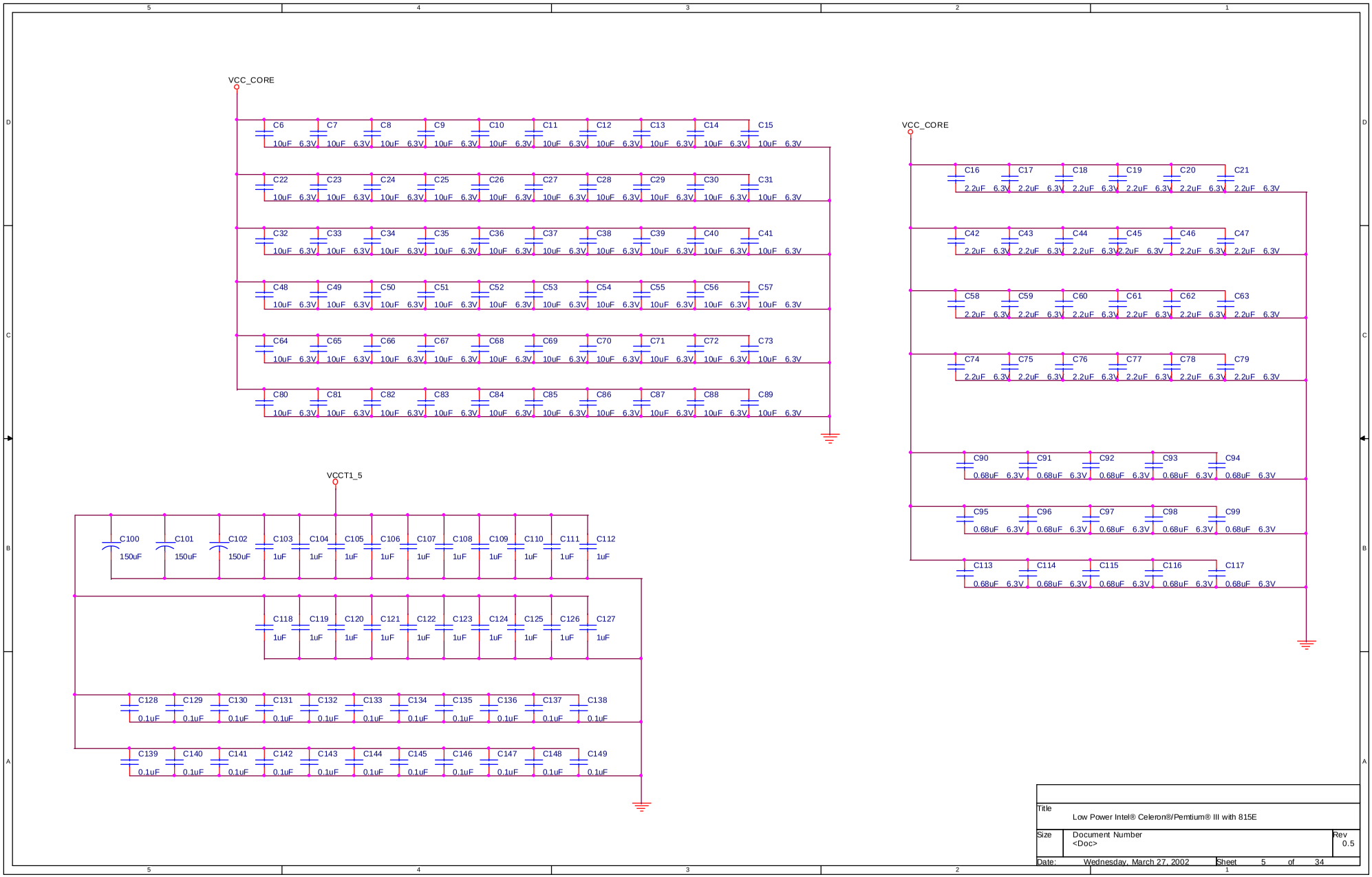

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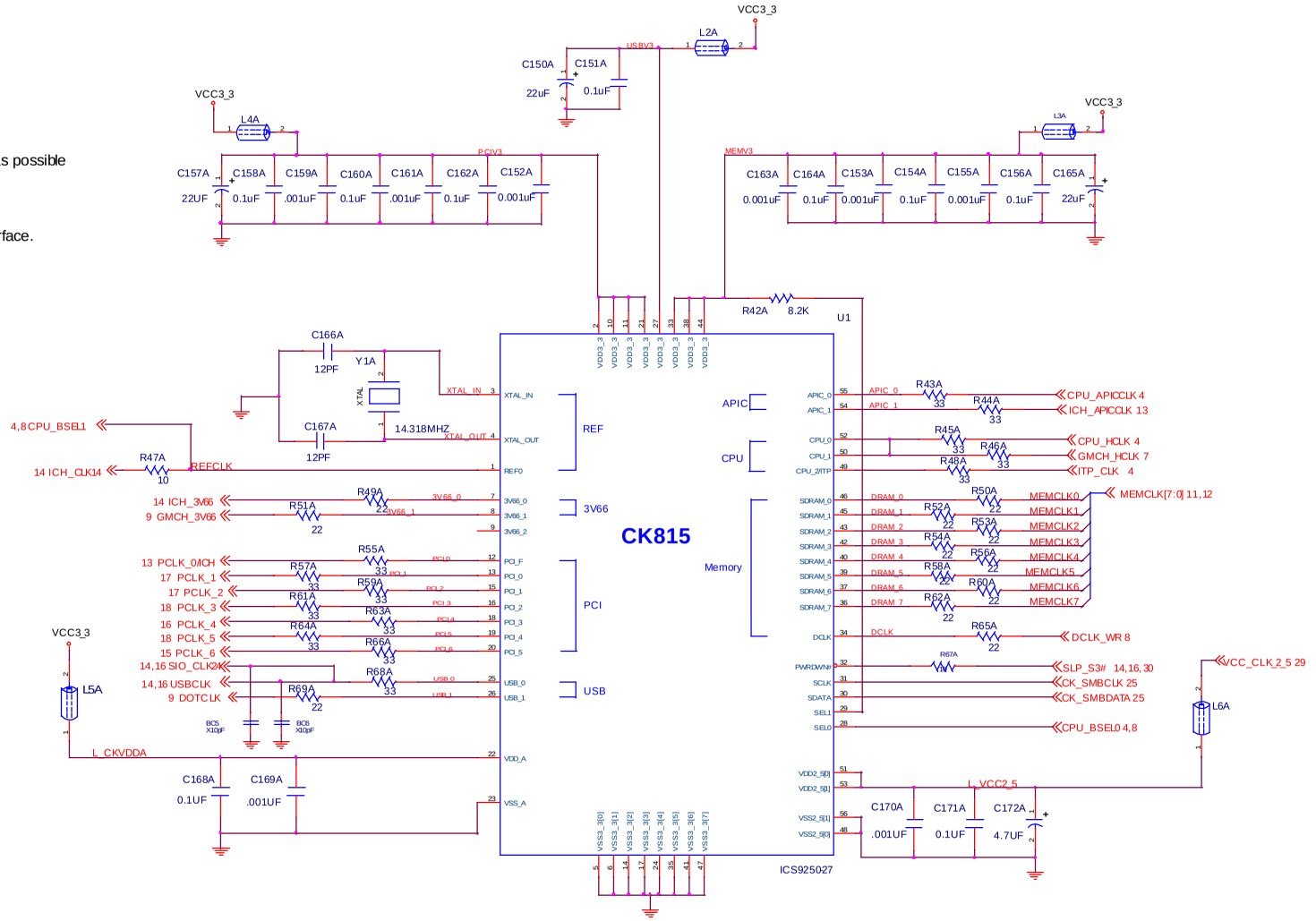
Clock Synthesizer

Notes:

- Place all decoupling caps as close to VCC/GND pins as possible
- PCI_0/ICH pin has to go to the ICH.
  (This clock cannot be turned off through SMBus)
- CPU_ITP pin must go to the ITP. It is the only
  CPU CLK that can be shut off through the SMBUS interface.



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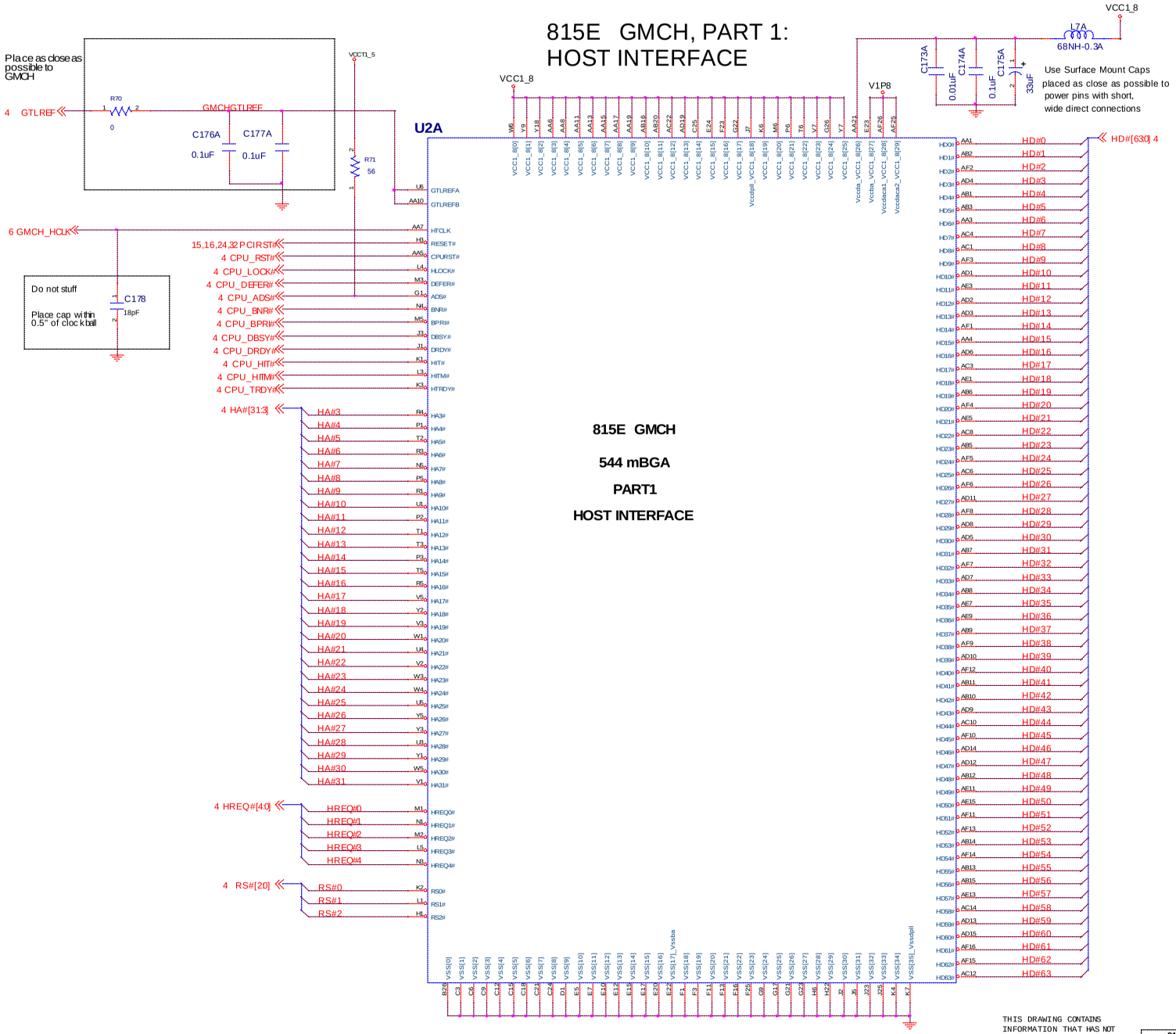
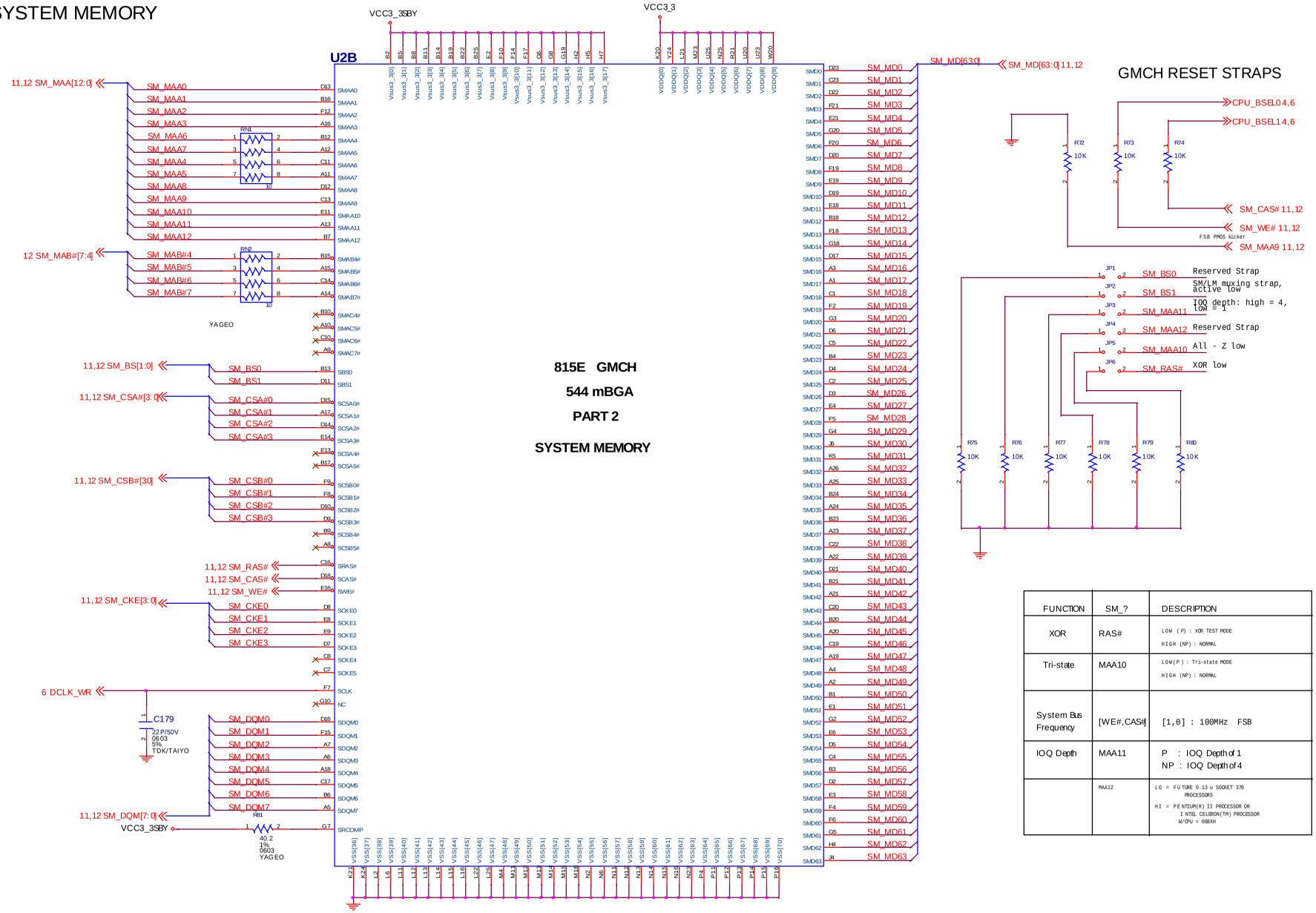
815E GMCH, PART 1: HOST INTERFACE



815E GMCH, PART 2:

SYSTEM MEMORY



FUNCTION	SM_?	DESCRIPTION
XOR	RAS#	LOW (P) : XOR TEST MODE HIGH (NP) : NORMAL
Tri-state	MAA10	LOW(P) : Tri-state MODE HIGH (NP) : NORMAL
System Bus Frequency	[WE#,CAS#]	[1,0] : 100MHz FSB
IOQ Depth	MAA11	P : IOQ Depth of 1 NP : IOQ Depth of 4
	MAA12	LO = FUTURE 0.13 u SOCKET 370 PROCESSORS HI = PENTIUM(R) II PROCESSOR OR INTEL CELERON(TM) PROCESSOR W/CPU = 06BXH

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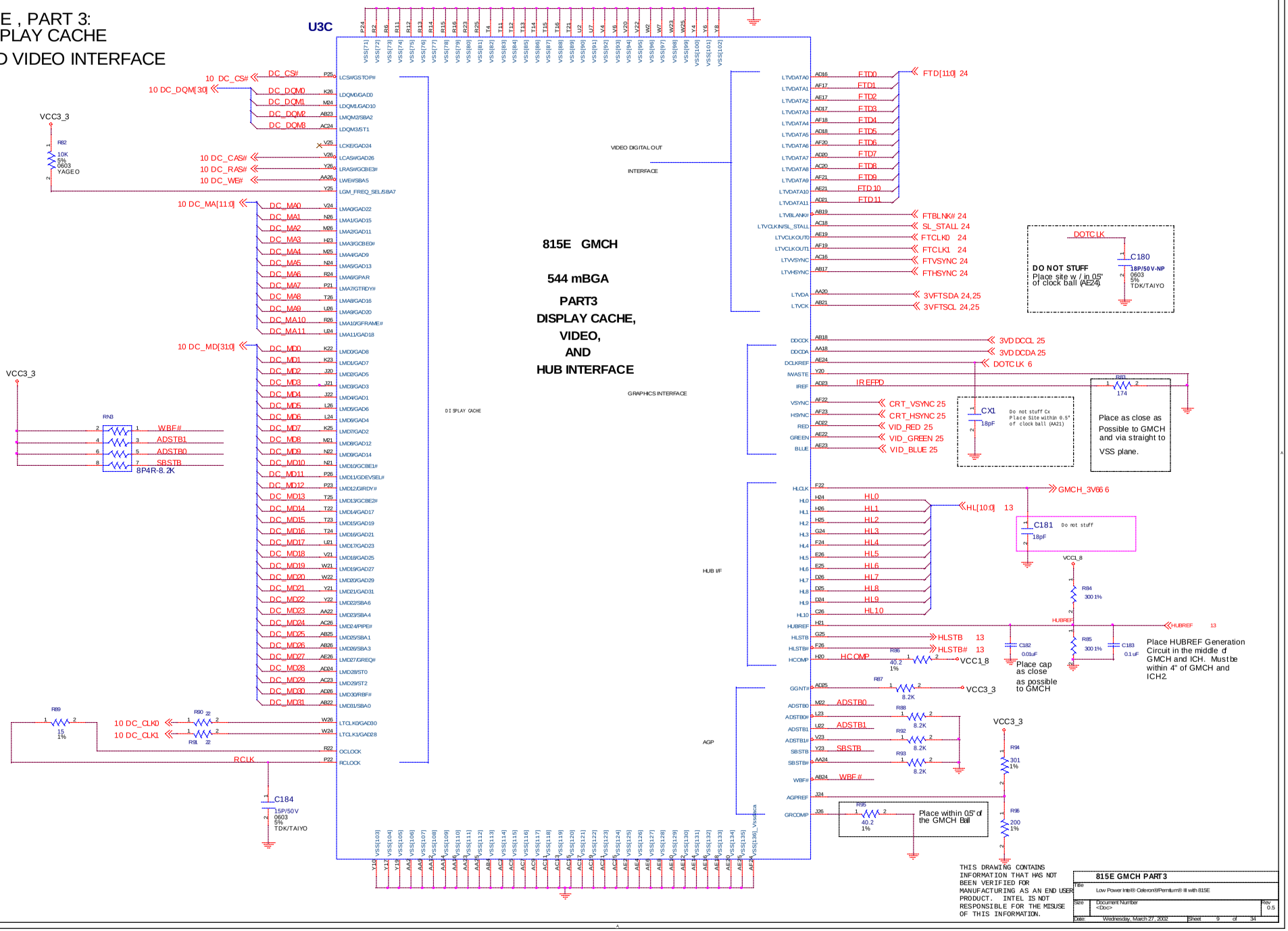
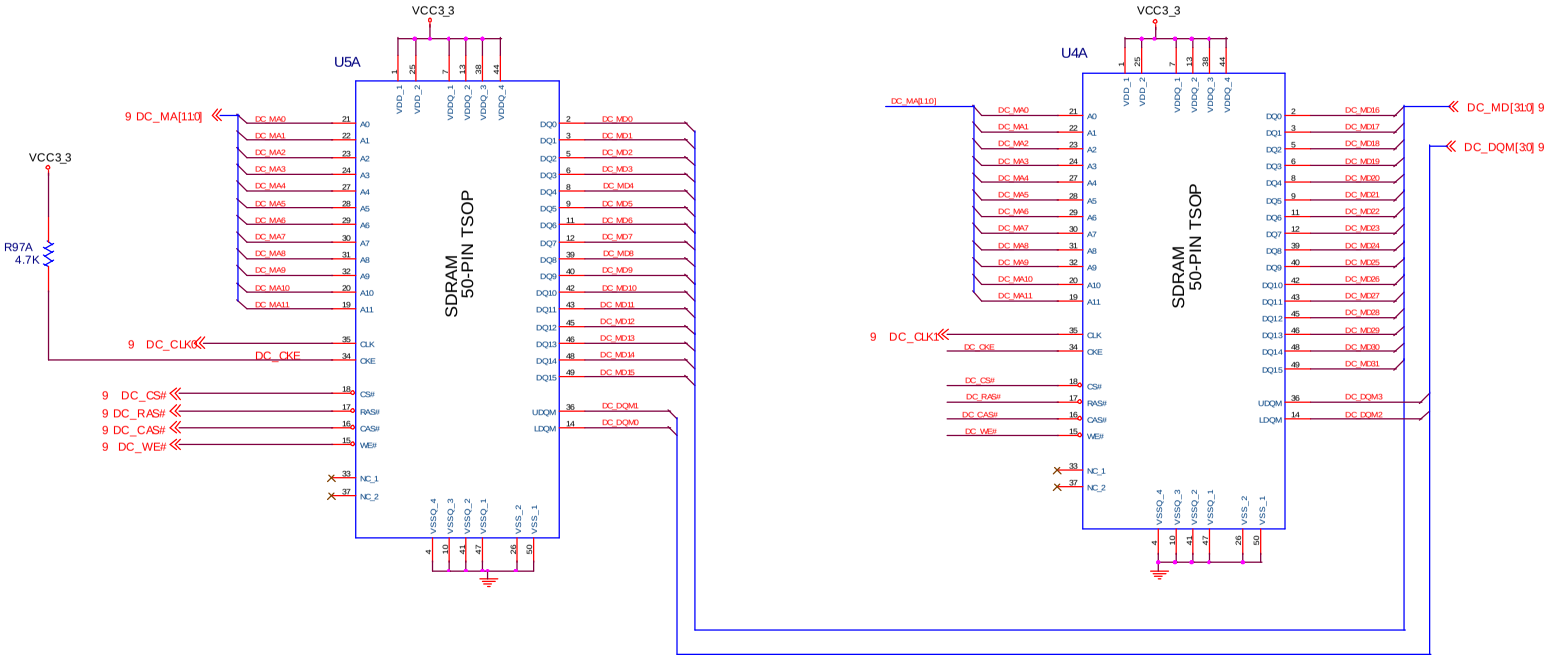
815E , PART 3:
DISPLAY CACHE
AND VIDEO INTERFACE



4MB Display Cache



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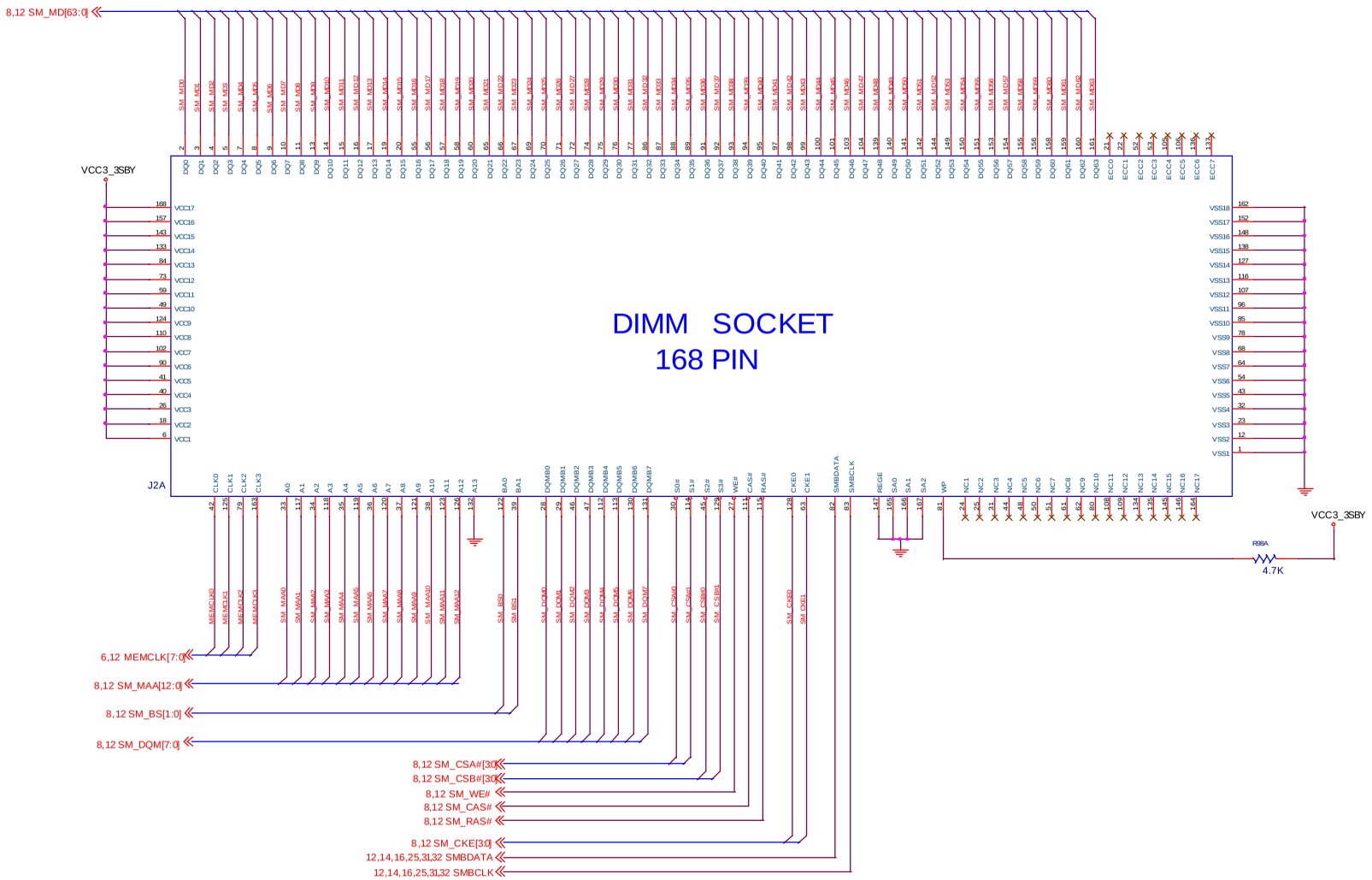
SYSTEM MEMORY



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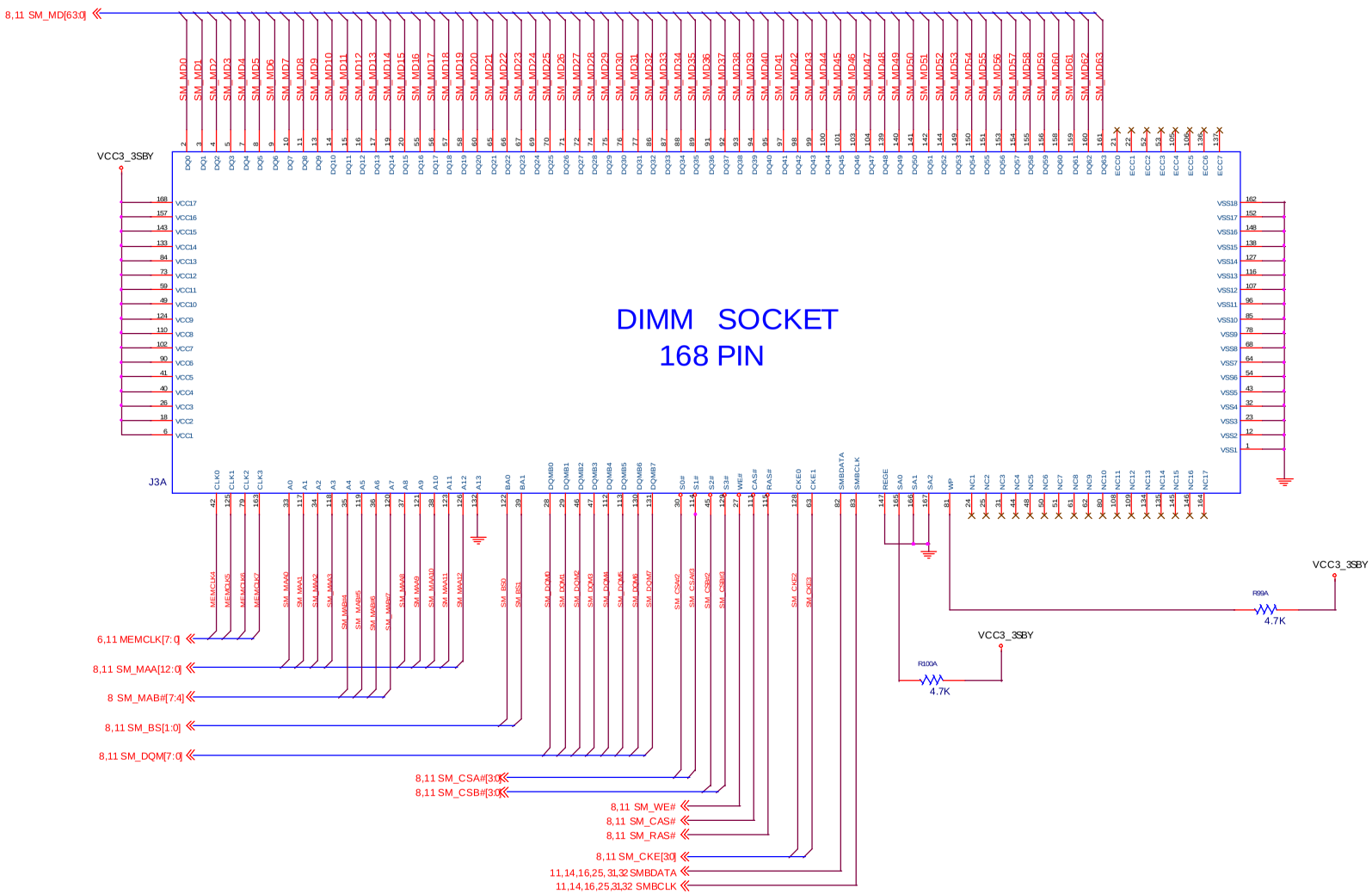
SYSTEM MEMORY



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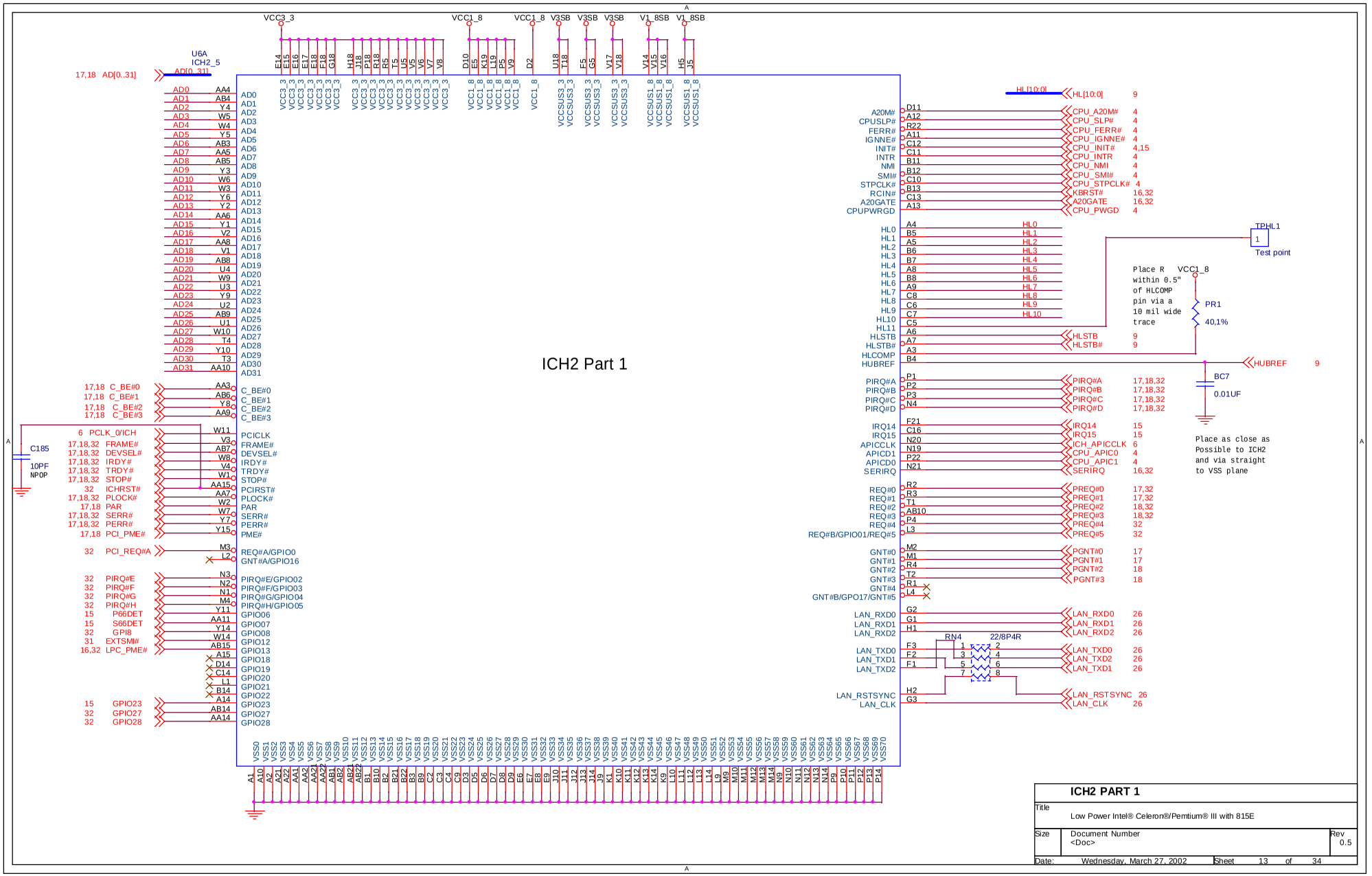
ICH2 Part 1
U6A
ICH2_5
17,18 AD[0..31]
VCC3_3
VCC1_8
V3SB
V1_8SB
HL[10:0]
Test point
TPHL1
Place R within 0.5" of HLCOMP pin via a 10 mil wide trace
PR1
40,1%
BC7
0.01UF
Place as close as Possible to ICH2 and via straight to VSS plane
C185
10PF
NP0P
RN4
22/8P4R
HUBREF
A20M#
CPUSLP#
FERR#
IGNNE#
INIT#
INTR
NMI
SMI#
STPCLK#
RCIN#
A20GATE
CPUPWRGD
HLSTB
HLSTB#
HLCOMP
PIRQ#A
PIRQ#B
PIRQ#C
PIRQ#D
IRQ14
IRQ15
APICCLK
APICD1
APICD0
SERIRQ
REQ#0
REQ#1
REQ#2
REQ#3
REQ#4
REQ#B/GPIO01/REQ#5
GNT#0
GNT#1
GNT#2
GNT#3
GNT#4
GNT#B/GPO17/GNT#5
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN_RSTSYNC
LAN_CLK
C_BE#0
C_BE#1
C_BE#2
C_BE#3
PCICLK
FRAME#
DEVSEL#
IRDY#
TRDY#
STOP#
PCIRST#
PLOCK#
PAR
SERR#
PERR#
PME#
REQ#A/GPIO0
GNT#A/GPIO16
PIRQ#E/GPIO02
PIRQ#F/GPIO03
PIRQ#G/GPIO04
PIRQ#H/GPIO05
GPIO06
GPIO07
GPIO08
GPIO12
GPIO13
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO27
GPIO28
ICH2 PART 1
Low Power Intel® Celeron®/Pemtium® III with 815E
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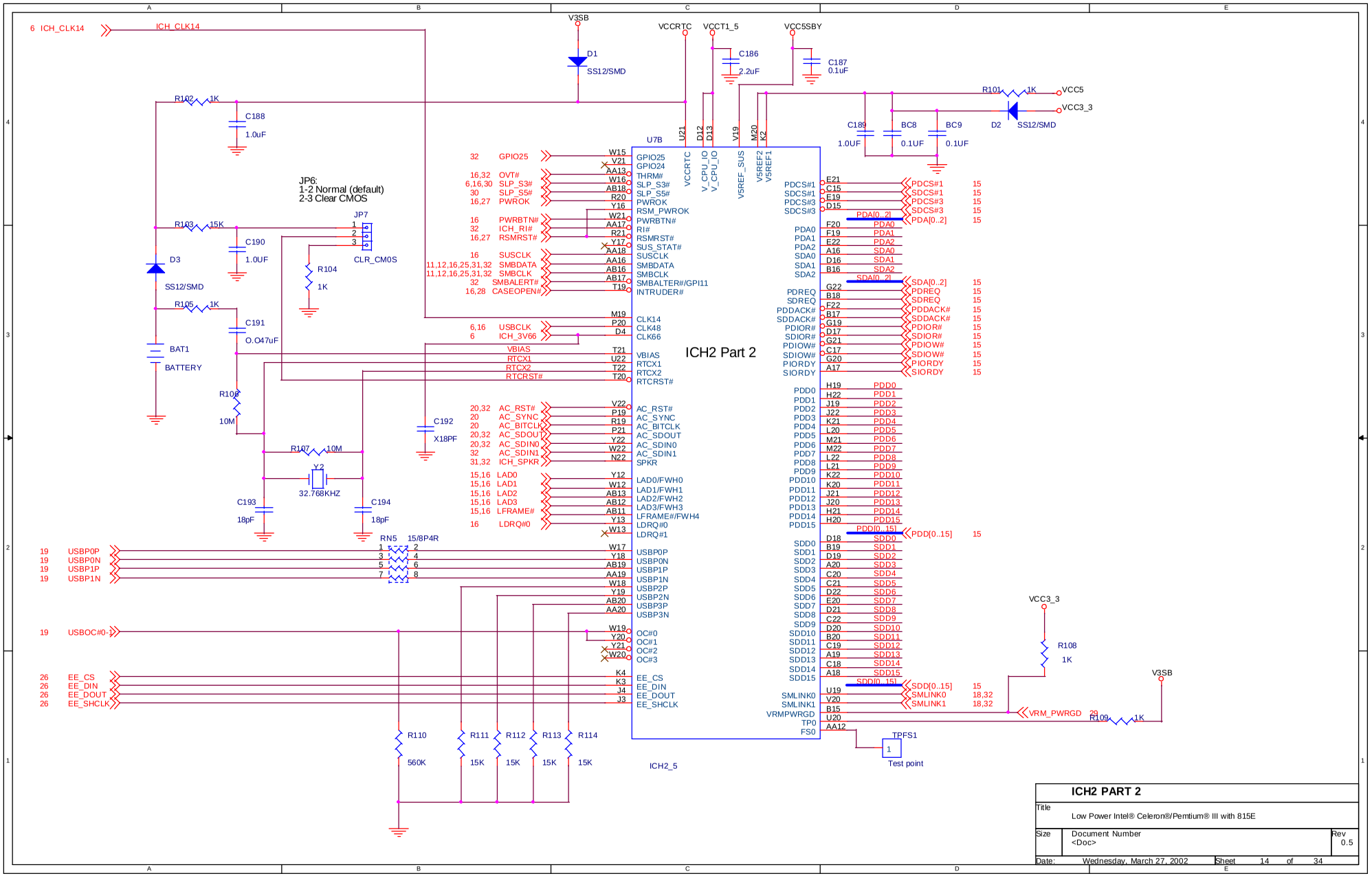
ICH2 Part 2
U7B
ICH2_5
JP6:
1-2 Normal (default)
2-3 Clear CMOS
CLR_CM0S
SS12/SMD
BATTERY
32.768KHZ
RN5 15/8P4R
Test point
ICH2 PART 2
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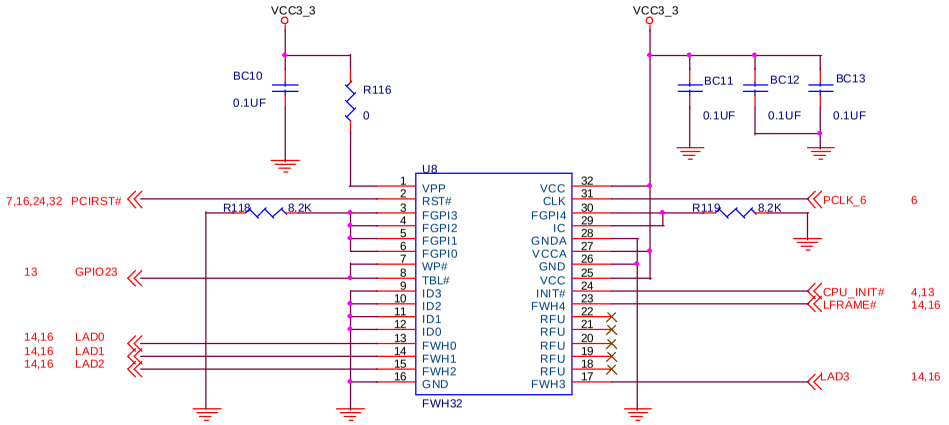
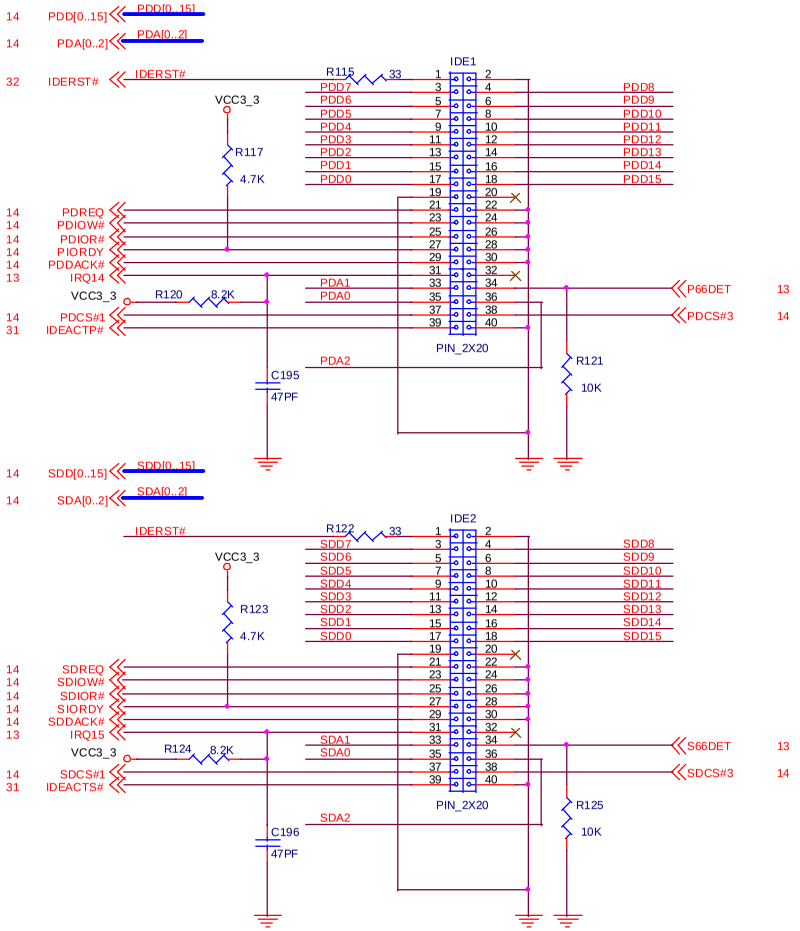
FWH



IDE



FWH AND IDE 1 & 2		
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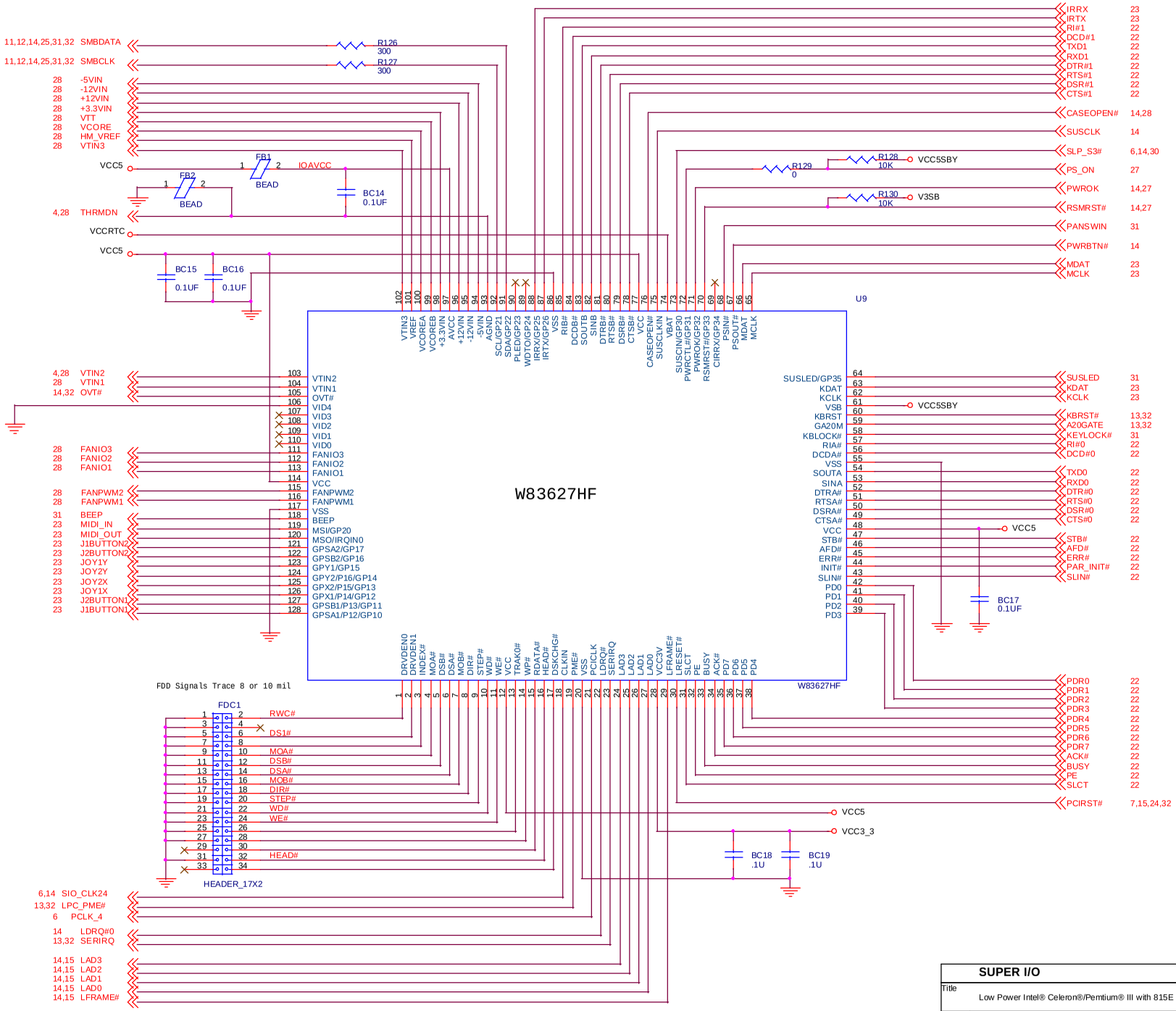
W83627HF
U9
FDC1
HEADER_17X2
FDD Signals Trace 8 or 10 mil
SUPER I/O
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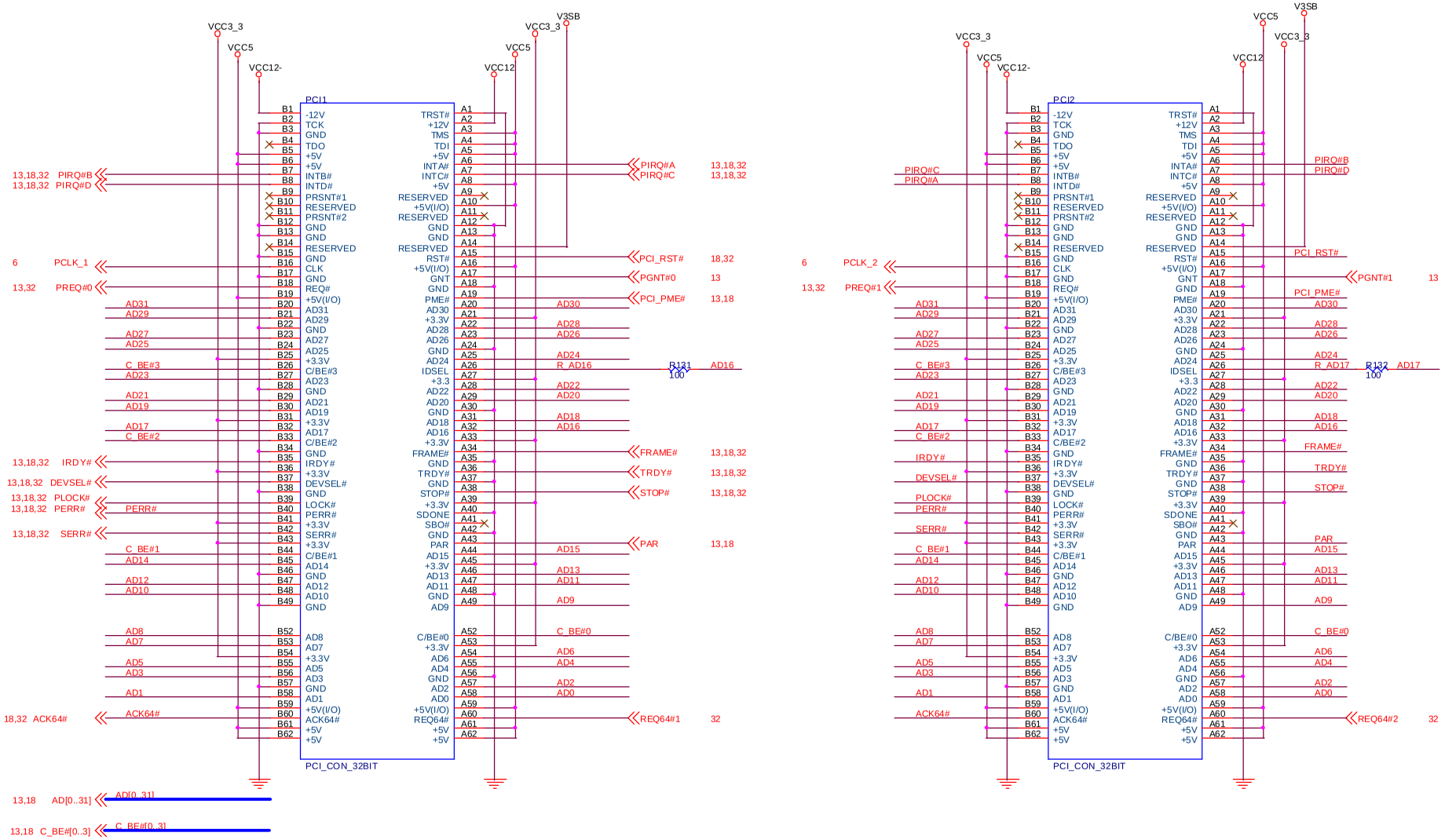
PCI1
PCI_CON_32BIT
PCI2
PCI_CON_32BIT
VCC3_3
VCC5
VCC12
V3SB
PIRQ#A
PIRQ#B
PIRQ#C
PIRQ#D
PCLK_1
PCLK_2
PREQ#0
PREQ#1
PCI_RST#
PGNT#0
PGNT#1
PCI_PME#
REQ64#1
REQ64#2
AD[0..31]
C_BE#[0..3]
R_AD16
R_AD17
R131
R132
100
PCI 1 & 2
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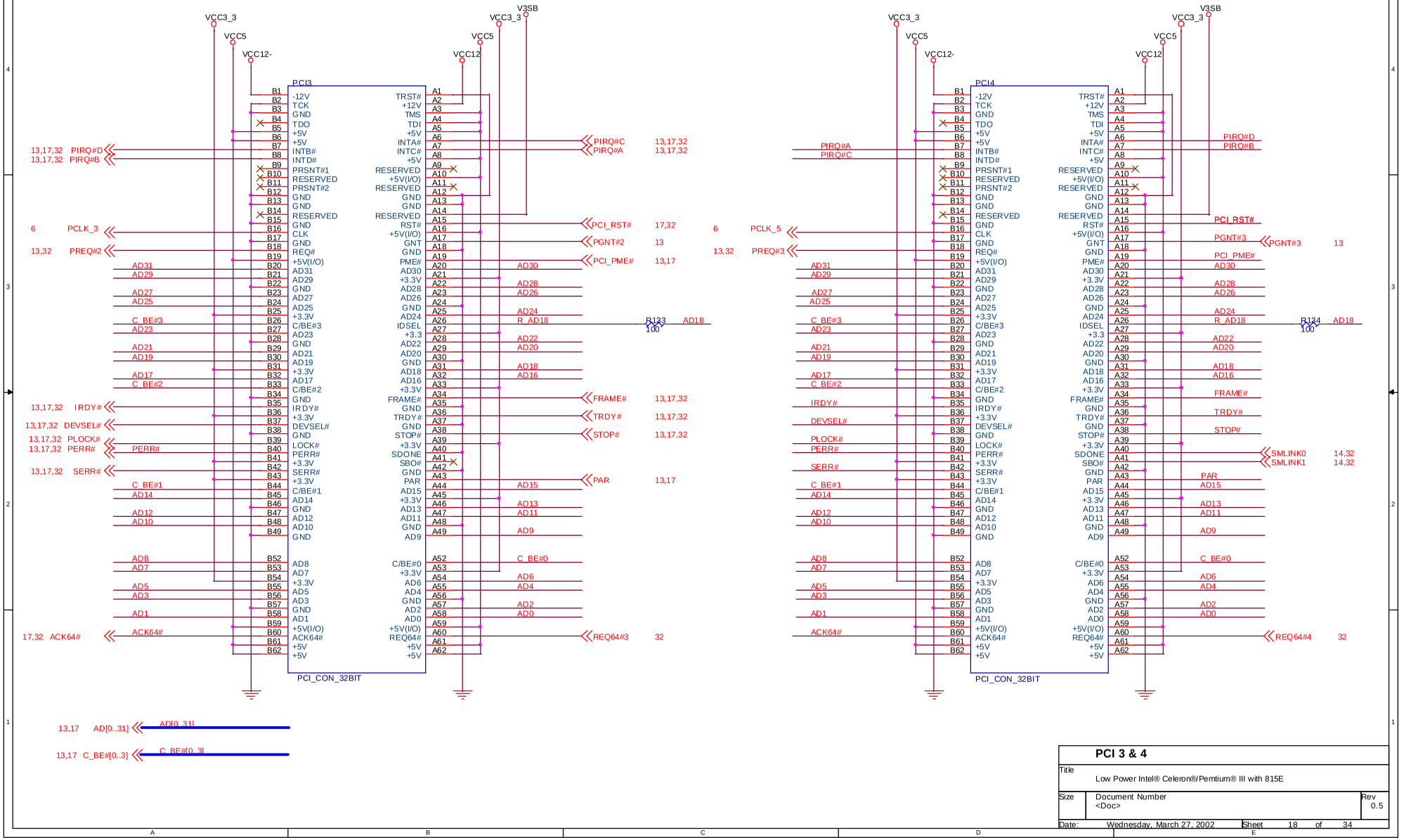

PCI 3 & 4

Title	Low Power Intel® Celeron®/Pemtium® III with 815E	
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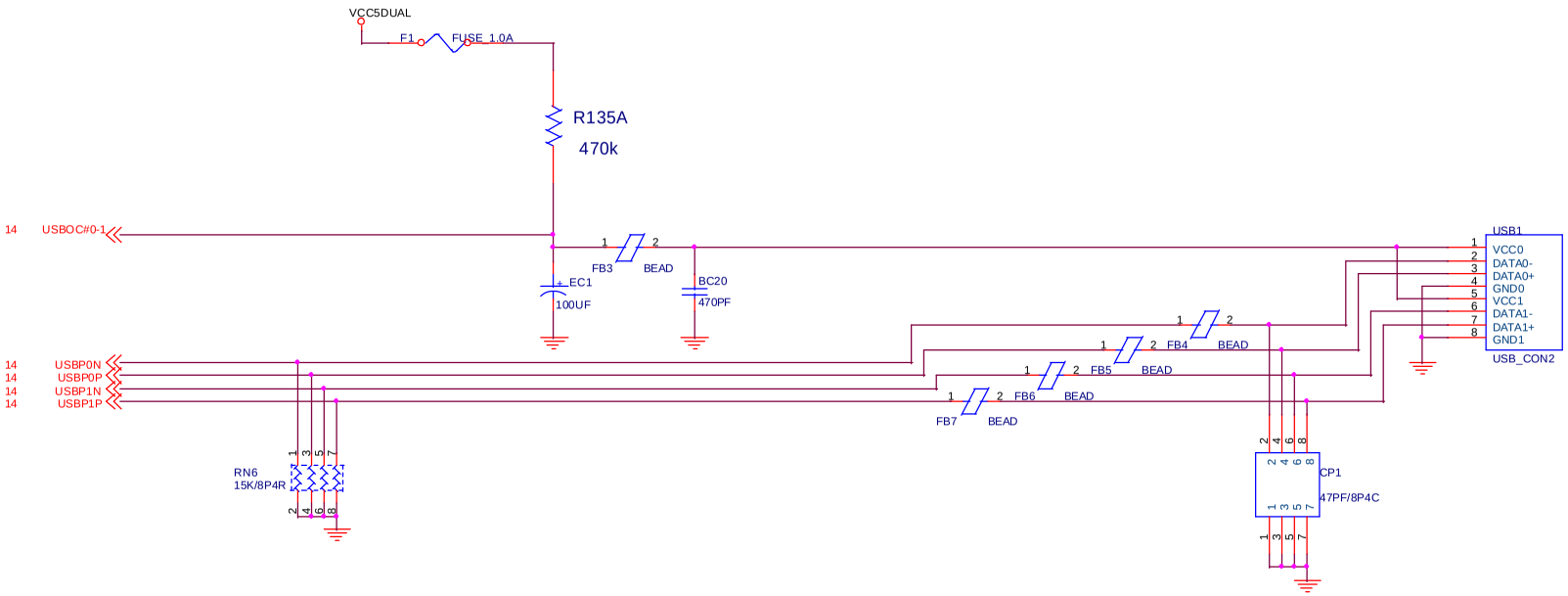

USB PORT 1 & 2

Title	Low Power Intel® Celeron®/Pemtium® III with 815E	
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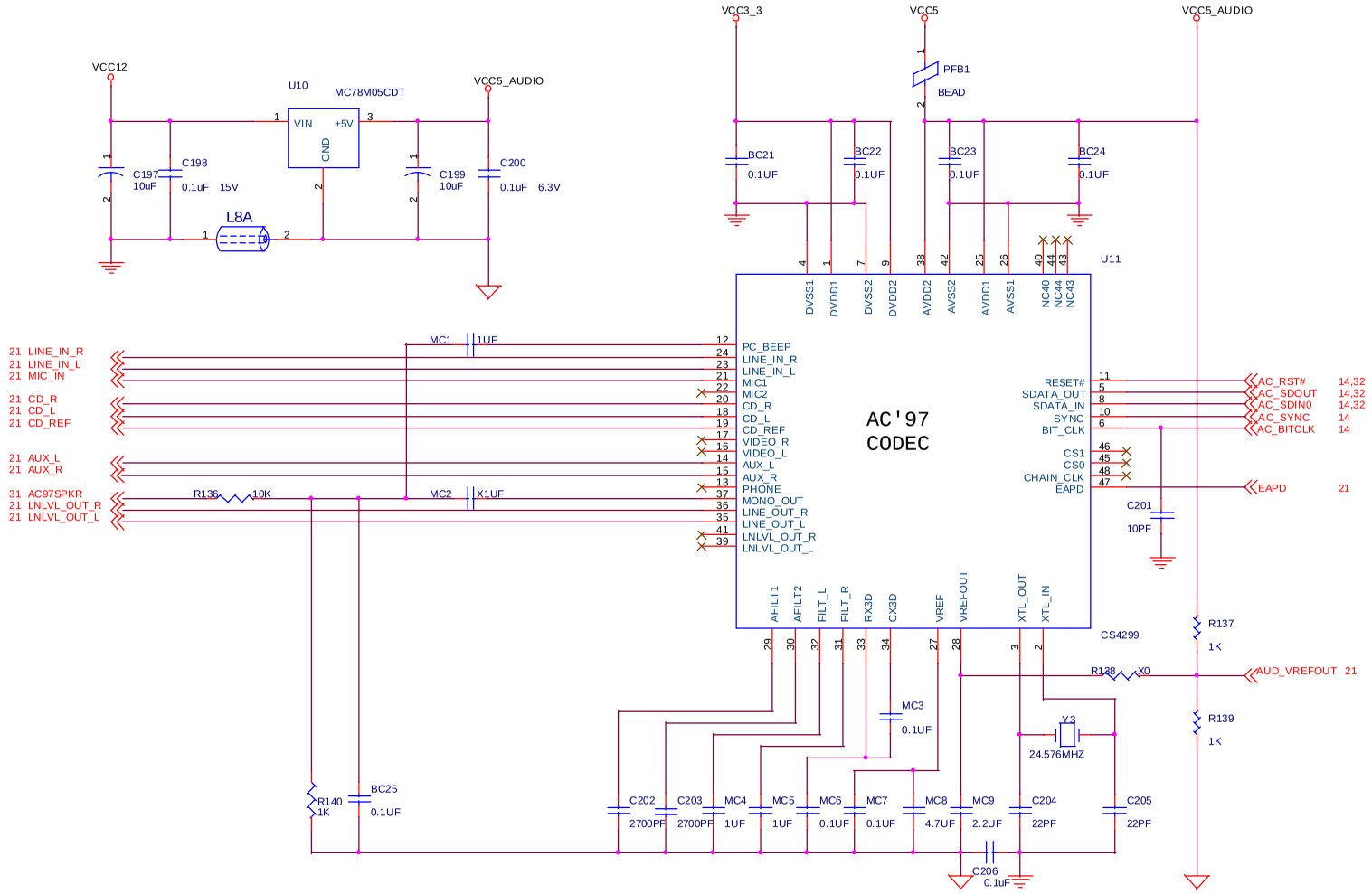

AC'97 CODEC		
Title	Low Power Intel® Celeron®/Pemtium® III with 815E	
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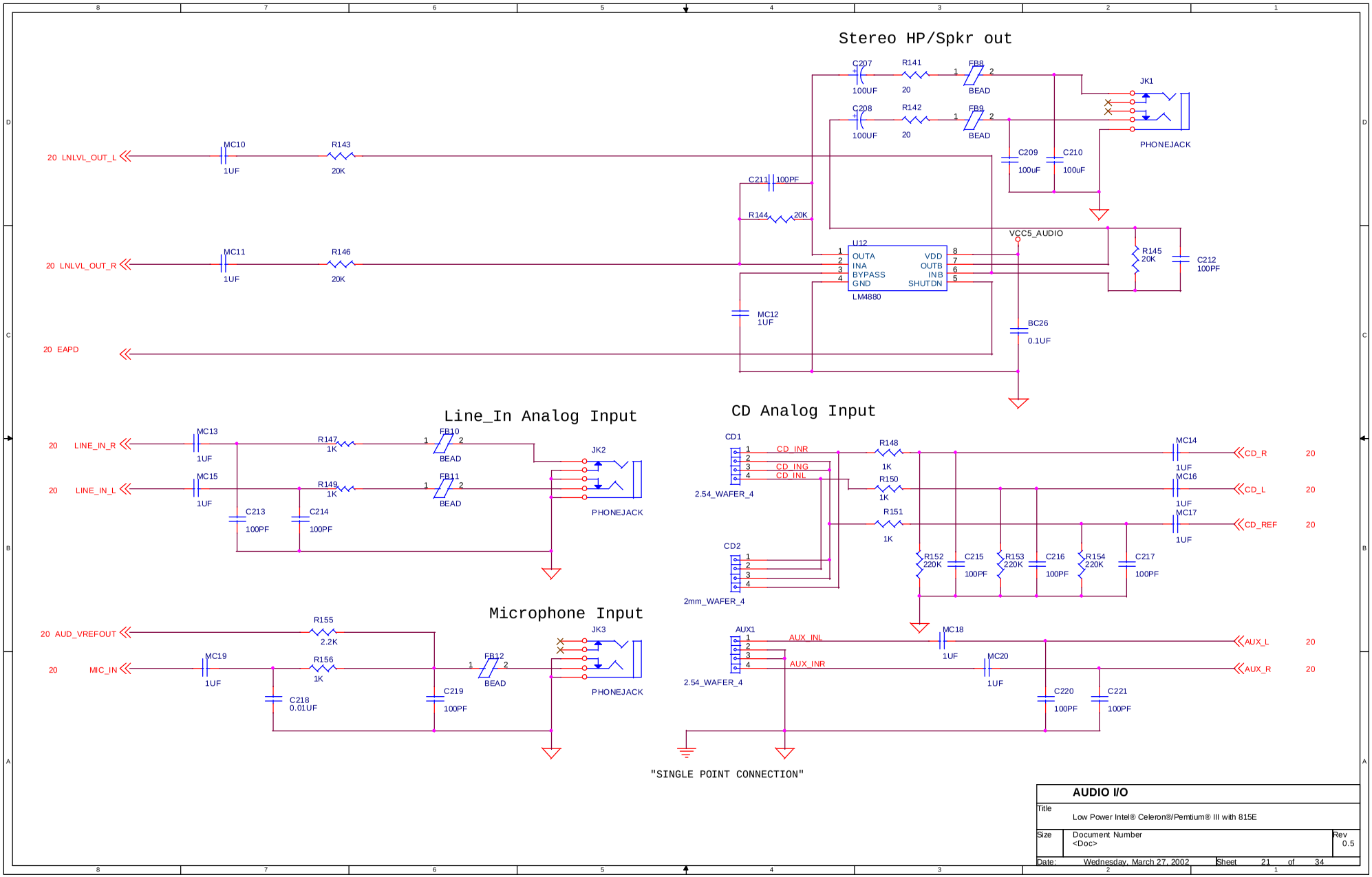
Stereo HP/Spkr out
20 LNLVL_OUT_L
MC10
1UF
R143
20K
20 LNLVL_OUT_R
MC11
1UF
R146
20K
20 EAPD
C207
100UF
R141
20
FB8
BEAD
C208
100UF
R142
20
FB9
BEAD
JK1
PHONEJACK
C209
100uF
C210
100uF
C211 100PF
R144 20K
U12
OUTA
INA
BYPASS
GND
VDD
OUTB
INB
SHUTDN
LM4880
VCC5_AUDIO
R145
20K
C212
100PF
MC12
1UF
BC26
0.1UF
Line_In Analog Input
20 LINE_IN_R
20 LINE_IN_L
MC13
1UF
MC15
1UF
R147
1K
R149
1K
FB10
BEAD
FB11
BEAD
C213
100PF
C214
100PF
JK2
PHONEJACK
CD Analog Input
CD1
CD_INR
CD_ING
CD_INL
2.54_WAFER_4
CD2
2mm_WAFER_4
R148
1K
R150
1K
R151
1K
MC14
1UF
MC16
1UF
MC17
1UF
CD_R
CD_L
CD_REF
R152
220K
C215
100PF
R153
220K
C216
100PF
R154
220K
C217
100PF
Microphone Input
20 AUD_VREFOUT
20 MIC_IN
R155
2.2K
MC19
1UF
R156
1K
C218
0.01UF
FB12
BEAD
C219
100PF
JK3
PHONEJACK
AUX1
AUX_INL
AUX_INR
2.54_WAFER_4
MC18
1UF
MC20
1UF
C220
100PF
C221
100PF
AUX_L
AUX_R
"SINGLE POINT CONNECTION"
AUDIO I/O
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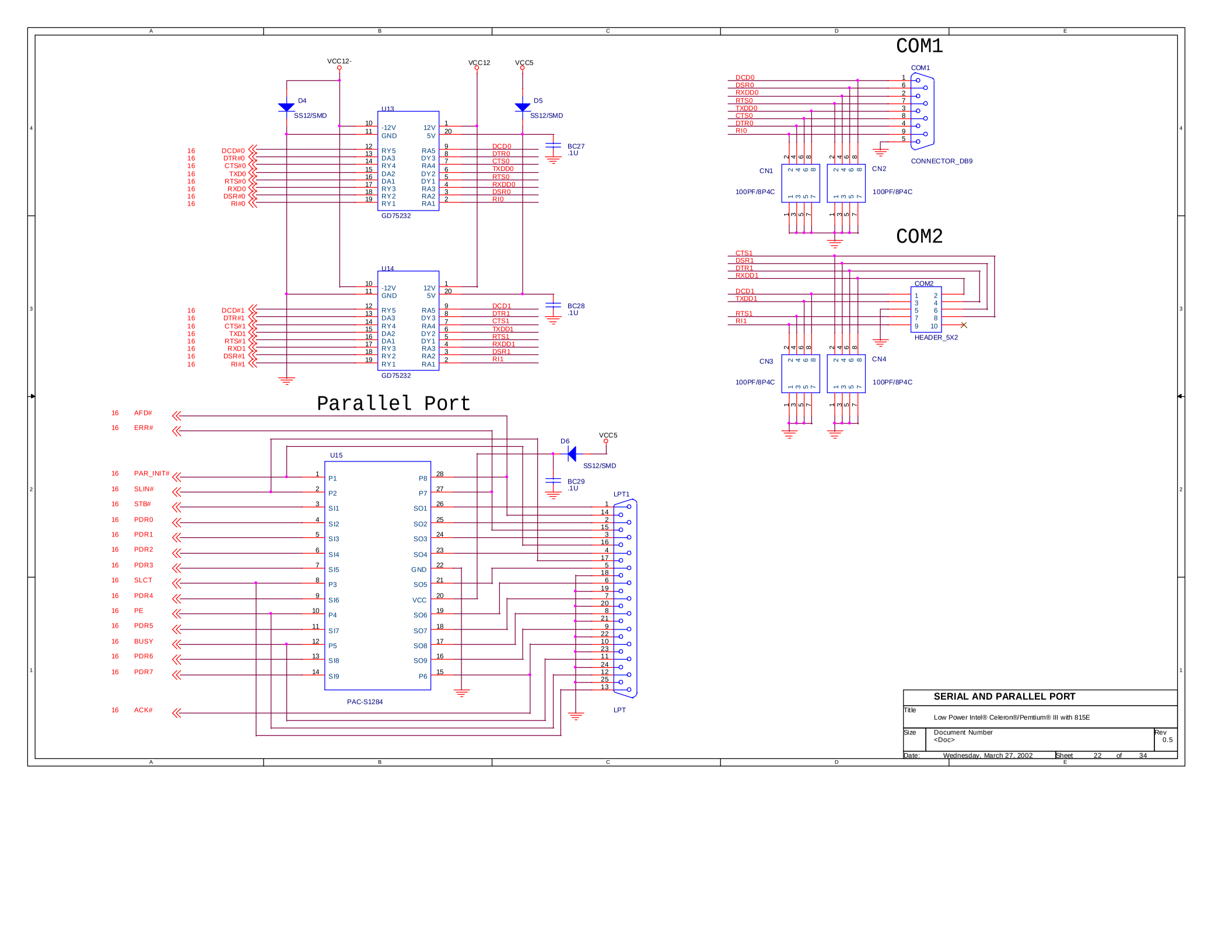
COM1
VCC12-
VCC12
VCC5
D4
SS12/SMD
D5
SS12/SMD
U13
-12V
GND
12V
5V
RY5
DA3
RY4
DA2
DA1
RY3
RY2
RY1
RA5
DY3
RA4
DY2
DY1
RA3
RA2
RA1
GD75232
DCD#0
DTR#0
CTS#0
TXD0
RTS#0
RXD0
DSR#0
RI#0
DCD0
DTR0
CTS0
TXDD0
RTS0
RXDD0
DSR0
RI0
BC27
.1U
U14
GD75232
DCD#1
DTR#1
CTS#1
TXD1
RTS#1
RXD1
DSR#1
RI#1
DCD1
DTR1
CTS1
TXDD1
RTS1
RXDD1
DSR1
RI1
BC28
.1U
COM1
CONNECTOR_DB9
CN1
CN2
100PF/8P4C
COM2
HEADER_5X2
CN3
CN4
Parallel Port
AFD#
ERR#
PAR_INIT#
SLIN#
STB#
PDR0
PDR1
PDR2
PDR3
SLCT
PDR4
PE
PDR5
BUSY
PDR6
PDR7
ACK#
U15
PAC-S1284
D6
SS12/SMD
BC29
.1U
LPT1
LPT
SERIAL AND PARALLEL PORT
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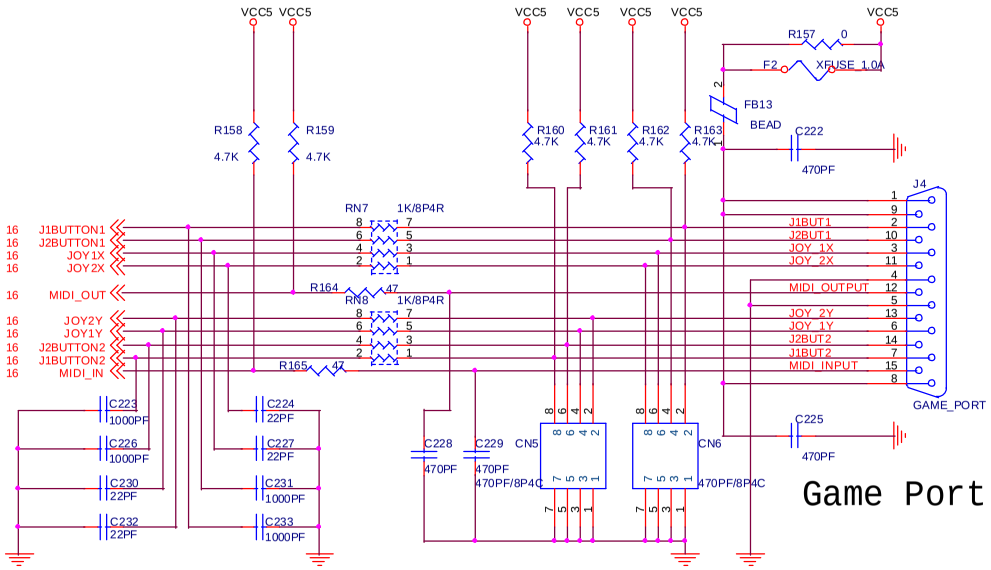

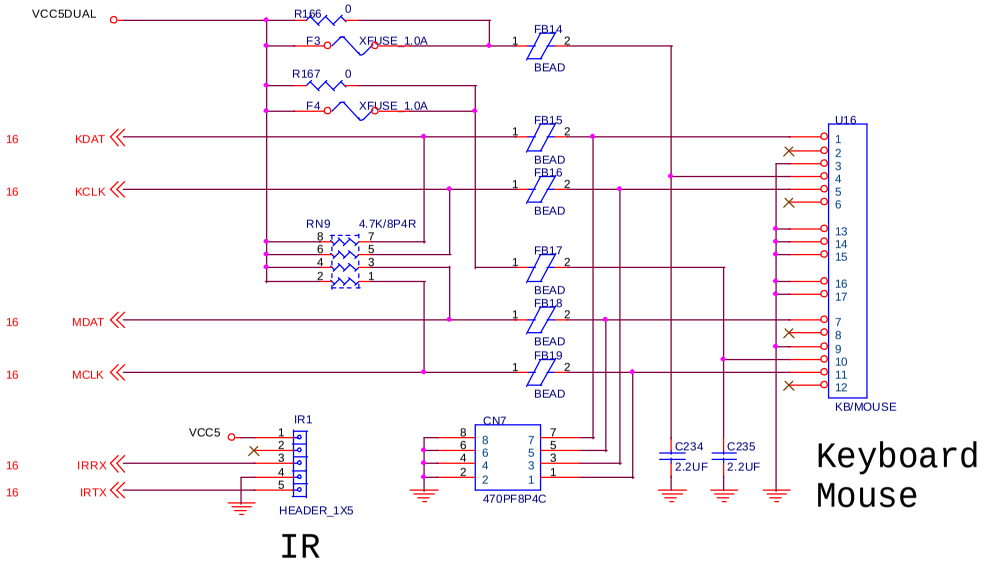

KEYBOARD, MOUSE, GAME & IR		
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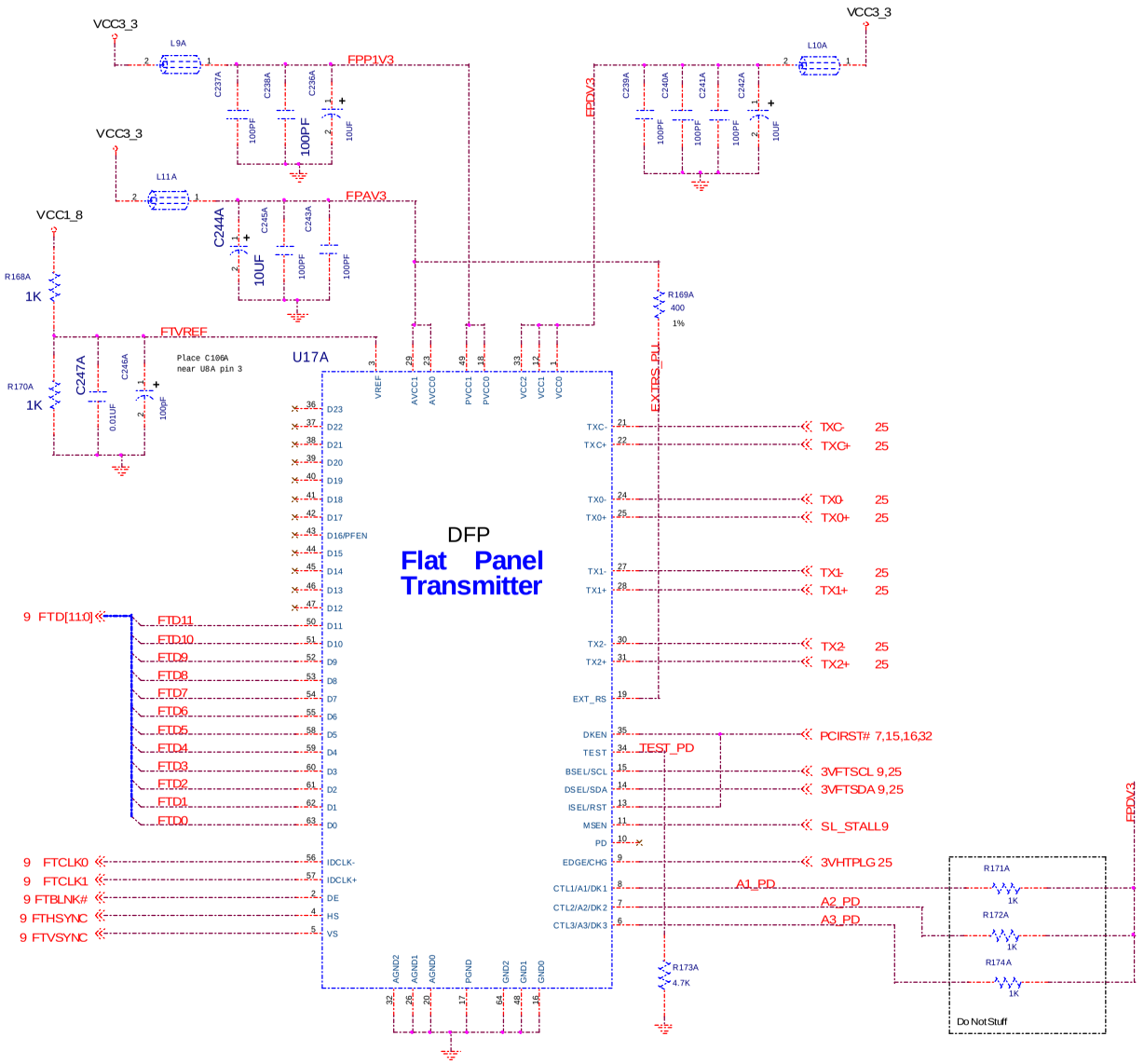
Digital Video Out



Title	DIGITAL VIDEO OUT	
	Low Power Intel® Celeron®/Pemtium® III with 815E	
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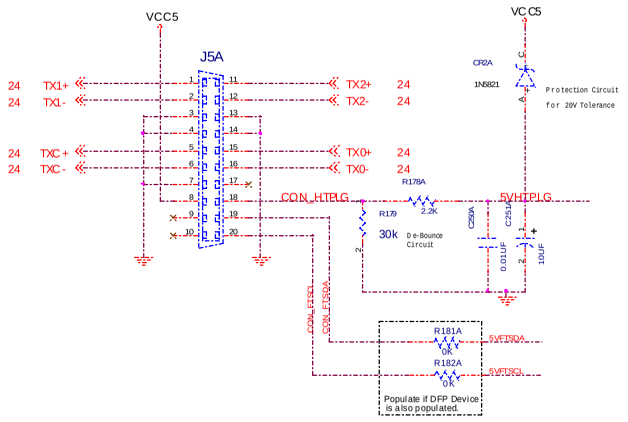
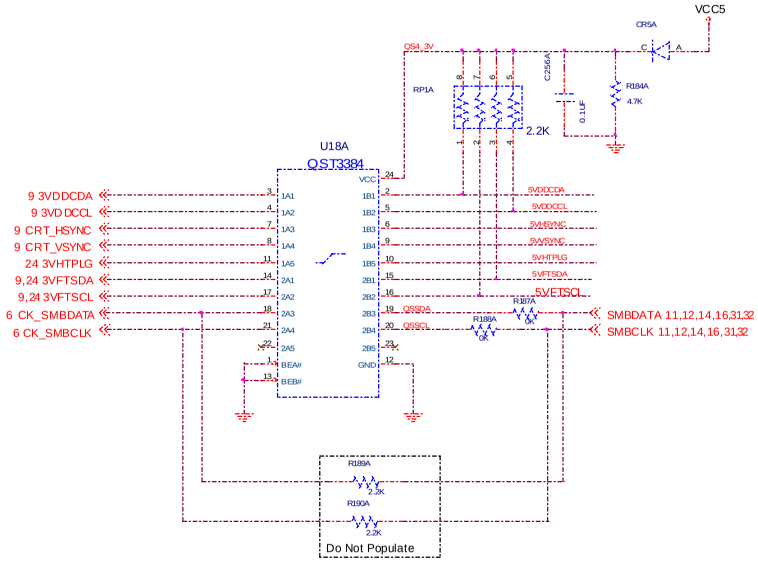
Video Connectors

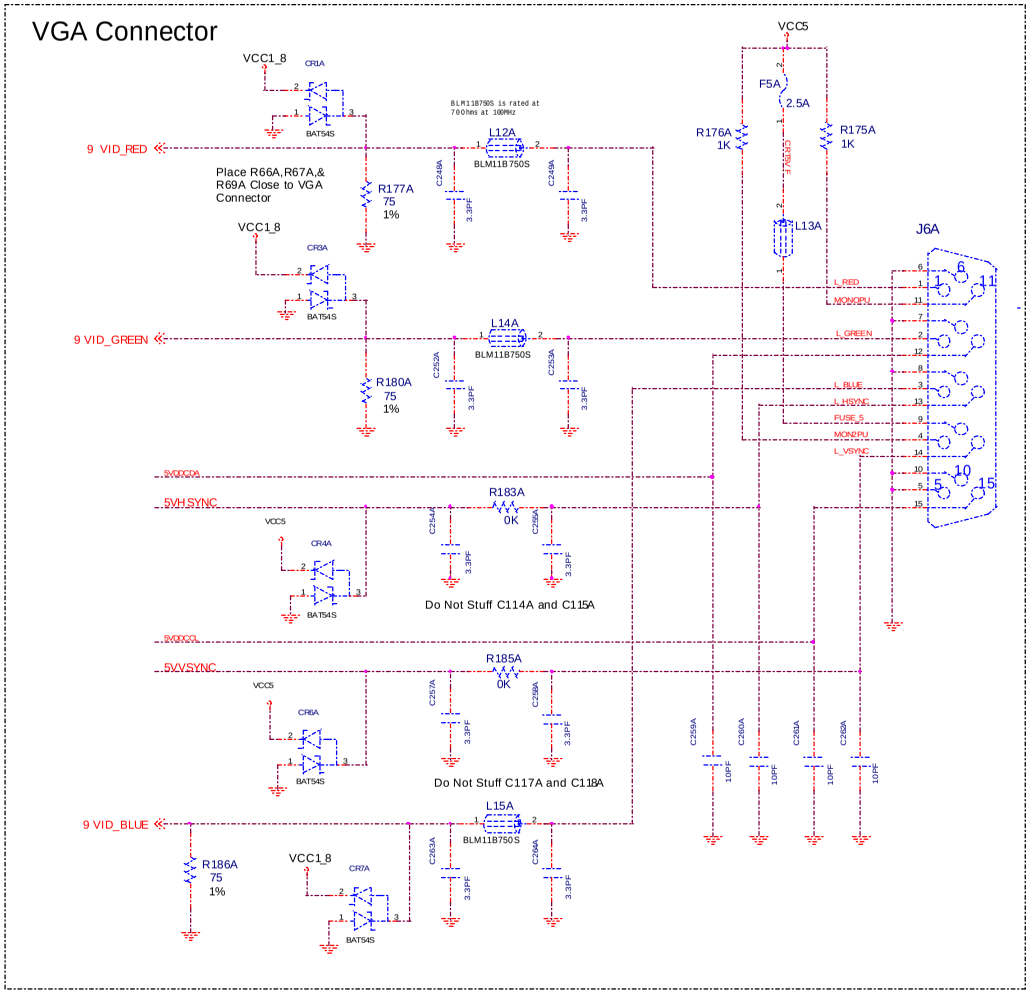
20 Pin Flat Panel Connector



5V to 3.3V Translation / Isolation



VGA Connector



Title:	VIDEO CONNECTORS	
	Low Power Intel® Celeron®/Pentium® III with 815E	
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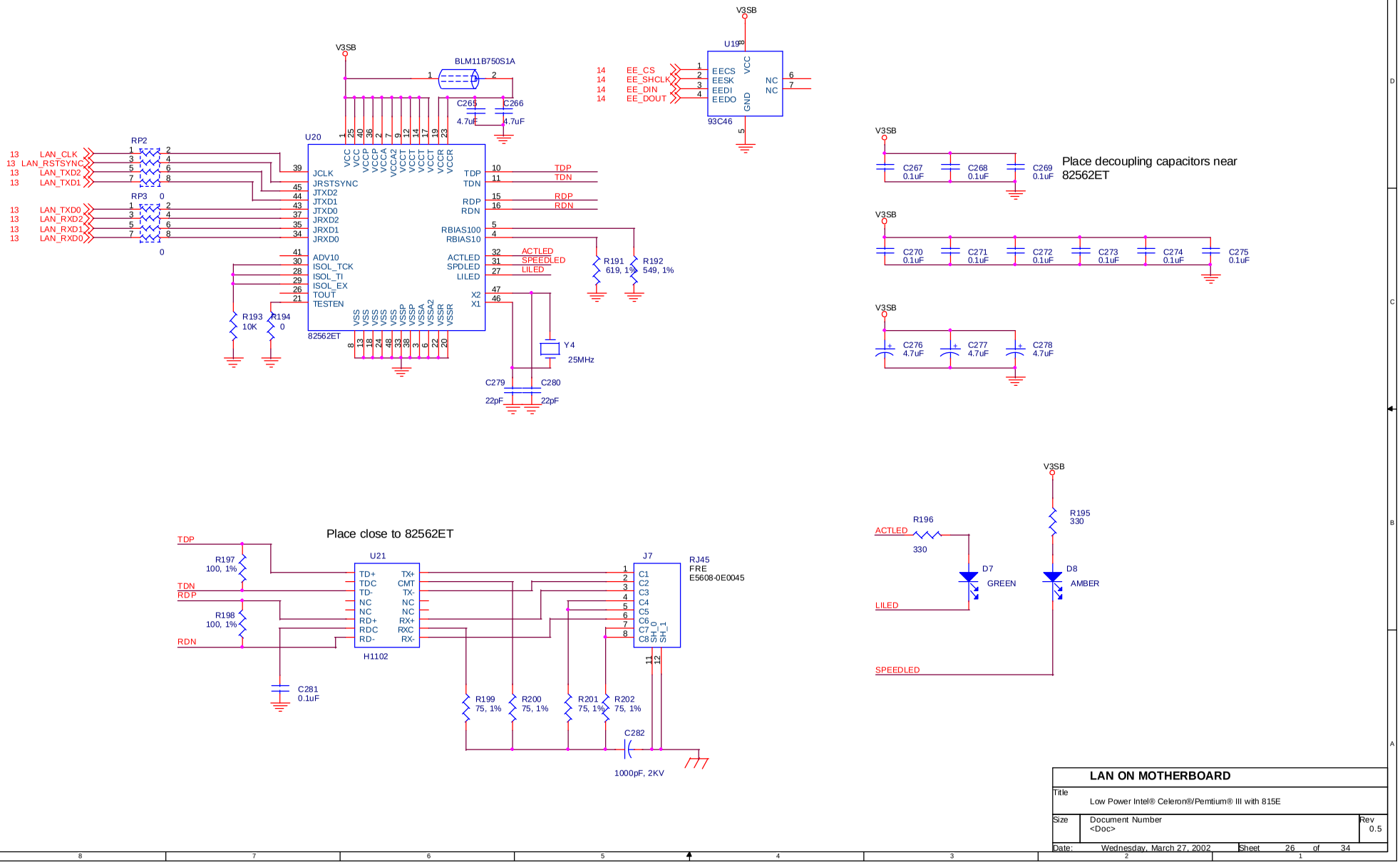

LAN ON MOTHERBOARD

Title	Low Power Intel® Celeron®/Pemtium® III with 815E	
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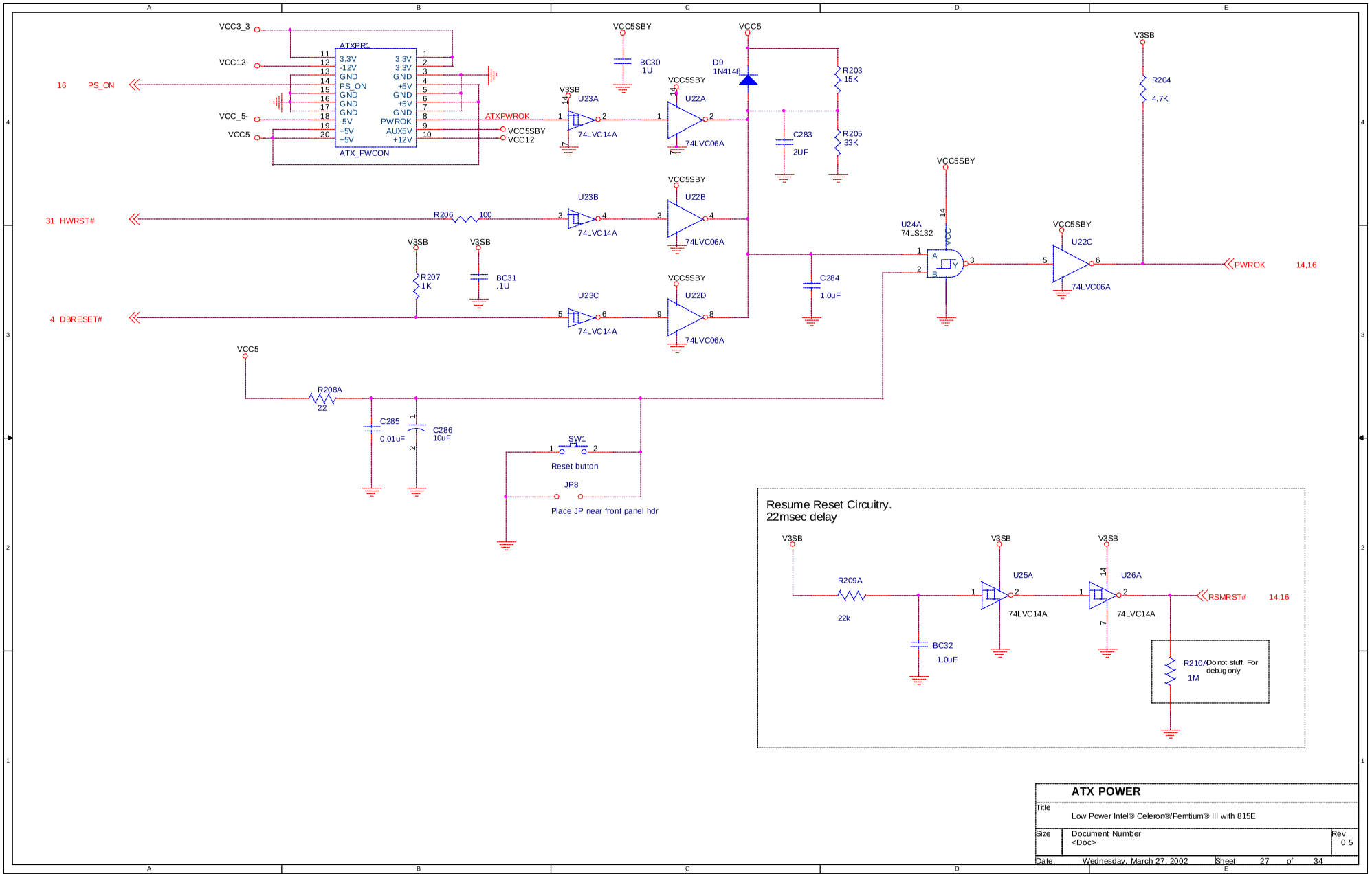

ATX POWER

Title	Low Power Intel® Celeron®/Pemtium® III with 815E	
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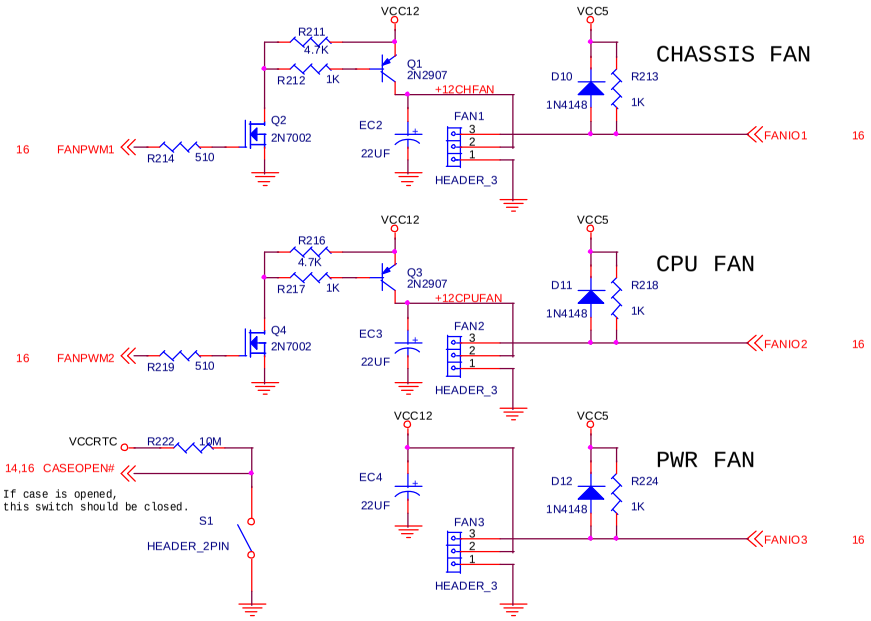

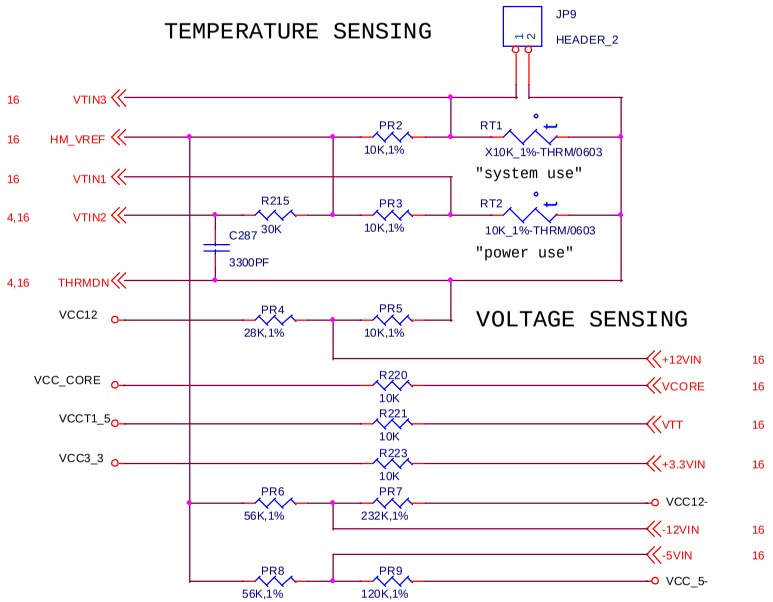

HARDWARE MONITOR		
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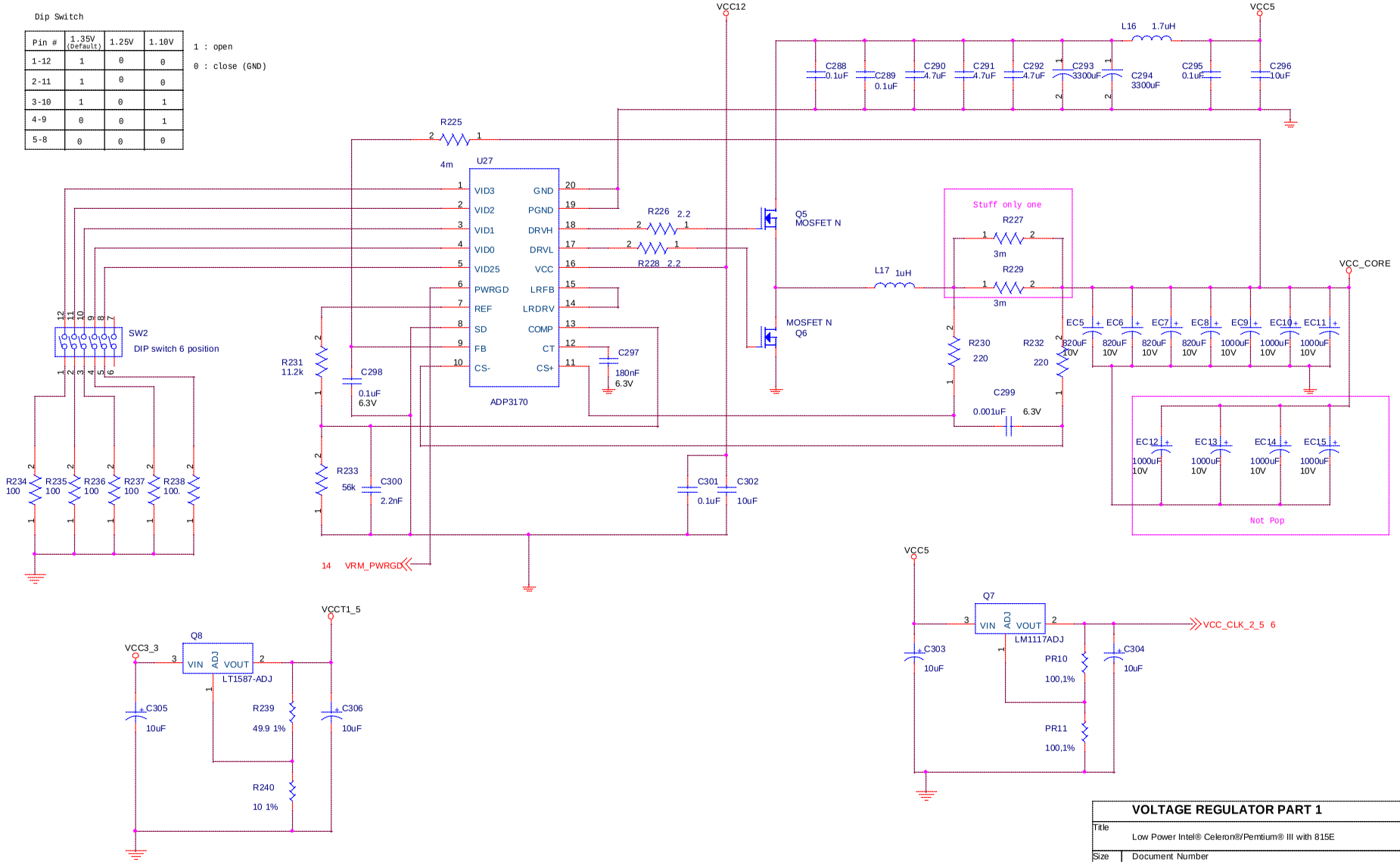
Dip Switch

Pin #	1.35V (Default)	1.25V	1.10V
1-12	1	0	0
2-11	1	0	0
3-10	1	0	1
4-9	0	0	1
5-8	0	0	0

1 : open

0 : close (GND)



VOLTAGE REGULATOR PART 1

Title	Low Power Intel® Celeron®/Pemtium® III with 815E	
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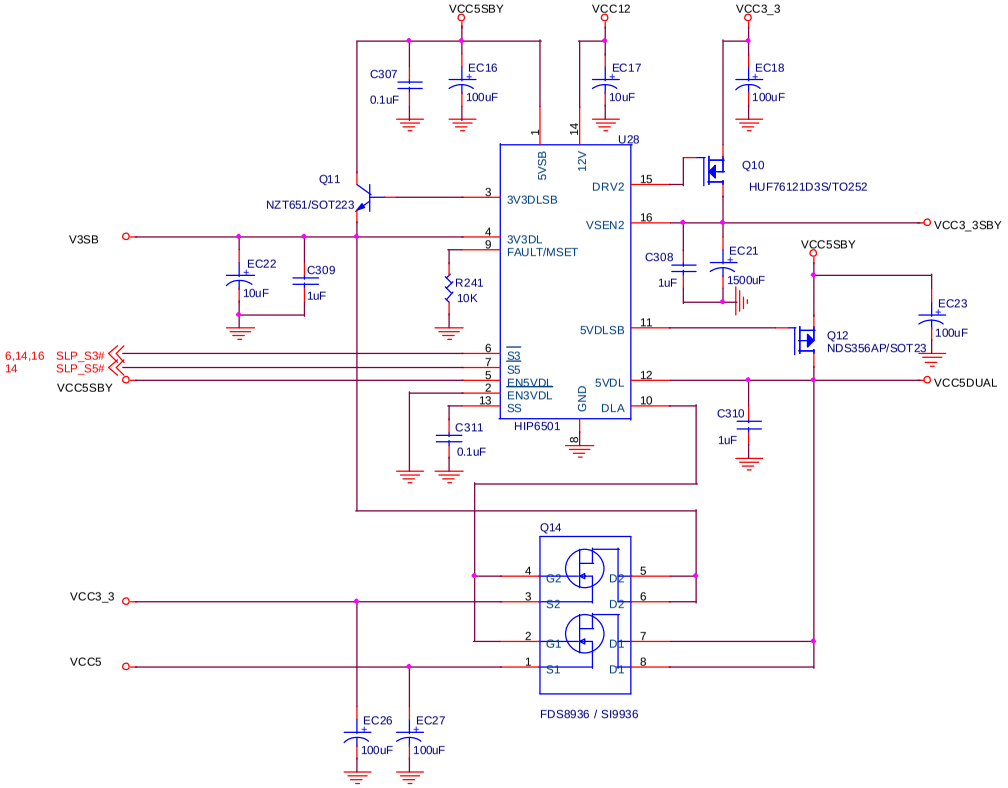

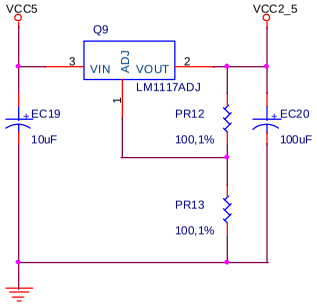

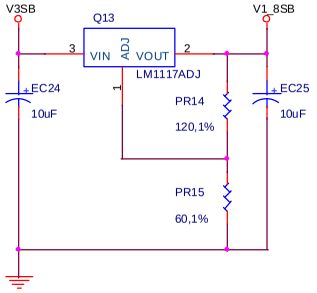

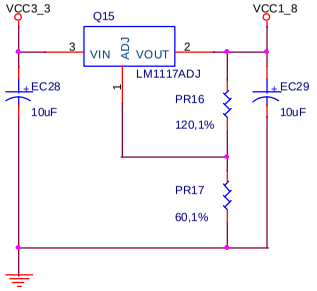

VOLTAGE REGULATOR PART 2

Title	Low Power Intel® Celeron®/Pemtium® III with 815E	
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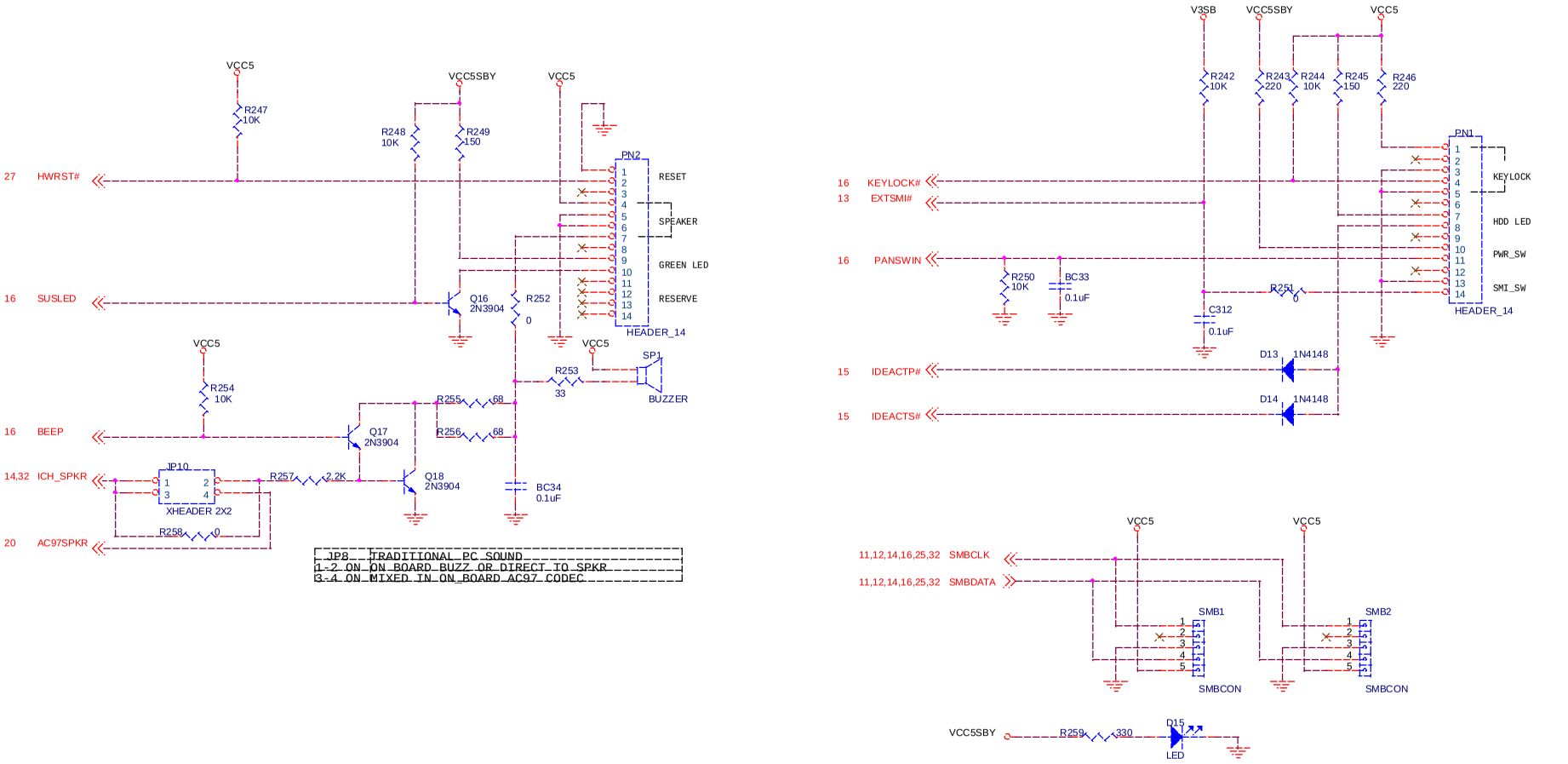

FRONT PANEL AND SMBUS

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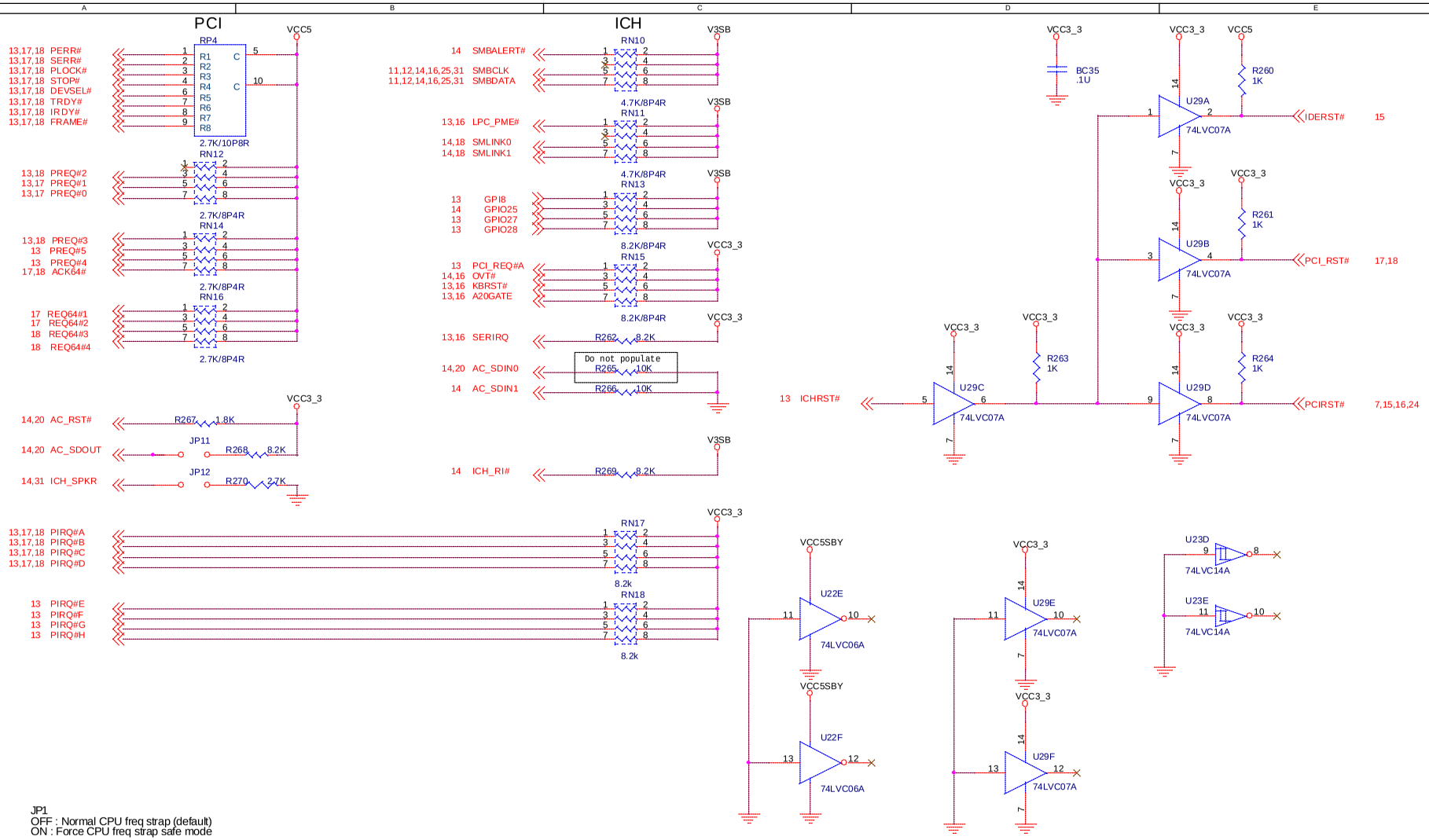

JP1
OFF : Normal CPU freq strap (default)
ON : Force CPU freq strap safe mode

JP5
OFF : Reboot on TCO timer timeout (default)
ON: No reboot on TCO timer timeout

PULL-UP RESISTORS

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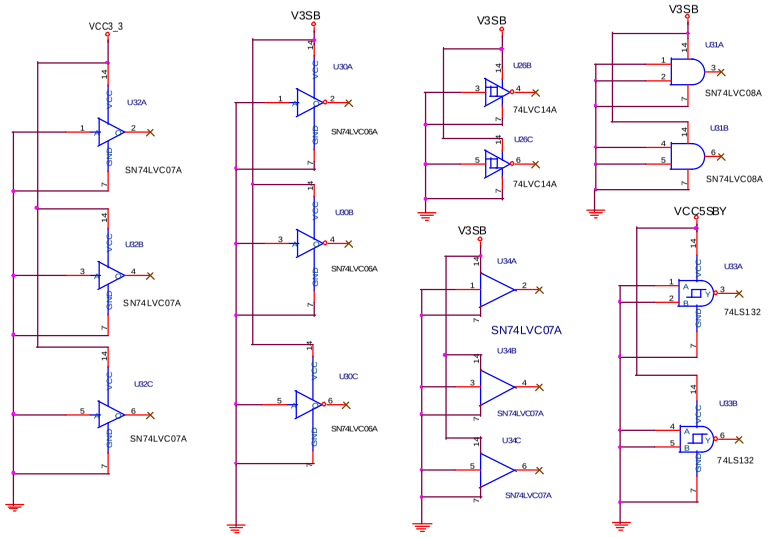
UNUSED GATES



Title	UNUSED GATES		
	Low Power Intel® Celeron®/Pentium® III with 815E		
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DECOUPLING CAPACITORS

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