Pentium® II Processor/ Intel® 440LX AGPset

Design Guide Update

May 1999

Notice: The Intel® 440LX AGPset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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Revision History

Rev.	Draft/Changes	Date
001	Initial Release	August 1998
002	Added General Design Consideration #2	May 1999

Preface

This document is an update to the specifications contained in the Intel® Pentium® II processor/440LX AGPset Design Guide Rev 1.0, April 1998, order number 297651-001.

References may also be made to the following documents: the Intel® 440LX AGPset: 82443LX (PAC) datasheet section, and the 82371AB (PIIX4) datasheet section of the Platform Components data book, order number 296467-009.

It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. This design guide is primarily targeted at the PC market segment and was first published in 1998. Those using this design guide should check for device availability before designing in any of the components included in this document

Nomenclature

General Design Considerations includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® 82440LX AGPset.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel® 440LX AGPset stepping. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
1	Doc	Implementing a RESET BUTTON for Desktop Based Systems
2	Doc	SLP# Connectivity in Multi-processor Systems

NO.	Plans	SCHEMATIC, LAYOUT AND ROUTING UPDATES
1	Doc	Guidelines to minimize ESD events that may cause loss of CMOS contents.
2	Doc	Correct Strapping for SMC FDC37C932FR Ultra IO device VBAT pin.

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Section 6.2.18, Ultra IO Support

General Design Considerations

1. Implementing a RESET BUTTON for Desktop Based Systems

The following should be considered when implementing a RESET BUTTON for desktop-based systems:

The system reset button has typically been connected indirectly to the PWROK input of the PiiX4/PiiX4E. This technique will not reset the suspend well logic, which includes the SMBus Host and Slave controllers. To reset the hardware in the suspend well, the reset button should be connected to the RSMRST# input of the PIIX4/PIIX4E. Assertion of RSMRST#, via a reset button, will result in a complete system reset. RSMRST# assertion will cause SUS[A-C]# to assert which results in the deassertion of PWROK if SUS[A-C]# controls the power supply PS-ON control signal. The deassertion of PWROK will cause the PIIX4/PIIX4E to assert PCIRST#, RSTDRV, and CPURST.

2. SLP# Connectivity in Multi-processor Systems

For multi-processor systems using the PiiX4/PiiX4E, the SLP# signal may be asserted to one of the processors before it is in a processor sleep state 3, and therefore not yet acknowledged. This could result in a wakeup problem.

Specifically, For PiiX4/PiiX4E based platforms, STPCLK# from the PiiX4E is connected to all processors, and SLP# from the PiiX4E is connected to all processors. The following sequence occurs:

1) OS writes to PMCNTRL register

2) PiiX4E asserts STPCLK#, then waits for Stop Grant

3) The processor acknowledges with a Stop Grant Acknowledge

4) PiiX4E asserts SLP# after receiving Stop Grant Acknowledge

While this sequence works for uni-processor systems, processors are put into Processor Sleep State 3, not State 5, during ACPI S1 state. This means that the SLP# signal *must not be connected* to any processor in multi-processor systems.

Note that disabling the SLEEP_EN bit in the PiiX4E Processor Control register is not an accecptable workaround for this issue since this bit only controls SLP# assertion in C3 state, not in S1 state.

Schematic, Layout and Routing Updates

1. Guidelines to Minimize ESD Events That May Cause Loss of CMOS Contents

Recommendations for New Board Designs:

1. Provide a 1uF X5R dielectric, monolithic, ceramic capacitor between the VCCRTC pin of the PIIX4/PIIX4E and the ground plane. This capacitor's positive connection should not be stubbed off the trace run and must be as close as possible to the PIIX4/PIIX4E. The capacitor must be no further than 0.5 inch from the PIIX4/PIIX4E. If a stub is required, it should be kept to a few mm maximum length. The ground connection should be made through a via to the ground plane, with no or minimal trace between the capacitor pad and the via.

2. Place the battery, 1K Ohm series current limit resistor, and the common-cathode isolation diode very close to the PIIX4/PIIX4E. If this is not possible, place the common-cathode diode and the 1K Ohm resistor as close to the 1uF capacitor as possible. Do not place these components between the capacitor and the PIIX4. The battery can be placed remotely from the PIIX4/PIIX4E.

3. On boards that have chassis-intrusion utilizing external logic powered by the VCCRTC pin, place the inverters as close to the common-cathode diode as possible. If this is not possible, keep the trace run near the center of the board.

4. Keep the PIIX4/PIIX4E VCCRTC trace away from the board edge. If this trace must run from opposite ends of the board, keep the trace run towards the board center, away from the board edge where contact could be made by people and equipment that handle the board.

Recommendations for Existing Board Designs:

1. The effectiveness of adding a 1uF capacitor, as identified above, needs to be determined by examining the routing and placement. For example, placing the capacitor far from the PiiX4 reduces its effectiveness.

2. Correct Strapping for SMC FDC37C932FR Ultra IO Device VBAT Pin

When the PIIX4/PIIX4E internal RTC is used, the SMC Ultra IO device, FDC37C932FR, VBAT pin must be connected to ground through between a 1K and 0 ohm pulldown resistor.

Documentation Changes

1. Design Checklist, section 6.2.18, Ultra IO Support

A new section will be added to section 6.2 as described below.

"When the PIIX4/PIIX4E internal RTC is used, ensure that the VBAT pin of the SMC Ultra IO device, FDC37C932FR, is connected to ground through between a 1K and 0 ohm pulldown resistor. Consult your IO device vendor for implementation guidelines for this or other IO devices."

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