Intel® 815EP Chipset Platform

Design Guide Update

April 2002

Notice: The Intel® 815EP Chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 290717-003

Contents

Revision History

Revision	Draft/Changes	Date
-001	Initial Release	July 2001
-002	Added Document Changes #32 – 42.	February 2002
-003	Added Document Changes #43 – 44	April 2002

Preface

This Design Guide Update document is an update to the specifications and information contained in the documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and document changes. This document is intended for hardware system manufacturers and for software developers of applications, operating system, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2000. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This update document contains a complete list of all known information types.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 815EP Chipset Platform Design Guide	290692-001

Nomenclature

General Design Considerations includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® 815EP Chipset.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Shaded: This item is either new or modified from the previous version of the document.

Number.	GENERAL DESIGN CONSIDERATIONS
1	Changed: Intel® 815EP Signal Names, Section 1.2.2.2; Text and Table Replaced

Number	SCHEMATIC, LAYOUT AND ROUTING UPDATES
	There are no Schematic, Layout and Routing Updates changes in this Design Guide Update revision.

Number	DOCUMENTATION CHANGES
1	Changed: USB General Guidelines, Section 9.5; Changed and Expanded
2	Changed: AC '97, Section 9.3; Expanded

Number	DOCUMENTATION CHANGES
3	Added: AC '97 Audio Codec Detect Circuit and Configuration Options, Section 9.3.1
4	Added: SPKR Pin Considerations, Section 9.3.2
5	Added: Disabling the Native USB Interface of the ICH2, Section 9.5.1
6	Changed: LAN Layout Guidelines, Section 9.11; Modified
7	Changed: LAN Connect Interface Checklist, Section 12.4.3; Expanded
8	Changed: AC '97 Checklist, 12.4.14; Expanded
9	Changed: LPC/FWH Guidelines, Section 9.12; Expanded
10	Added: FWH Decoupling, Section 9.12.3
11	Changed: Primary IDE Connector Requirements, Section 9.2.3; Expanded
12	Changed: Secondary IDE Connector Requirements, Section 9.2.4; Expanded
13	Changed: Intel® 82562ET / 82562EH Dual Footprint Guidelines, Section 9.11.5; Modified
14	Added: 3.3V/V5REF Sequencing, Section 11.4.3
15	Added: RTC-Well Input Strap Requirements, Section 9.10.8
16	Changed: LAN Layout Guidelines, Section 9.11; Expanded
17	Changed: General Trace Routing Considerations, Section 9.11.2.1; Modified
18	Changed: Intel® 82562ET / 82562EM Termination Resistors, Section 9.11.4.3, Modified
19	Changed: Intel® 82562ET / 82562EH Dual Footprint Guidelines, Section 9.11.5, Modified
20	Changed: PCI Interface, Section 12.4.1; Modified
21	Changed: Power Management, Section 12.4.9; Modified
22	Changed: RTC-Well Input Strap Requirements, Section 9.10.8; Title Changed
23	Changed: RTC Crystal, Section 9.10.1; Modified
24	Changed: RTC, RTCX1-RTCX2 Checklist Item, Section 12.4.13; Modified
25	Changed: General Design Considerations, Section 2; Expanded
26	Changed: 82562ET / 82562EH Dual Footprint Guidelines, Section 9.11.5; Modified
27	Changed: FWH Vpp Design Guidelines, Section 9.12.2; Expanded
28	Added: Intel® 82562ET/EM Disable Guidelines, Section 9.11.4.6
29	Changed: RTC, Section 12.4.13; Expanded
30	Changed: USB, Section 9.5; Modified
31	Changed: RTC Crystal, Section 9.10.1, Figure 52, ICH2 RTC Crystal Circuit Capacitor C1 Value; Modified
32	Added Information and Figure to Section 9.10.8, Power-Well Isolation Control Strap Requirements.
33	Changed Section 12.4.9, Power Management.
34	Added Information to Section 1.2.2.1, Intel® 82815EP MCH. Packaging/Power
35	Replaced Figure 72, Power Delivery Map
36	Added Section 8.5 Power_Supply PS_ON Considerations
37	Changed Section 12.4.13, RTC, Add SUSCLK to the Checklist

Number	DOCUMENTATION CHANGES
38	Changed Section 12.4.16, Power, Modify Checklist Recommendations for 5V_REF_SUS
39	Changed Section 13.3.3, 3.3V/V5REF Sequencing
40	Changed Figure 59, Trace Routing, in Section 9.11.2.1, General Trace Routing Considerations
41	Changed Table 30, Intel® CK-815 (2-DIMM) Clocks, in Section 10.1, 2-DIMM Clocking
42	Changed Table 31, Intel® CK-815 (3-DIMM) Clocks, in Section 10.2, 3-DIMM Clocking
43	Changed Section 11.4.3, 3.3V/V5REF Sequencing
44	Changed Figure 72, Power Delivery Map, in Section 11, Power Delivery

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General Design Considerations

1. Changed: Intel® 815EP Signal Names, Section 1.2.2.2; Text and Table Replaced

The section is replaced with the following information. Note, changes are highlighted by indentation and underlining:

1.2.2.2 Intel® 815E to Intel® 815EP Signal Name Changes

82815E pins associated with display interface signals, digital video out/TV-out signals, and some clock, power, and ground signals have name changes. The following table shows the old 82815E signal name, the ball number, and the new 82815EP signal name. *New designs for new 815EP boards should use pull-ups or pull-downs as indicated by the 815EP signal name. 815E boards using 815EP devices may leave the associated 815E pins in the original 815E configuration.*

Table 1. Intel® 82815E to Intel® 82815EP Pin Name Changes

815E Signal Name	Ball#	815EP Signal Name
LTVDATA0	AD16	NC
LTVDATA1	AF17	NC
LTVDATA2	AE17	NC
LTVDATA3	AD17	NC
LTVDATA4	AF18	NC
LTVDATA5	AD18	NC
LTVDATA6	AF20	NC
LTVDATA7	AD20	NC
LTVDATA8	AC20	NC
LTVDATA9	AF21	NC
LTVDATA10	AE21	NC
LTVDATA11	AD21	NC
LTVBLANK#	AB19	NC
TVCLKIN/INT#	AC18	PU1.8
LTVCLKOUT0	AE19	NC
LTVCLKOUT1	AF19	NC
LTVVSYNC	AC16	NC
LTVHSYNC	AB17	NC
LTVDA	AA20	*PU3.3*
LTVCK	AB21	*PU3.3*
DDCK	AB18	*PU3.3*
DDDA	AA18	*PU3.3*
DCLKREF	AE24	PD
IWASTE	Y20	*CDG*
IREF	AD23	PD
VSYNC	AF22	NC
HSYNC	AF23	NC
RED	AD22	NC
GREEN	AE22	NC
BLUE	AE23	NC
LOCLK	R22	NC
LRCLK	P22	PD
VSSDA	Y19	VSS
VSSDACA	AE25	VSS
VCCDA	*AA21*	*VCCDA*

NC = No Connect. These pins should float

PU3.3 = *Pull Up to 3.3 V through a weak pull-up resistor. (8.2 kΩ to 10 kΩ resistor.) Note that these pins in an 815EP platform can no longer function as GPIO(x) pins.*

PD = Pull-Down. These pins should be pulled down to ground through a weak pull-down resistor. (8.2 kΩ to 10 kΩ resistor.)

VSS = Connect to ground.

PU1.8 = Pull-Up to 1.8 V through a weak pull-up resistor. (8.2 kΩ to 10 kΩ resistor.)

VCCDA **=** *VCCDA, VCCDACA1, and VCCDACA2 (using the 815E signal names.) These pins in a new platform designed to use only the 815EP device provide bias to the core voltage. The original 815E VCCDA, VCCDACA1, and VCCDACA2 connections to a VCC1.8 supply must be retained in an 815EP platform.*

CDG **=** *Connect directly to ground. IWASTE (Ball# Y20) does not require a pull down resistor. Connect this pin directly to ground.*

Schematic, Layout and Routing Updates

There are no Schematic, Layout and Routing Updates changes in this Design Guide Update revision.

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Documentation Changes

1. Changed: USB General Guidelines, Section 9.5; Changed and Expanded

The following changes have been implemented in Section 9.5, *USB* (page 102).

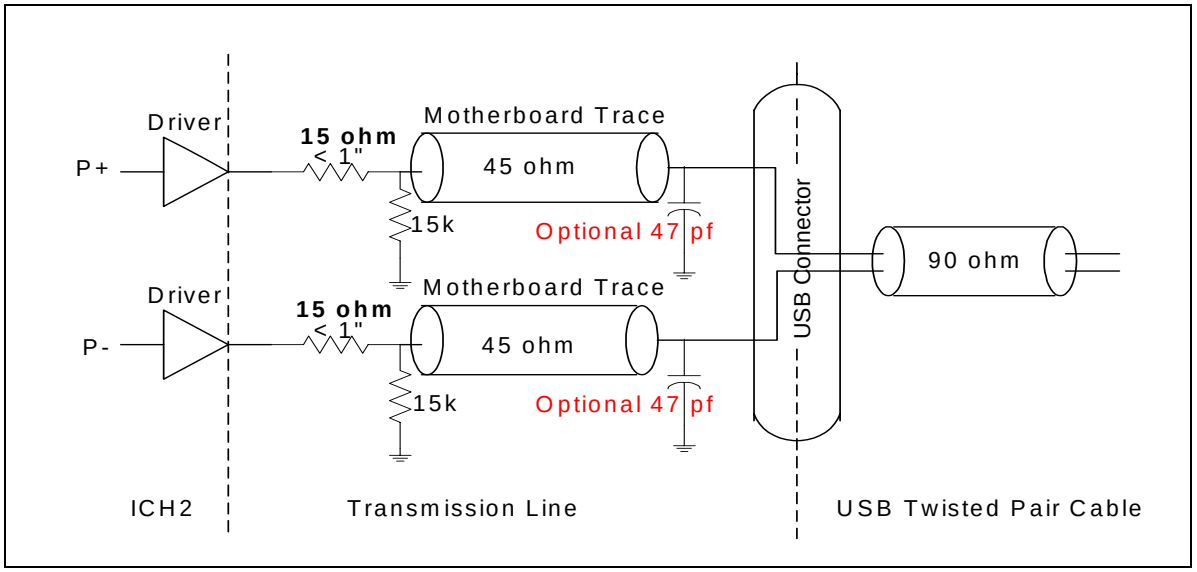
The third bullet is changed to read:

- An optional 47 pF cap may be placed as close to the USB connector as possible on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). This cap can be used for signal quality (rise/fall time) and to help minimize EMI radiation.

The sixth bullet is changed to read:

- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. Lastly, do not route over plane splits.

Figure 49, USB Data Signals, page 103, is replaced with the following figure:



2. Changed: AC ’97, Section 9.3; Expanded

After the third paragraph (which begins, “Intel has. . .”), following Figure 47, add the following paragraph:.

The AC ’97 interface can be routed using 5 mil traces with 5 mil space between the traces. Maximum length between ICH2 to CODEC/CNR is 14 inches in a tee topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4 inches for the AC-link. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

3. Added: AC ’97 Audio Codec Detect Circuit and Configuration Options, Section 9.3.1

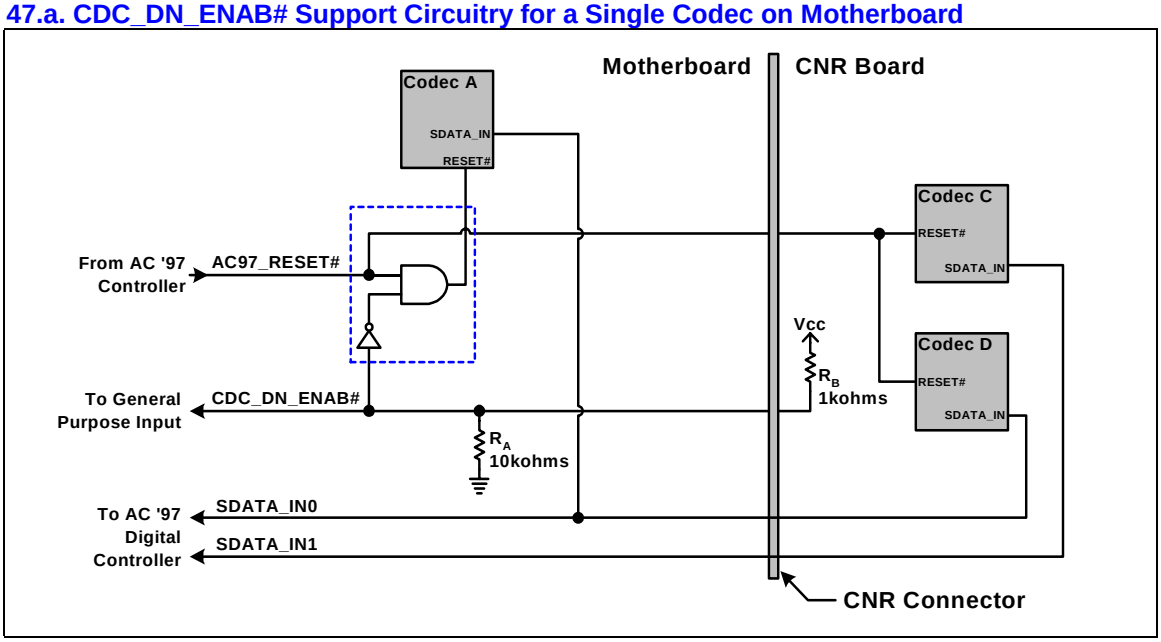
9.3.1 AC ’97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Please refer to Intel’s White Paper Recommendations for ICHx/AC ’97 Audio (Motherboard and Communication and Network Riser) for Intel’s recommended codec configurations.

To support more than two channels of audio output, the ICH2 allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC ’97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

The following circuits (Figure 47.a., Figure 47.b, Figure 47.c., and Figure 47.d.) show the adaptability of a system with the modification of R_A and R_B combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration and allows the configuration of the link to be determined by the BIOS so that the correct PnP IDs can be loaded.

Figure 47.a. CDC_DN_ENAB# Support Circuitry for a Single Codec on Motherboard



As shown in Figure 47.a., when a single codec is located on the motherboard, the resistor R_A and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented, on the motherboard. This circuitry is required in order to disable the motherboard codec when a CNR is installed which contains two AC ’97 codecs (or a single AC ’97 codec which must be the primary codec on the AC-Link).

By installing resistor R_B (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset) and the codec(s) on the CNR take control of the AC-link. One possible example of using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

The architecture shown in Figure 47.b. has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor R_B on the CNR to 100 kΩ). An example of one such upgrade is increasing from two-channel to four or six-channel audio.

Both Figure 47.b. and Figure 47.c. show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_IN*n* line as to not conflict with the motherboard codec(s).

Figure 47.b. CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade

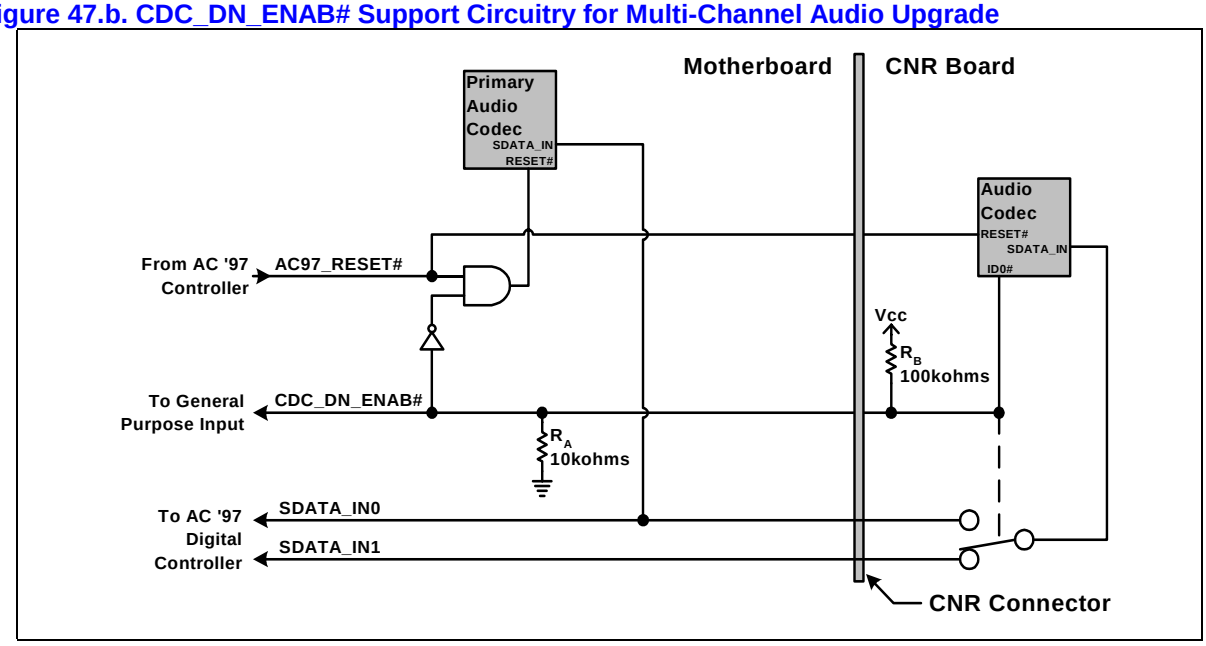


Figure 47.c. shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration the resistor, R_B, has been changed to 100 kΩ.

Figure 47.c. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / One-Codec on CNR

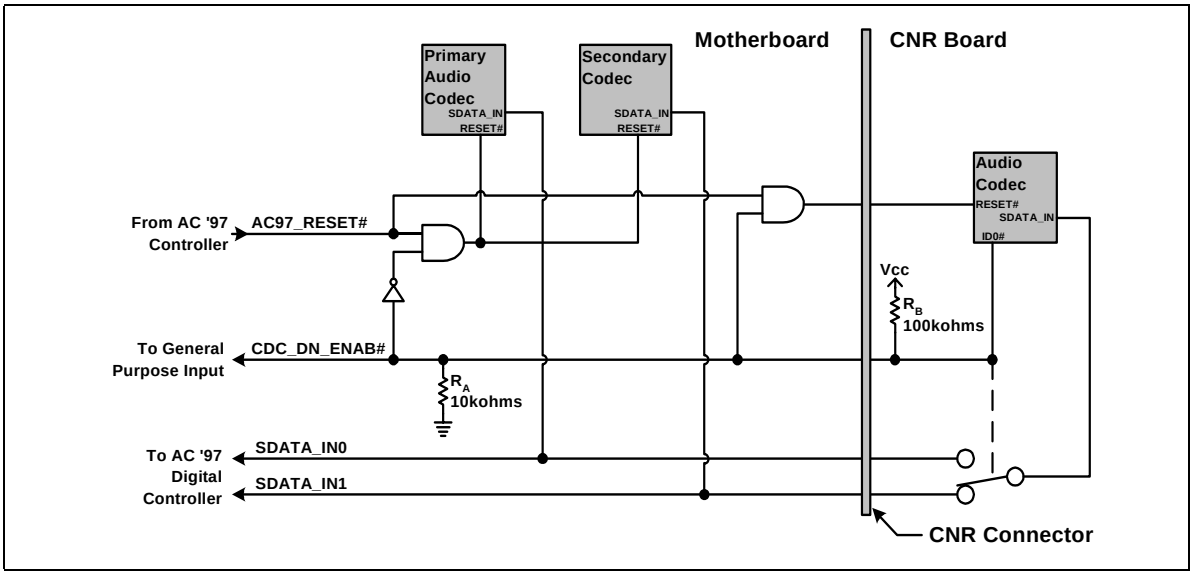
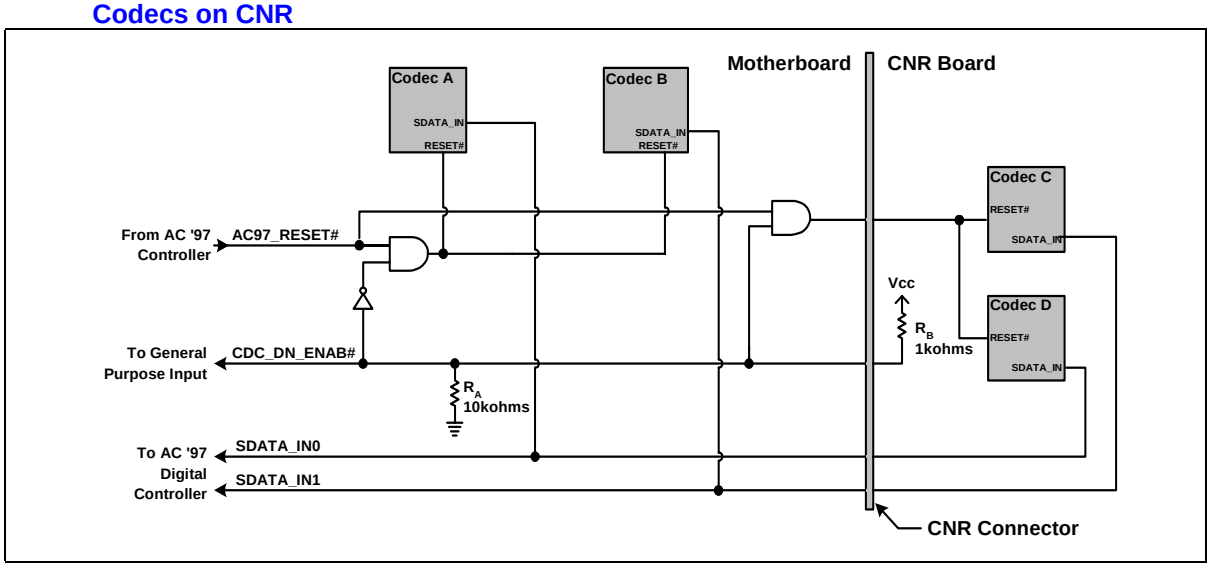


Figure 47.d. shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by R_A being 10 kΩ and R_B being 1 kΩ.

Figure 47.d. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / Two-Codecs on CNR



Circuit Notes

1. While it is possible to disable down codecs, as shown in Figure 47.a. and Figure 47.d., it is recommended against for reasons cited in the ICHx/AC'97 White Paper, including avoidance of shipping redundant and/or non-functional audio jacks.
2. All CNR designs include resistor R_B. The value of R_B is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
3. Any CNR with two codecs must implement R_B with value 1 kΩ. If there is one codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff R_B. If implemented, R_B must be connected to the same power well as the codec so that it is valid whenever the codec has power.
4. A motherboard with one or more codecs down must implement R_A with a value of 10 kΩ.
5. The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is *required* to be connected to a GPI; a connection to a GPIO is *strongly recommended* for testing purposes.

Table 25.a. Signal Descriptions

CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC '97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC '97 Interface.
AC97_RESET#	Reset signal from the AC '97 Digital Controller (ICH2).
SDATA_IN*n*	AC '97 serial data from an AC '97-compliant codec to an AC '97-compliant controller (i.e., the ICH2).

Valid Codec Configurations

Table 25.b. Codec Configurations

Valid Codec Configurations
AC(Primary)
MC(Primary)
AMC(Primary)
AC(Primary) + MC(Secondary)
AC(Primary) + AC(Secondary)
AC(Primary) + AMC(Secondary)

Invalid Codec Configurations
MC(Primary) + X(any other type of codec)
AMC(Primary) + AMC(Secondary)
AMC(Primary) + MC(Secondary)

4. Added: SPKR Pin Considerations, Section 9.3.2

9.3.2 SPKR Pin Considerations

The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 kΩ. Failure to due so will cause the TCO Timer Reboot function to be erroneously disabled. SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of POWEROK. When enabled, the ICH2 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull up resistor (the resistor is only enabled during boot/reset). Therefore its default state when the pin is a "no connect" is a logical one or enabled. To disable the feature, a jumper can be populated to pull the signal line low. The value of the pulldown must be such that the voltage divider caused by the pull down and integrated pull up resistors will be read as logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or lower than the integrated pull up resistor. It is therefore strongly recommended that the effective impedance be greater than 50 kΩ and the pulldown resistor be less than 7.3 kΩ.

5. Added: Disabling the Native USB Interface of the Intel® ICH2, Section 9.5.1

9.5.1 Disabling the Native USB Interface of Intel® ICH2

The ICH2 native USB interface can be disabled. This can be done when an external PCI based USB controller is being implemented in the platform. To disable the native USB Interface, ensure the differential pairs are pulled down thru 15 kΩ resistors, ensure the OC[3:0]# signals are de-asserted by pulling them up weakly to VCC3SBY, and that both function 2 and 4 are disabled via the D31:F0;FUNC_DIS register. Ensure that the 48 MHz USB clock is connected to the ICH2 and is kept running. This clock must be maintained even though the internal USB functions are disabled.

6. Changed: LAN Layout Guidelines, Section 9.11; Modified

Section 9.11.1, *ICH2 – LAN Interconnect Guidelines*, add the following sentence to the last paragraph:

> The AC Characteristics for this interface is found in the ICH2 EDS Addendum (Doc# FM-1720). Dual footprint guidelines are found in Section 4.17.5.

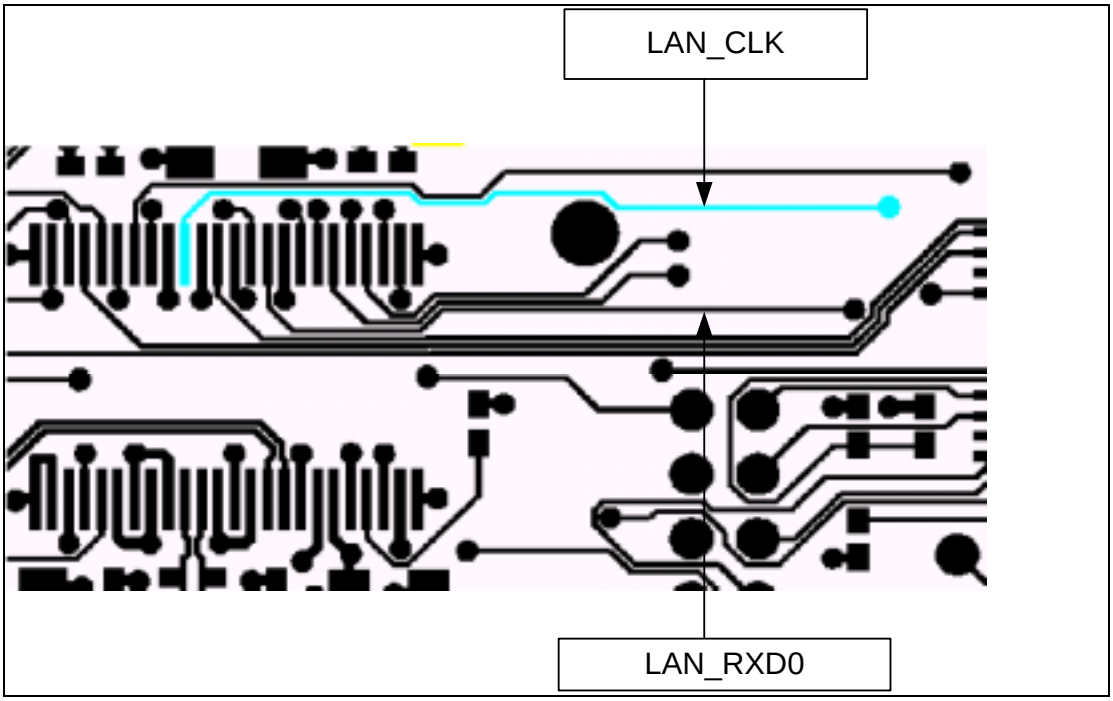
Section 9.11.1.2, *Point-to-Point Interconnect*. Table 28, *Single-Solution Interconnect Length Requirements*, is changed to show:

Configuration	L	Comment
82562EH	4.5” to 10”	Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected.
82562ET	3.5” to 10”	
CNR	3” to 9”	The trace length from the connector to LOM should be 0.5” to 3.0”

Section 9.11.1.3, *LOM/CNR Interconnect*, Table 29, *LOM/CNR Length Requirements*, is changed to show:

Configuration	A	B	C	D
82562EH	0.5” to 6.0”	4.0” to (10.0” – A)		
82562ET	0.5” to 7.0”	3.0” to (10.0” – A)		
Dual footprint	0.5” to 6.5”	3.5” to (10.0” – A)		
82562ET/EH card*	0.5” to 6.5”		2.5” to (9” – A)	0.5” to 3.0”

Section 9.11.1.4, *Signal Routing and Layout*, Figure 58, *LAN_CLK Routing Example* is changed to show:



Section 9.11.2.1, *General Trace Routing Considerations*, the sixth bullet is changed to read:

Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils recommended).

Section 9.11.2.1, *General Trace Routing Considerations*, the eighth bullet is changed to read:

For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45 degree bends instead. Refer to Figure 59, *Trace Routing*.

Section 9.11.2.1.1, *Trace Geometry and Length*, the following sentence is added to the last paragraph:

Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board.

Section 9.11.2.1.2, *Signal Isolation*, change the first bullet to read:

Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together.

Section 9.11.2.2.1, *General Power and Ground Plane Considerations*, change the last bullet to read:

Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1. 6 mm (59.0 mil). This is a ***critical*** requirement needed to past FCC part 68 testing for Phoneline connection. Note: For worldwide certification a trench of 2.5 mm is required. In North America, the spacing requirement is 1.6 mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5-mm spacing.

Section 9.11.2.3, *A 4-Layer Board Design*. change the material under the heading *Ground Plane* to read:

A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the 82562 digital ground using a ground cutout, etc.

Section 9.11.2.4, *Common Physical Layout Issues*. change item 3 to read:

3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (<= 1 inch).

Section 9.11.2.4, Com*mon Physical Layout Issues*. Change the Note at the end of the paragraph to read:

Note: It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces. Close should be considered to be less than 0.030 inch between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

7. Changed: LAN Connect Interface Checklist, Section 12.4.3; Expanded

12.4.3 LAN Connect Interface

Checklist Items	Recommendations	Comments
1	Trace Spacing: 5 mils wide, 10 mil spacing	
2	LAN Max Trace Length ICH2 to CNR: L = 3” to 9” (0.5” to 3” on card)	To meet timing requirements
3	Stubs due to R-pak CNR/LOM stuffing option should not be present.	To minimize inductance
4	Maximum Trace Lengths: ICH2 to 82562EH: L = 4 inches; 82562EM: L = 4.5 inches to 8.5 inches.	To meet timing requirements
5	Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches (clock must be longest trace)	To meet timing and signal quality requirements
6	Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN phy.	To meet timing and signal quality requirements
7	Keep the total length of each differential pair under 4 inches.	Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and or degraded receive BER.
8	Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	To minimize cross-talk
9	Distance between differential traces and any other signal line is 100 mils. (300 mils recommended)	To minimize cross-talk
10	Route 5 mils on 7 mils for differential pairs (out of LAN phy)	To meet timing and signal quality requirements
11	Differential trace impedance should be controlled to be ~100 Ω.	To meet timing and signal quality requirements
12	For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends.	To meet timing and signal quality requirements
13	Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
14	Do not route traces and vias under crystals or oscillators.	This will prevent coupling to or from the clock
15	Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	To control trace EMI radiation
16	Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors
17	Vias to decoupling capacitors should be sufficiently large in diameter.	To decrease series inductance
18	Avoid routing high-speed LAN* or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, CPU, or other similar devices.	To minimize cross-talk

Checklist Items	Recommendations	Comments
19	Isolate I/O signals from high-speed signals.	To minimize cross-talk
20	Place the 82562ET/EM part more than 1.5 inches away from any board edge.	This minimizes the potential for EMI radiation problems
21	Place at least one bulk capacitor (4.7 µF or greater) on each side of the 82562ET/EM.	Research and development has shown that this is a robust design requirement
22	Place decoupling caps (0.1 µF) as close to the 82562ET/EM as possible.	
23 LAN_CLK	Connect to LAN_CLK on Platform LAN Connect Device.	
24 LAN_RXD[2:0]	Connect to LAN_RXD on Platform LAN Connect Device. ICH2 contains integrated 9 kΩ pull-up resistors on interface.	
25 LAN_TXD[2:0] LAN_RSTSYNC	Connect to LAN_TXD on Platform LAN Connect Device.	

8. Changed: AC '97 Checklist, 12.4.14; Expanded

Section 12.4.14, is expanded by adding the following items to the existing checklist:

1. 12.4.14. AC '97

Checklist Items	Recommendations	Comments
1	Z_0 AC '97 = 60 Ω ± 15%	
2	5-mil trace width, 5-mil spacing between traces	
3	Max Trace Length ICH2/Codec/CNR = 14 inches	

9. Changed: LPC/FWH Guidelines, Section 9.12; Expanded

Section 9.12, *LPC/FWH*, is expanded as shown:

9.12. LPC/FWH

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

10. Added: FWH Decoupling, Section 9.12.3

9.12.3 FWH Decoupling

A 0.1 µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the Vcc supply pins and the Vss ground pin to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the Vcc supply pins.

11. Changed: Primary IDE Connector Requirements, Section 9.2.3; Expanded

Section 9.2.3, *Primary IDE Connector Requirements*, add this bullet to the bullet list below Figure 45:

- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

12. Changed: Secondary IDE Connector Requirements, Section 9.2.4; Expanded

Section 9.2.4, *Secondary IDE Connector Requirements*, add this bullet to the bullet list below Figure 46:

- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

13. Changed: Intel® 82562ET / 82562EH Dual Footprint Guidelines, Section 9.11.5; Modified

Section 9.11.5, *82562ET / 82562EH Dual Footprint Guidelines*, beneath Figure 67, *Dual-Footprint Analog Interface*, is a list of additional guidelines for this configuration. Change the first bullet concerning length to read:

- L = 0.5 inch to 6.5 inches

14. Added: 3.3V/V5REF Sequencing, Section 11.4.3

11.4.3 3.3V/V5REF Sequencing

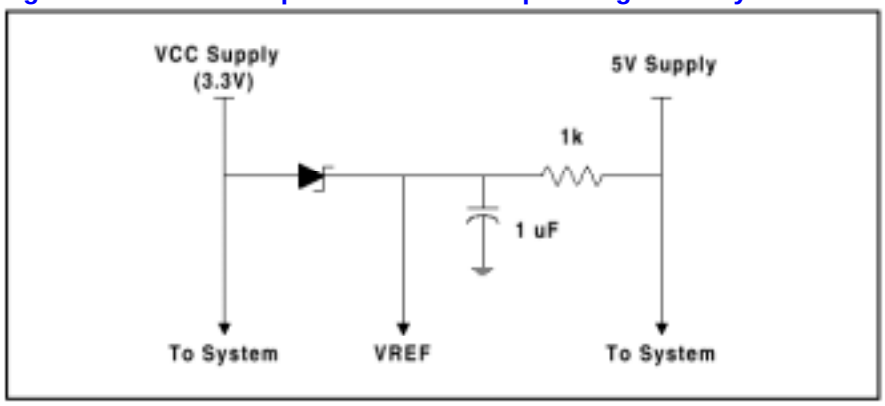
V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before or simultaneously to VCC3_3. It must also power down after or simultaneous to VCC3_3. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 77.a. shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result,

V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USBOC. If these signals are not needed during suspend, V5REF_Sus can be hooked to the VccSus3_3 rail.

Figure 77.a. Example 3.3V/V5REF Sequencing Circuitry



15. Added: RTC-Well Input Strap Requirements, Section 9.10.8

9.10.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 54 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

16. Changed: LAN Layout Guidelines, Section 9.11; Expanded

Two sentences are added to the first paragraph of Section 9.11, *LAN Layout Guidelines*, as shown.

9.11 LAN Layout Guidelines

The ICH2 provides several options for integrated LAN capability. The platform supports several components depending on the target market. These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

17. Changed: General Trace Routing Considerations, Section 9.11.2.1; Modified

Bullet 5 of Para 9.11.2.1, General Trace Routing Considerations is changed to read:

Do not route the transmit differential traces closer than 100 mils to the receive differential traces.

18. Changed: Intel® 82562ET / 82562EM Termination Resistors, Section 9.11.4.3, Modified

The first paragraph shown under Para 9.11.4.3, 82562ET / 82562EM Termination Resistors, has an incorrect resistor value for the 1% receive differential pairs (RDP/RDN). The value is changed from 100 Ω to 120 Ω. The paragraph should read:

The 100 Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120 Ω (1%) receive differential pairs (RDP/RDN) should be placed as close to the LAN connect component (82562ET or 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e. 82562ET), including the wire impedance reflected through the transformer.

19. Changed: Intel® 82562ET / 82562EH Dual Footprint Guidelines, Section 9.11.5, Modified

The first paragraph shown under Section 9.11.5, *82562ET / 82562EM Dual Footprint Guidelines*, references an incorrect section of the Design Guide. The fourth sentence of the paragraph should read:

The guidelines called out in Sections 9.11.1 through 9.11.4 apply to this configuration.

20. Changed: PCI Interface, Section 12.4.1; Modified

The PME# checklist item in Section 12.4.1, *PCI Interface*, is changed as shown below:

PME#	This signal has an integrated pull-up of 24K.

21. Changed: Power Management, Section 12.4.9; Modified

The PWRBTN# checklist item in Section 12.4.9, *Power Management*, is changed as shown below:

PWRBTN#	This signal has an integrated pull-up of 24K.

22. Changed: RTC-Well Input Strap Requirements, Section 9.10.8; Title Changed

The title of Section 9.10.8. is changed to *Power-Well Isolation Control Strap Requirements*.

23. Changed: RTC Crystal, Section 9.10.1; Modified

Section 9.10.1, *RTC Crystal*, Figure 52, *External Circuitry for the ICH2 RTC,* Note 1, is changed as shown below:

1. The exact capacitor value needs to be based on what the crystal maker recommends. (Typical values for C2 and C3 are 18 pF for a crystal with CLOAD=12.5 pF)

24. Changed: RTC, RTCX1-RTCX2 Checklist Item, Section 12.4.13; Modified

The first sentence in the RTCX1-RTCX2 checklist item in Section 12.4.13, *RTC*, is changed as shown below:

RTCX1 RTCX2	Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor and use 18 pF decoupling caps (assuming crystal with CLOAD=12.5 pF) at each signal.

25. Changed: General Design Considerations, Section 2; Expanded

The last paragraph of Section 2, *General Design Considerations*, has the following material added to it so that the paragraph reads as follows:

> Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in the following figure. If this stack-up is not used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

26. Changed: Intel® 82562ET / 82562EH Dual Footprint Guidelines, Section 9.11.5; Modified

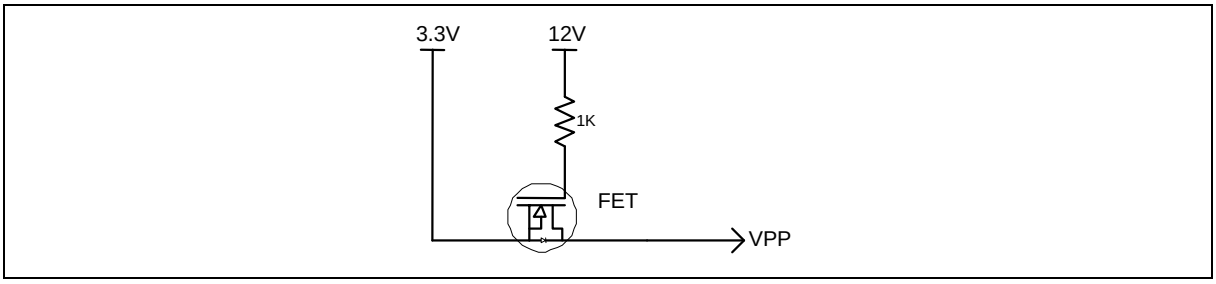
The bullets under Figure 67, *Dual-Footprint Analog Interface*, describe additional guidelines for Figures 66 and 67. The first bullet defines the "L" in Figure 62, *Dual Footprint LAN Connect Interface*. The "L" value is changed to 3.5 inches to 10 inches.

27. Changed: FWH Vpp Design Guidelines, Section 9.12.2; Expanded

Section 9.12.2., *FWH Vpp Design Guidelines*, has the following paragraph and figure added as shown below:

> In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 72.1 FWH VPP Isolation Circuitry

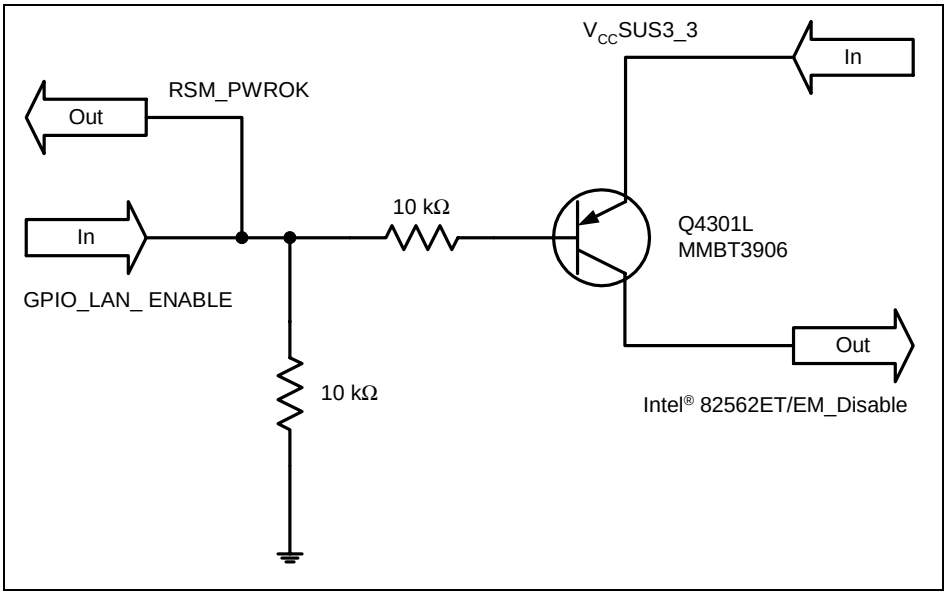


28. Added: Intel® 82562ET/EM Disable Guidelines, Section 9.11.4.6

9.11.4.6 Intel® 82562ET/EM Disable Guidelines

To disable the Intel 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS, by controlling the GPIO, can disable the LAN microcontroller.

Figure 64.1 : Intel® 82562ET/EM Disable Circuit



There are four pins which are used to put 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

The four control signals shown in the above table should be configured as follows: Test_En should be pulled-down through a 100 Ω resistor. The remaining three control signals should each be connected through 100 Ω series resistors to the common node "82562ET/EM_Disable" of the disable circuit.

29. Changed: RTC, Section 12.4.13; Expanded

The following checklist item is added to Section 12.4.3, *RTC*:

RTCRST#	Ensure 10 ms-20 ms RC delay (8.2 K & 2.2 µF) See Figure, *RTCRST External Circuit for the ICH2 RTC*.

30. Changed: USB, Section 9.5; Modified

The third bullet in Section 9.5, *USB*, is changed to read as follows:

An optional cap (0 pF – 47pF) may be placed as close to the USB connector side of the series resistors on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). This cap should be sized to minimize EMI radiation while still maintaining signal quality (rise/fall time, Vcrs, etc.).

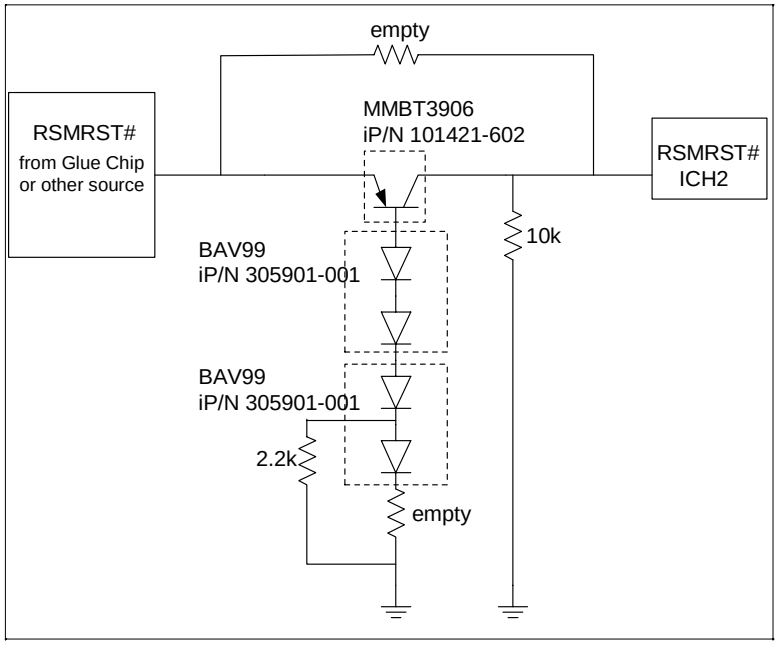
31. Changed: RTC Crystal, Section 9.10.1, Figure 52, Intel® ICH2 RTC Crystal Capacitor C1 Value; Changed

Reference Section 9.10.1, Figure 52, *External Circuitry for the ICH2 RTC*. The value of Capacitor C1 in Figure 52 is changed from 2.2 pF to 0.047 µF.

32. Added Information and Figure to Section 9.10.8, Power-Well Isolation Control Strap Requirements

Add the following information and figure to Section 9.10.8, *Power-Well Isolation Control Strap Requirements*:

The circuit shown in the figure below should be implemented to control well isolation between the 3.3V resume and RTC power-wells. Failure to implement this circuit may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power).



33. Changed Section 12.4.9, Power Management

Change the Recommendations for RSMRST# in Section 12.4.9, *Power Management*, to read as shown below:

"Connect to power monitoring logic, and should go high no sooner than 10 ms after both VccSUS3_3 and VccSus1_8 have reached their nominal voltages. Requires weak pull-down. Also requires well isolation control as directed in Section 10.10.8."

34. Added Information to Section 1.2.2.1, Intel® 82815EP MCH. Packaging/Power

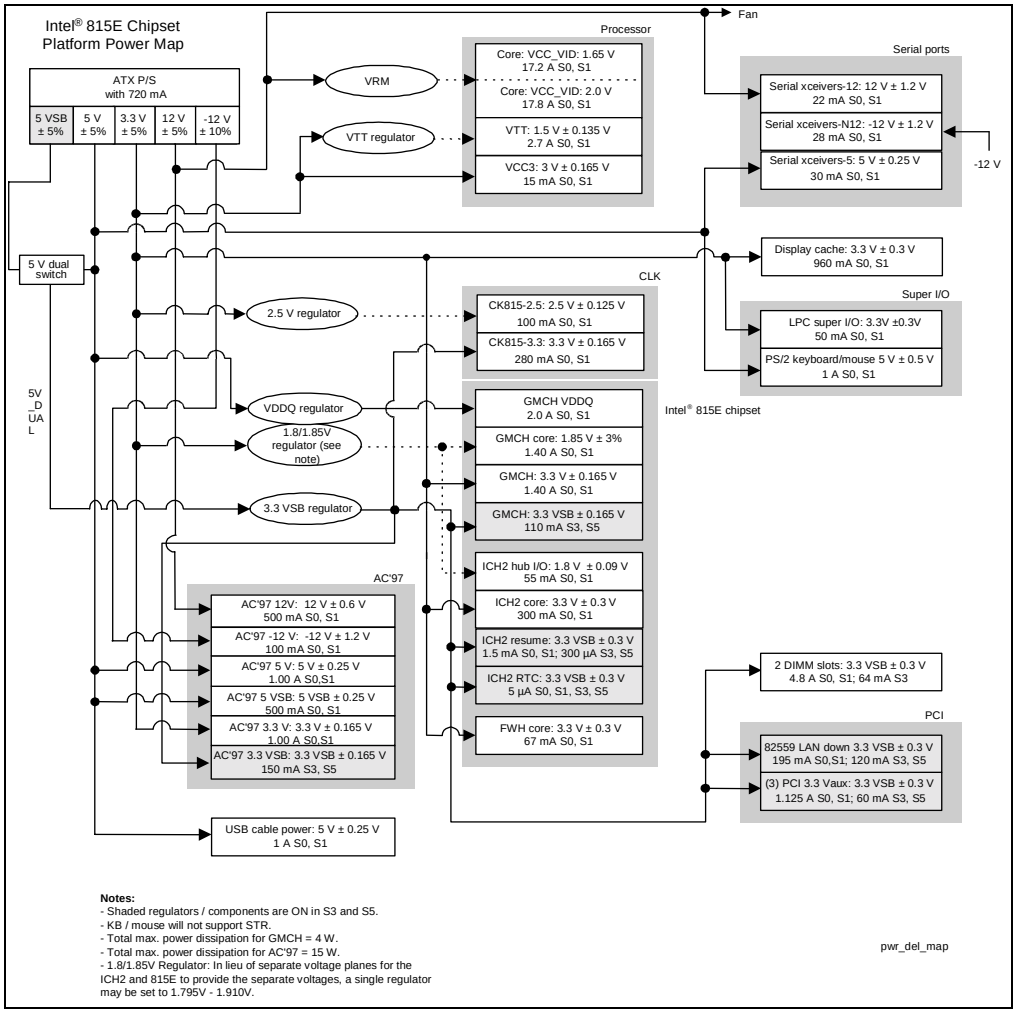
Reference Section 1.2.2.1, *Intel® 82815EP MCH, Packaging/Power*. Add the following information to the bullet so that it reads:

1.85 V core and mixed 3.3 V, 1.5 V, and AGTL+ IO. Note that the 82801BA ICH2 has a 1.8 V requirement and the 82815EP MCH has a 1.85 V requirement. Instead of separate voltage regulators to meet these requirements, a single voltage regulator can be set to 1.79 5V to 1.910V. See Figure 72, the *Power Delivery Map*.

35. Replaced Figure 72, Power Delivery Map

Figure 72, Power Delivery Map, is replaced with the following:

Figure 72. Power Delivery Map



36. Added Section 8.5 Power_Supply PS_ON Considerations

The following new section is added:

8.5 Power_Supply PS_ON Considerations

– If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10–100 mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

–The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

–The platform designer must ensure that the power supply used with the platform is not affected by this issue.

37. Changed Section 12.4.13, RTC, Add SUSCLK to the Checklist

Add the following as a new checklist item to Section 12.4.13, *RTC*:

SUSCLK	• To assist in RTC circuit debug, route SUSCLK to a test point if SUSCLK is unused.

38. Changed Section 12.4.16, Power, Modify Checklist Recommendations for 5V_REF_SUS

Change the second bullet in the Recommendations column of the 5V_REF_SUS to the following:

V5REF_SUS affects 5 V-tolerance for all USB pins and can be connected to VccSUS3_3 if ICH2 USB is not supported in the platform. If USB is supported, 5VREF_SUS must be connected to 5V_AUX, which remains powered during S5.

39. Changed Section 11.4.3, 3.3V/V5REF Sequencing

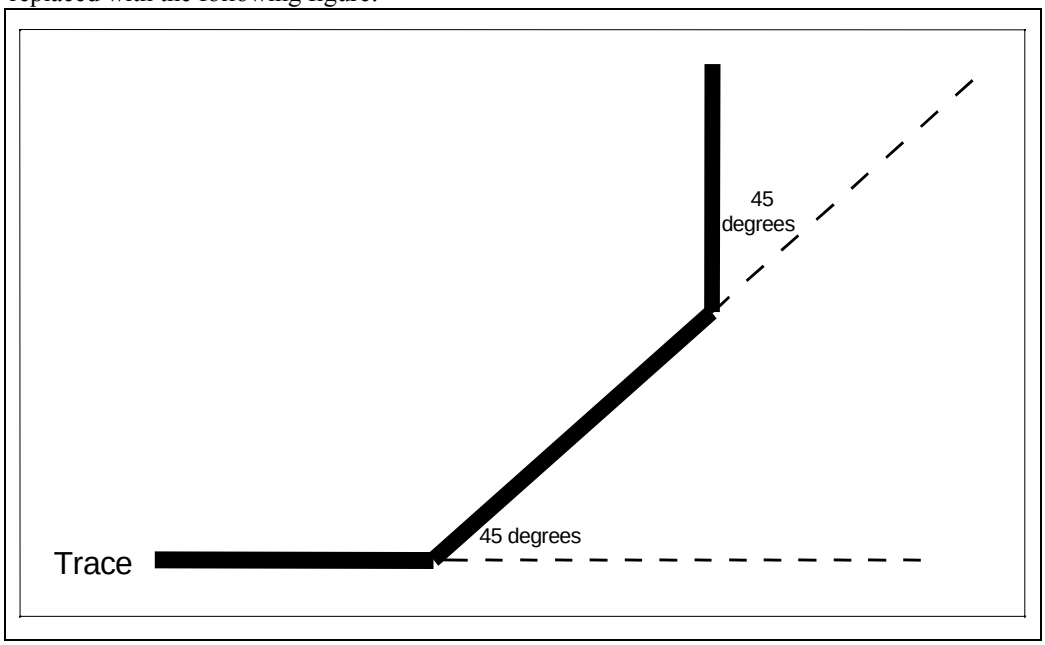
Change the second and third paragraphs of Section 11.4.3, *3.3V/V5REF Sequencing*, to the following:

This rule also applies to the stand-by rails. However, in most platforms the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USB pins (both over-current and data lines). If USB is not implemented in the system then V5REF_SUS can be connected to the VccSus3_3 rail. Otherwise when USB is supported, V5REF_SUS must be connected to 5V_AUX, which remains powered during S5.

40. Changed Figure 59, Trace Routing, in Section 9.11.2.1, General Trace Routing Considerations

Figure 59, Trace Routing, in Section 9.11.2.1, *General Trace Routing Considerations*, is replaced with the following figure:



41. Changed Table 30, Intel® CK-815 (2-DIMM) Clocks, in Section 10.1, 2-DIMM Clocking

The frequency entry for the 9 SDRAM clocks in Table 30, Intel® CK-815 (2-DIMM) Clocks, in Section 10.1, *2-DIMM Clocking*, is changed to "100/133 MHz".

Also, the first bullet under Table 30 is changed to show "100/133 MHz".

42. Changed Table 31, Intel® CK-815 (3-DIMM) Clocks, in Section 10.2, 3-DIMM Clocking

The frequency entry for the 9 SDRAM clocks in Table 31, Intel® CK-815 (3-DIMM) Clocks, in Section 10.2, *3-DIMM Clocking*, is changed to "100/133 MHz".

43. Changed Section 11.4.3, 3.3V/V5REF Sequencing

Section 11.4.3, *3.3V/V5REF Sequencing*, was added by Document Change #14 and modified by Document Change #39 in the public *Intel® 815EP Chipset Platform Design Guide Update* 290717-002, dated February 2002. Change the first paragraph of Section 11.4.3, *3.3V/V5REF Sequencing*, to the following:

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0 .7 V. The rule must be followed in order to ensure the safety

of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 77.a. shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

44. Changed Figure 72, Power Delivery Map, in Section 11, Power Delivery

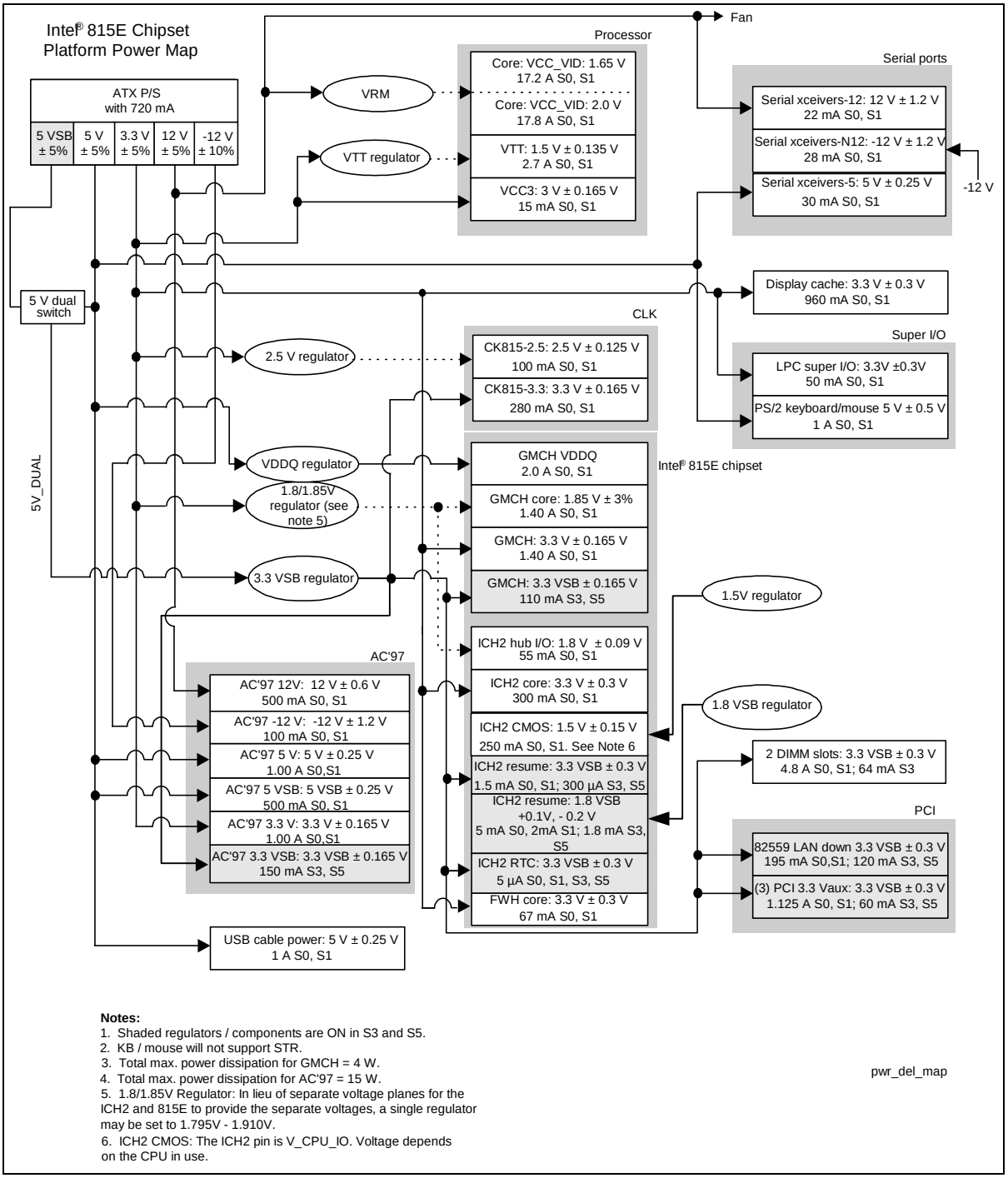
Figure 72, Power Delivery Map, in Section 11, *Power Delivery*, was replaced by Document Change #35 in the public *Intel® 815EP Chipset Platform Design Guide Update* 290717-002, dated February 2002. Figure 72 has two additional changes in the ICH2 section.

(1) One ICH2 power plane is added to it. This added ICH2 power plane is "ICH2 V5REF_SUS". This power plane has always existed in the ICH2. It is not new. This addition to the Power Delivery Map simply shows this ICH2 plane.

(2) The block labeled "ICH2 5V" is renamed to "ICH2 V5REF".

These two changes above also reflect the actual pin names on the ICH2.

Figure 72, *Power Delivery Map*, is replaced with the following:



Notes:
1. Shaded regulators / components are ON in S3 and S5.
2. KB / mouse will not support STR.
3. Total max. power dissipation for GMCH = 4 W.
4. Total max. power dissipation for AC'97 = 15 W.
5. 1.8/1.85V Regulator: In lieu of separate voltage planes for the ICH2 and 815E to provide the separate voltages, a single regulator may be set to 1.795V - 1.910V.
6. ICH2 CMOS: The ICH2 pin is V_CPU_IO. Voltage depends on the CPU in use.