Intel® 840 Chipset Platform

Design Guide

July 2000

Order Number: 298021-003

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Revision History

Revision	Description	Date
-001	Initial Release.	October 1999
-002	• Minor edits throughout for clarity. • Added P64H decoupling information. • Updated Figure 4-22, “High Speed CMOS Termination”. • Added Figure 4-25, “RSL Signal Routing Guidelines”. • Updated Figure 4-27, “AGP 2.0 V_{REF} Generation and Distribution for 1.5V and 3.3V Cards“. • Updated Figure 4-30, “MCH Single Hub Interface Reference Divider Circuit”. • Updated Figure 4-31, “MCH/ICH Locally Generated Hub Interface Reference Divider Circuit“. • Updated Table 7-1, “Thermal Design Power”.	January 2000
-003	• Minor edits throughout for clarity.	July 2000

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Introduction

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Introduction 1

This design guide organizes Intel's design recommendations for Intel® 840 chipset systems. In addition to providing motherboard design recommendations such as layout and routing guidelines, this document also addresses possible system design issues (e.g., thermal requirements for Intel® 840 chipset systems).

This document presents design recommendations, board schematics, debug recommendations, and a system checklist that should be used in system design. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues.

The debug recommendations should be consulted when debugging a Intel® 840 chipset system; however, these debug recommendations should be understood before completing board.

The Intel board schematics in Appendix A can be used as a reference for board designers. A feature list is provided at the beginning of the appendix. Although the schematics cover specific designs, the core schematics for each chipset component remains the same for most Intel® 840 chipset platforms. The appendix provides a set of reference schematics for each chipset component, in addition to common motherboard options. Additional flexibility is possible through other permutations of these options and components.

1.1 About This Design Guide

This design guide is intended for hardware designers who are experienced with PC architectures and board design. The design guide assumes that the designer has a working knowledge of the vocabulary and practices of PC hardware design.

- This chapter introduces the designer to the purpose and organization of this design guide, and provides a list of references of related documents. This chapter also provides an overview of the Intel® 820 chipset.
- Chapter 2, "Intel® Pentium® III Processor Layout Guidelines"—This chapter provides design guidelines for the Intel® Pentium® III processor including processor-specific layout guidelines.
- Chapter 3, "Intel® Pentium® III Xeon™ Processor at 600+ MHz Layout Guidelines"—This chapter provides design guidelines for the Intel® Pentium® III Xeon™ processor at 600+ MHz including processor-specific layout guidelines.
- Chapter 4, "Layout and Routing Guidelines"—This chapter provides a detailed set of motherboard layout and routing guidelines for designing an Intel® 820 chipset based platform. The motherboard functional units are covered (e.g., chipset component placement, system bus routing, system memory layout, display cache interface, hub interface, IDE, AC'97, USB, interrupts, SMBUS, PCD, LPC/FWH Flash BIOS, and RTC).
- Chapter 5, "System Bus: AGTL+ Design Guidelines"— AGTL+ guidelines and theory of operation are discussed. This chapter also provides more detail about the methodologies used to develop the guidelines.
- Chapter 6, "Clocking"— This chapter provides motherboard clocking guidelines (e.g., clock architecture, routing, capacitor sites, clock power decoupling, and clock skew).
- Chapter 7, "System Design Consideration"— This chapter includes guidelines regarding power delivery, decoupling, thermal, and power sequencing.

- Chapter 8, “Design Considerations/Checklist”— This chapter provides a design review checklist.
- Appendix A, “Reference Schematics”— This appendix provides a set of schematics for reference board. A feature list for the board design is also provided.

1.2 References

- *Intel® 840 Chipset: Intel® 82840 Memory Controller Hub (MCH)* Datasheet (Order Number: 298020)
- *Intel® 82801AA (ICH) and Intel® 82801AB (ICH0) I/O Controller Hub* Datasheet (Order Number: 290655)
- *Intel® 82802AB/82802AC FirmWare Hub (FWH)* Datasheet (Order Number: 290658)
- *Pentium® II Processor AGTL+ Guidelines* (Order Number: 243330)
- *Pentium® II Processor Power Distribution Guideline (*Order Number: 243332)
- *Pentium® II Processor Developer's Manual* (Order Number: 243341)
- *Intel® Pentium® III Processor Datasheet* (Order #244452)
- *Pentium® III Processor Specification Update* (latest off of website)
- *AP 907 Pentium III processor Power Distribution Guidelines* (Order Number 245085)
- *AP-585 Pentium II Processor AGTL+ Guidelines* (Order Number: 243330)
- *AP-587 Pentium II Processor Power Distribution Guidelines* (Order Number: 243332)
- CK98 Clock Synthesizer/Driver Specification
- CK133 Clock Synthesizer/Driver Specification
- *PCI Local Bus Specification*, Revision 2.2
- *Universal Serial Bus Specification*, Revision 1.0
- *VRM 8.4 DC-DC Converter Design Guidelines* (when available)
- AC’97 Component Specification, Revision 2.1
- Accelerated Graphics Port Interface Specification, Revision 2.0
- AGP Pro Specification, Revision 1.0
- Low Pin Count Interface Specification, Revision 1.0
- PCI Local Bus Specification, Revision 2.1
- PCI Local Bus Specification, Revision 2.2 ECNs
- PCI-PCI Bridge Specification, Revision 1.0
- PCI Bus Power Management Interface Specification, Revision 1.0
- Universal Serial Bus Specification, Revision 1.1

1.3 System Overview

The Intel® 840 chipset is a workstation/server chipset designed for Intel's Pentium® II processor and Intel® Pentium® III Xeon™ processor at 600+ MHz based architectures. This chipset allows flexibility for dual-processor configurations with a 133 MHz (2-way) system bus. The Intel® 840 chipset consists of 2 main components: Memory Controller Hub (MCH) and I/O Controller Hub (ICH). Architectural expansion is provided with memory expansion card, and PCI 64-bit Hub (P64H). The Intel® 840 chipset components are interconnected via an interface called hub interface. The hub interface design provides an efficient communication between the chipset components.

Additional hardware platform features, supported by Intel® 840 chipset, include AGP 4X, RDRAM, Ultra ATA/66, Low Pin Count interface (LPC), and Universal Serial Bus (USB). The Intel® 840 chipset architecture removes the requirement for the ISA expansion bus that was traditionally integrated into the I/O subsystem of PCIsets/AGPsets. Thus removing many conflicts experienced when installing legacy ISA hardware and drivers.

Intel® 840 chipset is ACPI compliant and supports Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-off power management states. Through the use of an appropriate LAN device, Intel® 840 chipset also supports wake-on-LAN* for remote administration and troubleshooting.

1.3.1 Intel® 840 chipset Components

This section provides an overview of the Memory Controller Hub (MCH) and I/O Controller Hub (ICH). Additional functionality can be provided using memory expansion (MRH-R memory repeater hubs) and the PCI 64-bit Hub.

1.3.1.1 Memory Controller Hub (MCH)

The MCH component contains the processor interface, DRAM controller, P64H interface, AGP interface and ICH interface. It communicates with the Intel® 840 chipset I/O controller (ICH) and the P64H over the hub interface. It supports dual channels of Direct RDRAM and AGP 4X data transfers. The MCH also contains advanced power management logic.

The Intel® 840 chipset MCH contains the following functionality:

- Provides Dual Channel Pre-Fetched Architecture
- Supports dual processor configuration at 133 MHz
- AGTL + host bus supporting 32 or 36 bit host addressing
- Dual Direct RDRAM channels support for 300 MHz or 400 MHz operation
- 8 GB RDRAM devices support
- AGP interface with 4X SBA/Data Transfer and 2X/4X Fast Write capability
- 8 bit/66 MHz hub interface A to ICH
- 16 bit/66 MHz hub interface B to P64H
- Fully optimized data paths and buffering
- Distributed arbitration for highly concurrent operation

1.3.1.2 I/O Controller Hub (ICH)

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many I/O functions. The ICH integrates:

- Upstream hub interface for access to the MCH
- 2 channel Ultra ATA/66 Bus Master IDE controller
- USB controller
- I/O APIC
- SMBus controller
- FWH Interface (FWH Flash BIOS interface)
- LPC interface
- AC'97 2.1 interface
- PCI 2.2 interface
- Integrated System Management controller
- Alert-on-LAN

The ICH also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces.

1.3.1.3 Memory Repeater Hub for RDRAM (MRH-R)

The MRH-R component provides the capability to support multiple RDRAM channels from an "expansion channel." The expansion channel is the interconnect between the Intel® 840 chipset MCH and the MRH-R. Each MRH-R can support up to 2 "stick" channels. The MRH-R acts as a pass-through logic with fixed delay for read and write accesses from expansion channels to RDRAM channels. The MRH-R features also include:

- Maximum of 1 GB memory per channel
- Nap Entry/Exit, Power down Exit, Refresh and Precharge on a channel upon request from memory controller
- Core logic gating to minimize power consumption
- Clock generation for Direct Rambus* Clock Generator (DRCG)
- Integrated SMBus controller to read/write data from/to SPD EEPROM on the RIMMs

1.3.1.4 PCI 64-bit Hub (P64H)

The PCI-64 Hub(P64H) is a peripheral chip that performs PCI bridging functions between the hub interface and the PCI Bus and is used as an integral part of the Intel® 840 chipset. The P64H has a 16-bit primary hub interface to the Memory Controller Hub (MCH) and a secondary 64-bit PCI Bus interface. The 64-bit interfaces inter-operates transparently with either 64-bit or 32-bit devices. The P64H is fully compliant with the *PCI Local Bus Specification, Revision 2.2.*

The P64H integrated functions include:

- Integrated PCI low skew clock driver
- I/O APIC

1.3.2 Bandwidth Summary

Table 1-1. Intel® 840 Chipset Platform Bandwidth Summary

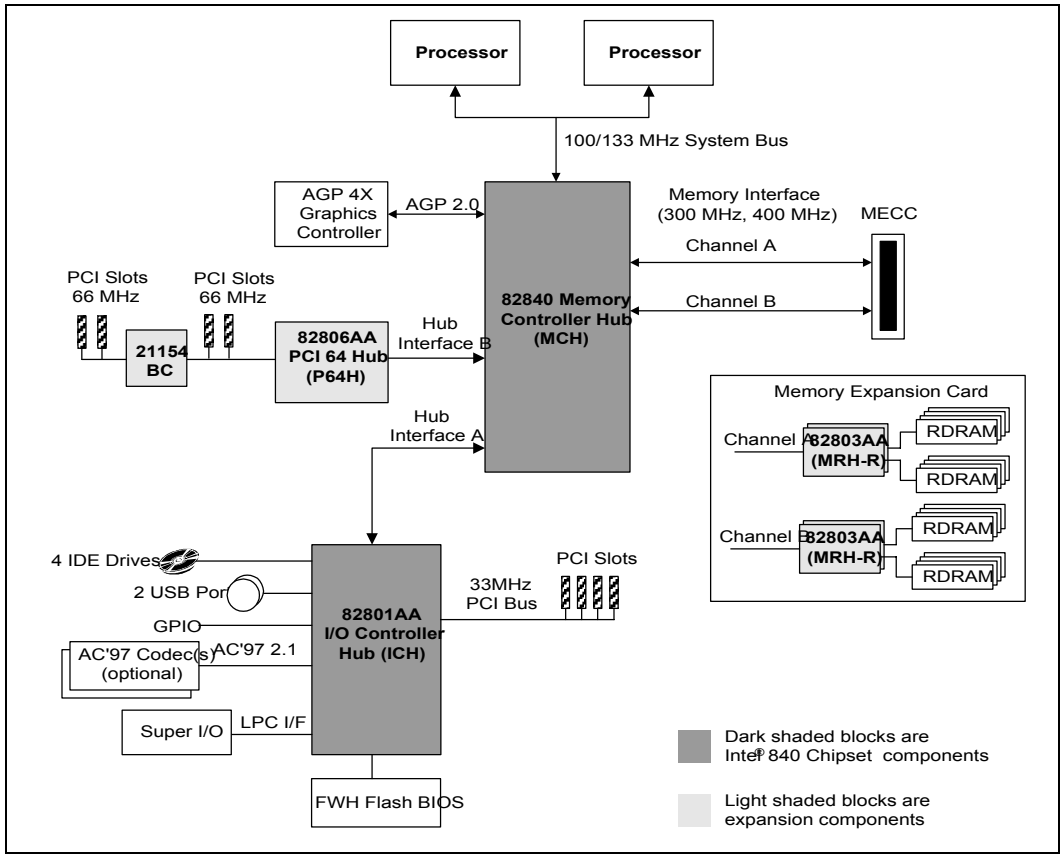
Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Msamples/s)	Data Width (Bytes)	Bandwidth (MB/s)
Processor Bus (2-way)	133	1	133	8	1066
Processor Bus (MP)	100	1	100	8	800
AGP 2.0	66	4	266	4	1066
Hub interface A	66	4	266	1	266
Hub interface B	66	4	266	2	533
PCI 2.2 (32 bit)	33	1	33	4	133
PCI 2.2 (64 bit)	66	1	66	8	528

1.3.3 System Configuration

1.3.3.1 2-Way Platform Configuration

Figure 1-1 shows the 2-way platform configuration.

Figure 1-1. Intel® 840 Chipset 2-Way Configuration



1.4 Platform Initiatives

1.4.1 Memory Expansion Card (MEC) and Connector (MECC)

The MEC concept is intended to provide flexibility and scalability of memory to a Intel® 840 chipset-based workstation and server platforms.

1.4.2 Direct RDRAM

The Direct RDRAM initiative will provide the memory bandwidth necessary to obtain optimal performance from the processor as well as a high performance AGP graphics controller. The MCH RDRAM interface supports 300 MHz and 400 MHz operations; the latter delivers 1.6 GB/s of theoretical memory bandwidth and twice the memory bandwidth of 100 MHz SDRAM systems. Coupled with the greater bandwidth, the RDRAM protocol, provides substantially more efficient data transfer. The RDRAM memory interface can achieve greater than 95% utilization of the 1.6 GB/s theoretical maximum bandwidth.

In addition to the RDRAM's performance features, this new memory architecture provides enhanced power management capabilities. The powerdown mode of operation will enable Intel® 840 chipset based system to cost effectively support suspend-to-RAM.

Industry leading DRAM vendors have agreed to develop RDRAMs and module vendors will be developing RDRAM Inline Memory Modules (RIMMs). RIMMs are approximately the same form factor as SDRAM DIMMs.

1.4.3 Accelerated Graphics Port

1.4.3.1 AGP

The Accelerated Graphics Port (AGP) is a high performance, component level interconnect targeted at 3D graphical display applications. AGP is based on a set of performance extensions or enhancements to the PCI bus. The AGP interface is optimized for a point-to-point topology using either 1.5V or 3.3V signaling. The baseline performance level utilizes a 66 MHz clock to provide a peak bandwidth of 266 MB/s. There are two options for higher performance levels- 2x mode and 4x mode. The 2x mode provides a peak bandwidth of 533 MB/s and 4x mode provides a peak bandwidth of 1066 MB/s.

Refer to the *Accelerated Graphics Port Interface Specification, Revision 2.0* and *AGP Design Guide (1X, 2X and 4X Modes & 1.5V and 3.3V Signaling), Revision 1.0* for complete details.

1.4.3.2 AGP Pro

AGP Pro specifies an extension to the AGP graphics bus connection for the high-performance workstation market segment. The AGP Pro specifications include electrical, mechanical and thermal requirements for the AGP Pro connector, card and chassis. It will also include examples of possible thermal solutions.

AGP Pro is expected to deliver up to four times the electrical power of the standard AGP interface through an extension to the AGP connector and provision of sufficient space for dissipating this increased power. AGP Pro also allows for multiple slot implementations where an AGP Pro Card is coupled with one or more PCI cards. Finally, the spec allows for flexible utilization of the thermal space provided for cards that dissipate significantly less than the maximum power-envelope. AGP Pro will retain mechanical and functional compatibility with AGP implying that an AGP Card can plug into an AGP Pro connector though the reverse will not be allowed.

Refer to the *AGP Pro Specification 1.0* for complete details at http://www.agp.org

1.4.4 21154BC PCI-PCI Bridge

The Intel 21154BC is a PCI-PCI bridge and is fully compliant with the PCI Local Bus Specification, Revision 2.2. The 21154BC is a 66 MHz/64-bit device and it can operate its PCI bus at either 33 MHz or 66 MHz. It provides full support for delayed transactions, which enables the buffering of memory read, I/O and configuration transactions.

Refer to http://developer.intel.com/design/bridge/techdocs/ for related documentation.

1.4.5 Intel® i960 RM I/O Processor

The Intel® i960 RM I/O processor integrates a high performance 80960 "core" processor with PCI functionality. The integrated processor addresses the needs of intelligent I/O applications like RAID. Coupled with a standard PCI SCSI controller like the LSI Logic SYM53C895 PCI-to-ULTRA2 SCSI controller drives a new price point for intelligent I/O applications like RAID.

The Intel® i960 RM I/O Processor integrates the following functionality:

- 100 MHz i960 core processor
- PCI-PCI bridge functionality
- Address translation unit
- I20 Messaging unit
- Separate DMA controllers for each PCI bus
- Support for up to 128 MBs of 66 MHz ECC protected SDRAM
- Separate 8-bit bus for FLASH interface
- Fully optimized data paths and buffering
- Application accelerator for hardware offload of XOR functions
- I^2C Bus Interface Unit for server management attach
- Secondary PCI bus arbiter

Refer to http://developer.intel.com/design/iio/designex/ for related design guide information.

1.4.6 Hub Interface

As I/O speed increases, the demand placed on the PCI bus has become significant. With the addition of AC'97, ATA/66 and existing USB, I/O requirement could impact the PCI bus performance. Intel® 840 chipset's hub interface architecture ensures that the I/O subsystem will receive adequate bandwidth. By placing the I/O bridge on the hub interface, it allows the I/O functions to obtain the necessary bandwidth for peak performance. In addition, the hub interface's lower pin count allows a smaller package for the memory controller.

1.4.7 Clocks

A new clock synthesizer/generator specification has been defined for the Intel® 840 chipset platform—CK133-W and CK133-WS.

The CK133W generally used in the workstation platforms. It shares the same pin out as CK133. Its features include:

- 14.31818 MHz Xtal Oscillator Input
- Four copies of 100/133 MHz processor clocks (cycle jitter=150 ps @ 2.5V)
- Two processor/2 outputs
- Four copies of fixed 66 MHz at 3.3V clocks
- Eight copies of PCI clocks
- Three copies of I/O APIC clocks at 16.667 MHz
- One copy of 48 MHz clock
- Two copies of 14.31818 MHz reference clocks
- Power Management Control Input pins
- Spread Spectrum Clocking support

The CK133-WS is generally used for server platforms. Its features include:

- 14.31818 MHz Xtal Oscillator Input
- Six copies of 100/133 MHz processor clocks (cycle jitter=150 ps @ 2.5V)
- Two processor/2 outputs
- Four copies of fixed 66 MHz at 3.3V clocks
- Six copies of I/O APIC clocks at ¼ CPUCLK or 16.667 MHz
- One copy of 48 MHz clock
- Spread Spectrum Clocking support

Reference the *CK98W/S Clock Synthesizer/Driver Specification* for complete details.

1.4.8 WTX Form Factor—Workstation Motherboard and System Specification

WTX is a new board-set and system form factor developed for the mid-range workstation market. This specification defines the board-set volume, interface between the board-set and chassis, I/O openings and thermal requirements. It also provides a number of design suggestions for motherboard and chassis development.

Several major IA workstation vendors worldwide worked jointly to define the WTX form factor and to incorporate flexibility to accommodate the best designs for current and future mid-range workstations. The specification and other information on WTX are available at http://www.wtx.org.

1.4.9 Manageability

The Intel® 840 platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

TCO Timer

The ICH integrates a programmable TCO Timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# which the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

Processor Present Indicator

The ICH looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction, the ICH will reboot the system at the safe-mode frequency multiplier.

ECC Error Reporting

Upon detecting an ECC error, the MCH has the ability to send one of several messages to the ICH. The MCH can tell the ICH to generate either an SMI#, NMI#, SERR#, or TCO interrupt.

Function Disable

The ICH provides the ability to disable the following functions: AC'97 Modem, AC'97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.

Intruder Detect

The ICH provides an input signal, INTRUDER#, that can be attached to a switch that is activated by the system case being opened. The ICH can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

SMBus

The ICH integrates an SMBus controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RIMMs and thermal sensors.

Alert-On-LAN

The ICH supports Alert-On-LAN. In response to a TCO event (intruder detect, thermal event, processor not booting) the ICH will send a hard coded message over the SMBus. A LAN controller can decode this SMBus message and send a message over the network to alert the network manager.

Refer to the *Wired for Management (WfM) Design Guide* for complete details,
URL: http://www.intel.com/ial/wfm/design/.

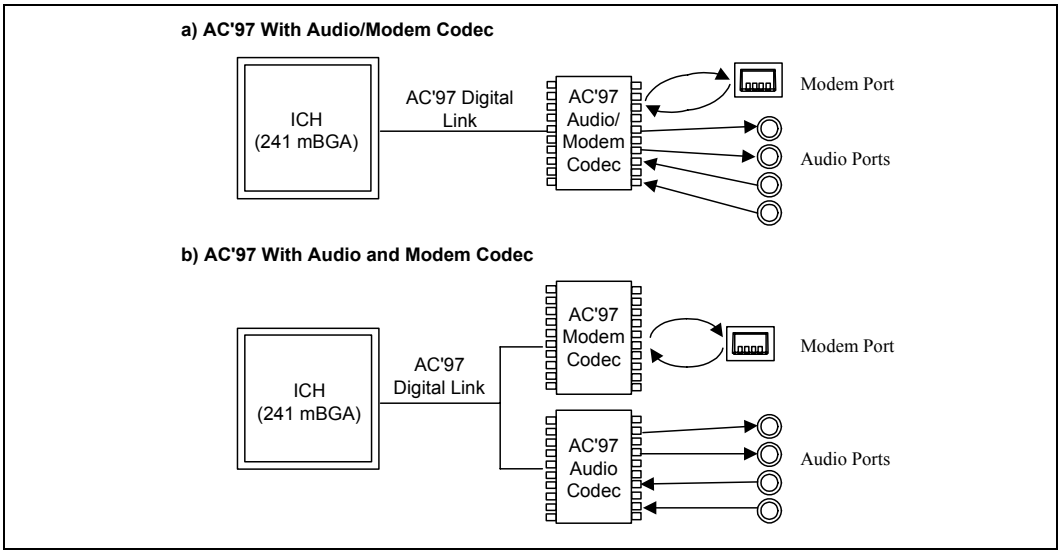
1.4.10 AC'97

The *Audio Codec '97 (AC'97) Specification* defines a digital link that can be used to attach an audio CODEC (AC), a modem codec (MC), an audio/modem codec (AMC), or both an AC and an MC. The AC'97 Specification defines the interface between the system logic and the audio/modem codec known as the AC'97 Digital Link. The ability to add cost-effective audio and modem solutions as the platform migrates away from ISA is important. In addition, the AC'97 audio and modem components are software configurable. AC'97 replaces ISA audio and modem functionality, improves overall platform integration, eases migration from ISA architecture, and reduces cost.

By using an audio codec, the AC'97 digital link allows for cost-effective, high-quality, integrated audio on the Intel® 840 chipset platform. In addition, an AC'97 soft modem can be implemented with the use of a modem codec. The integrated digital link allows two external codecs to be connected to the ICH. The system designer can provide audio with an audio codec or a modem with a modem codec. For systems requiring both audio and a modem, there are two solutions. The audio codec and the modem codec can be integrated into an AMC or separate audio and modem codecs can be connected to the ICH.

Modem implementation for different countries must be considered as telephone standards may vary. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located. The digital link in the ICH is AC'97 Rev. 2.1 compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left/right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

Figure 1-2. (a-b) AC '97 Connections



Refer to the *AC '97 Specification, Revision 2.1* at http://developer.intel.com/pc-supp/platform/ac97/, for complete details.

1.4.11 Low Pin Count (LPC) Interface

In the Intel® 840 chipset platform, the super I/O component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost super I/O designs. The LPC super I/O component requires the same feature set as traditional super I/O components. It generally includes a keyboard and mouse controller, floppy disk controller and serial and parallel ports. In addition to the standard super I/O features, an integrated game port is recommended because the AC'97 interface does not provide support for a game port. In a system with ISA audio, the game port typically existed on the audio card. The fifteen pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface.

Refer to the *Low Pin Count Interface Specification, Revision 1.0* at http://developer.intel.com/design/pcisets/lpc/INDEX.HTM for complete details. Consult your super I/O vendor for a comprehensive list of devices offered and features supported.

1.4.12 Ultra ATA

Ultra ATA "widens" the path to the hard drive by transferring twice as much data per clock cycle. The maximum disk drive burst data transfer rate increases from 16.6 Megabytes per second (MB/s) to 66 MB/s. Hard disk drive manufacturers can now bring higher performance products to market that will scale with the rest of the PC platform (faster hard drives to feed faster processors, memory and graphics).

The Ultra ATA protocol lets host computers (PCs) send and retrieve data faster, removing bottlenecks associated with data transfers -- especially during sequential operations. Users of new PCs will need less time to boot their systems and open applications, a direct result of the improved throughput provided by Ultra ATA. Current disk drive technology has been optimized to perform within the limits of the legacy protocol (16.6 MB/s). Raising the data transfer headroom results in moderate performance gains with today's drive technology. Even greater performance improvements will emerge as drive manufacturers introduce products which generate a faster data stream.

The ICH supports both the Ultra ATA/33 and Ultra ATA/66 protocols. Ultra ATA/66 is similar to the Ultra ATA/33 scheme and is intended to be device driver compatible. The Ultra ATA/66 logic operates at 66 MHz and can move 16-bits of data every 2 clocks
(for a maximum of 66 MB/s).

1.4.13 Universal Serial Bus (USB)

Universal Serial Bus (USB) simplifies the peripheral attaching and accessing process to the computer. It also eases the system configuration process from an end-user's perspective. The USB specification outlines a single connector-type for all PC peripherals, automatic detection/ configuration of the USB devices, and transfer types allowed in the bus.

In the Intel® 840 chipset-based platform, the ICH has an integrated USB Host Controller, and includes the root hub with two separate USB ports. The ICH Host Controller supports the standard Universal Host Controller Interface (UHCI) revision 1.0.

Refer to the *USB Specification, Revision 1.1* at http://www.usb.org for complete details.

1.5 Platform Compliance

1.5.1 PC 99

The PC 99 is intended to provide guidelines for hardware design that will result in the optimal user experience, particularly when the hardware is used with the Windows family of operating system. This document includes PC 99 requirements and recommendations for basic consumer and office implementations, such as desktop, mobile, and workstation systems, and Entertainment PC's. This document includes guidelines to address the following design issues:

- Design requirements for specific types of system that will run either Windows* 98 or Windows* NT operating systems.
- Design requirements related to OnNow design initiative, including requirements related to ACPI, Plug and Play device configuration, and power management in PC systems.
- Manageability requirements that focus on improving Windows 98 and Windows NT, with the end goal of reducing TCO.
- Clarification and additional design requirements for devices supported under Windows 98 and Windows NT, including new graphics and video device capabilities, DVD, scanners and digital cameras, and other devices.

For complete details, refer to the *PC 99 System Design Guide* at:
http://www.microsoft.com/windows/.

1.5.2 Hardware Design Guide for MS NT Servers

The Hardware Design Guide for Windows NT Server is co-authored by Intel Corporation and Microsoft* Corporation. The document outlines server requirements and recommendations for various price levels and performance levels. These guidelines are intended to enhance the user experience with the Windows* NT Server operating system. This document includes guidelines to address the following design issues:

- Features for basic commodity server design alternatives for small office/home office and Enterprise servers.
- Requirements for implementing the OnNow initiative, including those related to ACPI, Plug and Play device configuration, and power management in server systems.
- Implementation of devices supported under Windows NT Servers.
- Manageability features that help to reduce total cost of ownership under Windows* NT Server by providing support for maximum automation of administrative tasks with centralized control and maximum flexibility.

For complete information, refer to *Hardware Design Guide for Microsoft Windows NT Server* at:
http://www.microsoft.com/ntserver/ .

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Intel® Pentium® III Processor Layout Guidelines

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Intel® Pentium® III Processor Layout Guidelines 2

2.1 2-Way Intel® Pentium® III Processors / Intel® 840 Chipset Layout

The Intel® Pentium® III processor is the follow-on to the Pentium II processor, Pentium Pro processor, and the Pentium processor family and are the first high performance desktop processors with 133 MHz system bus clock. The Intel® 840 chipset has been designed to provide a high-performance memory, Advanced Graphics Port (AGP), and I/O subsystem to support Intel processors interfacing to the SC242 connector, which includes the Pentium III processors. The processors implement a synchronous, latched bus protocol that allows a full clock cycle for signal transmission and a full clock cycle for signal interpretation and generation. This protocol simplifies interconnect timing requirements and supports 133 MHz system bus designs using conventional interconnect technology. The processor system bus operates using Assisted Gunning Transceiver Logic, or AGTL+.

The goal of this layout guideline is to provide the system designer with the information needed for the 133 MHz DP processor and Intel 840 chipset AGTL+ bus portion of PCB layout. This layout guideline **does not** support designs using other chip sets. This section provides guidelines and methodologies that are to be used with good engineering practices. See the *Intel® Pentium® III Processor* Datasheet, and the applicable Intel 840 chipset specification for component specific electrical details. Intel strongly recommends running analog simulations using the available I/O buffer models together with layout information extracted from your specific design.

2.1.1 Definition of Terms

Term	Definition
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor system bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors for providing the high logic level and termination. The processor AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. Additionally, the processor Single Edge Connector (S.E.C.) cartridge contains 56 Ω pull-up resistors to provide termination at each bus load.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.

Term	Definition
Corner	Describes how a component performs when all parameters that could impact performance are adjusted to have the same impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. The results in performance of an electronic component that may change as a result of corners include (but are not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. Discussion of the "slow" corner would mean having a component operating at its slowest, weakest drive strength performance. Similar discussion of the "fast" corner would mean having a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.
Cross-talk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • **Backward Cross-talk.** Coupling which creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. • **Forward Cross-talk**. Coupling which creates a signal in a victim network that travels in the same direction as the aggressor's signal. • **Even Mode Cross-talk.** Coupling from multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • **Odd Mode Cross-talk.** Coupling from multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Edge Finger	The cartridge electrical contact that interfaces to the SC242 connector.
Flight Time	A term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as the time difference, between a signal at the input pin of a receiving agent crossing V_{REF} (adjusted to meet the receiver manufacturer's conditions required for AC timing specification; i.e., ringback, etc.) and the output pin of the driving agent crossing V_{REF}, if the driver was driving the TEST load used to specify the driver's AC timings. The V_{REF} Guardband takes into account sources of noise that may affect the way an AGTL+ signal becomes valid at the receiver. See the definition for Guardband.
GTL+	The bus technology used by the Pentium Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) technology. See the *Pentium® II Processor Developer's Manual* for more details of GTL+.
Network	The trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	Distance between extreme bus agents on the network and does not include the distance connecting the end bus agents to the termination resistors.
Overdrive Region	The voltage range, at a receiver, located above and below V_{REF} for signal integrity analysis. See the *Pentium® II Processor Developer's Manual* for more details.
Overshoot	Maximum voltage allowed for a signal at the processor core pad. See each processor's datasheet for overshoot specification.

Term	Definition
Pad	A feature of a semiconductor die contained within an internal logic package on the S.E.C cartridge substrate used to connect the die to the package bond wires. A pad is only observable in simulation.
Pin	A feature of a logic package contained within the S.E.C. cartridge used to connect the package to an internal substrate trace.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, etc. See the respective processor's datasheet for ringback specifications.
Settling Limit	Defines the maximum amount of ringing at the receiving pin that a signal must reach before its next transition. See the respective processor's datasheet for settling limit specifications.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
Simultaneous Switching Output (SSO) Effects	Refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "pushout"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the trunk terminating at the pad of an agent.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, terminating at agent pads.
Undershoot	Maximum voltage allowed for a signal to extend below VSS at the processor core pad. See the respective *processor's* datasheet for undershoot specifications.
Victim	A network that receives a coupled cross-talk signal from another network is called the victim network.
V_{REF} Guardband	A guardband (ΔV_{REF}) defined above and below V_{REF} to provide a more realistic model accounting for noise such as cross-talk, V_{TT} noise, and V_{REF} noise.

2.1.2 AGTL+ Design Guideline

The following step-by-step guideline was developed for systems based on two processor loads and one 82840 MCH load.

The guideline recommended in this section is based on experience developed at Intel while developing many different P6 family processor-based systems (Intel® Pentium® Pro processor, Intel® Pentium® II processor, and Intel® Pentium® III processor).

1. Begin with an initial timing analysis and topology definition
2. Perform pre-layout analog simulation for a detailed picture of a working "solution space" for the design. These pre-layout simulations help define routing rules prior to placement and routing.
3. After routing, extract the interconnect database and perform post-layout simulations to refine the timing and signal integrity analysis.
4. Validate the analog simulations when actual systems become available. The validation section describes a method for determining the flight time in the actual system.

Guideline Methodology:

- Initial Timing Analysis
- Determine General Topology, Layout, and Routing
- Pre-Layout Simulation
  - — Sensitivity sweep
  - — Monte Carlo Analysis
- Place and Route Board
  - — Estimate Component to Component Spacing for AGTL+ Signals
  - — Layout and Route Board
- Post-Layout Simulation
  - — Interconnect Extraction
  - — Inter-Symbol Interference (ISI), Cross-talk, and Monte Carlo Analysis
- Validation
  - — Measurements
  - — Determining Flight Time

2.1.3 Initial Timing Analysis

To complete the initial timing analysis, values for clock skew and clock jitter are needed, along with the component specifications. These equations contain a multi-bit adjustment factor, M_{ADJ}, to account for multi-bit switching effects such as SSO push-out or pull-in that are often hard to simulate. These equations **do not** take into consideration all signal integrity factors that affect timing. Additional timing margin should be budgeted to allow for these sources of noise.

Table 2-1 lists the AGTL+ component timings of the processors and 82840 MCH defined at the pins. These timings are for **reference only**; obtain each processor's specifications from its respective datasheet and appropriate Intel 840 chipset datasheet.

Table 2-1. Intel® Pentium® III Processor and 82840 MCH AGTL+ Parameters for Example Calculations[1]

IC Parameters	Intel® Pentium® III Processor Core at 133 MHz Bus	82840 MCH	Notes
Clock to Output maximum (T_{CO_MAX})	2.70	3.00	1,2,4
Clock to Output minimum (T_{CO_MIN})	-0.10	0.00	1,2,4
Setup time (T_{SU_MIN})	1.20	1.85	1,2,3,4
Hold time (T_{HOLD})	0.80	0.60	1,2,4

NOTES:
1. All times in nanoseconds.
2. Numbers in table are for reference only. These timing parameters are subject to change. Check the appropriate component documentation for valid timing parameter values.
3. T_{SU_MIN} = 1.85 ns assumes the 82840 MCH sees a minimum edge rate equal to 0.3 V/ns.
4. The Intel® Pentium III processor substrate nominal is set to 60 Ω ±15%

Table 2-1 gives an example of AGTL+ initial maximum flight time and Table 2-2 is an example minimum flight time calculation for a 133 MHz, 2-way Intel Peniutm III processor/Intel 840 chipset system bus. Note that assumed values for clock skew and clock jitter were used. **Clock skew and clock jitter values are dependent on the clock components and distribution method chosen for a particular design and must be budgeted into the initial timing equations as appropriate for each design.**

Table 2-1 and Table 2-2 assume:

- CLK_{SKEW} = 0.20 ns (Note: This assumes the clock driver pin-to-pin skew is reduced to 50 ps by tying two host clock outputs together (“ganging”) at clock driver output pins, and the PCB clock routing skew is 150 ps. System timing budget must assume 0.175 ns of clock driver skew if output are not tied together and clock driver that meets the CK98W/S or CK133 Clock Synthesizer/Driver Specification is being used.)
- CLK_{JITTER} = 0.25 ns

Some clock driver components may not support ganging the outputs together. Be sure to verify with your clock component vendor before ganging the outputs. See the respective processor’s datasheet, appropriate Intel 840 chipset documentation, and CK133 Clock Synthesizer/Driver Specification for details on clock skew and jitter specifications. Exact details of host clock routing topology are still under investigation and will be documented in the future release of this document. The new CK98W/S specification with tighter clock jitter, at 0.150 ns, is also available for design that need tighter control on jitter.

Table 2-2. Example T_{FLT_MAX} Calculations for 133 MHz Bus[1]

Driver	Receiver	Clk Period[2]	T_{CO_MAX}	T_{SU_MIN}	Clk_{SKEW}	Clk_{JITTER}	M_{ADJ}	Recommended T_{FLT_MAX}[3]
Processor	Processor	7.50	2.70	1.20	0.20	0.25	0.40	2.75
Processor	82840 MCH	7.50	2.70	1.85	0.20	0.25	0.40	2.10
82840 MCH	Processor	7.50	3.00	1.20	0.20	0.25	0.40	2.45

NOTES:
1. All times are in nanoseconds.
2. BCLK period = 7.50 ns at 133.33 MHz.
3. The flight times in this column include margin to account for the following phenomena that Intel has observed when multiple bits are switching simultaneously. These multi-bit effects can adversely affect flight time and signal quality and are sometimes not accounted for in simulation. Accordingly, maximum flight times depend on the baseboard design and additional adjustment factors or margins are recommended.
   - SSO push-out or pull-in.
   - Rising or falling edge rate degradation at the receiver caused by inductance in the current return path, requiring extrapolation that causes additional delay.
   - Cross-talk on the PCB and internal to the package can cause variation in the signals.

   There are additional effects that may not necessarily be covered by the multi-bit adjustment factor and should be budgeted as appropriate to the baseboard design. Examples include:

   - The effective board propagation constant (S_{EFF}), which is a function of:
     — Dielectric constant (ε_r) of the PCB material.
     — The trace type connecting the components (stripline or microstrip).
     — The length of the trace and the load of the components on the trace. Note that the board propagation constant multiplied by the trace length is a component of the flight time but not necessarily equal to the flight time.

Table 2-3. Example T_{FLT_MIN} Calculations (Frequency Independent)[1]

Driver	Receiver	T_{HOLD}	Clk_{SKEW}	T_{CO_MIN}	Recommended T_{FLT_MIN}
Processor	Processor	0.80	0.20	-0.10	1.20
Processor	840 MCH	0.60	0.20	-0.10	0.90
MCH	Processor	0.80	0.20	0.00	1.00

NOTES:
1. All times in nanoseconds.

2.1.4 General Topology

Table 2-4 provides segment descriptions and length recommendations for the investigated topology shown in Figure 2-1. Segment lengths are defined at the pins of the devices or components. For 2-way processors / Intel® 840 chipset designs, a termination card must be placed in the unused slot when only one processor is populated. To ensure signal integrity requirements, it is required that all system bus signal segments (L1, L2, L3) be referenced to the ground plane for the entire route.

Figure 2-1. Intel® Pentium® III Processor Dual Processor Configuration

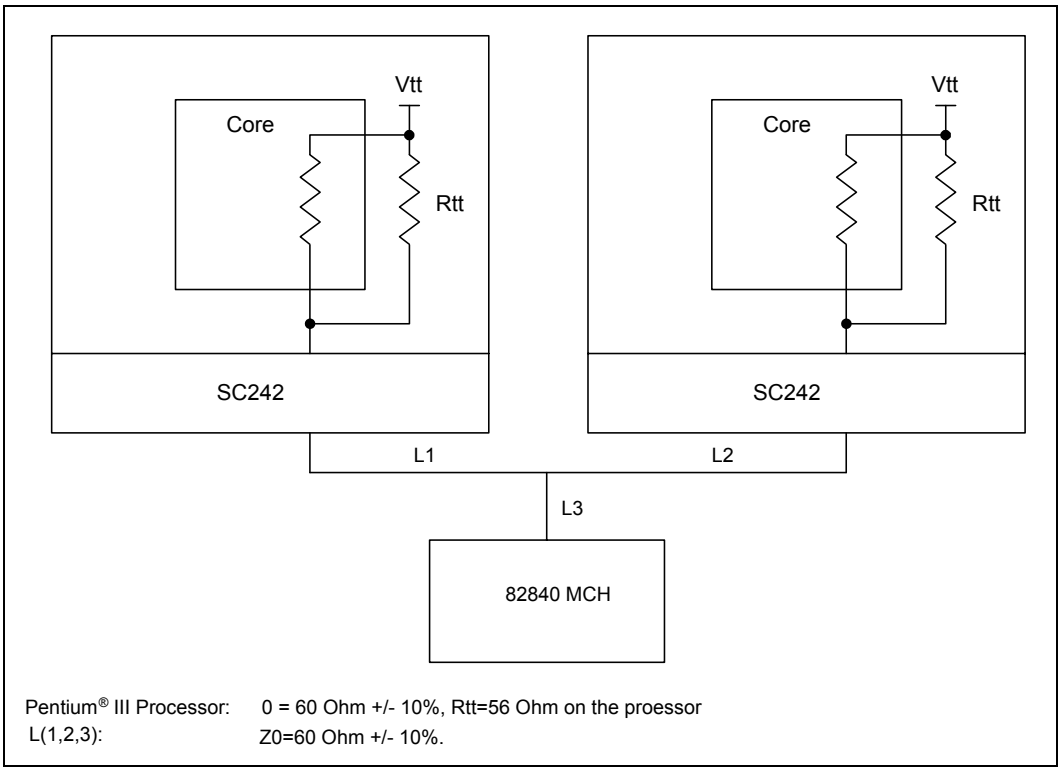


Table 2-4. Segments Descriptions and Lengths for Figure 2-1

Segment	Description	Min length (inches)	Max length (inches)
L1	SC242 connector to Center point	1.20	1.80
L2	SC242 connector to Center point	1.20	1.80
L3	Chip set breakout stub	2.00	2.50
L1+L3 or L2+L3	SC242 distance from MCH	3.20	4.30
L1 + L2	SC242 spacing		3.00

NOTES:
1. L1, L2 must be length matched to within ±0.6”.
2. All AGTL+ bus signals must be references to the ground lane for the entire route. See appendix C.

2.1.5 Power/Reference Planes, PCB Stackup, and High Frequency Decoupling

2.1.5.1 Power Distribution

Designs using the Pentium III processor require several different voltages. The following paragraphs describe some of the impact of two common methods used to distribute the required voltages. Refer to the *Flexible Motherboard Power Distribution Guidelines* for more information on power distribution.

The most conservative method of distributing these voltages is for each of them to have a dedicated plane. If any of these planes are used as an "AC ground" reference for traces to control trace impedance on the board, then the plane needs to be AC coupled to the system ground plane. This method may require more total layers in the PCB than other methods. 1 ounce/ft^2 thick copper is recommended for all power and reference planes.

A second method of power distribution is to use partial planes in the immediate area needing the power, and to place these planes on a routing layer on an as-needed basis. These planes still need to be decoupled to ground to ensure stable voltages for the components being supplied. This method has the disadvantage of reducing area that can be used to route traces. These partial planes may also change the impedance of adjacent trace layers. For instance, the impedance calculations may have been done for microstrip geometry, and adding a partial plane on the other side of the trace layer may turn the microstrip into a stripline.

2.1.5.2 Reference Planes and PCB Stackup

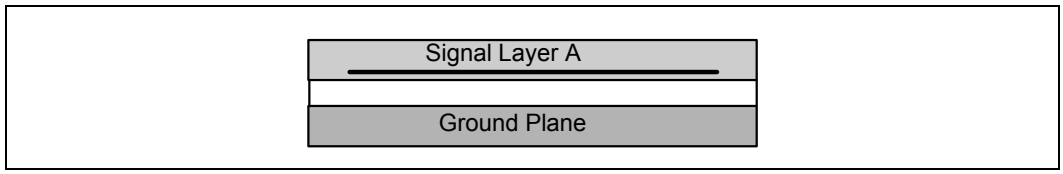
The type and number of layers for the PCB need to be chosen to balance many requirements. Many of these requirements include:

- The maximum trace resistance for AGTL+ signal paths should not exceed 2 Ω Depending on the trace width chosen and PCB vendor's process tolerance, this may require 1 ounce/ft^2 thick copper instead of 1/2 ounce/ft^2 thickness. A higher trace resistivity increases the voltage drop along the trace, which reduces the falling edge noise margin.
- Providing enough routing channels to support the minimum and maximum timing requirements of the components.
- Providing stable voltage distribution for each of the components.
- Providing uniform impedance for the processor bus and other signals as needed.
- Provide a ground plane under the principal component side of the baseboard. Preferably under both sides if active components are mounted on both sides.
- Minimizing coupling/cross-talk between the networks.
- Minimizing RF emissions.
- Maximizing PCB yield.
- Minimizing PCB cost.
- Minimizing cost to assemble PCB.

The following baseboard layout requirements should help processor signal integrity requirements and reduce the amount of Simultaneous Switching Output (SSO) effects experienced.

It is **strongly recommended** that baseboard stackup be arranged such that AGTL+ signals are referenced to a ground (VSS) plane, and that the AGTL+ signals do not traverse multiple signal layers. Deviating from either guideline can create discontinuities in the signal's return path that can lead to large SSO effects that degrade timing and noise margin. Designing an AGTL+ platform incorporating discontinuities will expose the platform to a risk that is very hard to predict in pre-layout simulation. Figure 2-2 shows the ideal case where a particular signal is routed entirely within the same signal layer, with a ground layer as the single reference plane.

Figure 2-2. One Signal Layer and One Reference Plane



When it is not possible to route the entire AGTL+ signal on a single VSS referenced layer, there are methods to reduce the effects of layer switches. The best alternative is to allow the signals to change layers while staying referenced to the same plane (see Figure 2-3). Figure 2-4 shows another method of minimizing layer switch discontinuities, but may be less effective than Figure 2-3. In this case, the signal still references the same type of reference plane (ground). In such a case, it is important to stitch (i.e., connect) the two ground planes together with vias in the vicinity of the signal transition via.

Figure 2-3. Layer Switch with One Reference Plane

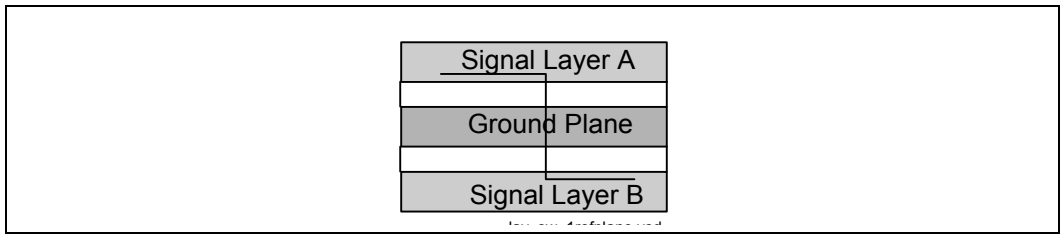
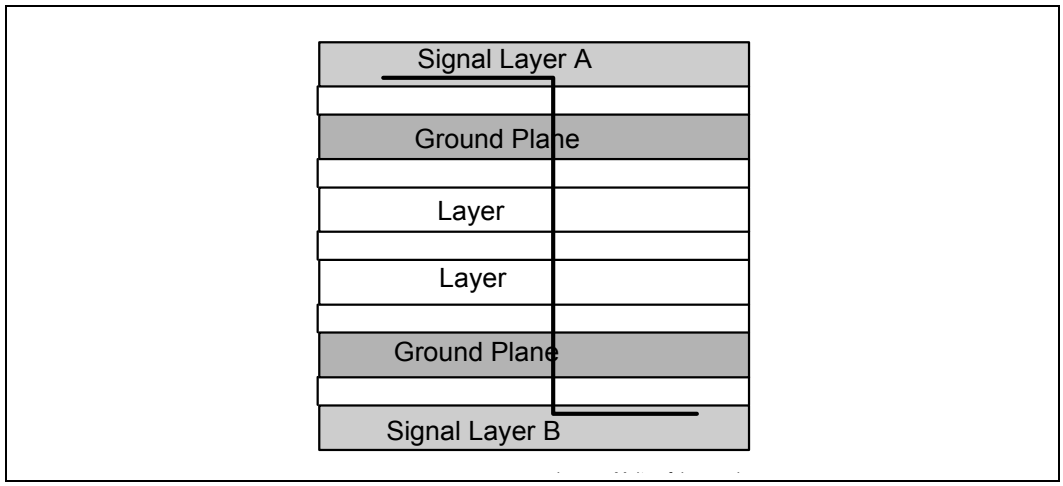


Figure 2-4. Layer Switch with Multiple Reference Planes (same type)



When routing and stackup constraints require that an AGTL+ signal reference VCC or multiple planes, special care must be given to minimize the SSO impact to timing and noise margin. The best method of reducing adverse effects is to add high-frequency decoupling where the transitions occur, as shown in Figure 2-5 and Figure 2-6. Such decoupling should, again, be in the vicinity of the signal transition via and use capacitors with minimal effective series resistance (ESR) and effective series inductance (ESL). When placing the caps it is recommended to space the VSS and VCC vias as close as possible and/or use dual vias since the via inductance may sometimes be higher than the actual capacitor inductance.

Figure 2-5. Layer Switch with Multiple Reference Planes

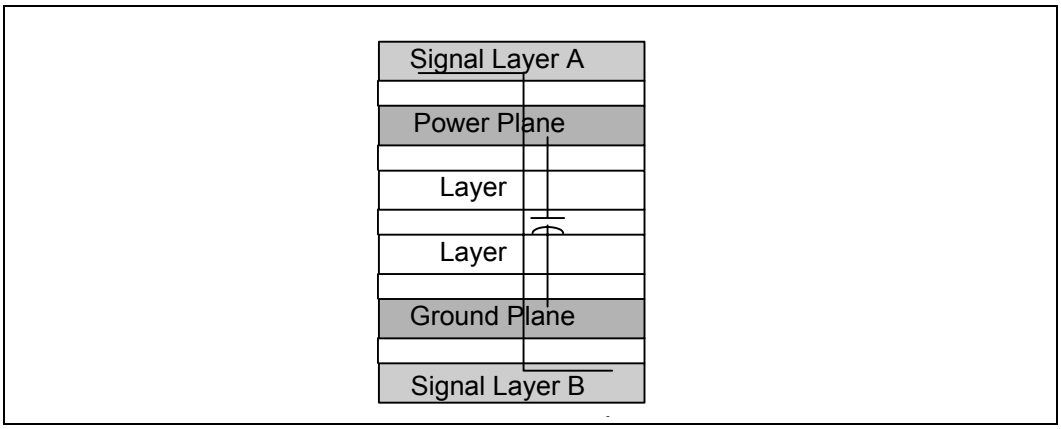
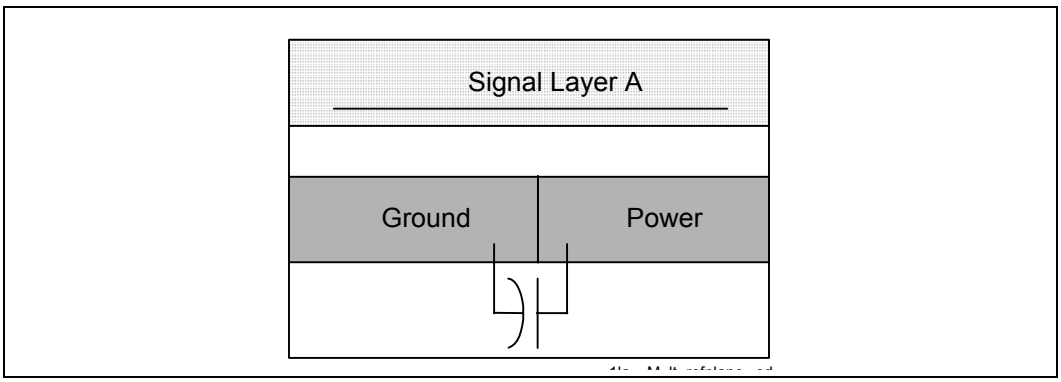


Figure 2-6. One Layer with Multiple Reference Planes



2.1.5.3 High Frequency Decoupling

This section contains several high frequency decoupling recommendations that will improve the return path for an AGTL+ signal. These design recommendations will very likely reduce the amount of SSO effects.

Just as layer switching and multiple reference planes can create discontinuities in an AGTL+ signal return path, discontinuities may also occur when a signal transitions between the baseboard and cartridge. Therefore, providing adequate high-frequency decoupling across $V_{CC_{CORE}}$ and ground at the SC242 connector interface on the baseboard will minimize the discontinuity in the signal's reference plane at this junction.

Note: These additional high-frequency decoupling capacitors are in addition to the high-frequency decoupling already on the processor.

Transmission line geometry also influences the return path of the reference plane. The following are decoupling recommendations that take this into consideration:

- A signal that transitions from a stripline to another stripline should have close proximity decoupling between all four reference planes.
- A signal that transitions from a stripline to a microstrip (or vice versa) should have close proximity decoupling between the three reference planes.
- A signal that transitions from a stripline or microstrip through vias or pins to a component (Intel 840 MCH, etc.) should have close proximity decoupling across all involved reference planes to ground for the device.

2.1.5.4 SC242 Connector

Intel studies indicate that the use of thermal reliefs on the connector pin layout pattern (especially ground pins) should be minimized. Such reliefs (cartwheels or wagon-wheels) increase the net ground inductance and reduce the integrity of the ground plane to which many signals are referenced. Increased ground inductance has been shown to aggravate SSO effects. Also, the anti-pad diameters (clearance holes in the planes) for the signal pins should be minimized since large anti-pads also reduce the integrity of the ground plane and increase inductance.

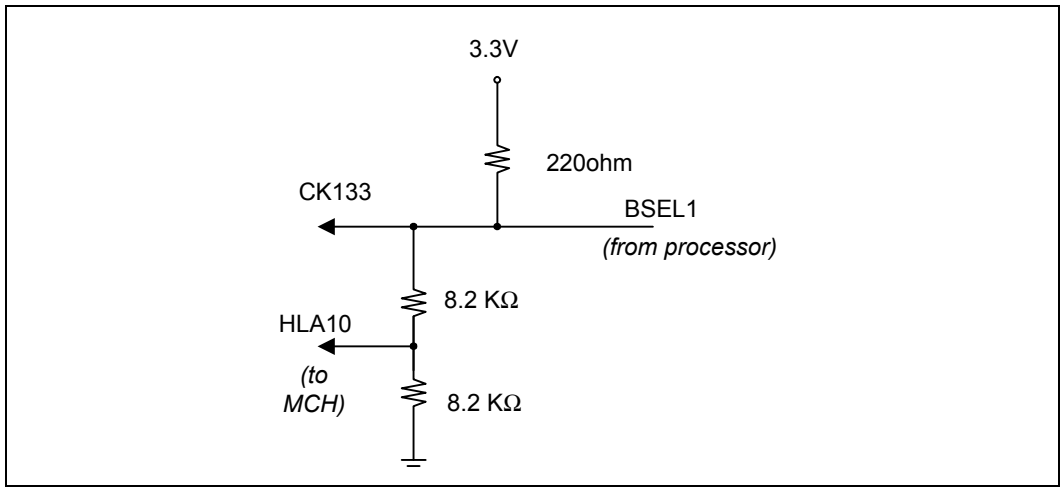
Some additional layout and EMI-reduction guidelines regarding the SC242 connector follow:

- Extend power/ground planes up to the SC242 connector pins.
- Extend the reference planes for AGTL+ and other controlled-impedance signals up to the SC242 connector pins.
- Minimize or remove thermal reliefs on power/ground pins.
- Route VTT power with the widest signal trace or mini-plane as possible. Place decoupling caps across VTT and ground in the vicinity of the connector pins.
- Use a ground plane under the principal component side of the baseboard (and secondary side if it contains active components).
- Distribute decoupling capacitors across power and ground pins evenly around the connector (less than 0.5 inch spacing) on the primary and secondary sides.
- Minimize serpentine traces on outer layers.

2.2 System Bus Strapping Option

The value of the BSEL0 and BSEL1 pins must be properly designed to ensure 133 MHz frequency. The HLA strapping should be placed as close as possible to the MCH. The strapping option shown in Figure 2-7 is applicable for the Intel® Pentium® III processor.

Figure 2-7. Intel® Pentium® III Processor and 82840 MCH System Bus Strapping



2.3 Intel® Pentium® III Processor Pull-Up Values

Table 2-5 list pull-up resistor values for Intel® Pentium® III processor signals in a DP design and should be used as a guideline. The specific value should be calculated for each design. In a 2-way system, dual pull-ups are required on each of the PICD[1:0] signals, and should be placed near the two extreme ends of the trace. Also, pull-up resistors for processor CMOS outputs should near the processor.

Table 2-5. Pull-Up Resistor Values

Signal	Resistor	Signal	Resistor
BSEL[1:0]	220 Ω[1]	STPCLK#	150Ω
FERR#	150 Ω	INIT#	150Ω
TDO	150 Ω	PREQ#	200-330Ω
A20M#	150 Ω	TCK	1.0 KΩ
IGNNE#	150 Ω	TMS	1.0 KΩ
LINT0/INTR	150 Ω	TDI	150-33 0Ω
LINT1/NMI	150 Ω	PICD[1:0]	300-330 Ω
SMI	150 Ω	PWRGOOD	48-6750 Ω
SLP	150 Ω		

NOTES:
1. *Unless noted, the signals listed should be pulled-up to 2.5V.
2. BSEL[1:0] must be pulled up to 3.3V.

2.4 S.E.C.C. 2 Grounding Retention Mechanism (GRM)

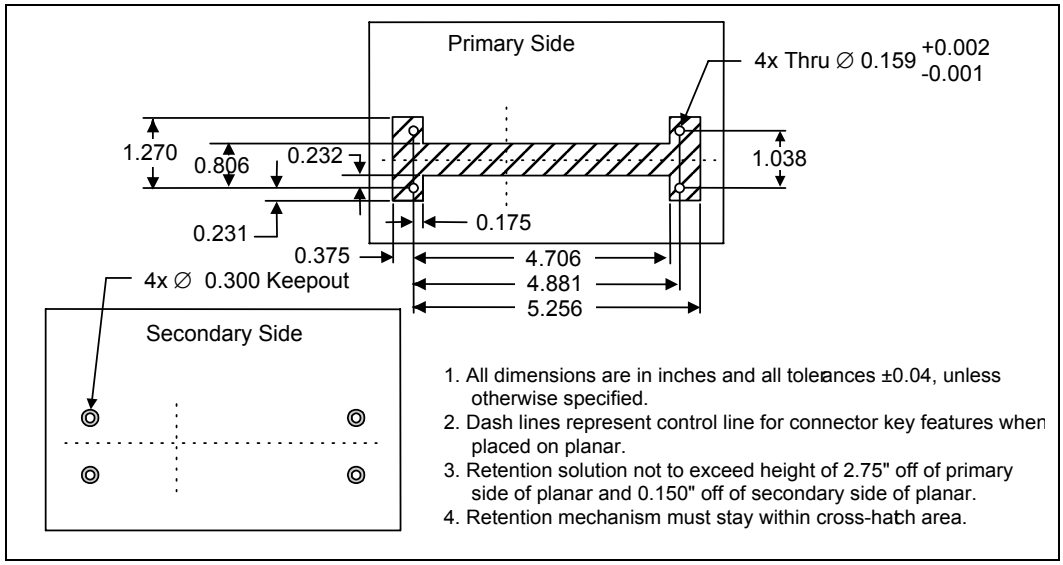
Intel is enabling a new S.E.P.P. style retention mechanism, which will provide a grounding path for the heat sink on processors in the S.E.C.C. 2 package. This solution is referred to as the S.E.C.C.2 Grounding Retention Mechanism (GRM). OEMs who choose to utilize this new solution will need to add grounding pads on the primary side of the motherboard, which will interface with the enabled GRM. If the motherboard or heat sink do not have the proper interfaces, then the GRM may not be utilized to its full ability, and/or damage could occur to the motherboard.

The most notable interface requirement to accommodate the GRM is the addition of grounding pads around two of the Retention Mechanism (RM) mounting holes within the existing RM keep-out zone on the motherboard. The other interface is a contact area on the heat sink flanges. The interface size and locations for the motherboard are discussed in detail further in this section.

The reference design GRM is asymmetric, and requires 0.159” mounting holes. To minimize the impact to trace routing, only two ground pads are required. This makes it necessary to key the GRM to prevent the ground clips from being installed on solder mask instead of the grounding pads. This keying is accomplished by making the GRM asymmetric. The requirement for the 0.159” mounting holes is for the supported plastic fastener attachment mechanism.

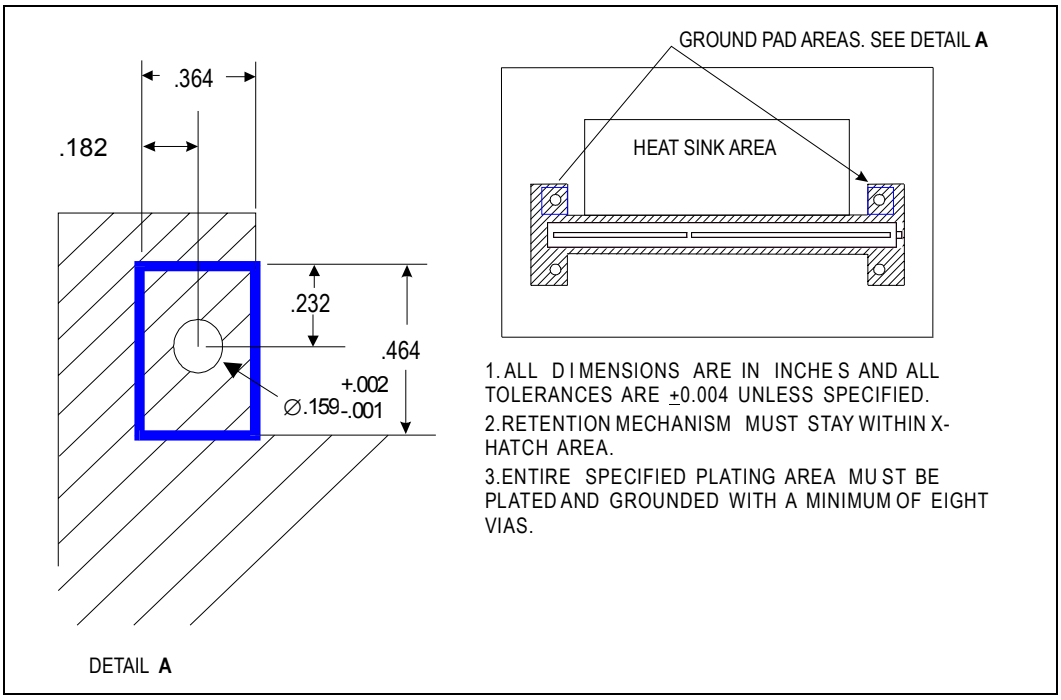
Motherboard Interfaces

Figure 2-8. Hole Location and Keep-out Zones for Support Components



NOTES:
1. Hole Location and Keep-out Zones for Support Components (from the motherboard surface to 0.100” above the motherboard surfaces)
2. The dashed lines represent the centerlines for the connector keying features

Figure 2-9. Detailed Drawing of Minimum Ground Pad Size and Location



NOTE: **NOTE: DRAWING NOT TO SCALE

It is not recommended to use the GRM without the minimum size ground pads in the correct locations. If the GRM is used without the correct pads, there is a high risk that the metal clip that grounds to the motherboard will be touching the solder mask on the top layer of the board, and possibly short out traces immediately beneath the solder mask, resulting in board failure. The required thickness of the trace is 1/2 oz. (less than .001").

Grounded Retention Mechanism (GRM) Vendor Information

The SEPP style Grounded Retention Mechanism is available from the vendors below:

ITW/Fastex (Direct Sales to major OEMs)
Caroline Wirtz
(847) 299-2222

Pencom (Distributor for ITW/Fastex)
Lisa Gibb
(650) 593-3288

3

Intel® Pentium® III Xeon™ Processor at 600+ MHz with 256K L2 Cache Size Layout Guidelines

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Intel® Pentium® III Xeon™ Processor at 600+ MHz Layout Guidelines 3

This section provides layout guidelines for 2-Way Intel® Pentium® III Xeon™ processor at 600+ MHz with 256k L2 cache size / Intel 840 chipset baseboard designs. The following guidelines are based on extensive simulation analysis and are intended to support both 2-way Intel® Pentium® III Xeon™ processor at 600+ MHz with 256k L2 cache size operation at 133 MHz system bus frequency.

3.1 Initial Timing Analysis

Intel highly recommends performing simulations as part of the board design process. This includes pre-layout simulations to provide a passing and robust solution space. Run post-layout simulations based on the extracted board layout to verify that the layout meets timing and noise requirements. Simulations are required for all designs that deviate from the recommended layout guidelines.

Table 3-1 and Table 3-2 show a recommended setup and hold margin timing budget for a 133 MHz system bus supporting 2-way Intel® Pentium® III Xeon™ processor at 600+ MHz operation with the Intel 840 chipset. The recommended topologies should support the maximum and minimum flight times suggested in these tables. The processor and chipset timing values used in these tables are for reference only and should be taken from the latest datasheet. The following timing equations were used to calculate the minimum and maximum flight times:

$$T_{FLT\_MAX} \leq Period - T_{CO\_MAX} - T_{SU\_MIN} - CLK_{SKEW} - CLK_{JITTER} - M_{ADJ}$$

$$T_{FLT\_MIN} \geq T_{HOLD} + CLK_{SKEW} - T_{CO\_MIN} + M_{ADJ}$$

These timing tables make assumptions about the clock skew and jitter and are not meant to be clock specific (e.g., clock driver skew is assumed to be 0 ns by ganging the outputs together at a clock driver device that supports this operation). Clock skew and jitter values are dependent on the components and clock distribution method chosen for a particular design and **must** be budgeted into these timing equations as appropriate for each design. Also note that the Madj factor is meant to account for multi-bit switching effects that may worsen the flight time and/or signal quality and are not always seen in simulation. This factor is highly dependent on how high-speed design practices are implemented on the baseboard (e.g., decoupling, signal return paths) and should be budgeted accordingly to each design.

The maximum and minimum flight times suggested for this topology make certain assumptions as described in the next section. Any deviations from these assumptions must be analyzed to verify that the recommended topology and flight times are still valid. These flight times also assume that the component AGTL+ signal quality requirements are met or derated properly. See the appropriate component documentation for more details.

Table 3-1. 133 MHz Setup Margin Timing

Driver	Receiver	Period	Tco_max	Tsu_min	Clock Skew	Clock Jitter	Madj	Max Tflt
Processor	Processor	7.50	2.65	1.20	0.15	0.15	0.40	2.95
Processor	Chipset	7.50	2.65	1.70	0.15	0.15	0.40	2.45
Chipset	Processor	7.50	3.00	1.20	0.15	0.15	0.40	2.60

NOTE: All units in nanoseconds.

Table 3-2. Hold Margin Timing

Driver	Receiver	Tco_min	Thold	Clock Skew	Madj	Min Tflight
Processor	Processor	-0.05	0.85	0.15	0.20	1.25
Processor	Chipset	-0.05	0.55	0.15	0.20	0.95
Chipset	Processor	0.00	0.85	0.15	0.20	1.20

NOTE: All units in nanoseconds.

3.2 General Topology

Figure 3-1 shows the recommended "3-legged star" topology for the 2-way design. This topology requires an 85 Ω pull-up resistor in the center of the star. The processor cartridge already contains a 150 Ω pull-up resistor, but the 82840 MCH also requires a 150 Ω pull-up resistor located on the baseboard with a very short stub length.

Figure 3-1. Recommended 2-Way Network Topology

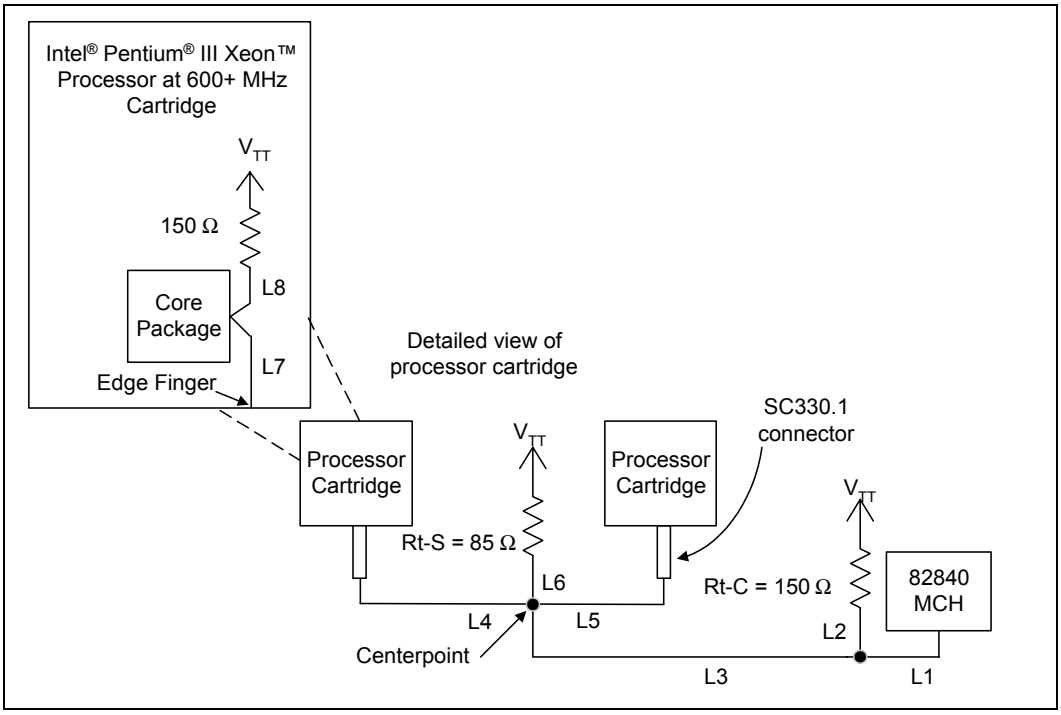


Table 3-3. Supported Segment Lengths (Star Solution Shown in Figure 3-1)

Length	Min (inches)	Max (inches)
L1	0.0	1.25
L2	- - -	0.25
L3	3.0	3.50
L4	0.95	1.45
L5	0.95	1.45
L6	- - -	0.25

NOTES:
1. See Intel® Pentium® III Xeon™ processor at 600+ MHz I/O buffer models for lengths L7 and L8.
2. Length segments L4 and L5 do not have to be equal, but Intel recommends matching these segments lengths as close as possible to provide a more electrically balanced layout. This recommendation is based on post-layout processor and baseboard simulations.

There are some key assumptions:

- V_{TT} must be maintained at 1.5V ±2%.
- V_{REF} must be maintained at $2/3V_{TT}$ ±50 mV.
- Motherboard impedance, Zo, is 60 Ω±15%.
- Signal propagation delay is between 2.0 ns/ft and 2.2 ns/ft on baseboard and cartridge.
- Dielectric constant, εr, is 4.5.
- Baseboard termination resistors are 5% tolerance
- Slow and faster corner AGTL+ I/O buffer models

3.3 Crosstalk Routing Guidelines

To ensure adequate levels of crosstalk, follow these trace width:spacing recommendations on the baseboard:

- Intragroup AGTL+: 5:10 or 6:12 (units in mils)
- Intergroup AGTL+: 5:15 or 6:18
- AGTL+ to non-AGTL+: 5:20 or 6:24

Intragroup AGTL+ refers to AGTL+ signals in the same group. Intergroup AGTL+ refers to AGTL+ signals in different groups. For a signal listing of AGTL+ groups, see Section 3.4 in the *Intel® Pentium® Pro Processor Family Developer's Manual, Volume 1*. An example of a non-AGTL+ signal is CMOS.

3.4 BREQ# Routing

Table 3-4 shows the recommended interconnect for 2-way Intel® Pentium® III Xeon™ processor at 600+ MHz systems. Note that BREQ2# and BREQ3# routes are not necessary since agents 2 and 3 would not exist (would not make requests) in this 2-way configuration. The unused BR pins (e.g., BR2# and BR3# on agent 0) do not require pull-ups on the baseboard since all AGTL+ signals are terminated on the processor. Route the BREQ0# and BREQ1# signals using the 3-legged star topology. While BREQ1# only connects to the two SC330.1 processor connectors, be sure to incorporate the chip set stub and 150 Ω termination resistor as this is the recommended topology for **all** AGTL+ signals.

Table 3-4. BR[3:0]# Signal Rotating Interconnect, 2-way

Bus Signal	Agent 0	Agent 1
BREQ0#*	BR0#	BR3#
BREQ1#	BR1#	BR0#

NOTE: *This signal is routed to the 82840 MCH.

3.5 Overshoot/Undershoot Limits

For the Intel® Pentium® III Xeon™ processor at 600+ MHz, the maximum absolute overshoot voltage limit has been increased from 2.0 V to 2.1 V. However, this value is still based on very preliminary studies and is subject to change. Refer to the *Intel® Pentium® III Xeon™ processor at 600+ MHz* datasheet for more information on overshoot specifications. There is also a time dependent, non-linear overshoot and undershoot requirement that is dependent on the amplitude and duration of the overshoot/undershoot. Any deviations from the layout guidelines recommended in this chapter will require additional overshoot/undershoot verification in order to make sure these specifications are met.

For the Intel® Pentium® III Xeon™ 1M/2M processors, the maximum absolute overshoot voltage limit has been increased from 2.0 V to 2.1V. However, this value is still based on very preliminary studies and still subject to change. Refer to the *Intel® Pentium® III Xeon™ Processor* datasheet for more information on overshoot specifications. There is also a time dependent, non-linear overshoot and undershoot requirement that is dependent on the amplitude and duration of the overshoot/undershoot. Any deviations from the layout guidelines recommended in this chapter will require additional overshoot/undershoot verification in order to make sure these specifications are met.

3.6 Wired-OR Signals

There are six “wired-OR” AGTL+ signals that can be driven by more than one agent simultaneously. When a signal is asserted (driven electrically low) by two agents on the same clock edge, the two falling wave fronts will meet at some point on the bus. This can create a large undershoot and ringback. Pay special attention during the layout and validation of these signals to prevent signal quality violations. The signals are AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#.

3.7 Signal Return Path Considerations

Adequate signal return path is very important for maintaining signal quality and timing margin for a high-speed bus such as AGTL+. Failure to address these effects may result in excessive signal flight time push-out, overshoot/undershoot, and ringback violations. The best way to maintain high-speed signal return path is to reference a single ground plane (preferred) or single power plane that is continuous for the entire length of the signal route. Avoid routing layer switches and multiple reference planes as these create discontinuities in the signal return path. When routing layer switches are unavoidable, minimize possible adverse effects on return path by making sure the signal still references either the **same plane or same type** of reference plane. If a layer switch occurs where the signal references the same type of plane located on another layer, then vias should be inserted in the immediate vicinity of the layer switch to allow the return current to traverse from one plane to another. If a layer switch occurs where the signal references a different type of plane located on another layer, then place fast-response decoupling capacitors in the immediate vicinity of the layer switch. Fast-response decoupling caps should also be placed in the immediate vicinity of any partial plane breaks if being used as a signal's reference plane. Ideally, the signal should not have any reference plane breaks cutting across the entire signal path.

3.8 AGTL+ Hold Time

Since the initial release of this document, the Intel® Pentium® III Xeon™ processor at 600+ MHz's AGTL+ hold time specification has been reduced from 0.85 ns to 0.80 ns. This provides 50 ps of additional minimum flight time margin where the Intel® Pentium® III Xeon™ processor at 600+ MHz is the receiving agent. Refer to the *Intel® Pentium® III Xeon™ processor at 600+ MHz* datasheet for all processor specifications.

3.9 Power/Reference Planes, PCB Stackup, and High Frequency Decoupling

3.9.1 Power Distribution

Designs using the Intel® Pentium® III Xeon™ processor at 600+ MHz require several different voltages. The most conservative method of distributing these voltages is for each of them to have a dedicated plane. If any of these planes is to be used as an "AC ground" reference, then the plane needs to be AC coupled to the system ground plane. Without proper AC coupling, high-speed signals (e.g., AGTL+) that reference this plane may experience signal integrity and timing effects from non-ideal signal return path. A second method of power distribution is to use partial planes in the immediate area needing power, and to place these planes on a routing layer on an as-needed basis. These planes still need to be decoupled to ground to ensure stable voltages for the components being supplied. Partial plane boundaries should not cut across the path of any high-speed signal as this creates breaks in the signal return path. When these types of breaks are absolutely unavoidable, the effects may be minimized with the use of fast response decoupling in the vicinity of the breaks. See the Signal Return Path Considerations section for more details. Use 1 ounce/ft^2 thick copper for all power and reference planes to provide acceptable AC and DC plane effects. See the *Flexible Motherboard Power Distribution and Control for Intel® Pentium® III Xeon™ Processors* for more details on power design.

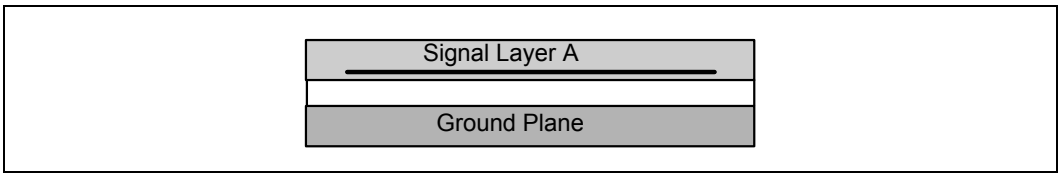
The type and number of layers for the PCB need to be chosen to balance many requirements. Many of these requirements include:

- The maximum trace resistance for AGTL+ signal paths should not exceed 2 Ω Depending on the trace width chosen and PCB vendor's process tolerance, this may require 1 ounce/ft^2 thick copper instead of 1/2 ounce/ft^2 thickness. A higher trace resistivity increases the voltage drop along the trace, which reduces the falling edge noise margin.
- Providing enough routing channels to support the minimum and maximum timing requirements of the components.
- Providing stable voltage distribution for each of the components.
- Providing uniform impedance for the processor bus and other signals as needed.
- Provide a ground plane under the principal component side of the baseboard. Preferably under both sides if active components are mounted on both sides.
- Minimizing coupling/cross-talk between the networks.
- Minimizing RF emissions.
- Maximizing PCB yield.
- Minimizing PCB cost.
- Minimizing cost to assemble PCB.

The following baseboard layout requirements should help processor signal integrity requirements and reduce the amount of Simultaneous Switching Output (SSO) effects experienced.

It is **strongly recommended** that baseboard stackup be arranged such that AGTL+ signals are referenced to a ground (VSS) plane, and that the AGTL+ signals do not traverse multiple signal layers. Deviating from either guideline can create discontinuities in the signal's return path that can lead to large SSO effects that degrade timing and noise margin. Designing an AGTL+ platform incorporating discontinuities will expose the platform to a risk that is very hard to predict in pre-layout simulation. Figure 3-2 shows the ideal case where a particular signal is routed entirely within the same signal layer, with a ground layer as the single reference plane.

Figure 3-2. One Signal Layer and One Reference Plane



When it is not possible to route the entire AGTL+ signal on a single VSS referenced layer, there are methods to reduce the effects of layer switches. The best alternative is to allow the signals to change layers while staying referenced to the same plane (see Figure 3-3). Figure 3-4 shows another method of minimizing layer switch discontinuities, but may be less effective than Figure 3-3. In this case, the signal still references the same type of reference plane (ground). In such a case, it is important to stitch (i.e., connect) the two ground planes together with vias in the vicinity of the signal transition via.

Figure 3-3. Layer Switch with One Reference Plane

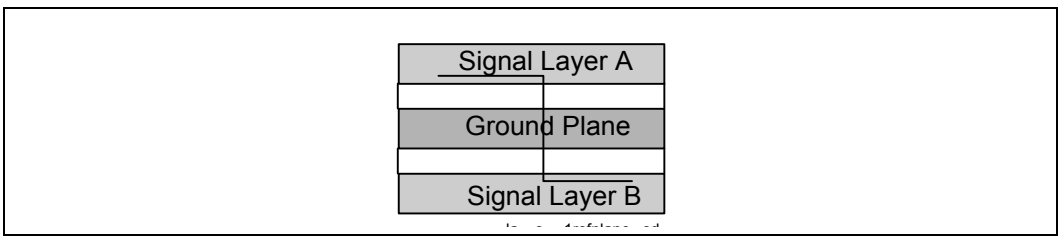
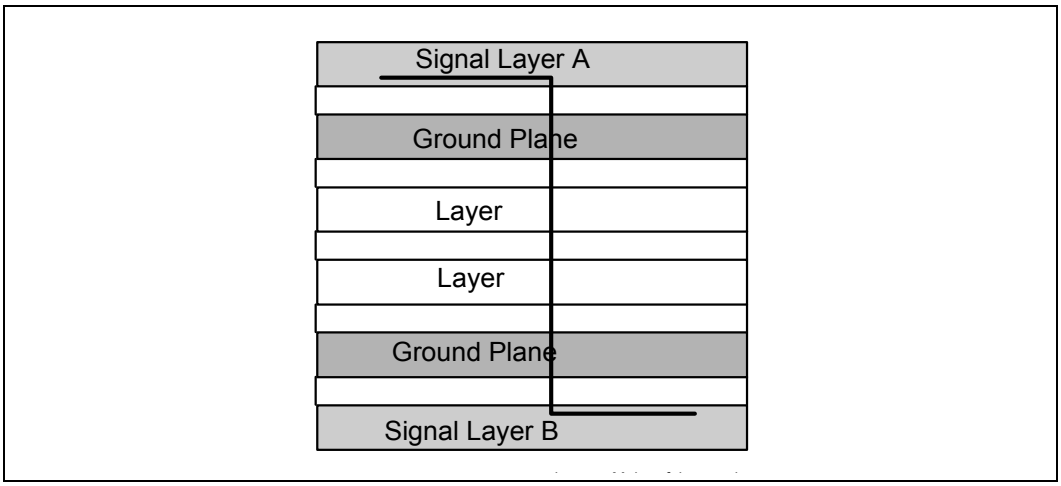


Figure 3-4. Layer Switch with Multiple Reference Planes (same type)



When routing and stackup constraints require that an AGTL+ signal reference VCC or multiple planes, special care must be given to minimize the SSO impact to timing and noise margin. The best method of reducing adverse effects is to add high-frequency decoupling wherever the transitions occur, as shown in Figure 3-5 and Figure 3-6. Such decoupling should, again, be in the vicinity of the signal transition via and use capacitors with minimal effective series resistance (ESR) and effective series inductance (ESL). When placing the caps it is recommended to space the VSS and VCC vias as close as possible and/or use dual vias since the via inductance may sometimes be higher than the actual capacitor inductance.

Figure 3-5. Layer Switch with Multiple Reference Planes

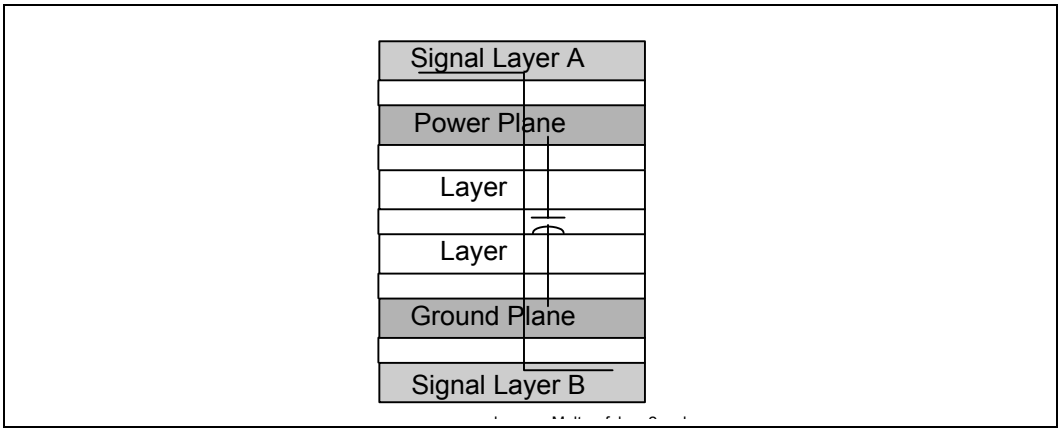
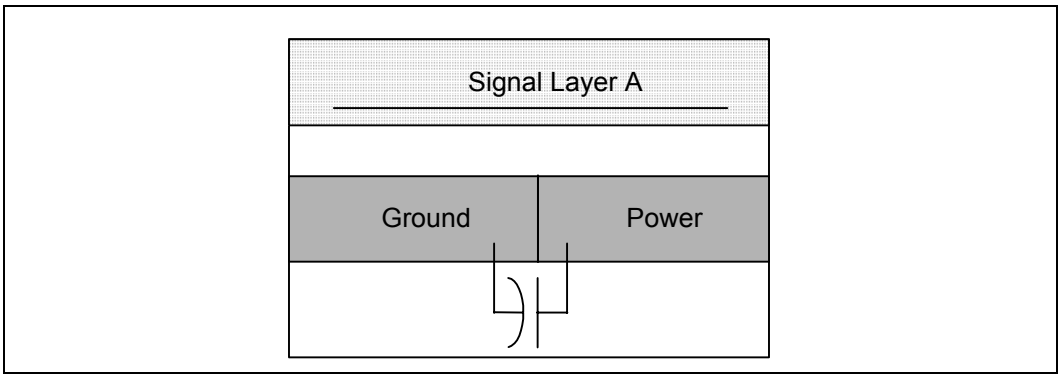


Figure 3-6. One Layer with Multiple Reference Planes



3.9.1.1 High Frequency Decoupling

This section contains several high frequency decoupling recommendations that will improve the return path for an AGTL+ signal. These design recommendations will very likely reduce the amount of SSO effects.

Just as layer switching and multiple reference planes can create discontinuities in an AGTL+ signal return path, discontinuities may also occur when a signal transitions between the baseboard and cartridge. Therefore, providing adequate high-frequency decoupling across VCC_{CORE} and ground at the SC330 connector interface on the baseboard will minimize the discontinuity in the signal's reference plane at this junction. Please note that these additional high-frequency decoupling capacitors are in addition to the high-frequency decoupling already on the processor.

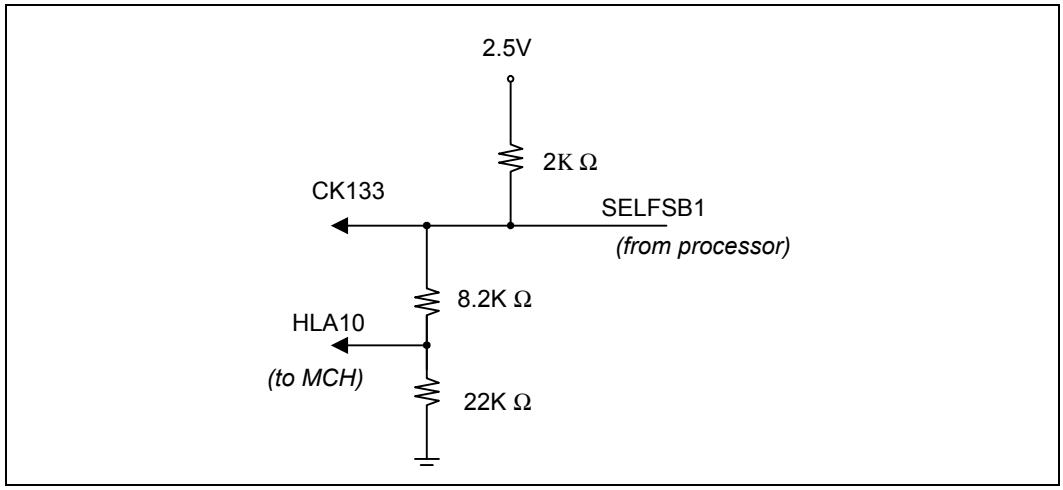
Transmission line geometry also influences the return path of the reference plane. The following are decoupling recommendations that take this into consideration:

- A signal that transitions from a stripline to another stripline should have close proximity decoupling between all four reference planes.
- A signal that transitions from a stripline to a microstrip (or vice versa) should have close proximity decoupling between the three reference planes.
- A signal that transitions from a stripline or microstrip through vias or pins to a component (Intel 840 MCH, etc.) should have close proximity decoupling across all involved reference planes to ground for the device.

3.10 System Bus Strapping

As an output from the processor cartridge, the value of SELFSB1 must be properly designed to allow the system bus frequency (133 MHz) to be automatically determined. The strapping option in Figure 3-7 is applicable for all 2-way flexible Pentium® III Xeon™ processor with Intel® 840 chipset design only. The HLA10 strap option should be placed as close as possible to the 82840 MCH.

Figure 3-7. Intel® Pentium® III Xeon™ Processor at 600+ MHz and 82840 MCH System Bus Strapping



To enable ECC on the system bus, the MCH ST0 (AGP) signal pin must be pulled-down to GND via a 1 KΩ resistor. Otherwise, no additional pull-up or pull-down is required to disable ECC on the system bus support.

3.11 Pull-Up Values

The following tables document pull-up resistor values for Intel® Pentium® III Xeon™ processor at 600+ MHz signals and should be used as a guideline. The specific value should be calculated for each design.

In a 2-way system, dual pull-ups are required on all CMOS/APIC signals. All of the signals in this table, except for PWEGOOD, PREQ#, THERMTRIP#, and TRST# need dual ended 300 Ω termination. Also, pull-up resistors for processor CMOS outputs should near the processor.

Table 3-5. Pullup Resistor Values

Signal	Resistor
A20M#	300 Ω
FERR#	300 Ω
FLUSH#	300 Ω
HINIT#(INIT#)	300 Ω
IERR#	300Ω
IGNNE#	300 Ω
LINT0/INTR LINT1/NMI	300 Ω
PWRGOOD	48–6750 Ω
SLP#	300 Ω
SMI#	300 Ω
STPCLK#	300 Ω
PICD[1:0]	300 Ω
PREQ#	150–330 Ω
TD0 (TDI)	150 Ω
TD1 (TDO)	150 Ω
THERMTRIP#	300 Ω[1]
TMS	1 KΩ
TRST#	680 Ω[2]

NOTES:
1. *Unless noted, the signals listed should be pulled-up to 2.5V.
2. If not used, THERMTRIP# can be left as a no connect signal. Otherwise, this signal requires a 300 Ω pull-up to 2.5V.
3. TRST# connects to the ITP and processors, and requires 680 Ω pull-down to GND.

4

Layout and Routing Guidelines

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Layout and Routing Guidelines 4

4.1 Board Manufacturing

This section provides motherboard layout and routing guidelines for a Intel® 840 chipset-based system. For the component functionality information, refer to the respective specification.

Although layout and routing guidelines are provided, it is still recommended that OEM's simulate all signals to ensure proper signal integrity and flight time. Complete signal integrity and timing simulation is important whether or not the design deviates from below layout and routing guidelines.

4.1.1 General Recommendation

The nominal trace impedance used is 60 Ω±10%. When calculating flight times, it is important to consider the minimum and maximum impedance trace based on the switching neighboring traces. Wider spaces between traces may be used since this can minimize trace-to-trace coupling, and reduce cross talk.

All recommendations, described in this document assume a **5** mil wide signal trace unless otherwise specified. If wider traces are used, the trace spacing must be adjusted accordingly (linearly). For example, it is recommended that AGP signals be routed with minimum of **5** mil traces on **20** mil spaces (ratio 1:4). An increase to **6** mil trace width, requires the trace spacing be adjusted to **24** mil, maintaining the 1:4 ratio.

These guidelines were generated based on an eight layer board stack-up. Other stack-ups may be used but thorough simulation is highly recommended.

4.1.2 Stack-up Requirement

The Intel® 840 platform requires a board stack-up with a 4.5 mil prepreg on the outer layer. This change in dimension (previously, typically 7 mil) is required because of the signaling environment used for Direct RDRAM, AGP 2.0 and hub link. The RDRAM Channel is designed for 28 Ω and mismatched impedance will cause signal reflections that will reduce voltage and timing margins. For example, with a 2X clock at 400 MHz operation, which equals a 1.25 ns sampling window, only 100ps is allotted for total channel timing error. Channel error results not only from PCB impedance, but also PCB and Z0 process variation. Therefore, it is critical to attain the required 28 Ω impedance.

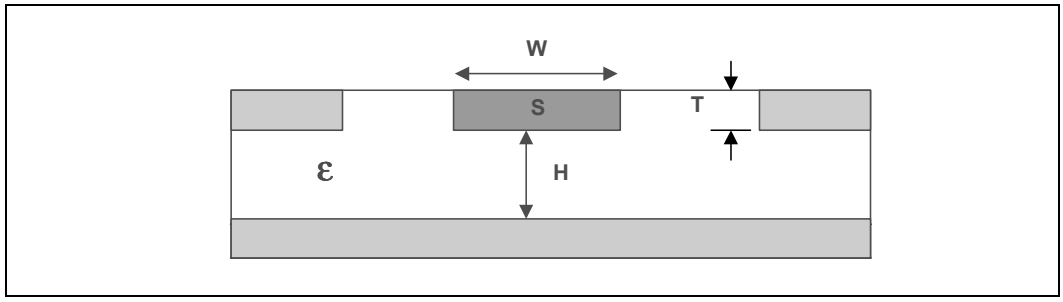
4.1.2.1 PCB Material

PCB tolerances determine Z0 variation. Those tolerances include trace width, prepreg thickness, plating thickness, and dielectric constant. The prepreg type impacts the H tolerance and e_r tolerance, which includes single ply, 2-ply, and resin content. To design to the correct Z0 variation, PCBs, typically, need to meet the following:

- Height tolerance ±10% (~ 0.4mil)
- Width tolerance ±2.5% (~ 0.4mil)
- ε_r tolerance ±5% (~0.2)

The stack-up requirement must be 28 Ω±10%.

Figure 4-1. 28 Ω Trace Geometry



Steps to design and meet the tight tolerance requirements may include:

- Specify the material to be used
- Calculate board geometry for the desired impedance - or use the example stackup provided
- Build test boards and coupons
- Measure the board impedance using an TDR and follow the procedures in the *Intel's Impedance Test Methodology* document. This document is available on the Intel developer's web site.
- Measure board geometry with cross-section
- Adjust design parameters and/or material as required
- Build a new board, re-measure the key parameters and be prepared to generate one or two board iterations

4.1.2.2 Inner Layer Routing

Inner layer routing has many possible stack-up combinations. The initial TDR should fall within acceptable limits, 28 Ω±10%, with these parameters. It is important to consider the ground floods and stitching as well. Figure 4-2 shows examples of the Stripline and Microstrip cross sections.

Figure 4-2. Micro-Strip Cross Section for 28 Ω Trace

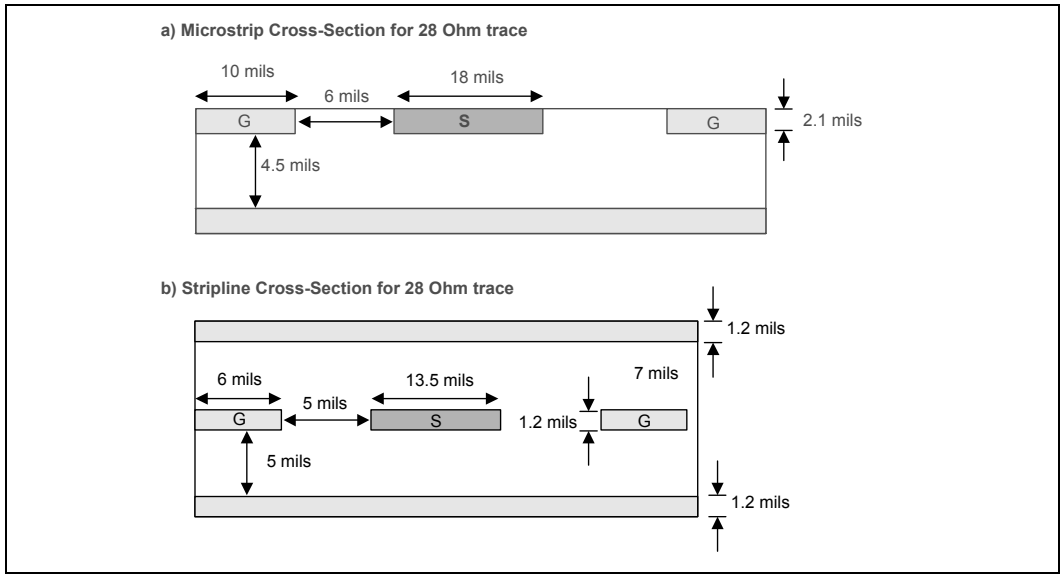


Table 4-1. 3D Field Solver vs. ZCALC

	1	2	3	4	5	6
H	4.5	4.5	4.2	4.8	4.5	4.5
W	18	18	18	18	17	179
W1	18.1	18.1	18.1	18.1	17.1	19.1
T	1.4	2.8	1.4	1.4	1.4	1.4
εr	4.5	4.5	4.5	4.5	4.5	4.5
Z0 (3D)	29.0	28.4	27.6	30.4	30.2	27.9
Z0 (zcalc)	29.1	28.7	27.7	30.4	3.02	28.0

4.1.2.3 Board Stack-Up

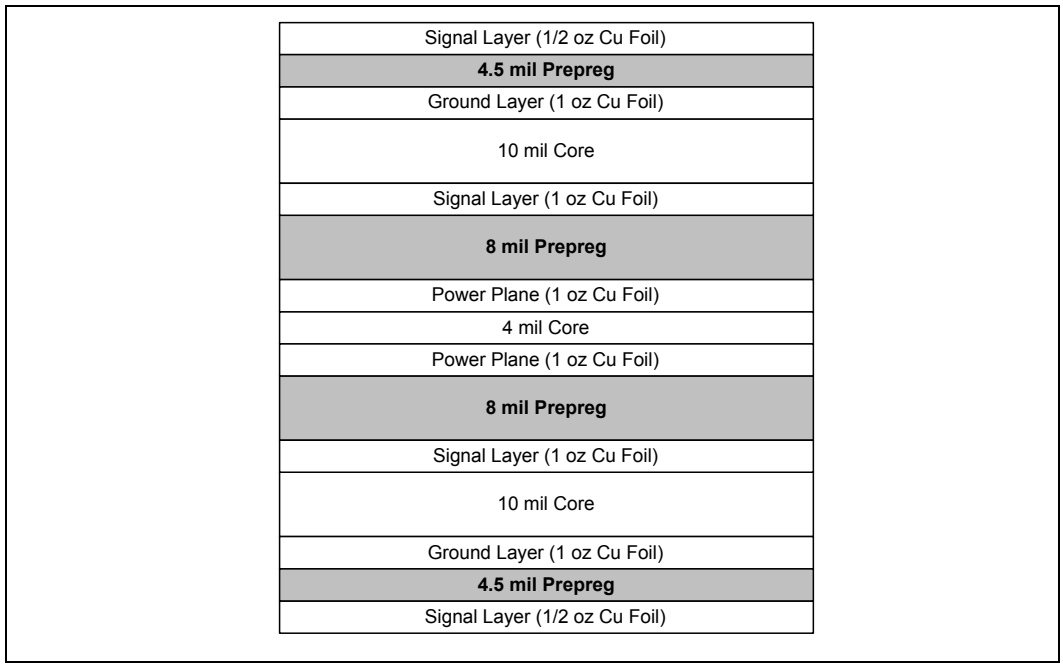
The board stack-up shown is an example of an 8-layer workstation or server platform. The additional prepreg thickness is recommended to accommodate the high-speed signal environment. For example: Direct RDRAM, MEC interface, AGP, and hub interfaces.

There are two popular prepreg types:

- 7628 Cloth, 1 ply.007” when cured with 40% resin
- 2116 Cloth, 1 ply.0045” when cured with 53% resin

Although 7628 Cloth is more common, it is recommended that 2116 Cloth be used because it better accommodates the high speed signals impedance and layout requirements. Other board stack-ups can be achieved but it is important to maintain the traces on inner and outer layers as close to 60 Ω as possible. It is also important to maintain the 4.5 mil prepreg that is needed to keep the 18 mil RDRAM RSL traces at 28 Ω impedance.

Figure 4-3. 8-Layer Board Stack-up Example



4.1.3 Component Quadrant Layout

The preliminary quadrant layouts shown are an approximate. Only the exact ball assignment should be used to conduct routing analysis. Reference the specific component's datasheet.

Figure 4-4. MCH 544mBGA Quadrant Layout (Topview)

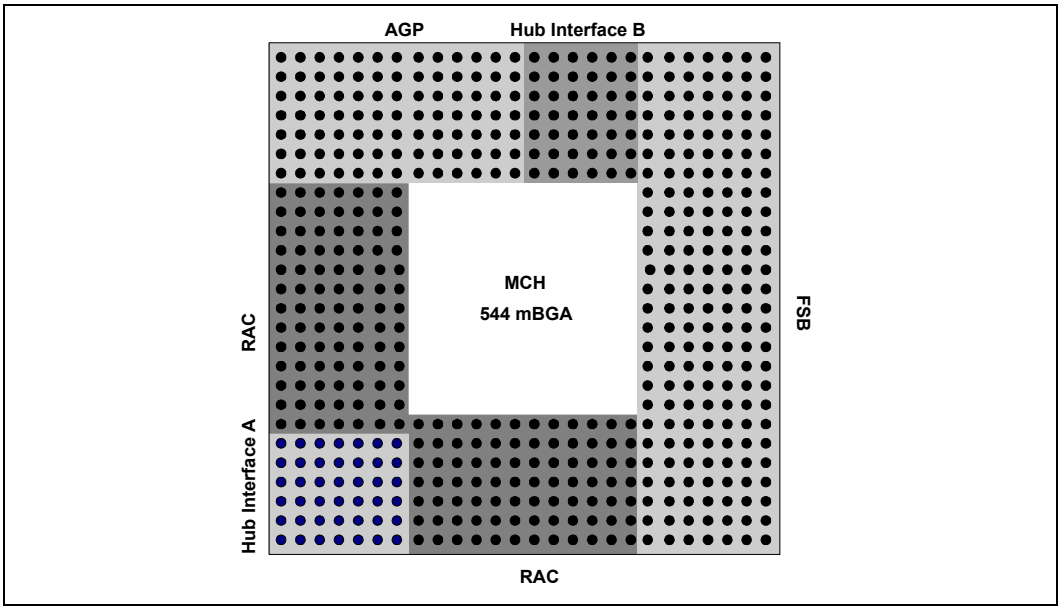


Figure 4-5. ICH 241mBGA Quadrant Layout (Topview)

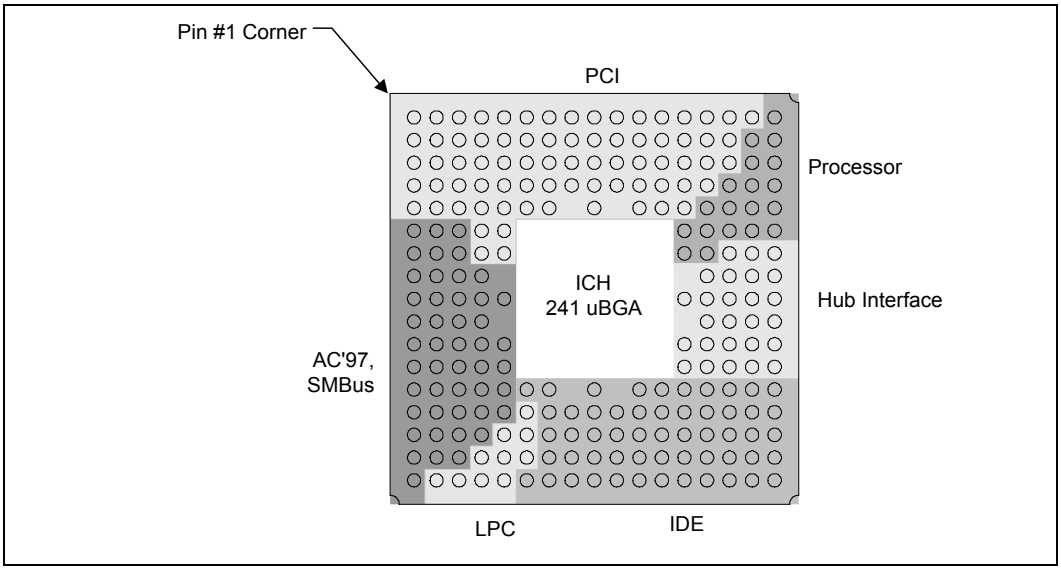


Figure 4-6. P64H 241mBGA Quadrant Layout (Topview)

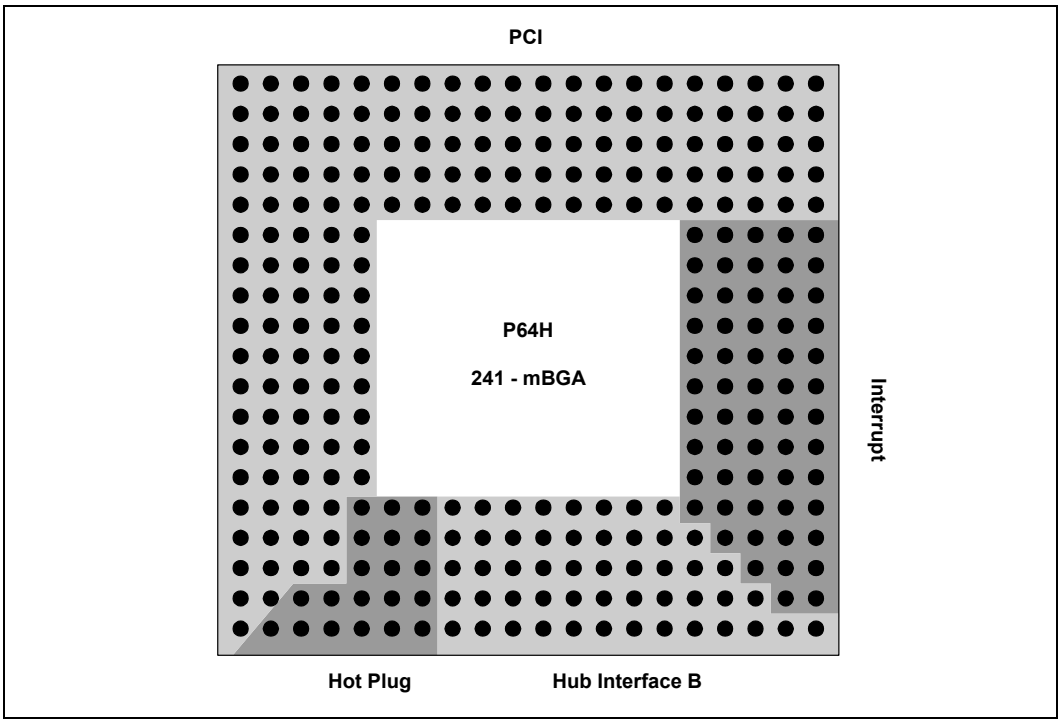
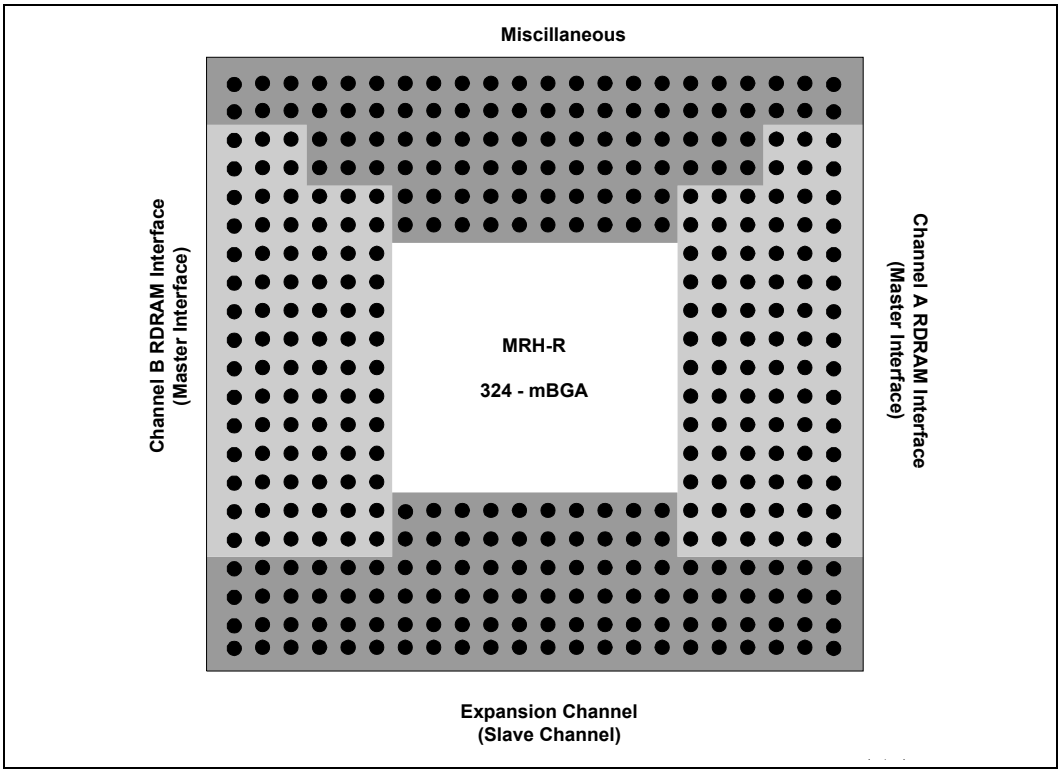


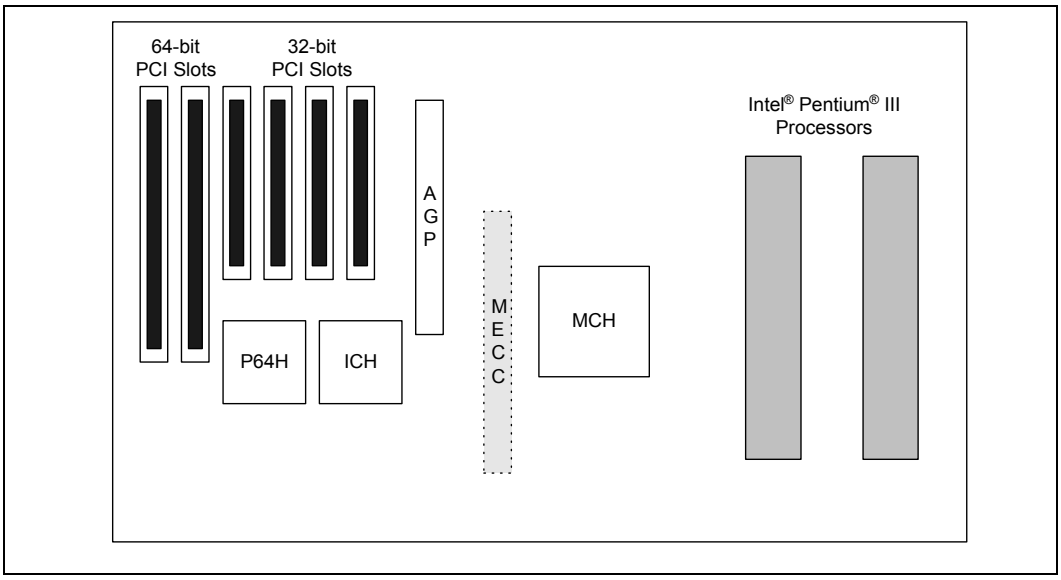
Figure 4-7. MRH-R 324mBGA Quadrant Layout (Topview)



4.1.4 Intel® 840 Chipset Component Placement

Figure 4-8 is for references only. These figures do not represent actual size or exact location.

Figure 4-8. Dual Processor WTX Component Placement Example



4.2 Memory Interface

The perfect matching of transmission line impedance and uniform trace length are essential for the Direct RDRAM interface to work properly. Maintaining 28 Ω (±10%) loaded impedance for every RSL (Rambus* Signaling Level) signal requires some changes to the standard trace width and board prepreg thickness

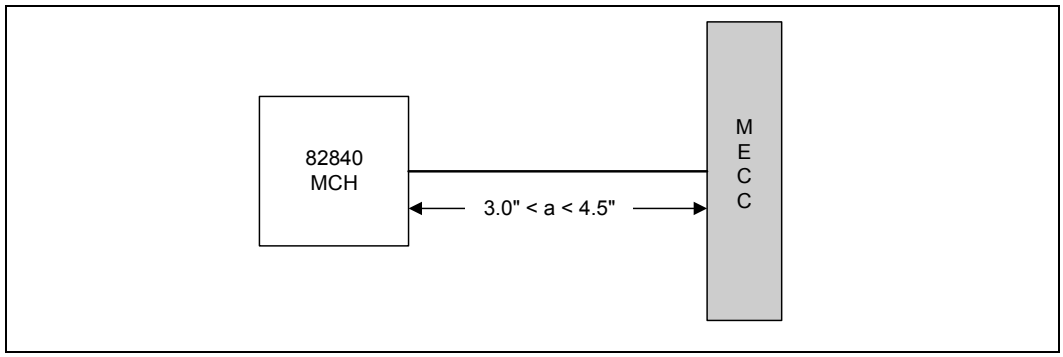
Typically, to achieve 28 Ω nominal impedance with 7 mil prepreg, it will require 28 mil wide traces. 28 mils wide traces are too wide to break out of the two rows of RSL signals on the 82840 MCH. To reduce the trace width, a 4.5 mil prepreg is required. This thinner prepreg allows 18 mil wide traces to meet the 28 Ω (±10%) nominal impedance requirement. The signals on RDRAM Channels are broken into three groups: RSL, CMOS and Clock signals:

- RSL Signals
  - DQA[8:0]
  - DQB[8:0]
  - RQ[7:0]
- CMOS Signals
  - CMD (high speed CMOS signals)
  - SCK (high speed CMOS signals)
  - SIO
- Clock Signals
  - CTM
  - CTM#
  - CFM
  - CFM#

4.2.1 Memory Design with MEC/MECC (Outer Layer Routing)

The Memory Expansion Card (MEC) concept is intended to provide flexibility and scalability of memory to a Intel® 840 chipset-based workstation and server platform. The Intel® 840 chipset will support both RIMMs down and MECC configurations. For routing guidelines for the Memory Expansion Card (MEC), please reference the Intel® 840 Chipset: Workstation/Server MEC Design Guide document. The MCH-to-MECC routing guidelines are based on the usage of a Memory Expansion Card Connector (MECC) that meets the RIMM connector specification electrical characteristics.

Figure 4-9. RDRAM Channel Signal Groups



All RDRAM signals between 82840 MCH and MECC should be maintained between 3.0” (min) and 4.5” (max). Although channels A and B are not required to match one another, the difference between channels should be minimized and must meet MCH levelization requirements.

Refere to the Intel® 840 Chipset: Workstation/Server MEC Design Guide for complete RSL and other signal routing guidelines to the MRH-R expansion device.

To maintain 28 Ω trace impedance, the RSL signals must be 18mil wide. To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace between adjacent RSL signals. The 10 mil ground isolation traces must be connected to ground with a via every 1”. A 6 mil gap is required between the RSL signals and ground isolation traces. To ensure uniform traces, the trace width variation must be uniform on all RSL signals at every neck down. The RSL signals within each channel must be length matched to ±10 mils in the line section between the MCH and first MRH-R device on the MEC using trace length matching methods.

Also, all RSL signals must have the same number of vias. It may be necessary to place additional vias (dummy VIAS) on RSL signals, even if VIAS are not needed, to meet the via loading (equal number of VIAS) requirement. Reference the Intel® 840 Chipset: Workstation/Server MEC Design Guide for complete RSL and other signal routing guidelines to the MRH-R expansion device.

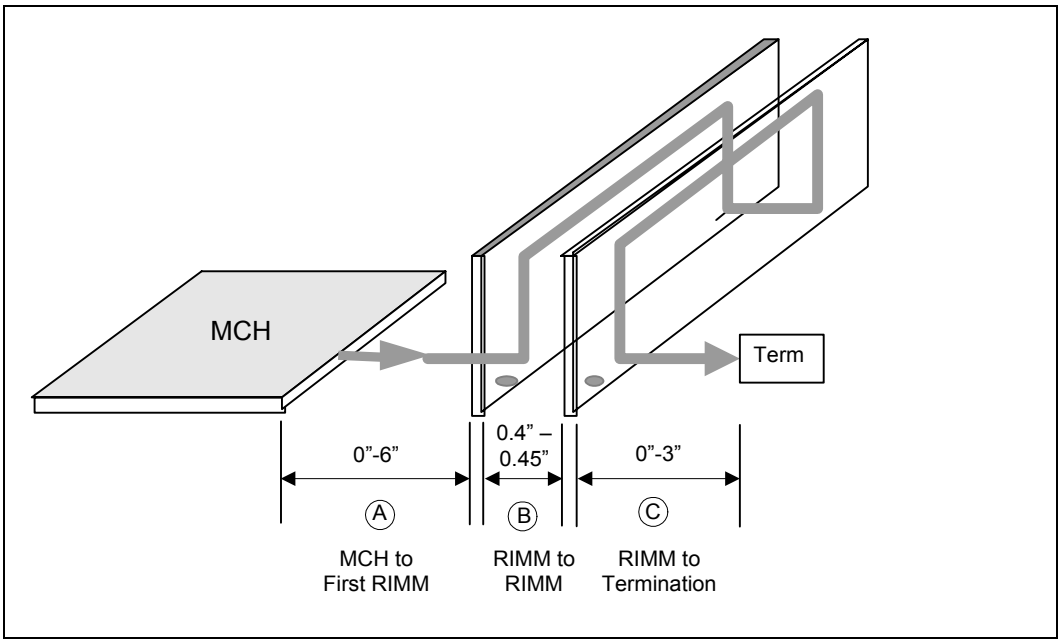
4.2.1.1 RIMMs on the Motherboard (Outer Layer Routing)

The RDRAM layout guidelines below are applicable for outer-layer routing for each channel. Additional layout guidelines will be available in future release of this design guide.

RSL Signals

The RSL signals enter the first RIMM on the left side, propagates through the RIMM, and then exit on the right. The signal continues through the rest of the existing RIMMs until it is terminated at V_{term}. The unpopulated slot must have continuity modules in place to ensure that the signals propagate to the termination. Refer to http://www.rambus.com for more information regarding the Direct RDRAM technology.

Figure 4-10. RSL Routing Dimensions for 2 RIMMs



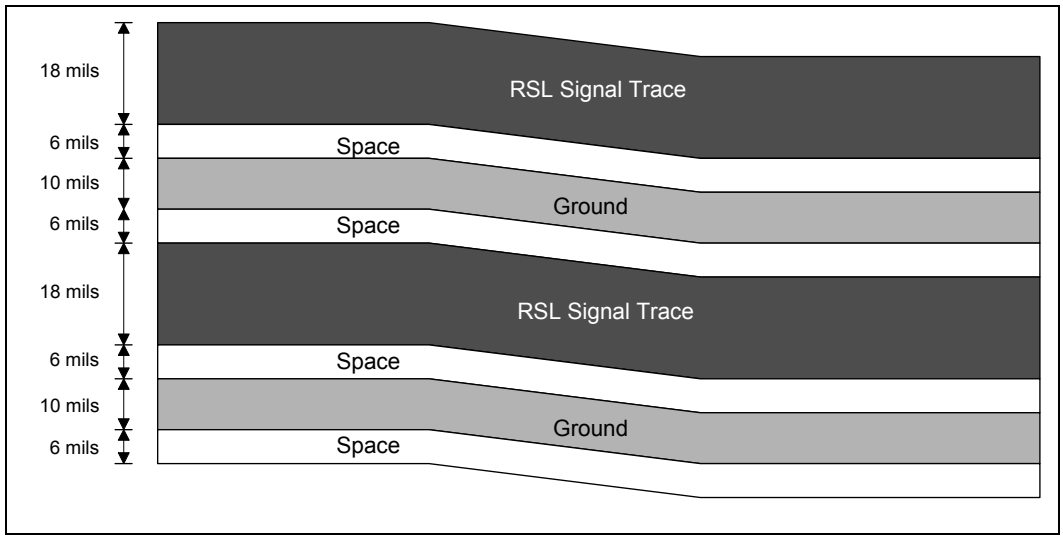
With the 82840 MCH, it is possible to achieve longer trace length A (MCH to the 1st RIMM connector) in a two RIMMs per RDRAM channel implementation. Although channels A and B minimized are not required to match one another the difference between channels should be minimized and must meet MCH levelization requirements.

Table 4-2. Trace Lengths: RSL Routing for 2 RIMMs (see Figure 4-10)

Reference Section	Trace Description	Trace Length
A	MCH to first RIMM connector	0” to 6”
B	RIMM connector to RIMM connector	0.4” to 0.45”
C	RIMM to Termination	0” to 3”

To maintain a nominal 28 Ω trace impedance, the RSL signals must be 18 mils wide. To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace between adjacent RSL signals through all section “A,” “B” and “C”. The 10 mil ground isolation traces must be connected to ground with a via every 1”. A 6 mil gap is required between the RSL signals and the ground isolation trace. To ensure uniform trace lines, trace width variation must be uniform on all RSL signals at every neck-down for each line section. The RSL signals within each channel must be length matched to ±10 mils in line section “A” and ±2 mils in both line sections labeled “B” using the trace length matching methods described in the next section. Also, all RSL signals must have the same number of vias. It may be necessary to place additional vias (dummy vias) on certain RSL signals, even if vias are not needed, to meet the via loading (equal number of vias) requirement. There is no trace length-matching requirement for traces in section ‘C’.

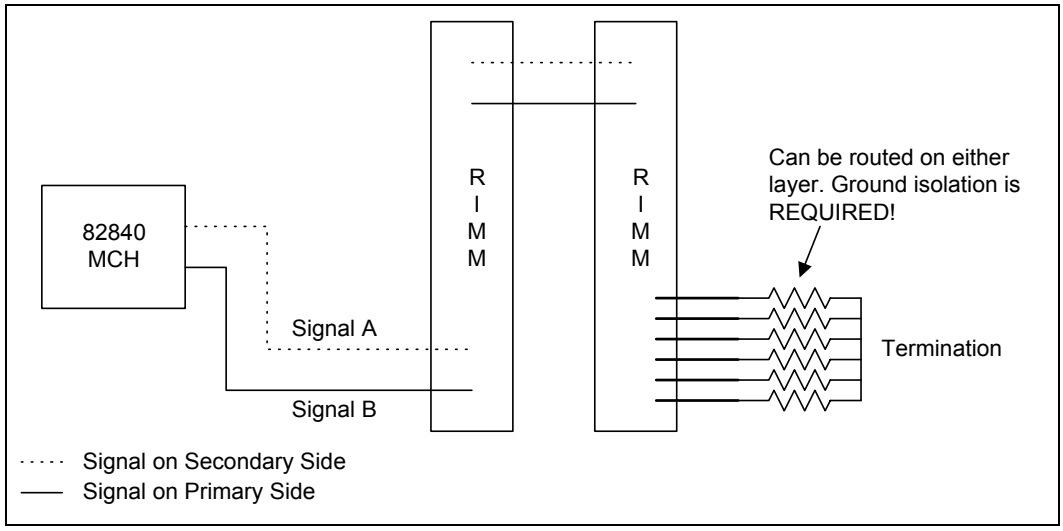
Figure 4-11. RSL Routing Diagram



RSL Signal Layer Alteration

All RSL signals must alternate layers as they are routed through the channel. For example, a signal routed on the primary side from the MCH to the first RIMM socket, must be routed on the secondary side from the first RIMM to the second RIMM (signal B). If a signal is routed on the secondary layer from the MCH to the first RIMM socket, it must then be routed on the primary side from the first RIMM to the second (signal A). Signals can be routed on either layer from the last RIMM to the termination resistors.

Figure 4-12. RSL Signal Layer Alteration



NOTES:

MCH to 1st RIMM	**1st RIMM to 2nd RIMM**
Primary Side	Secondary Side
Secondary Side	Primary Side

RSL Signal Termination

All RSL signals must be terminated to 1.8V (Vterm) using 27 Ω 2% or 28 Ω 1% resistors at the end of the channel opposite the MCH. Resistor packs are acceptable. Vterm must be decoupled using very high-speed bypass capacitors (one 0.1 uF ceramic chip capacitor per two RSL lines) near the terminating resistors. Additionally, bulk capacitance is required. Assuming a linear regulator with approximate 20 µs response time, two 100 µF tantalum capacitors are recommended. The trace length between the last RIMM and the termination resistors should be less than 3". Length matching in this section of the channel is not required. The Vterm power- island should be at LEAST 50 mils wide. This voltage is not required during Suspend-to-RAM (STR).

Figure 4-13. Direct RDRAM Termination

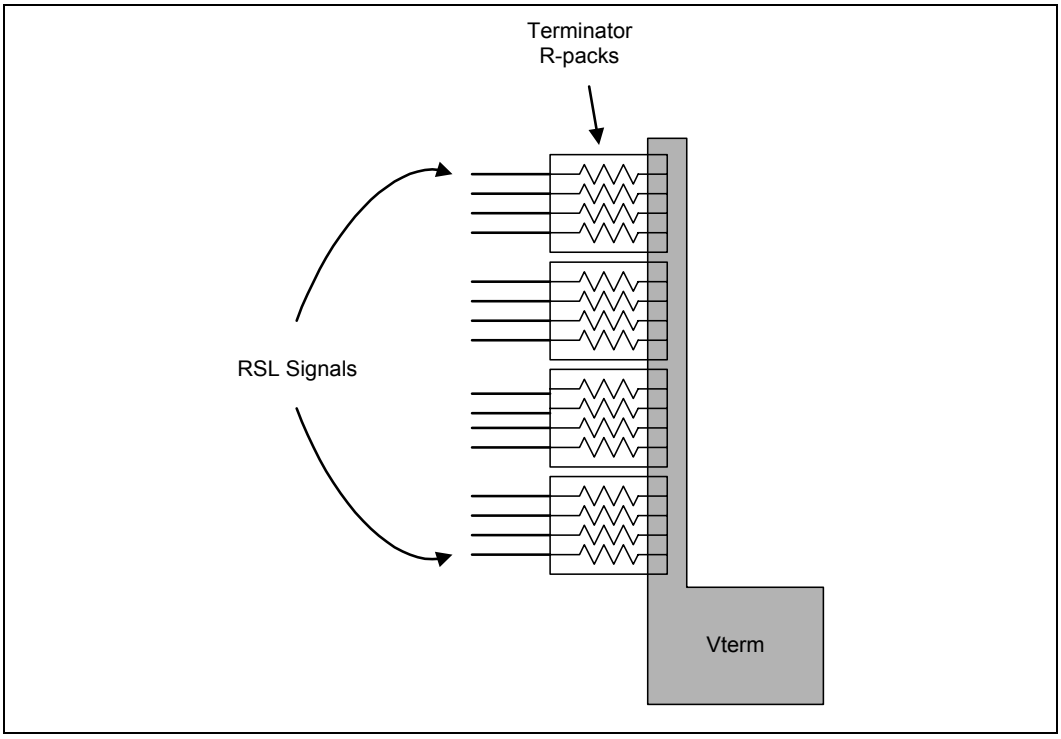
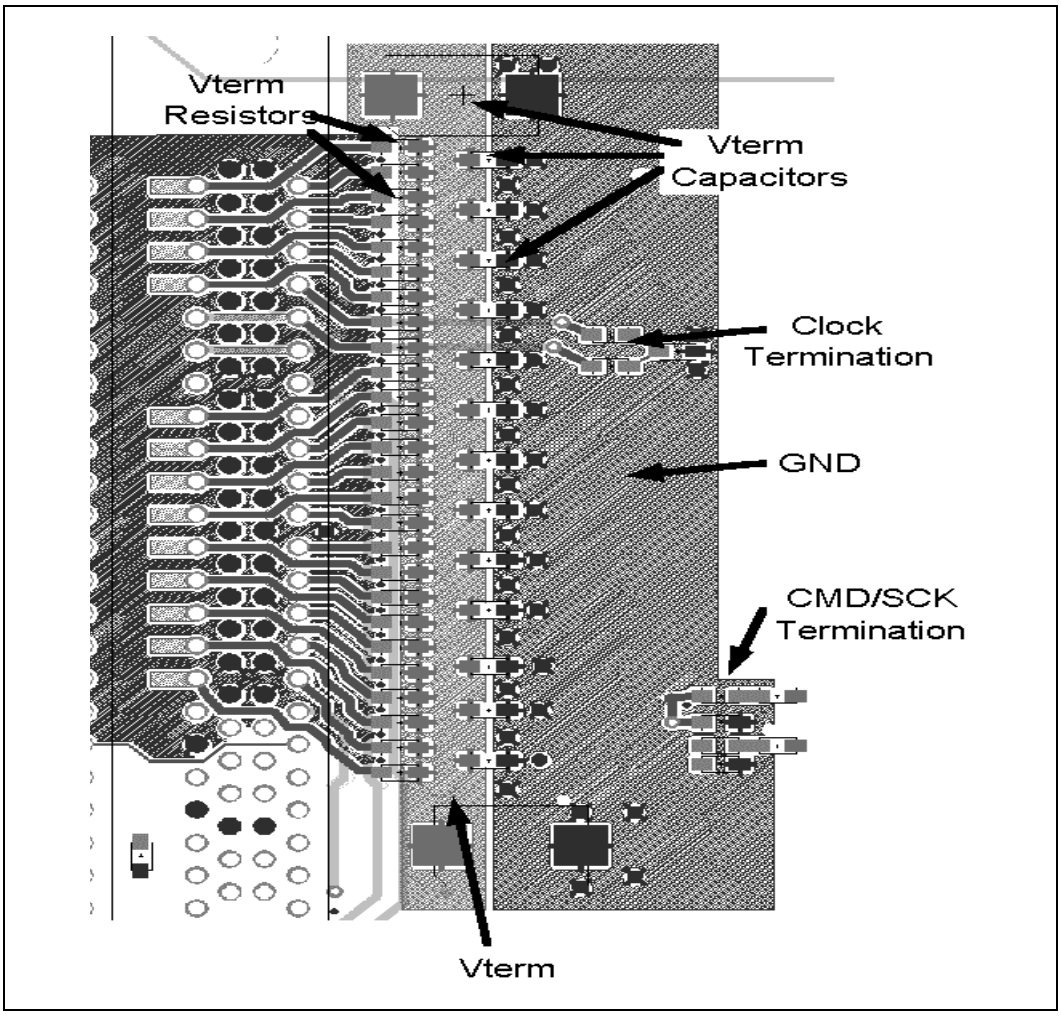


Figure 4-14. Rambus Termination Example



It is necessary to compensate for the electrical characteristic difference between a “dummy” and “real” VIAs. Refer to the VIA Compensation section for more details.

RDRAM Connector Compensation

The RIMM connector inductance causes an impedance discontinuity on the Rambus* channel. This may reduce voltage and timing margin.

To compensate for the inductance of the connector, approximately 0.65 pF–0.85 pF compensating capacitive tab (C-TAB) is required on each RSL connector pin. This compensating capacitance must be added to the following connector pins at each connector:

LCTM	LCTM#	RCTM	RCTM#
LCFM	LCFM#	RCFM	RCFM#
LROW[2:0]	RROW[2:0]	LCOL[4:0]	RCOL[4:0]
RDQA[8:0]	LDQA[8:0]	RDQB[8:0]	LDQB[8:0]

This can be achieved on the motherboard by adding a copper tab to the specified RSL pins at each connector. The target value is approximately 0.65 pF–0.85 pF. The copper tab area for the recommended stackup was determined through simulation. The placement of the copper tabs can be on any signal layer, independent of the layer on which the RSL signal is routed.

Equation 4-1 is an approximation that can be used for calculating copper tab area on an outer layer.

Equation 4-1. Copper Tab Area Calculation (Outer Layer)

$$\text{Length*Width} = \text{Area} = C_{plate} * \text{Thickness of prepreg} / [(\varepsilon_0)(\varepsilon_r)] * (1.1)$$

- C_{plate} = Capacitance of the plates
- $\varepsilon_0 = 2.25 \times 10^{-16}$ Farads/mil
- ε_r = Relative dielectric constant of prepreg material
- Thickness of prepreg = Stackup dependent
- Length, Width = Dimensions in mils of copper plate to be added
- Factor of 1.1 accounts for fringe capacitance.

Based on the stackup requirement outlined in the *Intel® 840 Chipset Platform Design Guide*, the copper tab area should be 2800 to 3600 sq mils. Different stackups require different copper tab area. Table 4-3 shows the suggested copper tab area:

Table 4-3. Copper Tab Area Calculation

Dielectric Thickness (D)	Separation Between Signal Traces & Copper Tab	Minimum Ground Flood	Air Gap between Signal & GND Flood	Compensating Capacitance in C_{plate} (pF)	CTAB Area (A) in sq mils	CTAB Shape
4.5	6	10	6	0.65	2800	140 L x 20 W 70 L x 40W

Based on Equation 4-1, the area is 2800 sq mils, where ε_r is 4.2 and D is 4.5. These values are based on 2116 prepreg material.

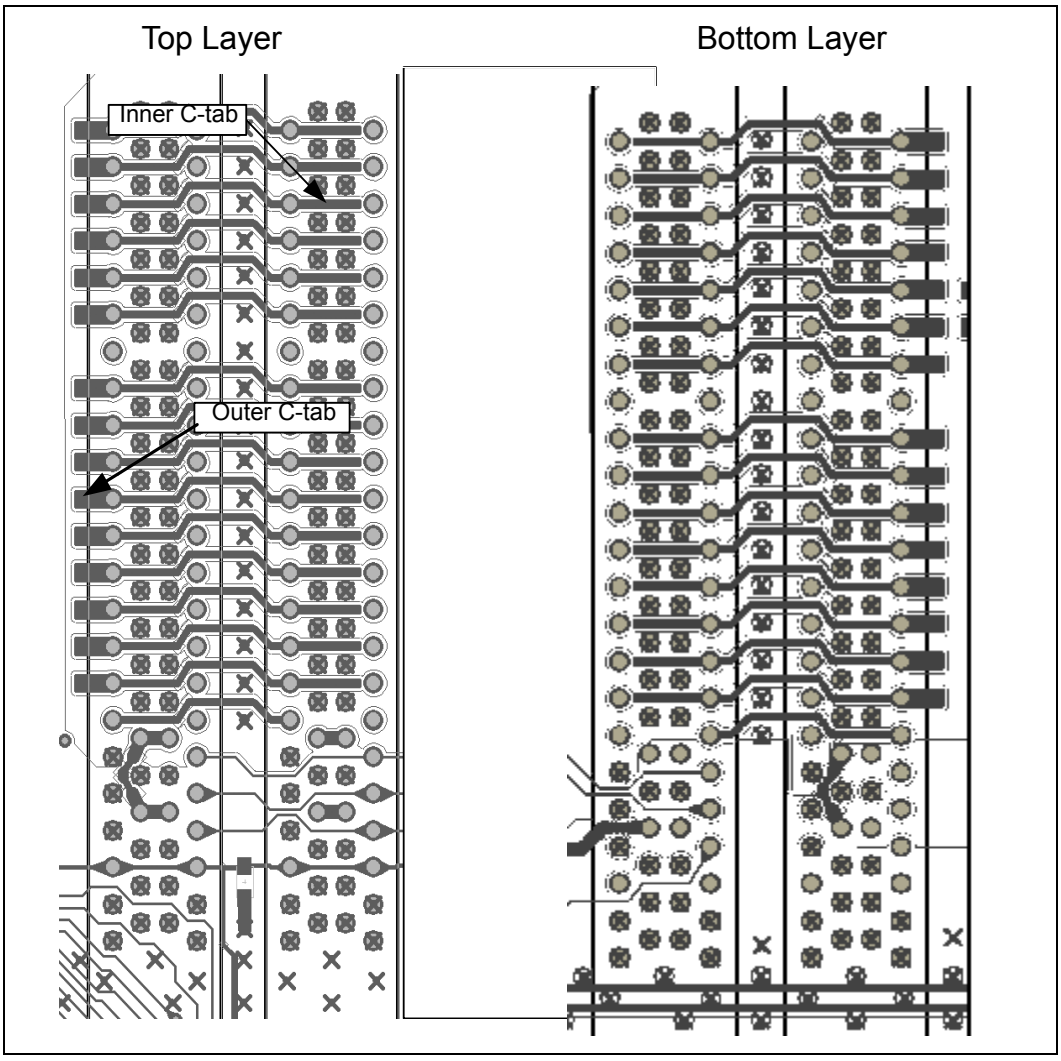
Note that more than one copper tab shape may be used (as shown in Figure 4-15). The tab dimensions are based on copper area over the ground plane. The actual length and width of the tabs may be different due to routing constraints (e.g., if tab must extend to center of hole or anti-pad), however each copper tab should have equivalent area. The copper tabs, in the following figures, have the following dimensions:

Inner CTAB (C_A)= 140 (length) x 20 (width)

Outer CTAB (C_B)= 70 (length) x 40 (width)

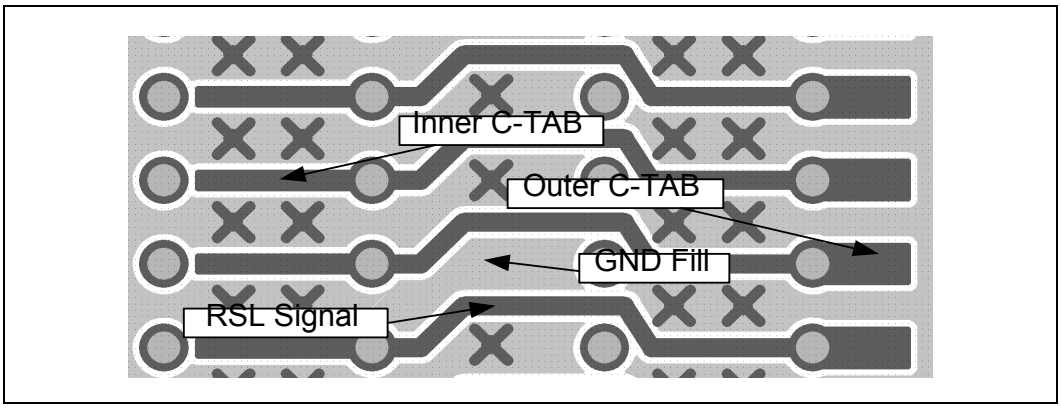
Figure 4-15, and Figure 4-16 show a routing example of tab compensation capacitors**. Note that ground floods, around the RIMM pins, must not be interrupted by the capacitor tabs**, and they must be connected to avoid discontinuity in the ground plane as shown. Also, compensating capacitive tabs (C-TAB) are required at the connector pins for SCK and CMD signals.

Figure 4-15. C-Tab Example (Top and Bottom Layers)



- Ground floods were removed for picture clarity.

Figure 4-16. Close-up of C-TABs



Direct RDRAM Ground Plane Reference

The ground reference island under the RSL signals must be continuous from the last RIMM to the back of the termination capacitors and resistors. The return current will flow through the Vterm capacitors into the ground island and under the RSL traces. Any split in the ground island will provide a sub-optimal return path. In a 4-layer board, this will require the Vterm island to be on an outer layer. The Vterm island should ALWAYS be placed on the top layer as shown in the "Rambus Termination Example".

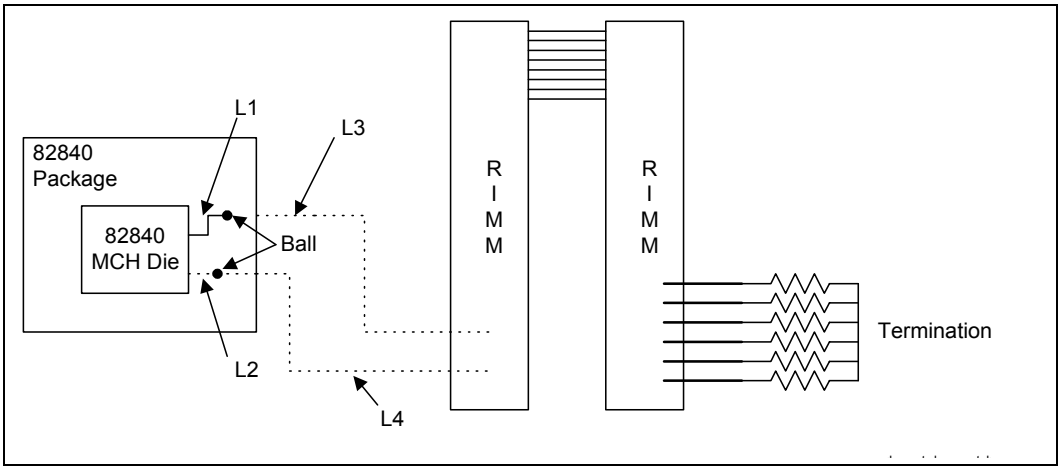
Length Matching Method

- **Package Dimension (ΔL_{PKG}):** a representation of the length from the pad to the ball.
- **Board Trace Length (L_{MB}):** the trace length on the board.
- **Nominal RSL Length:** the length to which all signals are matched. The Nominal RSL Length is an arbitrary to which all the RSL signals will be matched (within 10 mils).

L1, L2 = ΔL_{PKG} = Package Dimension

L3, L4 = ΔL_{PCB} = Board Trace Length

Figure 4-17. RDRAM Trace Length Matching Example



To allow for greater routing flexibility, the RSL signals require pad-to-pin length matching between the 82840 MCH to the first RIMM connector or 82840 MCH to the MECC. If only the trace lengths between the balls of the 82840 MCH to the pins of RIMM connector are matched, then the length mismatch between the pad (on the die) and the ball has not been compensated. All RSL signals, per channel, are required to have matching trace lengths from pad-to-pin within ±10 mils.

- RSL signals length match requirement
  - — L1 and L3 must be length matched to L2 and L4 within +/10 mils.

Equation 4-2. Compensated trace length calculation

$$\Delta L_{PCB} = (\Delta L_{PKG} * \text{Package}_{\text{TRACE VELOCITY}}) / \text{PCB}_{\text{TRACE VELOCITY}}$$

The PCB trace length for each signal is a calculated value, and may vary with designs. The actual package trace velocity is between 177 ps/in and 183 ps/in. The nominal trace velocity of 180 ps/in can be used when calculating the compensated PCB trace length. The $PCB_{TRACE\ VELOCITY}$ is board dependent.

The RSL signal lengths (ΔL_{PKG}) can be normalized to either the shortest or longest RSL trace using the below equation (Normalized trace length calculation). Refer to the *Intel® 840 Chipset: 82840 Memory Controller Hub (MCH)* Datasheet for specific package traces. Note that this ballout document provides RSL signal lengths **NORMALIZED TO THE LONGEST** trace length. Additional RSL length matching on the MEC, with the MRH-R, will be available in the Intel® 840 Chipset Workstation/Server MEC Design Guide.

Equation 4-3. Normalized trace length calculation

$$\text{New } \Delta L_{PKG} = \Delta L_{PKG} - \Delta L_{NORMALIZED\ RSL}$$

The RDRAM clocks (CTM, CTM#, CFM, and CFM#) must be longer than the RDRAM signals due to their increased trace velocity (because they are differential and routed as a pair). To calculate the length for each clock, the following formula should be used:

Clock Length = Nominal RSL Signal Length (package + board)* 1.021

The lengthening of the clock signals, to compensate for their trace velocity change, ONLY applies to routing between the MCH and the first RIMM. The clock signals should be matched in length to the RSL signals between RIMMs.

It is not necessary to account for CMOS signals package compensation. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be kept as minimum as possible (i.e., route the CMOS signals PCB trace length equal to nominal RSL PCB trace length).

VIA Compensation

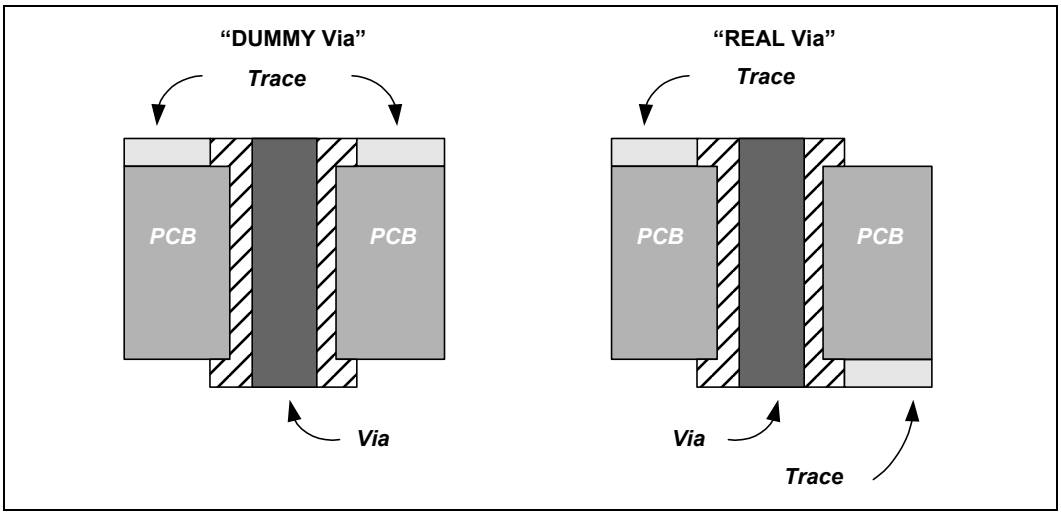
All signals must have the same number of VIAs. As a result, each trace will have 1 VIA (near the BGA pad) because some of the RSL signals must be routed on the bottom of the motherboard. It will be necessary to place "dummy" via on all signals that are routed on the top layer. The electrical characteristics between "dummy" via and "real" vias are not exact, so additional compensation is needed on each signal that has "dummy" via.

Each signal with dummy via must have 25 mils of additional trace length. The additional 25 mils trace length must be added to the signal, routed on the top layer, after length matching.

Real via = Dummy via + 25 mils of trace length.

It is important to compensated for the electrical difference between "real" and "dummy" vias.

Figure 4-18. "Dummy" vs. "Real" Vias



4.2.1.2 Intel® 840 Chipset RDRAM Interface Trace Length Compensation

These lengths must be considered when matching trace lengths as described in the design guide. Note that these lengths are normalized to 0 with the longest trace on the package. They do not represent the actual lengths from pad to ball.

The following formula is used to determine ΔL_{PCB} :

$$\Delta L_{PCB} = (\Delta L_{pkg} * V_{pkg}) / V_{PCB}$$

ΔL_{PCB} is the nominal Δ PCB trace length to be added on the PCB

ΔL_{Pkg} is the nominal Δ package trace length

V_{pkg} is the package trace velocity, and the nominal value is 180 ps/in

V_{PCB} is the PCB trace velocity

The data given can be re-normalized to start routing from a different ball. If a different RSL signal (other than longest trace) is used for the nominalization, simply use the following equation:

$$\text{New } \Delta L_{pkg}' = \Delta L_{pkg} - \Delta L_{RSL}$$

ΔL_{pkg} is the nominal Δ package trace length

ΔL_{rsl} is the RSL signal used for re-normalization

For example: For the MCH, if MCH CHA_CFM trace length is used for nominalization, then:

	ΔL_{pkg} (mils)	**New ΔL_{pkg}' (mils)**
CHA_CF	102.756	0.000
CHA_CFM	118.897	6.142
CHA_CT	130.315	27.559
:	:	:
:	:	:
CHA_RQ7	175.984	73.228

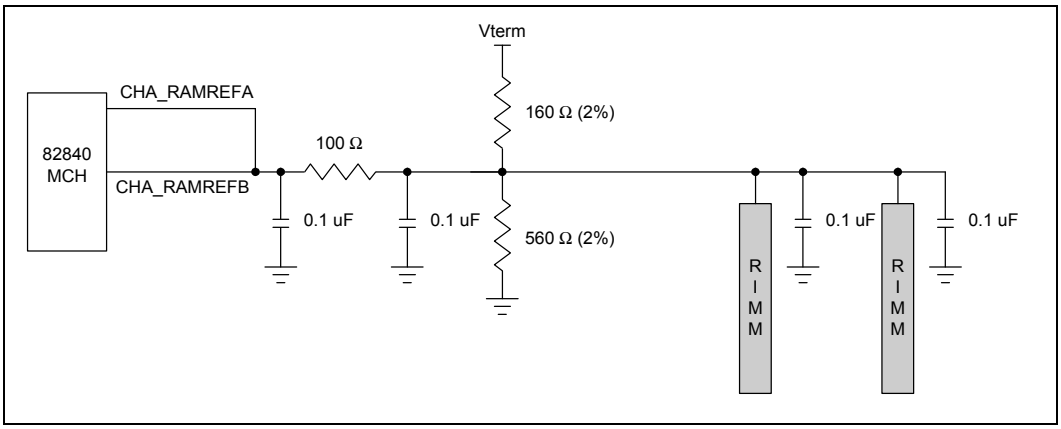
Table 4-4. MCH RSL Normalized Trace Length Data

Expansion Channel A ΔL_{PKG} Normalized to CHA_DQA8			Expansion Channel B ΔL_{PKG} Normalized to CHB_DQB7		
Signal	**Ball**	**ΔL_{PKG} (mils)**	**Signal**	**Ball**	**ΔL_{PKG} (mils)**
CHA_CFM	L1	102.756	CHB_CFM	AF11	103.543
CHA_ CFM#	L2	118.897	CHB_ CFM#	AE11	110.630
CHA_CTM	M2	130.315	CHB_CTM	AE12	109.842
CHA_CTM#	M1	117.716	CHB_CTM#	AF12	110.236
CHA_DQA0	K1	93.701	CHB_DQA0	AF10	101.968
CHA_ DQA1	K3	162.204	CHB_ DQA1	AD10	150.393
CHA_ DQA2	J1	40.551	CHB_ DQA2	AF9	81.102
CHA_ DQA3	J3	137.008	CHB_ DQA3	AD9	137.401
CHA_ DQA4	J2	87.795	CHB_ DQA4	AE9	115.354
CHA_ DQA5	H3	115.748	CHB_ DQA5	AD8	120.079
CHA_ DQA6	H1	61.811	CHB_ DQA6	AF8	48.425
CHA_ DQA7	G3	99.212	CHB_ DQA7	AD7	109.055
CHA_DQA8	G1	0.000	CHB_DQA8	AF7	29.921
CHA_DQB0	U3	143.307	CHB_DQB0	AD17	130.708
CHA_ DQB1	U1	122.441	CHB_ DQB1	AF17	72.441
CHA_ DQB2	V3	164.173	CHB_ DQB2	AD18	120.079
CHA_ DQB3	V1	111.417	CHB_ DQB3	AF18	69.291
CHA_ DQB4	W3	151.181	CHB_ DQB4	AD19	142.126
CHA_ DQB5	W1	68.504	CHB_ DQB5	AF19	34.252
CHA_ DQB6	V2	106.693	CHB_ DQB6	AE18	111.417
CHA_ DQB7	Y1	40.157	CHB_ DQB7	AF20	0.000
CHA_ DQB8	Y3	134.252	CHB_ DQB8	AD20	70.472
CHA_EXP0	P3	192.519	CHB_EXP0	AD14	160.236
CHA_EXP1	P2	129.921	CHB_EXP1	AE14	161.811
CHA_RQ0	T3	185.433	CHB_RQ0	AD16	152.362
CHA_ RQ1	T2	131.496	CHB_ RQ1	AE16	93.307
CHA_ RQ2	T1	126.378	CHB_ RQ2	AF16	98.425
CHA_ RQ3	R3	189.370	CHB_ RQ3	AD15	157.480
CHA_ RQ4	R1	85.039	CHB_ RQ4	AF15	106.693
CHA_ RQ5	P1	78.740	CHB_ RQ5	AF14	101.968
CHA_ RQ6	N1	124.409	CHB_ RQ6	AF13	112.205
CHA_ RQ7	N3	175.984	CHB_ RQ7	AD13	161.811

Direct RDRAM Reference

The RDRAM reference voltage (RAMREF) must be generated as shown above. RAMREF should be generated from a typical resistor divider using 2% tolerant resistors. Additionally, RAMREF must be decoupled locally at EACH RIMM connector, at the resistor divider and at the 82840 MCH. Finally, a 100 Ω series resistor is required near the MCH. The RAMREF signal should be routed with 6 mils wide traces.

Figure 4-19. RAMREF Generation Example Circuit

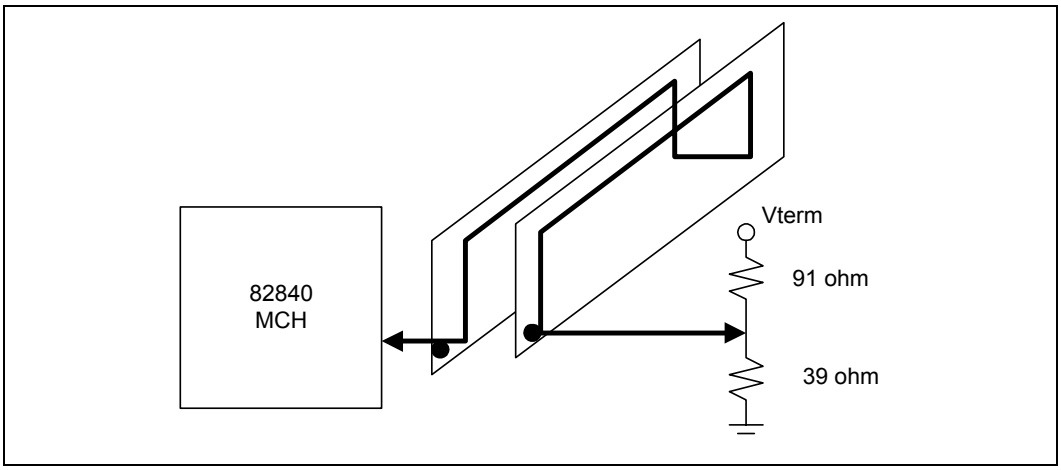


High Speed CMOS Routing

Due to the synchronous requirements between the RSL signals and the high-speed CMOS signals, these signals should be routed as part of the RSL channel. They must be impedance matched and properly terminated (using a different termination scheme than the RSL signals). It is not necessary to perform the length match calculation for high-speed CMOS signals. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be kept as minimal as possible (i.e., route the CMOS signals PCB trace length equal to nominal RSL PCB trace length). The high-speed CMOS signals should be routed in their respective positions in the channel.

The high speed CMOS signals (CMD and SCK) must be routed using 28 Ω traces. Using the recommended stackup, these signals will be 18 mils wide. The high-speed CMOS signals must be length matched to the RSL signals within 1200 mils (1.2") due to a timing requirement between CMOS and RSL signals during NAP Exit and PDN Exit. For the system to enter S3 mode reliably, both SCK and CMD signals must be terminated with a 91 Ω pull-up resistor and a 39 Ω pull-down resistor. These resistors must be 2% or better.

Figure 4-20. High Speed CMOS Termination



A CMOS voltage must be supplied to each RIMM. This CMOS voltage is used by the RDRAMs CMOS interface. This voltage (Vcmos) must be 1.8V and the maximum load is 3 ma.

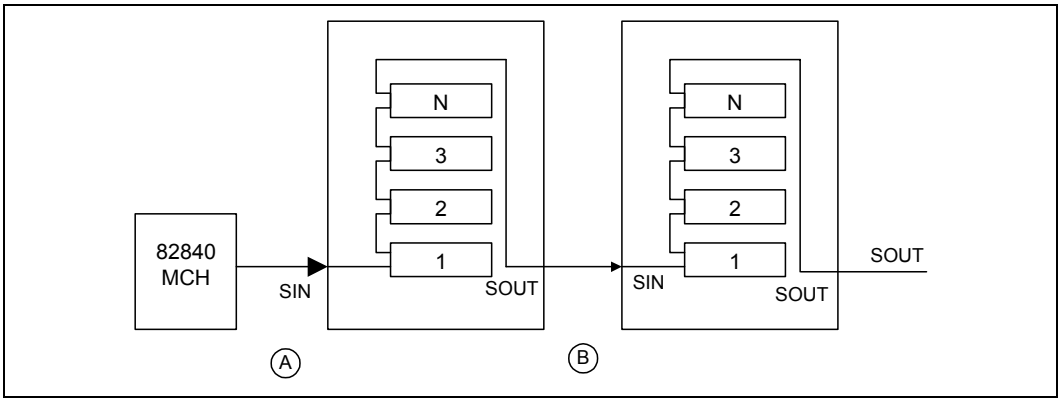
Additionally, this voltage must be supplied during suspend to RAM. Therefore, Vterm and Vcmos can't be generated from the same source (i.e., they can not be the same power plane). Due to the low power requirements of Vcmos, it can be generated by a 36 Ω/ 100 Ω resistor divider from 2.5V. The high-speed CMOS signals require AC termination as shown above, with two 56 Ω resistors.

4.2.1.3 SIO Routing

The SIO signal is a bi-directional signal that operates at 1 MHz. The SIO signal must be routed from RIMM connector to RIMM connectors shown below. The SIO signal enters the first RIMM, propagates through all the devices (this signals is buffered by each device) on the RIMM, and then exits the RIMM. The signal continues through the next RIMM.

The SIO signal is routed with a 5 mil wide, 60 Ω trace. This signal requires a 2.2 KΩ–10 KΩ terminating resistor on the last RIMM's SOUT pin.

Figure 4-21. SIO Routing Example



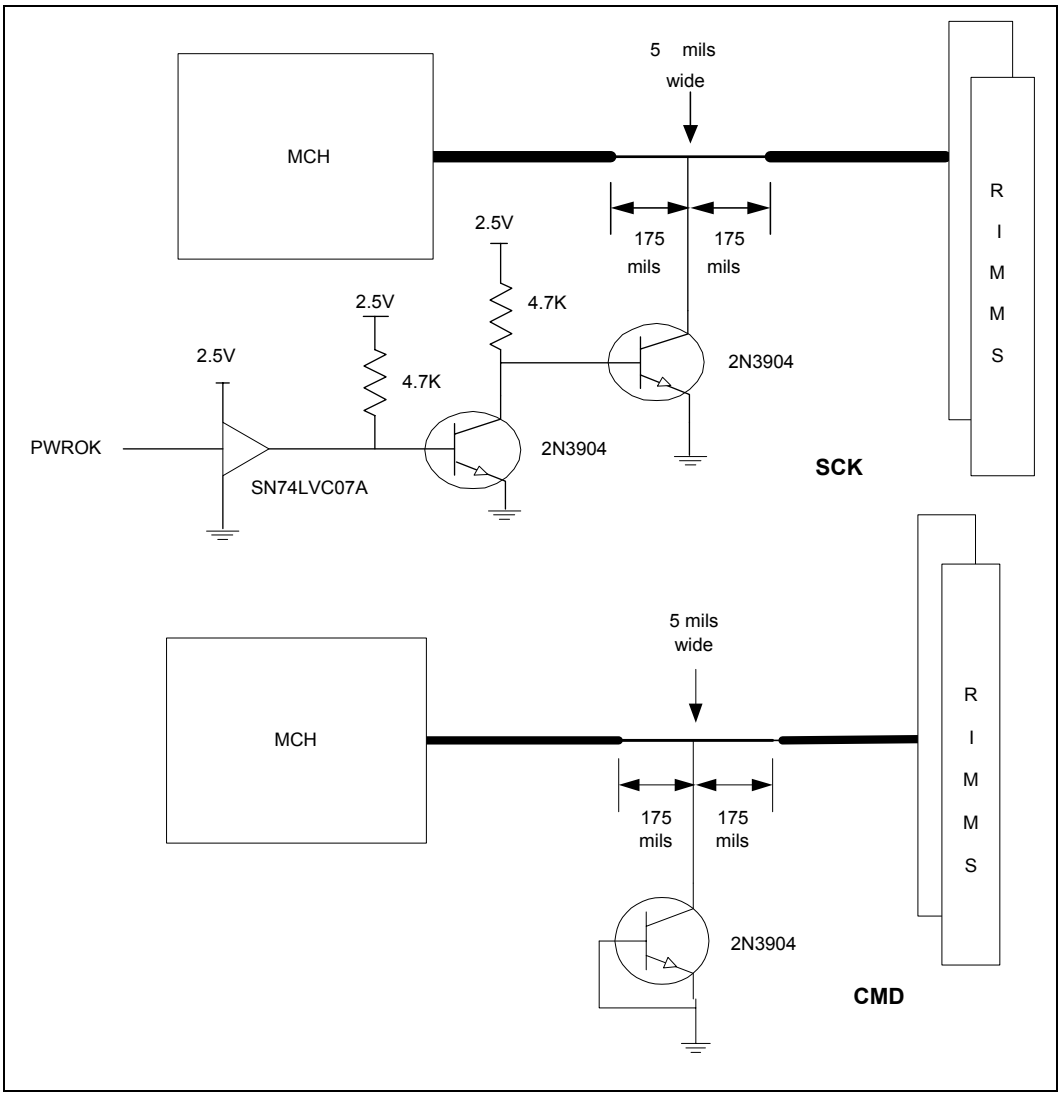
Suspend-to-RAM Shunt Transistor

When the Intel® 840 chipset based system enters or exits Suspend-to-RAM, power will be ramping to the 82840 MCH (i.e., it will be powering-up or powering-down). When power is ramping, the state of the 82840 MCH outputs is not guaranteed. Therefore, the 82840 MCH could drive the CMOS signals and issue CMOS commands. One of the commands (the only one the RDRAM would respond to) is the power-down exit command. To avoid the 82840 MCH inadvertently taking the RDRAMs out of power-down due to the CMOS interface being driven during power ramp, the SCK (CMOS clock) signal must be shunted to ground when the 82840 MCH is entering and exiting Suspend-to-RAM. This shunting can be accomplished using the NPN transistor shown in circuit shown in Figure 4-22. The transistor should have a Cobo of 4 pf or less (i.e., MMBT3904LT1).

In addition, to match the electrical characteristics on the SCK signal, the CMD signal needs a dummy transistor. This transistor's base should be tied to ground (i.e., always turned off).

To minimize impedance discontinuities, the traces for CMD and SCK must have a neck down from 18 mil traces to 5 mil traces for 175 mils on either side of the SCK/CMD attach point as shown below.

Figure 4-22. RDRAM CMOS Shunt Transistor



This implementation is applicable for RIMMs down solution only, and is not needed on the repeater channels. Also, this implementation is not necessary if Suspend-to-RAM is not supported within the system.

4.2.2 Test coupon design guidelines

Characterization and understanding of the trace impedance is critical for delivering reliable systems at the increased bus frequencies. Incorporating a test coupon design into the motherboard will make testing simpler and more accurate. The test coupon pattern must match the probe type being used.

The location of the test coupon is listed in order of preference below:

1st Choice (Ideal Location) = Memory section of the motherboard

2nd Choice = Any section of the motherboard

3rd Choice = Separate location in the panel

The *Intel Impedance Test Methodology Document* should be used to ensure boards are within the 28 Ω±10% requirement. The *Intel Controlled Impedance Design and Test Document* should be used for the test coupon design and implementation. These documents can be found at: http://developer.intel.com/design/chipsets/memory/rdram.htm – Select "Application Notes"

4.3 AGP 2.0

For detailed AGP Interface functionality (protocols, rules and signaling mechanisms, etc.) refer to the latest *AGP Interface Specification revision 2.0*, which can be obtained from http://www.agpforum.org. This design guide (*Intel® 840 Chipset Platform*) focuses only on specific Intel® 840 chipset platform recommendations.

The AGP Interface Specification revision 2.0 enhances the functionality of the original AGP Interface Specification (revision 1.0) by allowing 4X data transfers (4 data samples per clock) and 1.5 volt operation. In addition to these major enhancements, additional performance enhancement and clarifications, such as fast write capability, are included in revision 2.0 of the AGP Interface Specification. The Intel® 840 chipset is the first Intel chipset that supports the enhanced features of revision 2.0 of the AGP Interface Specification.

The 4X operation of the AGP interface provides for "quad-sampling" of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses (i.e., the data is sampled four times during each 66 MHz AGP clock). This means that each data cycle is ¼ of a 15 ns (66 MHz clock) or 3.75 ns. It is important to realize that 3.75 ns is the data cycle time; not the clock cycle time. During 2X operation, the data is sampled twice during a 66 MHz clock cycle, therefore the data cycle time is 7.5 ns.

To allow for these high-speed data transfers, the 2X mode of AGP operation uses source synchronous data strobing. During 4X operation, the AGP interface uses differential source synchronous strobing.

With data cycle times as small as 3.75 ns, and setup/hold times of 1ns, propagation delay mismatch is critical. In addition to reducing propagation delay mismatch, it is important to minimize noise. Noise on the data lines cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great, or there is noise on the interface, incorrect data will be sampled.

The low-voltage operation on AGP (1.5V) requires even more noise immunity. For example, during 1.5V operation, V_{ilmax} is 570 mv. Without proper isolation, crosstalk could create signal integrity issues.

The AGP signals are broken into three groups: 1X timing domain and 2X/4X timing domain signals. In addition, the 2X/4X timing domain signals are divided into three sets of signals (#1-#3). All signals must meet the minimum and maximum trace length, width and spacing requirements. The trace length matching requirements are only applicable between the 2X/4X timing domain signal sets.

Table 4-5. AGP 2.0 Signal Groups

1X Signals	Name
	CLK
	RBF#
	WBF#
	ST[2:0]
	PIPE#
	REQ#
	GNT#
	PAR
	FRAME#
	IRDY#
	TRDY#
	STOP#
	DEVSEL#

2X/4X Signals	Name
SET #1	AD[15:0]
	C/BE[1:0]#
	AD_STB0
	AD_STB0#[1]
SET #2	AD[31:16]
	C/BE[3:2]#
	AD_STB1
	AD_STB1#[1]
SET #3	SBA[7:0]
	SB_STB
	SB_STB#[1]

Misc.Signals	Name
	USB+
	USB-
	OVRCNT#
	PME#
	TYPDET#
	PERR#
	SERR#
	INTA#
	INTB#

NOTES:
1. Signals AD_STB1 and SB_STB are AGP 4X signals only.

Strobe signals are not used in the 1X AGP mode. In 2X AGP mode, AD[15:0] and C/BE[1:0]# are associated with AD_STB0, AD[31:16] and C/BE[3:2]# are associated with AD_STB1, and SBA[7:0] is associated with SB_STB. In 4X AGP mode, AD[15:0] and C/BE[1:0]# are associated with AD_STB0 and AD_STB0#, AD[31:16] and C/BE[3:2]# are associated with AD_STB1 and AD_STB1#, and SBA[7:0] is associated with SB_STB and SB_STB#.

4.3.1 General AGP Routing Guidelines

The following routing guidelines are recommended for an optimal system design. Though, these guidelines are not intended to replace thorough system validation on Intel® 840 chipset based products.

4.3.1.1 Decoupling

A minimum of six (6) 0.01 uF capacitors are required and must be placed as close as possible to the MCH. It is recommended that the capacitors be placed within 70 mils from the outer row of balls of the MCH for VDDQ decoupling. The designer should evenly distribute placement of decoupling capacitors among the AGP interface signal field. It is recommended that the designer use a low ESL ceramic capacitor, such as a 0603 body type, X7R dielectric.

In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition AGP signal from one reference signal plane to another. One extra 0.01 uF capacitor is required per 10 vias. The capacitor should be placed as close to the center of the via field as possible.

The designer should ensure that the AGP connector is well decoupled as described in the *AGP Design Guide, Revision 1.0*, section 1.5.3.3.

Note: To add the decoupling capacitors within 70 mils of the MCH and/or close to the vias, the trace spacing may be reduced as the traces go around each capacitor. The narrowing of space between traces should be minimal and for as short of a distance as possible (1” maximum).

4.3.1.2 Ground Reference

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the MCH to an AGP connector utilizing a minimum number of vias on each net; AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT# and ST[2:0].

In addition to the minimum signal set listed above, it is strongly recommended that half of all your AGP signals be reference to ground depending on board layout. An ideal design would have the complete AGP interface signal field referenced to ground.

The recommendations above are not specific to any particular PCB stackup, but are applicable to all Intel® Chipset designs.

4.3.2 1X Timing Domain Routing Guidelines

- The AGP 1X timing domain signals have a maximum trace length of 7.5 inches. This maximum length applies to ALL 1X timing domain signals.
- AGP 1X timing domain signals can be routed with 5 mils minimum trace separation.
- There is no trace length mismatch requirement for 1X timing domain signals.

4.3.3 2X/4X Timing Domain Routing Guidelines

These trace length guidelines apply to ALL 2X/4X timing domain signals. These signals should be routed using 5 mils wide (~60Ω) traces.

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum trace length for AGP 2X/4X interface signals is 7.5”.

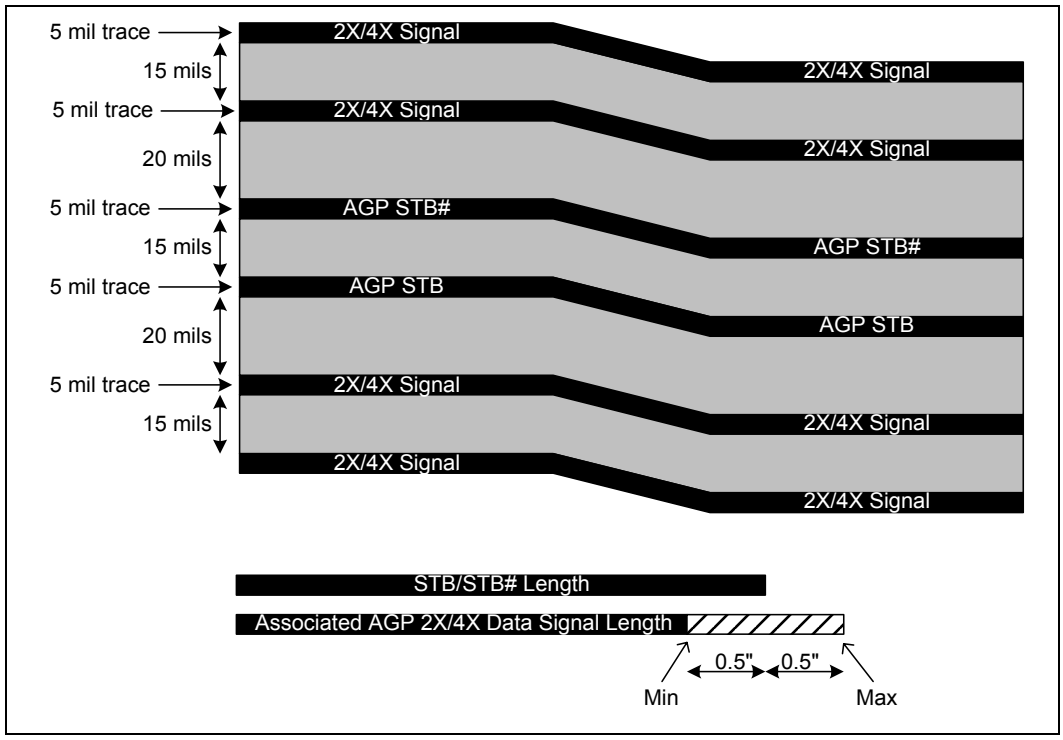
4.3.3.1 AGP Interfaces Signals < 6” Routing Guidelines

These guidelines are for designs that require less than 6 inches between the A.G.P. connector and the MCH. If the AGP interface is less than 6 inches, at least 1:3 trace spacing is required for 2X/4X lines (data and strobes). These 2X/4X signals must be matched to their associated strobe within ±0.5 inches.

For example, if a set of strobe signals (e.g., AD_STB0 & AD_STB0#) are 5.3” long, then the associated data signals (i.e., AD[15:0] & C/BE#[2:0]) can be 4.8” to 5.8”. Another example, if strobe set SB_STB & SB_STB# is 4.2” long, then the associated data signals (i.e., SBA[7:0]) can be 3.7” to 4.7”.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; special care must be taken when routing these signals. Because each strobe pair is a differential pair, the pair should be routed together (i.e., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1”.

Figure 4-23. AGP 2X/4X Routing Example for Interfaces < 6”



4.3.3.2 AGP Interfaces Signals ≥ 6” and ≤ 7.25” Routing Guidelines

Longer lines have more crosstalk. Therefore in order to reduce skew, longer line lengths require a greater amount of spacing between traces. For line lengths between 6 inches and 7.25 inches, 1:4 routing is required for all data lines and strobes. In this case, the line length mismatch must be less than ±0.125” within each signal group (between all data signals and the strobe signals).

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5” long, the data signals which are associated to those strobe signals (e.g., AD[15:0] and C/BE[2:0]#), can be 6.475” to 6.625” long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2” long, and the data signals which are associated to those strobe signals (e.g., SBA[7:0]), can be 6.075” to 6.325” long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them. Each strobe pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1” (that is, a strobe and its compliment must be the same length within 0.1”).

4.3.3.3 AGP Routing Summary

The 2X/4X Timing Domain Signals can be routed with 5 mil spacing when breaking out of the MCH 544 BGA. The routing must widen to the documented requirements within 0.3” of the MCH 544 BGA package.

When matching trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

It is important to reduce line length mismatch to ensure added margin. To reduce trace to trace coupling (cross talk), separate the traces as much as possible. All signals in a signal group should be routed on the same layer. The trace length and trace spacing requirements ***must*** not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to 0 as possible to provide timing margin.

Table 4-6. AGP Routing Summary

Signals Group	Max Length	Trace Spacing	Length Mismatch	Associated Strobe(s)	Notes
1X Timing Domain	7.5”	5 mil[1]	-	-	-
2X/4X Timing Domain					
SET #1	7.25”	20 mil[1]	±0.125”	AD_STB0 AD_STB0#	Strobe signal pair must be the same length
SET #2	7.25”	20 mil[1]	±0.125”	AD_STB1 AD_STB1#	Strobe signal pair must be the same length
SET #3	7.25”	20 mil[1]	±0.125”	SB_STB SB_STB#	Strobe signal pair must be the same length
2X/4X Timing Domain					
SET #1	6.0”	15 mil[1]	±0.5”	AD_STB0 AD_STB0#	Strobe signal pair must be the same length
SET #2	6.0”	15 mil[1]	±0.5”	AD_STB1 AD_STB1#	Strobe signal pair must be the same length
SET #3	6.0”	15 mil[1]	±0.5”	SB_STB SB_STB#	Strobe signal pair must be the same length

NOTE: Each strobe pair must be separated from other signals by at least 20 mils.

4.3.3.4 AGP Clock Skew

The maximum total AGP clock skew, between the 82840 MCH and the AGP component, is 1 ns for all transfer modes. This 1 ns skew, includes the skew and jitter originated by the motherboard, add-in card and clock synthesizer. Clock skew must be evaluated not only at a single threshold voltage but at all points of the clock edge that falls in the switching range. The 1 ns skew is divided such that the motherboard is allotted 0.9 ns. The motherboard designer must determine how the 0.9 ns is allotted between the board and the synthesizer.

4.3.3.5 VDDQ and TYPEDET#

AGP specifies two separate power planes: VCC and VDDQ. VCC is the core power for the graphics controller. This voltage is ALWAYS 3.3V. VDDQ is the interface voltage and is 3.3V for AGP 1.0 implementations. For the designer developing an AGP 1.0 motherboard, there is no distinction between VCC and VDDQ. Both are tied to the 3.3V power plane on the motherboard.

AGP 2.0 requires VCC and VDDQ to be tied to separate power planes. The AGP 2.0 Specification implements a TYPEDET# (type detect) signal on the AGP connector that determines the operating voltage of the AGP 2.0 interface (VDDQ). The motherboard must be able to provide either 1.5V or 3.3V to the add-in card depending on the state of the TYPEDET# signal. The 1.5V low-voltage operation applies only to VDDQ; Vcc is always 3.3V.

The TYPEDET# signal indicates whether the AGP 2.0 interface operates 1.5 volts or 3.3 volts. If TYPEDET# is floating (no connect) on an AGP add-in card, the interface is 3.3 volts. If TYPEDET# is shorted to ground, the interface is 1.5 volts.

Table 4-7. TYPEDET# and VDDQ Relationship

TYPEDET# (on the graphics add-in card)	VDDQ (supplied by the motherboard)
GND	1.5V
N/C	3.3V

The motherboard must provide 3.3V to the Vcc pins of the AGP connector. If the graphics controller requires a lower voltage, then the add-in card must regulate the 3.3V Vcc voltage to the controller's requirement. The graphics controller may ONLY power AGP I/O buffers with the VDDQ power pins.

Because of this, a flexible voltage regulator must be used to supply the appropriate voltage to VDDQ of the AGP connector.

Figure 4-24. AGP VDDQ Generation Example

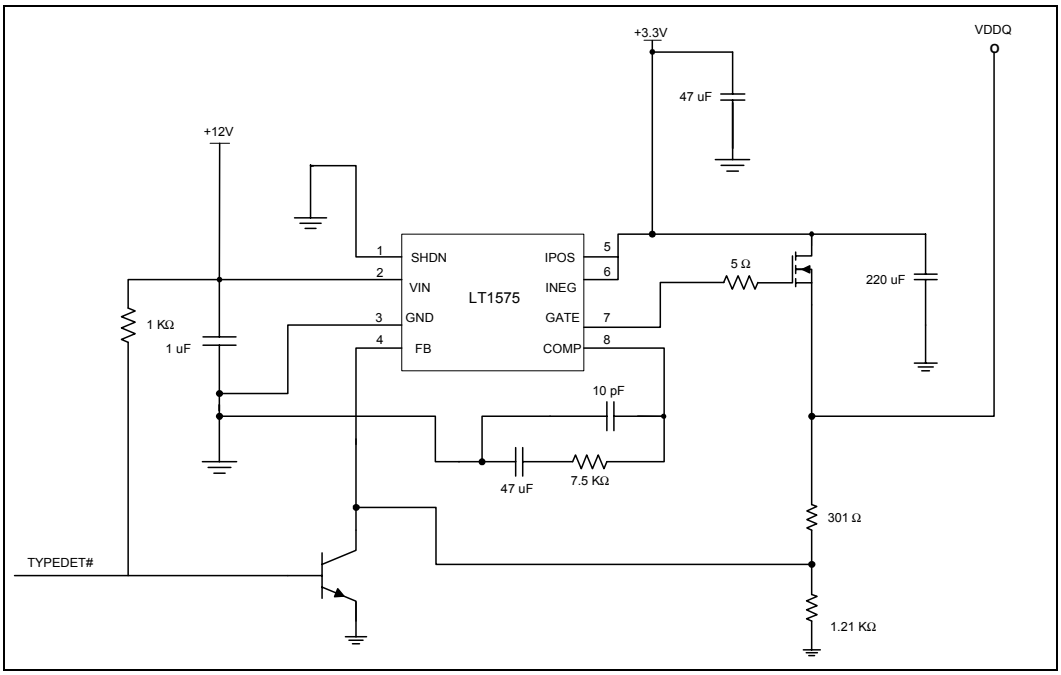


Figure 4-24 demonstrates one way to design the VDDQ voltage regulator. This regulator is a linear regulator with an external, low Rds_{on} FET. The source of the FET is connected to 3.3V. The regulator converts 3.3V to 1.5V or passes 3.3V depending on the state of TYPEDET#. If a linear regulator is used, it must draw power from 3.3V (not 5V) to control thermals (i.e., 5V regulated down to 1.5V with a linear regulator will dissipate approximately 7 W at 2 A). Because it must draw power from 3.3V and, in some situations, must simply pass that 3.3V to VDDQ (when a 3.3V add-in card is placed in the system), the regulator MUST use a low Rds_{on} FET.

AGP 1.0 ECR #44 modified $VDDQ3.3_{min}$ to 3.1V. Using an ATX power supply, the $3.3V_{min}$ is 3.168. Therefore, 68 mV of drop is allowed across the FET at 2A. This corresponds to a FET with a Rds_{on} of 34 mΩ

How does the regulator switch? The feedback resistor divider is set to 1.5V. When a 1.5V card is placed in the system, the transistor is off and the regulator regulates to 1.5V. When a 3.3V card is placed in the system, the transistor is on, and the feedback will be pulled to ground. When this happens, the regulator will drive the gate of the FET to nearly 12V. This will turn the FET on and pass 3.3V - 2A * Rds_{on} to VDDQ.

4.3.3.6 V_{REF} Generation

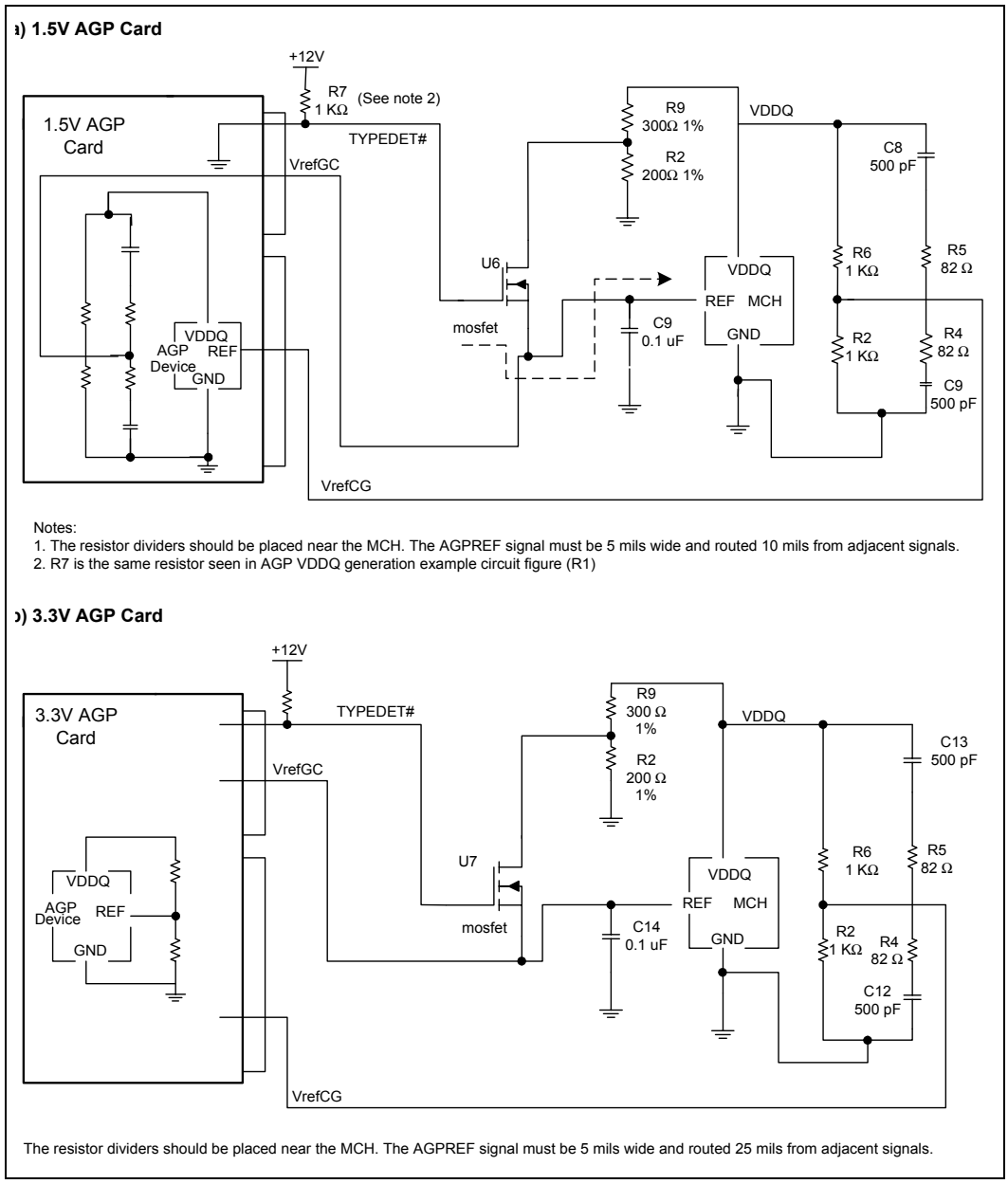
The 3.3V AGP cards will generate V_{REF} locally. The card has a resistor divider circuit that divides VDDQ down to V_{REF}. To account for differences between VDDQ and GND, 1.5V cards will use source generated V_{REF}; V_{REF} signal is generated at the graphics controller and sent to the MCH, and another V_{REF} is generated at the MCH and sent to the graphics controller.

For 1.5V add-in cards (only), both of the graphics controller and the MCH are required to generate V_{REF} and distribute it through the connector. Two signals have been defined, on the universal connector, to allow the V_{REF} passing:

- VREFGC- V_{REF} from the graphics controller to the chipset
- VREFCG- V_{REF} from the chipset to the graphics controller

The V_{REF} divider network should be placed near the AGP interface to achieve the common mode power supply effect. The minimum trace spacing around the V_{REF} signal must be 25 mils, to reduce cross talk and maintain signal integrity. V_{REF} must be 0.4VDDQ for 3.3V operation and 0.5VDDQ for 1.5V operation. One example of a “flexible” V_{REF} voltage divider circuit is shown below.

Figure 4-25. AGP 2.0 VREF Generation and Distribution for 1.5V and 3.3V Cards



4.3.3.7 Compensation

The MCH AGP interface supports resistive buffer compensation (AGPRCOMP). The AGPRCOMP signal must be tied to a 40 Ω2% or 39 Ω1% pull-down resistor to ground. This trace should be kept to 10 mils wide and less than 0.5” long.

4.3.3.8 AGP Pull-ups/Pull-down on AGP Signals

Some of the AGP signals may require either a pull-up resistor to VDDQ (not VCC3.3) or pull-down resistor to ground. This is to ensure stable values are maintained when agents are not actively driving the bus. The recommended AGP pull-up/pull-down resistor value is 8.2 KΩ (4 KΩ≤ R_{value} ≤16 KΩ). The AGP interface does not require external termination.

The trace stub length to the pull-up/pull-down resistor should be kept to a minimal to avoid signal reflection. This trace length is different for 1X and 2X/4X modes. A summary is shown in Table 4-8.

Table 4-8. AGP Pull-up/Pull-down Resistors

1X Timing Domain	
Signals	**PU/PD Requirement**
FRAME#	pull-up resistor to VDDQ
TRDY#	pull-up resistor to VDDQ
IRDY#	pull-up resistor to VDDQ
DEVSEL#	pull-up resistor to VDDQ
STOP#	pull-up resistor to VDDQ
SERR#	pull-up resistor to VDDQ
PERR#	pull-up resistor to VDDQ
RBF#	pull-up resistor to VDDQ
PIPE#	pull-up resistor to VDDQ
REQ#	pull-up resistor to VDDQ
WBF#	pull-up resistor to VDDQ
GNT#	pull-up resistor to VDDQ
ST[2:0]	Pull-up resistor to VDDQ
INTA#	Pulled to 3.3V
INTB#	Pulled to 3.3V

The trace stub to the pull-up resistor on the 1X timing signals should be kept to less than 0.5”. This is to avoid signal reflections from the stub. The strobe signals require pull-up/pull-down on the motherboard to ensure stable values when there are no agents driving the bus.

Table 4-9. 2X/4X AGP Pull-up and Pull-down Resistors

2X/4X Timing Domain	
Signals	**PU/PD Requirement**
AD_STB[1:0]	pull-up resistor to VDDQ
SB_STB	pull-up resistor to VDDQ
AD_STB[1:0]#	pull-down resistor to GND
SB_STB#	pull-down resistor to GND

The trace stub to the pull-up/pull-down resistor on the 2X/4X timing domain signals should be kept to less than 0.1” to avoid signals reflection from the stub. The recommended AGP pull-up/pull-down resistor value is 8.2 KΩ (4 KΩ≤ R_{value} ≤16 KΩ).

4.3.3.9 AGP Signal Voltage Tolerance List

The following AGP signals are 3.3V tolerant during 1.5V operation:

- PME#
- INTA#
- INTB#
- PERR#
- SERR#
- CLK
- RST

The following AGP signals are 5V tolerant (Refer to the USB Specification for more details.).

- USB+
- USB-
- OVRCNT#

Note: TYPDET# is a dedicated AGP signal. This is neither grounded nor a no connect (N/C) on AGP cards. All other signals, in the VDDQ group, are not 3.3V tolerant during 1.5V AGP operation.

4.3.3.10 AGP Connector

All AGP cards are either 3.3V or 1.5V cards. There are three types of AGP connector: 3.3V AGP connector, 1.5V AGP connector, Universal connector. The Universal connector offers the most flexibility in a platform.

Table 4-10. Connector/Add-in Card Interoperability

	1.5V Connector	3.3V Connector	Universal Connector
1.5V Card	YES	NO	YES
3.3V Card	NO	YES	YES

Table 4-11. Voltage/Data Rate Interoperability

	1X	2X	4X
1.5V VDDQ	YES	YES	YES
3.3V VDDQ	YES	YES	NO

4.3.3.11 Unused AGP interface

All recommended AGP pull-up and pull-down resistors are still required, if the MCH AGP interface is not used. AGP strobe signals (AD_STB0/AD_STB0#, AD_STB1/AD_STB1#, SB_STB/SB_STB#) can be left as no connects. In addition, the AGP Enable bit (AGP Command Register, offset A8-ABh) in the 840 MCH must be set to ‘0’.

4.4 Hub Interface

The MCH, ICH and P64H ballout assignment have been optimized to simplify the hub interface routing between these devices. Via transition should be minimized on the high-speed interface.

The hub interface signals are broken into two groups: data signals (HL) and strobe signals (HL_STB).

Figure 4-26. Hub Interface A (8-Bit) Routing Example

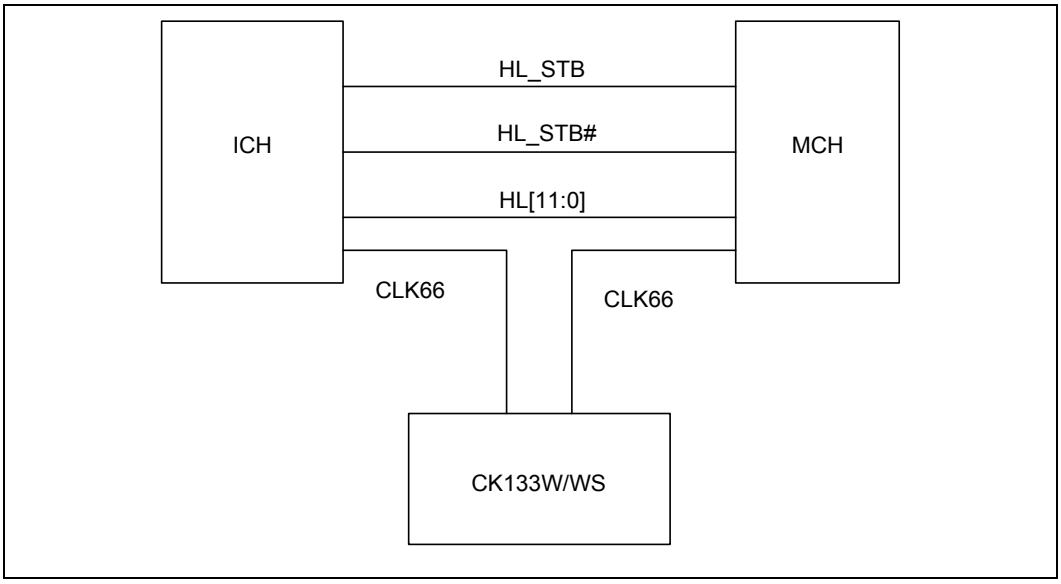
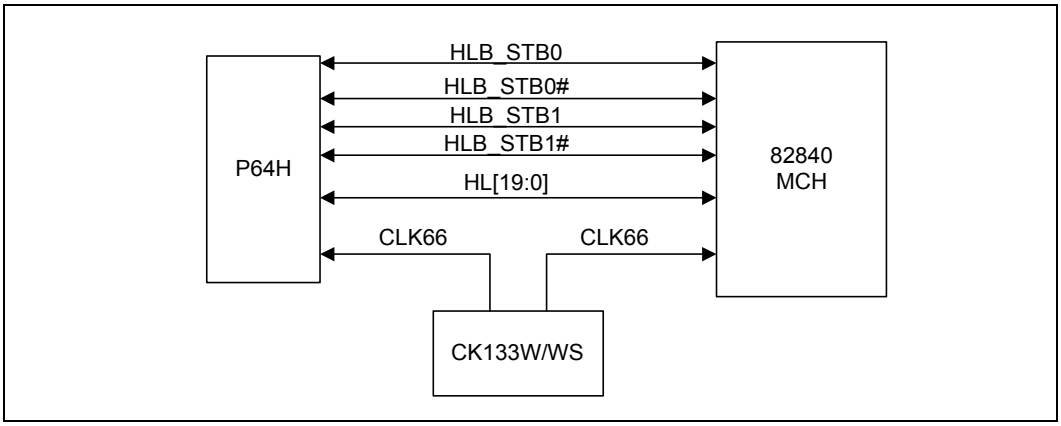


Figure 4-27. Hub Interface B (16-Bit) Routing Example



4.4.1 Hub Interface A (8-bit) to ICH

4.4.1.1 Hub Interface A Data Signals

Hub interface data signal traces should be routed 5 mils wide with 20 mils trace spacing (5 on 20). These signals can be routed 5 on 15 for navigation around components or mounting holes. To break out of the MCH and ICH package, the hub interface data signals can be routed 5 on 5. The signal must be separated to 5 on 20 within 300 mil of the package.

The maximum hub interface data signal trace length is 7". Each data signal must be matched within ±0.1" of the HL_STB differential pair.

4.4.1.2 Hub Interface A Strobe Signals

The hub interface strobe signals should be routed 5 mils wide with 20 mils trace spacing (5 on 20). This strobe pair should have a minimum of 20 mils spacing from any adjacent signals. The maximum length for the strobe signal is 7". The lengths for the strobe pair, HL_STB and HL_STB#, should be matched.

4.4.1.3 Hub Interface A (HLAREF) Generation/Distribution

HUBREF A is the hub interface reference voltage for the hub interface A and should be 0.9V ±2% (0.5*1.8V). This reference voltage can be generated locally or with a single HREF divider circuit. A HREF divider circuit example is shown below.

Figure 4-28. MCH/ICH Single Hub Interface Reference Divider Circuit

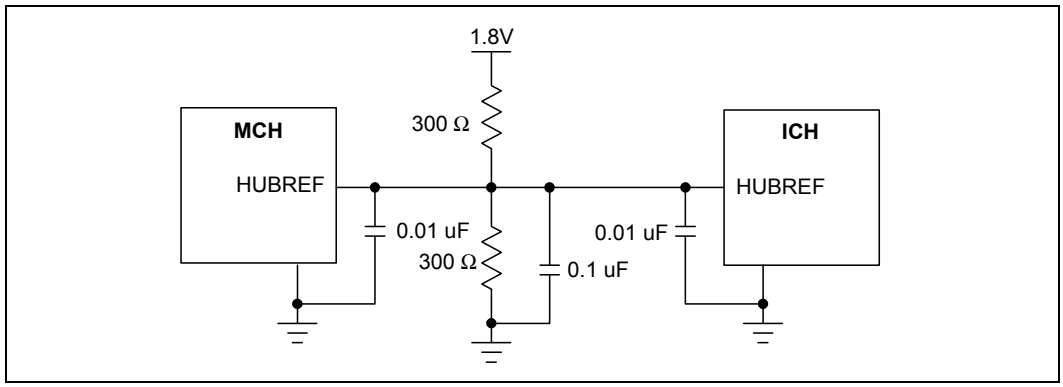
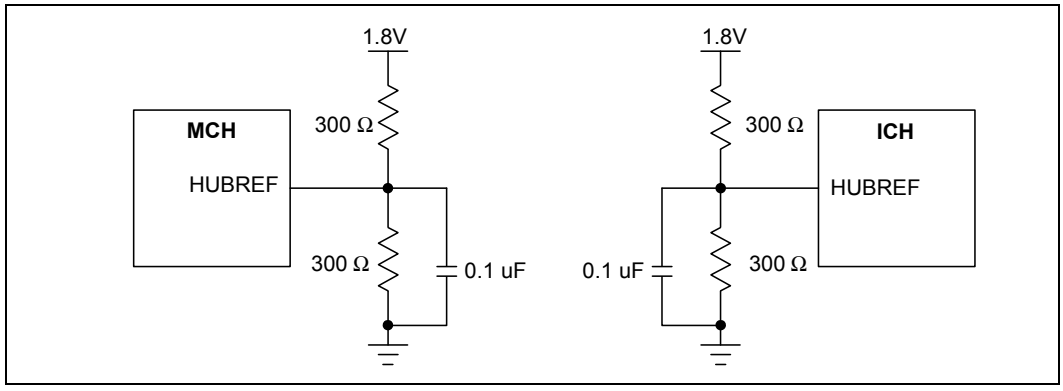


Figure 4-29. MCH/ICH Locally Generated Hub Interface Reference Divider Circuit



The resistor values must be equal and rated at 1% tolerance. These selected resistor values must also ensure that the reference voltage tolerance is maintained over the input leakage specification. The recommended range for the resistor is maintained over the entire input leakage specification. The recommended range for the resistor value is from a minimum of 100 Ω to a maximum of 1 ΩK (300 Ω shown in example)

The single HREF divider should not be located more than 4" from either MCH or ICH. If the reference dividers is located more than 4" away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HREF divider should be bypassed to ground at each component with a 0.01 uF capacitor located close to the component HREF pin. If the reference voltage is generated locally, the bypass capacitor needs to be close to the component HREF pin.

4.4.1.4 Hub Interface A Compensation

There are two options for the MCH and ICH hub interface compensation. HLCOMP is used by the ICH to adjust the buffer characteristics to specific board characteristics. The compensation can be either Impedance Compensation (ZCOMP) or Resistive Compensation (RCOMP).

- RCOMP: Tie the HLCOMP pins to a 40 Ω 2% or 39 Ω 1% pull-up resistor to 1.8V. This trace should be kept at less than 0.5” length and 10 mils wide trace.
- ZCOMP: The HLCOMP signals are routed via an 18” minimum length and 10 mil wide trace. This trace must be non-terminated and must not cross power plane splits. 15-20 mils separation between this signal and adjacent signal is recommended.

The MCH hub interface compensation for hub interface A can support either compensation methods. The same compensation method should be used at the MCH and ICH.

4.4.2 Hub Interface B (16-bit) to P64H

4.4.2.1 Data Signals

Hub interface data signal traces should be routed 5 mil wide with 20 mil trace spacing (5 on 20). These signals can be routed 5 on 15 for navigation around components or mounting holes. In order to break out of the MCH and P64H package, the hub interface data signals can be routed 5 on 5. The signal must be separated to 5 on 20 within 300 mil of the package.

The hub link interface B has minimum and maximum requirements. The minimum trace length for all hub interface B signals is 4.5”. The maximum hub interface signal trace length is 16”. Each data signal must be matched within ±0.1” of the HL_STB[1:0] differential pairs. There is no length match requirement between the data signals.

4.4.2.2 Strobe Signals

The hub interface strobe signals should be routed 5 mil wide with 20 mil trace spacing (5 on 20). This strobe pair should have a minimum of 20 mil spacing from any adjacent signals. The minimum trace length for the strobe signals is 4.5”. The maximum length for the strobe signals is 16”. The lengths for all of the strobe signals, HLB_STB0, HLB_STB0#, HLB_STB1 and HLB_STB1#, should be matched.

4.4.2.3 Hub Interface B HUBREF Generation/Distribution

HUBREF is the hub interface reference voltage and should be 2/3 VCC1_8 ±2%. This reference voltage can be generated locally or with a single HUBREF divider circuit. HBREF divider circuit examples are shown in Figure 4-30 and Figure 4-31.

Figure 4-30. 16-Bit Hub Interface with a Shared Reference Divider Circuit

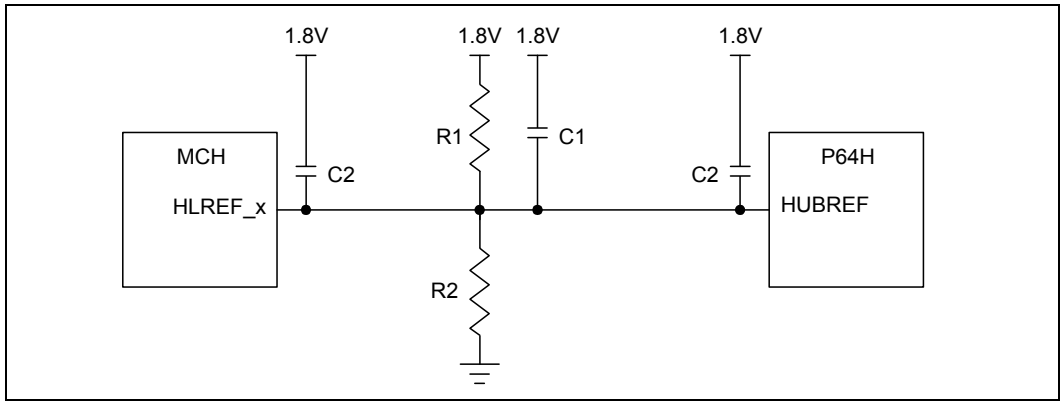
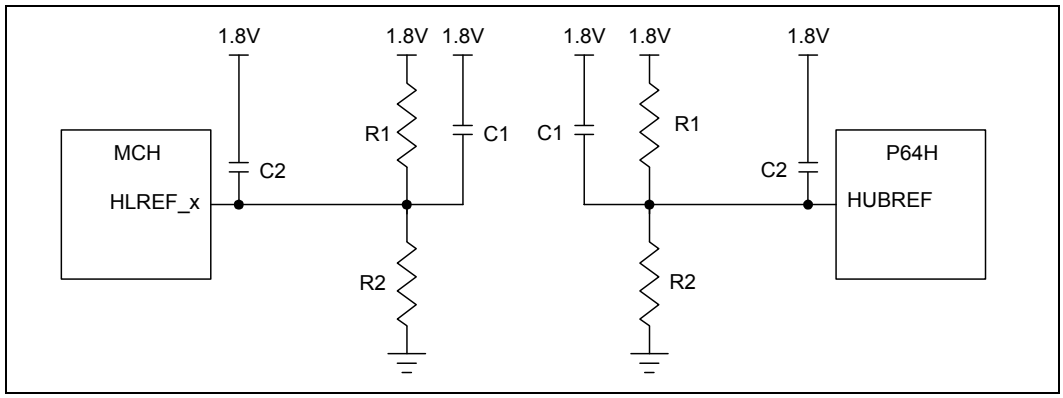


Figure 4-31. 16-Bit Hub Interface with Locally Generated Reference Divider Circuits



The resistor values, R1 and R2, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. A 0.1 uF capacitor (C1 in the above circuits) should be placed close to R1 and R2. Also, a 0.01 uF bypass capacitor (C2 in the above circuits) should be placed within 0.5 inches of each HUBREF pin.

It is recommended that the trace length from the divider circuit to the HLBREF pin be no longer than 3.5”. If more than a 3.5” trace length is necessary from either the P64H or the MCH, then it is recommended that the locally generated reference divider circuits be used instead of the shared reference divider circuit.

4.4.2.4 HLB_RCOMP Signal

HLB_RCOMP is used by the P64H to adjust the buffer characteristics to specific board characteristics. The HLB compensation requires Resistive Compensation (RCOMP).

- RCOMP: Tie the HLB_COMP pins to a 30 Ω 1% pull-down resistor to GND. This can done via a 10 mil wide trace and short (~0.5") trace.

The MCH hub interface compensation for hub interface B must use the same compensation method (RCOMP).

4.4.2.5 P64H 1.8V Decoupling

The P64H component can create current transients through the 1.8V pins upwards of ~500 mA/ns. To satisfy these power transients close attention to the 1.8V power distribution must be applied. A low inductive path to the P64H 1.8V balls and proper plane decoupling is critical.

It is recommended that a solid 1.8V plane be powered from the 1.8V source to the P64H. The width of this plane (ideally as wide as the hub interface ball quadrant) should be sufficient to supply current to the P64H under the maximum current conditions mentioned earlier. Ideally this plane should be placed above the core of the board stackup (closest to the component side). This 1.8V plane should be referenced to GND (<7 mils separation between 1.8V and GND) to optimize the mutual inductance between the two planes. This mutual inductance will help cancel out self inductance from the power balls on the package to the decoupling capacitors. If it is not possible to create these parallel planes, the decoupling recommended below needs to be enhanced and backside assembly should be considered for the high frequency capacitors. A minimum of 1 via per 1.8V P64H ball should be used to connect the P64H balls to this 1.8V plane.

It is recommended that three low ESR 0.1 uF capacitors (e.g., 0603 X7R) be placed close to the P64H on the 1.8V plane for high frequency decoupling. These capacitors should be placed as close as manufacturing tolerances allow to the edge of the P64H package. Bulk decoupling capacitors should also be placed near the P64H if the power supply is not located close enough to maintain proper power to the P64H component. It is recommended that bulk decoupling (>10 uF) needs to be provided within 2 inches of the P64H.

4.4.2.6 Unused Hub Interface B

If the hub interface B is not used, all HLB signals except the MCH HUBREF and HLBRCOMP can be left as no connect on the Intel® 840 chipset MCH. The 2/3 Vterm must still be applied to HUBREF if hub interface B is not used. Also a 30 Ω±1% pulled-down resistor to GND is required on HLBRCOMP. When the Intel® 840 chipset MCH detects that the P64H is not present, it will internally maintain the HLB signals at a "High" state and disable the PCI-to-PCI bridge for the hub interface B (MCH device 2).

4.5 Ultra ATA/66

This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels.

The ICH has two independent IDE channels. The ICH has integrated the 33 Ω series resistors that are typically required on the IDE data signals, running to the two ATA connectors. The IDE interface can be routed with 5 mil traces on 5 mil spaces, but must be less than 8 inches long (from ICH to IDE connector). Per each IDE channel, the difference between the shortest and longest signal must not be greater than 0.5”.

4.5.1 Cable Requirement

A new IDE cable is required for Ultra ATA/66. This cable is an 80-pin conductor cable; however the 40-pin connectors do not change. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground… All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the Small Form Factor Specification SFF-8049. This specification can be obtained from the Small Form Factor Committee.

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6” away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the motherboard ground and hard disk drives.
- **ICH Placement:** The ICH must be placed equal to OR less than 8” from the ATA connector(s).
- **PC99 requirement:** Support Cable Select for master-slave configuration. CSEL signal needs to be pulled down at the host side by using a 470 Ω pull-down resistor for each ATA connector.

4.5.2 Ultra ATA/66 Cable Detection

The ICH supports many Ultra DMA modes including ATA/66. The ICH needs to determine the installed IDE device mode and the type of cable to configure its own hardware and software to support it.

To determine if ATA/66 mode can be enabled, the Intel® 840 chipset requires the system BIOS to determine the cable type used in the system. There are two methods for the BIOS:

- Host Side Detection
- Device Side Detection

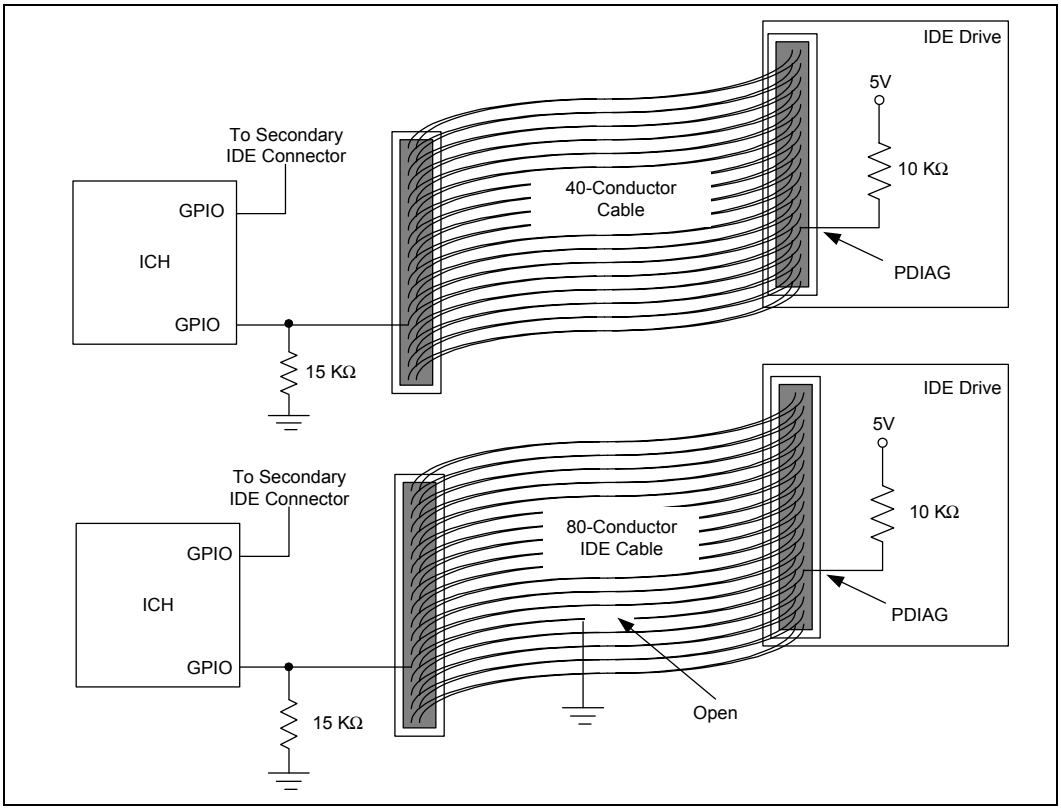
If the BIOS detects an 80-conductor cable, it may use with any Ultra DMA mode up to the highest transfer mode supported by both the ICH and the IDE device. Otherwise, the BIOS will only enable modes that do not require an 80-conductor cable (i.e., Ultra ATA/33 Mode). After the BIOS determines the Ultra ATA mode, the BIOS will configure the ICH hardware and software to match the selected mode.

4.5.2.1 Host Side Detection—BIOS Detects Cable Type Using GPIOs

Host side detection requires the use of two GPI pins (1 per IDE controller). The proper way to connect the PDIAG/CBLID signal of the IDE connector to the host is shown in Figure 4-32. Most of the ICH GPIO and all FWH Flash BIOS GPIs are not 5 volt tolerant. Since all IDE devices have a 10 KΩ pull-up resistor to 5 volts, a resistor divider circuit is needed to protect ICH and FWH Flash BIOS from 5V signaling. One suggestion, a 10 KΩ / 15 KΩ resistor divider circuit will produce approximately 3 volts for a logic high.

This mechanism allows the host, after diagnostics, to sample PDIAG/CBLID. If PDIAG/CBLIB is high, then there is 40-conductor cable in the system and ATA modes 3 and 4 should not be enabled. If PDIAG/CBLID is low, then there is an 80-conductor cable in the system.

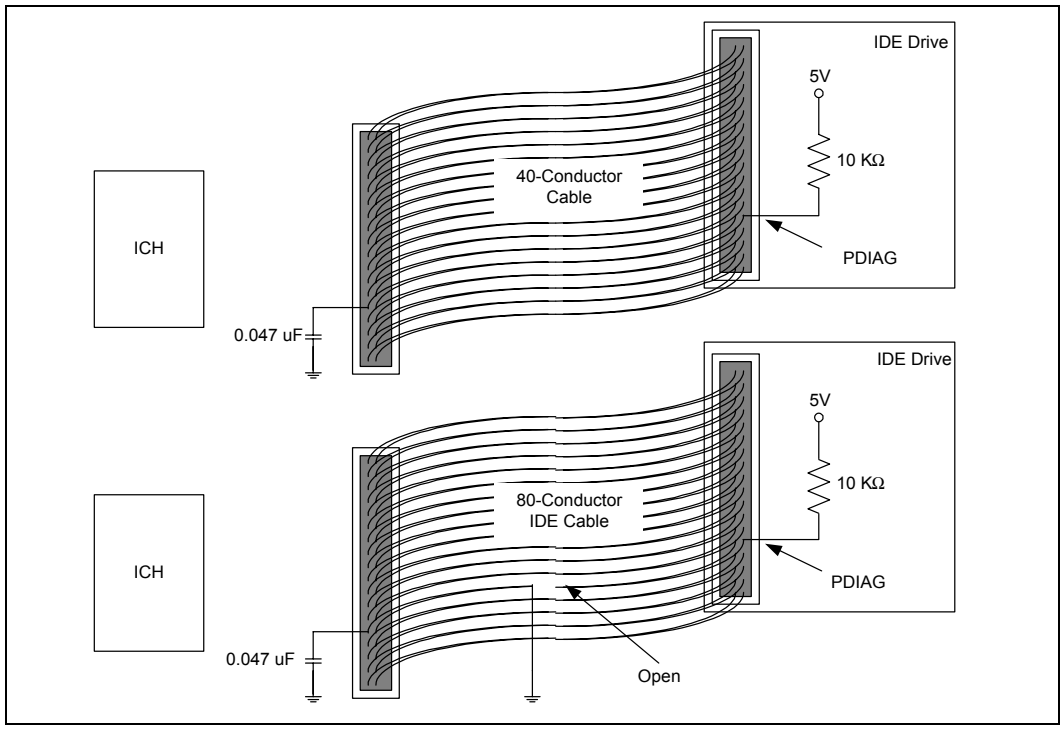
Figure 4-32. Host-side IDE Cable Detection #1



4.5.2.2 Device Side Detection—BIOS Queries IDE Drive for Cable Type

Device side detection requires only a 0.047 uF capacitor on the motherboard as shown in Figure 4-33. This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3 or 4 drive PDIAG/CBLID low and then release it (pulled up through a 10 KΩ resistor). The drive samples the PDIAG signal after releasing it. In an 80-conductor cable, PDIAG/CBLID is not connected; therefore, the capacitor has no effect. In a 40-conductor cable, PDIAG/CBLID is connected to the drive; thus, the signal rises more slowly. The drive can detect the difference in rise times and it reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

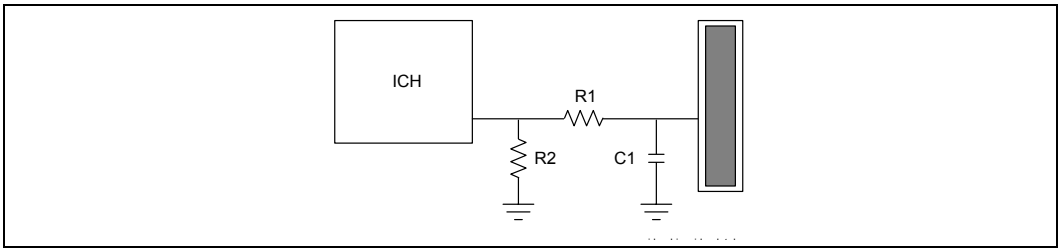
Figure 4-33. Driver-Side IDE Cable Detection #2



4.5.3 Layout for Host Side and Drive Side Cable Detection

- For Host-Side Detection
  - R1 is a 0 Ω resistor
  - R2 is a 15 KΩ resistor
  - C1 is not stuffed
- For Drive-Side Detection
  - R1 is not stuffed
  - R2 is not stuffed
  - C1 is a 0.047 uF capacitor

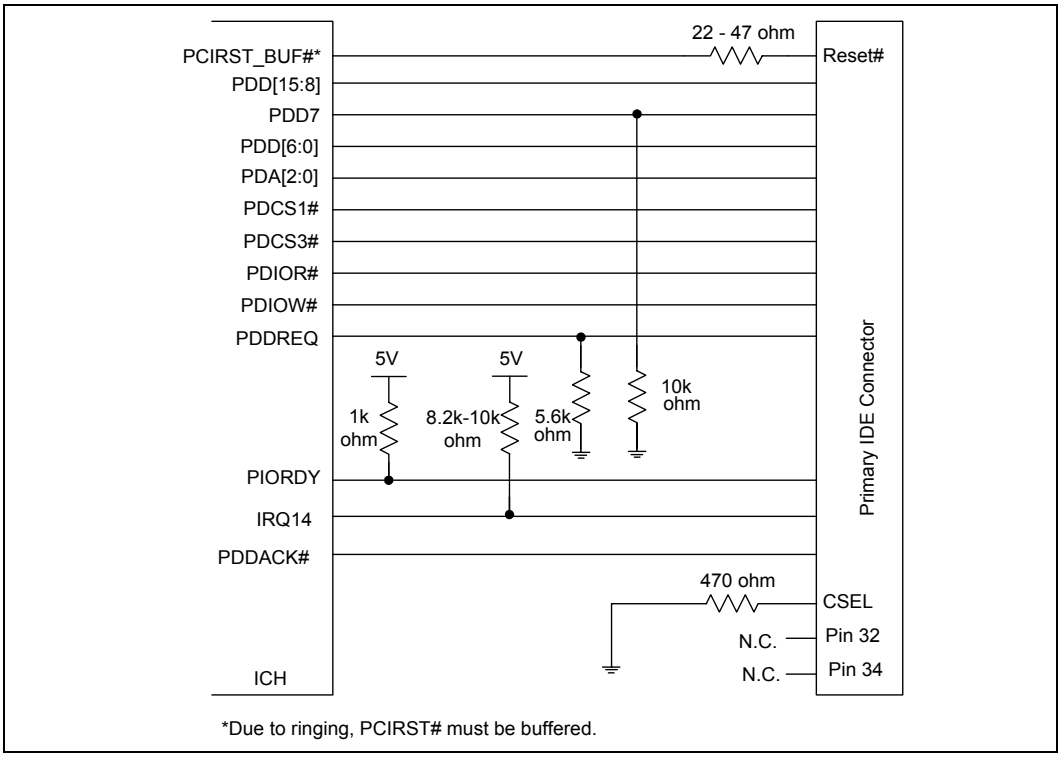
Figure 4-34. Driver Side IDE Detection Layout



4.5.4 Guidelines

- 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- A 8.2 KΩ–10 KΩ pull-up resistor is required on IRQ14 and IRQ15 to VCC5.
- A 10 KΩ pull-down resistor is required on PDD7 and SDD7 (as required by the ATA-4 specification).
- A 5.6 KΩ pull-down resistor is required on PDDREQ# and SDDREQ# (as required by the ATA-4 specification).
- A 1 KΩ pull-up resistor is required on PIORDY and SIORDY (as required by the ATA-4 specification).

Figure 4-35. Resistor Placement for Primary and Secondary IDE Connector



If the IDE interface is not used, the respective xDREQ and xIORDY signals should be grounded and output signals left as no connects. If both of the primary and secondary IDE interfaces are not used, the appropriate ICH bit should also be set to disable the IDE controller.

4.6 AC ’97

The ICH implements an AC’97 2.1 compliant digital controller. Any codec used with the ICH AC-link must be AC’97 2.1 compliant. Contact your codec IHV for information on AC’97 2.1 compliant products. The AC’97 2.1 specification is available on the Intel web site:

http://developer.intel.com/pc-supp/platform/ac97/index.htm

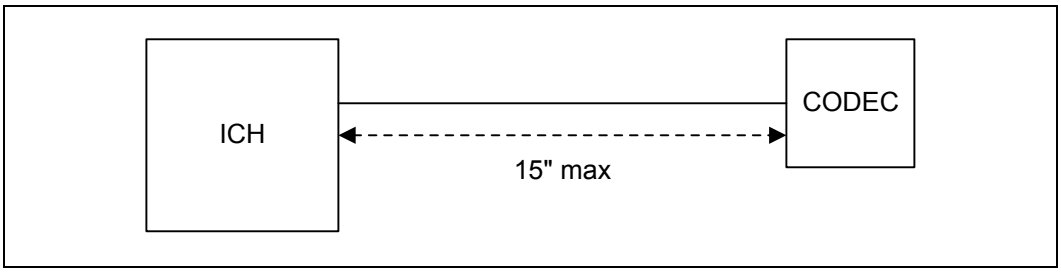
The ICH supports the following CODEC combinations:

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio (AC)	Modem (MC)
Audio/Modem (AMC)	None

As shown in the table, the ICH does not support two codecs of the same type on the link. For example, if an AMC is on the link, it must be the only codec. If an AC is on the link, another AC cannot be present.

4.6.1 AC’97 CODEC-Only

Figure 4-36. CODEC-only Topology Trace Length Requirements



When implementing the codec-only solution, unused SDIN signal must be pulled-down to GND via a weak resistor (~10KΩ).

4.6.2 Audio/Modem Riser Specification

Intel has developed a common connector specification known as the Audio/Modem Riser (AMR). This specification defines a mechanism for allowing OEM to add a plug-in card option. The AMR specification provides a mechanism for AC’97 CODECs to be on a riser card. This is important for modem CODECs as it helps ease international certification of the modem.

For increased part placement flexibility, there are two routing methods for the AC’97 interface: the *tee* topology and the *daisy-chain* topology. The AC’97 interface can be routed using 5 mil traces with 5 mil space between the traces.

Figure 4-37. Tee Topology Trace Length Requirements

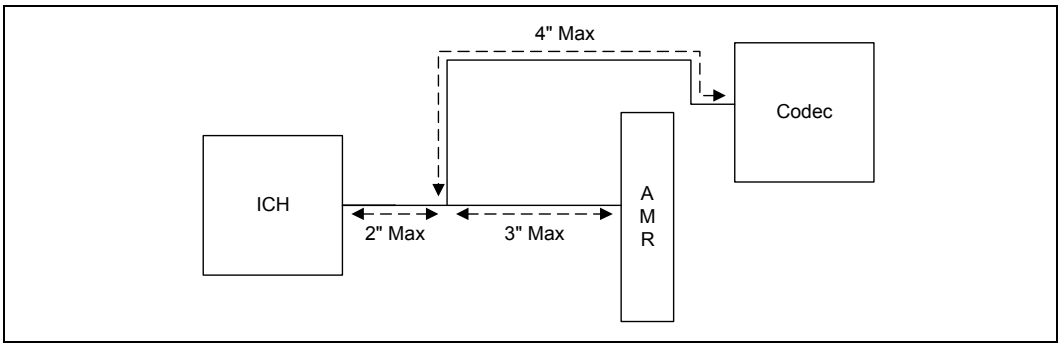
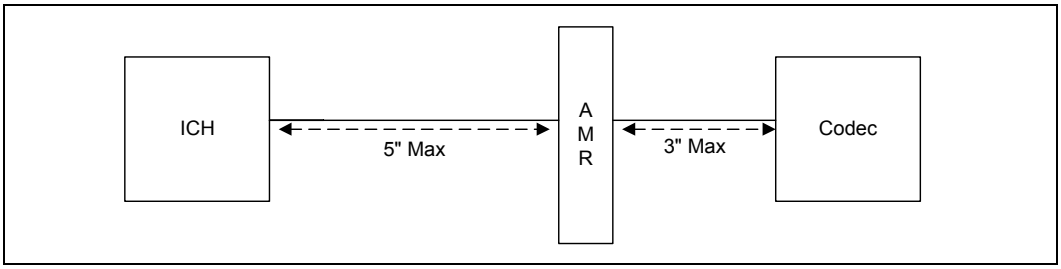


Figure 4-38. Daisy-Chain Topology Trace Length Requirements



Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH), and any other codec present. This clock is used as the time base for latching and driving data.

The ICH supports wake on ring from S1-S4 via the AC'97 link. The codec asserts SDATAIN to wake the system. For wake capability and/or caller ID, standby power must be provided to the modem codec.

There are integrated pull-down resistors on the ICH AC_SDIN0 and AC_SDIN1/GPIO9 signals. The pull-down resistor on these signals is only enabled when the ACLINK Shut Off bit, in the AC'97 Global Control Register (AC'97 I/ O Space) is set to '1'. This prevents the link from floating when the AC-link is "off" or when there is no codec present. Otherwise, the internal pull-down resistor is disabled and an external pull-down resistor is required.

4.6.3 AC'97 Signal Quality Requirements

In a lightly loaded system (e.g., single codec down), AC'97 signal integrity should be evaluated to confirm that the signal quality on the link is acceptable to the codec used in the design. A series resistor at the driver and a capacitor at the codec can be implemented to compensate for any signal integrity issues. The values used are design dependent and should be verified for correct timings. The ICH AC-link output buffers are designed to meet the AC'97 2.1 specification with the specified load of 50 pF.

4.6.4 AC'97 Motherboard Implementation

The following design considerations are provided for the implementation of an ICH0/ICH platform using AC'97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. These recommendations do not represent the only implementation or a complete checklist, but provides recommendations based on the ICH0/ICH platform.

- Codec Implementation
  - The motherboard can implement any valid combination of codecs on the motherboard and on the riser. For ease of homologation, it is recommended that a modem codec be implemented on the AMR module; however, nothing precludes a modem codec on the motherboard.
  - Only one primary codec can be present on the link. A maximum of two present codecs can be supported in an ICH platform.
  - If the motherboard implements an active primary codec on the motherboard and provides an AMR connector, it must tie PRI_DN# to ground.
  - The PRI_DN# pin is provided to indicate a primary codec is present on the motherboard. Therefore, the AMR module and/or codec must provide a means to prevent contention when this signal is asserted by the motherboard, without software intervention.
  - Components such as FET switches, buffers, or logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so will potentially interfere with timing margins and signal integrity.
  - If the motherboard requires that an AMR module override a primary codec down, a means of preventing contention on the AC-link must be provided for the onboard codec.
  - The ICH0/ICH supports Wake On Ring from S1-S4 states via the AC'97 link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. If no codec is attached to the link, internal pulldowns prevents the inputs from floating, therefore external resistors are not required. The ICH does not wake from the S5 state via the AC'97 link.
  - The SDATAIN[0:1] pins should not be left in a floating state if the pins are not connected and the AC-link is active—they should be pulled to ground through a weak (approximately 10 KΩ) pull-down resistor. If the AC-link is disabled (by setting the shut-off bit to 1), then the ICH's internal pull-down resistors are enabled, and thus there is no need for external pull-down resistors. However, if the AC-link is to be active, there should be pull-down resistors *on any SDATAIN signal that has the potential of not being connected to a codec*. For example, if a dedicated audio codec is on the motherboard, and cannot be disabled via a hardware jumper or stuffing option, then its SDATAIN signal does not need a pull-down resistor. If, however, the SDATAIN signal has no codec connected, or is connected to an AMR slot, or is connected to an onboard codec that can be hardware disabled, then the signal should have an external pull-down resistor to ground.

- AMR Slot Special Connections
  - **AUDIO_MUTE#:** No connect on the motherboard.
  - **AUDIO_PWRDN:** No connect on the motherboard. Codecs on the AMR card should implement a powerdown pin, per the AC'97 2.1 specification, to control the amplifier.
  - **MONO_PHONE:** Connect top onboard audio codec if supported.
  - **MONO_OUT/PC_BEEP:** Connect to SPKR output from the ICH0/ICH, or MONO_OUT from onboard codec.
  - **PRIMARY_DN#:** See discussion above.
  - **+5VDUAL/+5VSB:** Connect to VCC5 core on the motherboard, unless adequate power supply is available. An AMR card using this standby/dual supply should not prevent basic operation if this pin is connected to core power.
  - **S/P-DIF_IN:** Connect to ground on the motherboard.
  - **AC_SDATAIN[3:2]:** No connect on the motherboard. The ICH0/ICH supports a maximum of two codecs, which should be attached to SDATAIN[1:0].
  - **AC97_MSTRCLK:** Connect to ground on the motherboard.
- The ICH provides internal weak pulldowns. Therefore, the motherboard does not need to provide discrete pulldown resistors.

PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

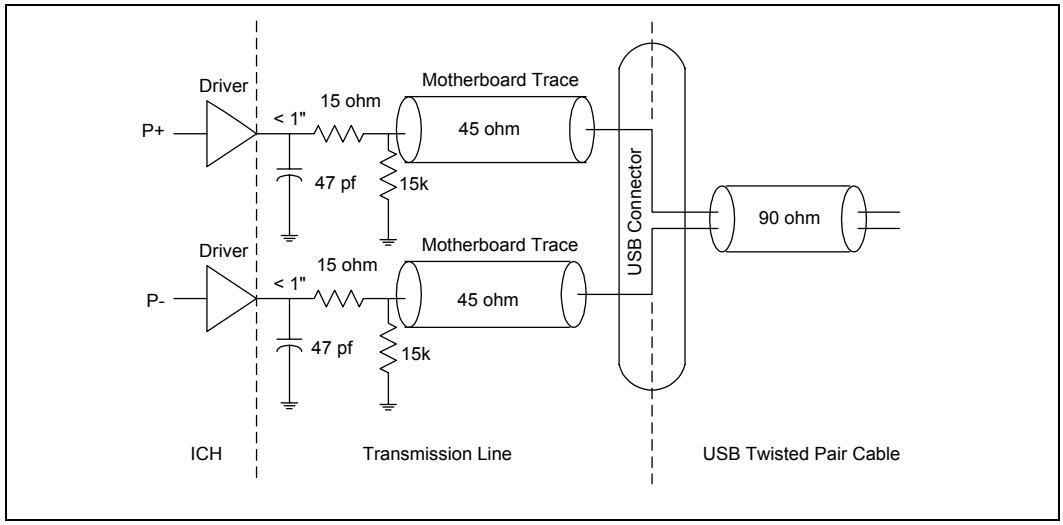
4.7 Universal Serial Bus (USB)

General USB guidelines:

- Unused USB ports should be terminated with 15K pull-down resistors on both P+/P- data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH (<1 inch). These series resistors are there for source termination of the reflected signal.
- 47 pF caps must be placed as close to the ICH as possible and on the ICH side of the series resistors on the USB data lines (P0+/-, P1+/-). These caps are there for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 KΩ ±5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0+/-, P1+/-), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0+/-, P1+/- signals should be 45 Ω (to ground) for each USB signal P+ or P-. Based on the suggested board stack-up (8-layer board stack-up and 60 Ω ±10% board impedance), it required that the traces be 9 mils wide. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90 Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting a 45 Ω impedance. The trace impedance can be controlled by carefully selecting the trace width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as 'critical signals' (i.e., hand routing preferred). The P+/P- signal pair must be routed together and not parallel with other signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent cross-talk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI.

Figure 4-39 illustrates the recommended USB schematic.

Figure 4-39. USB Data Signals



- Recommended USB Trace Characteristics
  - Impedance 'Z0' = 45.4 Ω
  - Line Delay = 160.2 ps
  - Capacitance = 3.5 pF
  - Inductance = 7.3 nH
  - Resistance at 20° C = 53.9 mΩ

4.8 APIC/CMOS Bus

4.8.1 2-way SC242 / Intel® 840 Chipset APIC Bus Layout Guidelines

Intel recommends using in-line topology, as shown in Figure 4-40, for the APIC data signals (PICD[1:0]). The network should have dual-end termination with 330 Ω resistors. The combined routing lengths of L1+L2 should be between 0" and 12.0".

Figure 4-40. PICD[1:0] 2-Way Topology

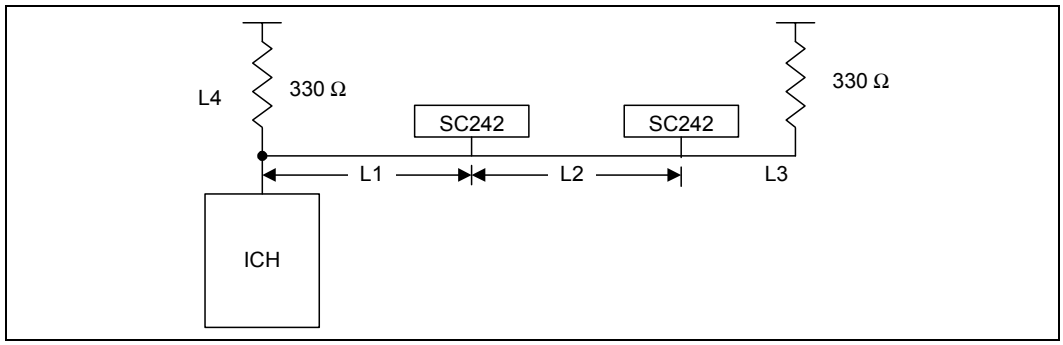


Table 4-12. Segment Lengths for PICD Topology (see Figure 4-40)

Length	Min (inches)	Max (inches)
L1 +L2	0	12
L3 (ICH to resistor stub)	TBD	TBD
L4 (2nd SC242 to resistor stub)	TBD	TBD

Key assumptions:

- The above routing assume Z= 60 Ω±10%.

4.8.2 2-way APIC and CMOS Bus Layout Guidelines for Intel® Pentium® III Xeon™ Processor at 600+ MHz

Figure 4-41 shows the layout guidelines for 2-way Intel® Pentium® III processor and 2-way Intel® Pentium® III Xeon™ processor at 600+ MHz systems based on the Intel 840 chipset. These guidelines are still preliminary, but simulations suggest that this daisy-chain, dual-ended termination topology and corresponding segment lengths will support timing and signal quality requirements for a 16.67 MHz bus frequency. Intel recommends APIC and CMOS bus simulation and good layout practices.

Figure 4-41. PICD[1:0] 2-Way Topology (SC330.1)

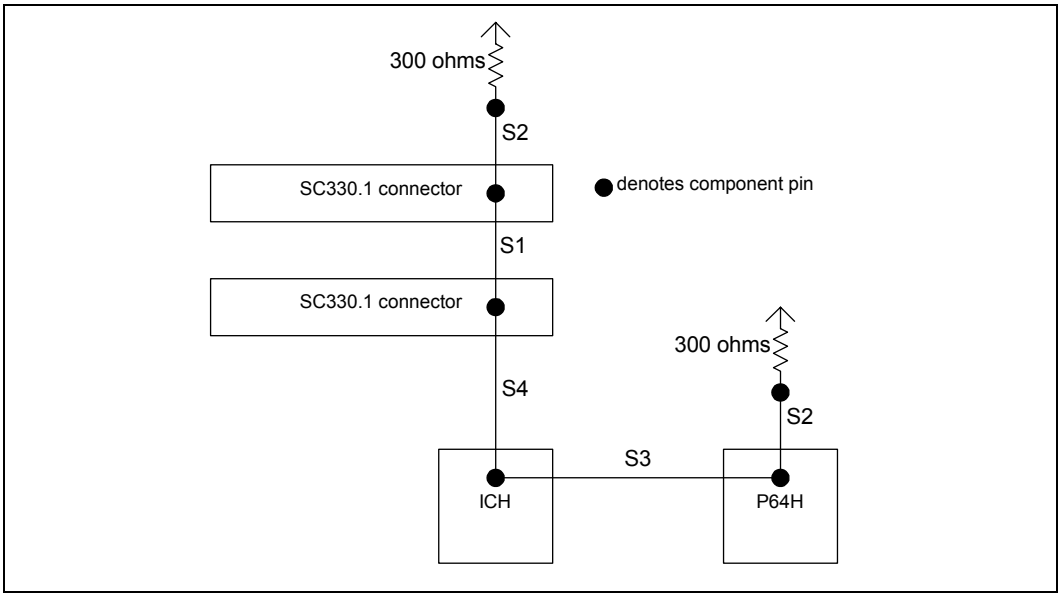


Table 4-13. Segment Lengths for PICD Topology (see Figure 4-41)

Length	Min (inches)	Max (inches)
S1	7	18
S2	0.25	1.0
S3	7	16
S4	9.5”	19.5”

4.8.3 Intel® Pentium® III Xeon™ processor at 600+ MHz APIC Bus Design Considerations

The Intel® Pentium® III Xeon™ processor at 600+ MHz contains a new 2.5V signal specification that involves the CMOS, TAP, and APIC (PICD[1:0]) signals; namely, an I/O capacitance value (Con) of approximately 25 pF max. This max value includes the total capacitance contribution from a voltage clamp added to the Intel® Pentium® III Xeon™ processor at 600+ MHz substrate to help protect the core from overshoot levels. Con does not include cartridge trace capacitance, which is 3 pF/inch. Figure 4-42 summarizes the *Intel® Pentium® III Xeon™ processor at 600+ MHz Datasheet* Con specification.

Figure 4-42. CMOS, TAP, Clock and APIC Signal Groups, DC Specifications at the Processor Core

Symbol	Parameter	Min	Max	Unit	Notes
Con	I/O Pin Capacitance		25	PF	1

NOTE:
1. Total capacitance of processor core and voltage clamp device. Does not include cartridge trace capacitance. Applies to all CMOS, TAP, Clock, and APIC signals except BCLK and PICCLK.

In addition, Intel® Pentium® III Xeon™ processor at 600+ MHz PICD[1:0] Valid Delay timings now differentiate between rising and falling edge transitions as follows:

PICD[1:0] Valid Delay (Rising Edge) = 8.7 ns

PICD[1:0] Valid Delay (Falling Edge) = 12.0 ns

Note: These timings are still specified at the core pin with a 150 Ω resistor load pulled-up to 2.5V. In addition, Intel® Pentium® III Xeon™ processor at 600+ MHz PICD[1:0] Setup Time has been reduced (improved) from 8.0 ns to 5.0 ns.

Note: The processor timings in this section are not official specifications. Reference the appropriate processor datasheet for official processor specifications.

APIC Bus Specification Implications

The additional I/O capacitance associated with the voltage clamp will increase the signal propagation time (compared to a Pentium III Xeon processor system) since the RC time constant of the signal path increases. This increased capacitance will most likely impact the APIC bus since it is synchronous and uses PICCLK (i.e., the increased propagation time may affect receiver setup margin). APIC bus flight time will likely be limited by rising edge transitions since the resistance term used would be the effective pull-up resistance on this signal (assumed to be 150 Ω). The resistance term for falling edges is equal to the core nmos on-resistance plus voltage clamp on-resistance (approximately 25 Ω).

Improvements to the rising edge PICD valid delay spec will provide some relief to the RC propagation delay effects. Also, the improved PICD setup time will provide substantial relief to timing paths where the processor is the receiving agent. However, since APIC behavior is strongly dependent on baseboard layout and APIC components chosen, Intel highly recommends that system designers perform an analysis to better understand the impact of these changes. The following section provides two examples for performing a first-pass timing calculation.

Design Considerations

The following analyses for 2-way Intel® Pentium® III Xeon™ processor at 600+ MHz systems will help determine the impact to various systems and APIC bus topologies.

For APIC bus timing analysis, the system flight time is broken into two components: straight propagation delay (T_{prop}), and delay due to the RC time constant of the bus (T_{RC}). See Equation 4-4. T_{RC} is derived from the effective pull-up resistance and the total system capacitance. Nevertheless, this simple analysis is meant as a starting point for understanding capacitance loading effects and should be reinforced by APIC bus simulations.

Equation 4-4. Total System Flight Time

$$T_{system} = T_{prop} + T_{RC}$$

T_{prop} = (Longest point-to-point distance) * (Worst-case propagation delay)

T_{RC} is derived from solving $V(t) = V(0)e^{-T_{RC}/\tau}$ for T_{RC}.

$T_{RC} = -\tau \ln [V(t)/V(0)]$

$V(0) = 2.5V$ since the signal is terminated to 2.5V.

$V(t) = 1.25V$ since this is the voltage reference used for timings.

$\tau = R_{eff} * C_{total}$ and $C_{total} = C_{T\text{-}line} + C_{CPU}$

2-way Example

Consider a 2-way system with the following APIC bus parameters:

- Total trace routing of 20 inches. This defines the total trace length contribution from all individual trace segments (e.g., processors, termination resistor stubs, SC330.1 connectors, and additional APIC agent routing). This total length already includes two Intel® Pentium® III Xeon™ processor at 600+ MHz cartridges, each with 4 inches (720 ps) total trace between the core and edge finger.
- Longest component point-to-point routing distance of 15 inches.
- Nominal board impedance of 60 Ω
- Worst-case (slowest) propagation delay of 180 ps/inch.
- Transmission line capacitance of 3.0 pF/inch (From the above impedance and propagation delay).
- Effective pull-up resistance of 150 Ω

For this board design:

- T_{prop} = 15 inches * 180 ps/inch = 2.70 ns
- $C_{T\text{-}line}$ = 20 inches * 3 pF/inch = 60 pF
- C_{CPU} = 2 processors * 25 pF = 50 pF
- C_{total} = 60 pF + 50 pF = 110 pF
- τ = 150 Ω * 110 pF = 16.5 ns
- T_{RC} = 11.4 ns
- T_{system} = 2.70 ns + 11.4 ns = 14.1 ns

Using the simple timing equation below (with driver T_{co}, T_{system}, and receiver T_{setup}), this system shows margin running at 33.33 MHz (30.0 ns period). This timing equation specifically applies to the processor-to-processor flight path. Timing analysis involving additional APIC agents requires using their appropriate timing parameters in the timing equation below. Note that clock skew and jitter effects must still be considered.

$$T_{co} + T_{system} + T_{setup} = T_{period}$$

8.7 ns + 14.1 ns + 5.0 ns = 27.8 ns

Margin to 33.33 MHz = 30 ns – 27.8 ns = 2.2 ns

4.8.4 ICH I/O APIC

If the ICH I/O APIC is not used, PICCLK must still be connected to the processor. The processor PICD[1:0] must be pulled-up with a 10 KΩ resistor to 2.5V.

4.8.5 P64H I/O APIC

If the P64H I/OAPIC is not used, entries for this I/O APIC should not be reported in the MP Table. Section 4.3.4 of the *Multi-Processor (MP) Specification* has the format for the INTIN line entry and Appendix #D of this specification contains the format of the PCI IRQ entries (i.e., Device #, function # and bus # based and INT[D:A] that have to be reported when INTIN line is used. Reference the Multi-Processor Specification for complete details.

External pull-up resistors should be placed on all unused IRQ, APICD[1:0] and APICCLK signals.

4.9 Low Pin Count Interface (LPC) / FWH Flash BIOS

4.9.1 In Circuit FWH Flash BIOS Programming

All cycles destined for the FWH Flash BIOS will appear on PCI. The ICH hub interface to PCI Bridge will put all processor boot cycles out on PCI (before sending them out on the FWH Flash BIOS interface). If the ICH is set for subtractive decode, these boot cycles can be accepted by a positive decode agent out on PCI. This enables the ability to boot from of a PCI card that positively decodes these memory cycles. If a PCI boot card is inserted and the ICH is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot off a ROM behind the 82380AB/AC. Once you have booted from the PCI card, you could potentially program the FWH Flash BIOS in circuit and program the ICH CMOS.

4.9.2 FWH Flash BIOS Vpp Design Guidelines

The Vpp pin on the FWH Flash BIOS is used for programming the flash cells. The FWH Flash BIOS supports Vpp of 3.3V or 12V. If Vpp is 12V, the flash cells will program about 50% faster that at 3.3V. However, the FWH Flash BIOS only supports 12V Vpp for 80 hours. The 12V Vpp is useful in a programmer environment. The Vpp pin on the FWH Flash BIOS needs to be tied to 3.3V for normal operation.

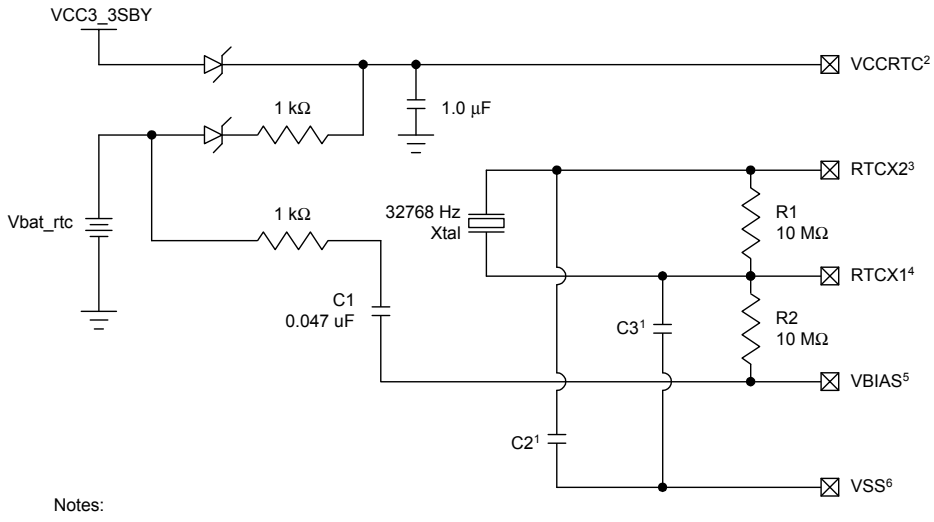
4.10 RTC

The ICH contains a real time clock (RTC) with 256 bytes of battery backed SRAM. This internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down. The RTC also maintains the CMOS memory used by the BIOS, and a backup battery to keep the clock running and the CMOS fresh when the PC is switched off.

4.10.1 RTC Crystal

The ICH RTC module requires an external oscillating source of 32.768 KHz connected on the RTCX1 and RTCX2 pins. Figure 4-43 represents the external circuitry that comprises the oscillator of the ICH RTC.

Figure 4-43. External Circuitry for ICH RTC



Notes:

1. The exact capacitor value needs to be based on what the crystal maker recommends.
2. VccRTC: Power for RTC Well.
3. RTCX2: Crystal Input 2 — Connect to the 32.768 KHz crystal.
4. RTCX1: Crystal Input 1 — Connect to the 32.768 KHz crystal.
5. VBIAS: RTC BIAS Voltage — This pin is used to provide a reference voltage; this DC voltage sets a current which is mirrored throughout the oscillator and buffer circuitry.
6. Vss: Ground.

4.10.2 External Capacitors

To maintain the RTC accuracy, the external capacitor C1 must be set to 0.047 uF and the external capacitor values (C2 and C3) should be chosen to support the manufacturer's specified load capacitance (C_{load}) for the crystal. The values should also account for C_{load} with parasitic capacitance of the trace, socket (if used), and package. By adding the external capacitor values with the capacitance of the trace, socket, and package, the capacitor value will be better matched to the actual load capacitance of the crystal used.

The following equation can be used to choose the external capacitance values (C2 and C3):

$$Cload = (C2^{*} C3)/(C2+C3) + Cparasitic$$

C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain the 32.768 kHz.

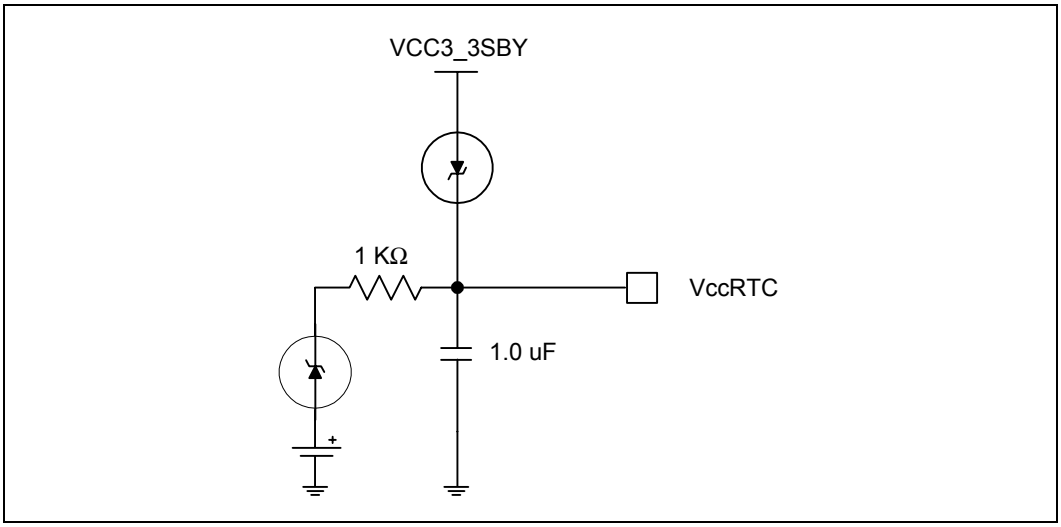
4.10.3 RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH is not powered by the system. Example batteries are the Duracell* 2032, 2025, or 2016 (or equivalent). Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 uA, the battery life will be at least: 170,000 uAh / 3 uA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0V to 3.3V.

The battery must be connected to the ICH via an isolation diode circuit. The diode circuit allows the ICH RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 4-44 is an example of a diode circuitry that can be used.

Figure 4-44. A Diode Circuit to Connect RTC External Battery



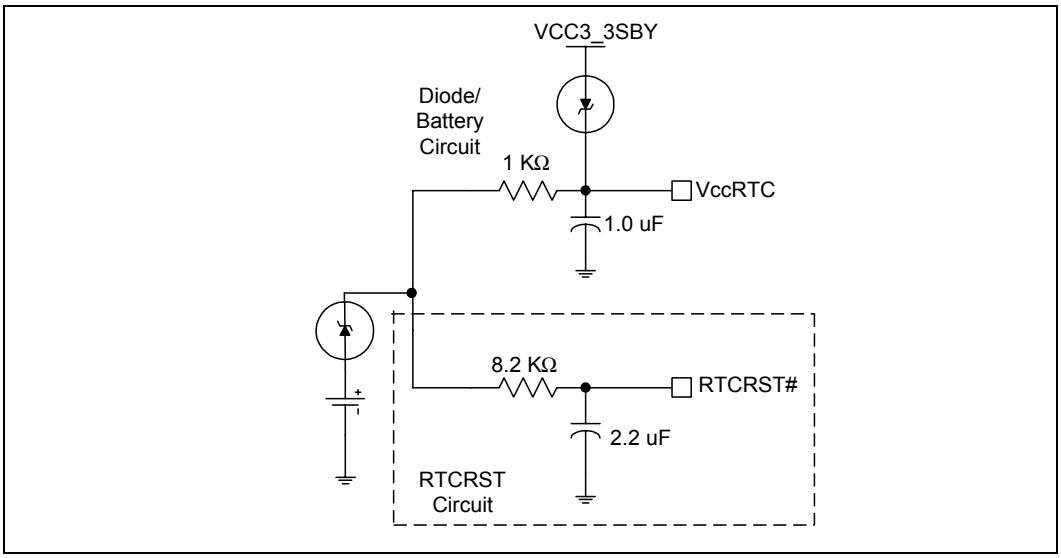
A standby power supply should be to provide continuous power to the RTC when available. This will significantly increase the RTC battery life and the RTC accuracy.

4.10.4 RTC External RTCRST Circuit

The ICH RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC Well. The external capacitor (2.2 uF), external resistor (8.2 KΩ) and the RTC battery (Vbat) were selected to create a RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10-20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains '1' until software clears it. As a result of this, when the system boots, the BIOS will know if the RTC battery has been removed.

This RTCRST circuit is combined with the diode circuit which allows RTC-well to be powered by the battery when the system power is not available.

Figure 4-45. RTCRST External Circuit for the ICH RTC



4.10.5 VBIAS Clarification

RTC Routing Guidelines

All RTC OSC signals (RTCX1, RTCX2, and VBIAS) should all be routed with trace lengths of less than 1". It is recommended to minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them), and place a ground plane under all of the external RTC circuitry. Do not route any switching signals under the external components (unless on the other side of the ground plane).

VBIAS DC Voltage and Noise Measurements

Steady state VBIAS will be a DC voltage of about 0.38V ±0.06V. VBIAS will be "kicked" when the battery is inserted to about 0.7-1.0V, but it will come back to its DC value within a few ms.

Excess noise on VBIAS can cause the ICH internal oscillator to misbehave or even stop completely. Therefore it is important to minimize the noise, to 200mV or less, on VBIAS. To minimize noise of VBIAS, implement the above routing guidelines and the external RTC circuitry described in the ICH datasheet.

Note: VBIAS is very sensitive and cannot be directly probed. It can be probed through a 0.01 uF capacitor.

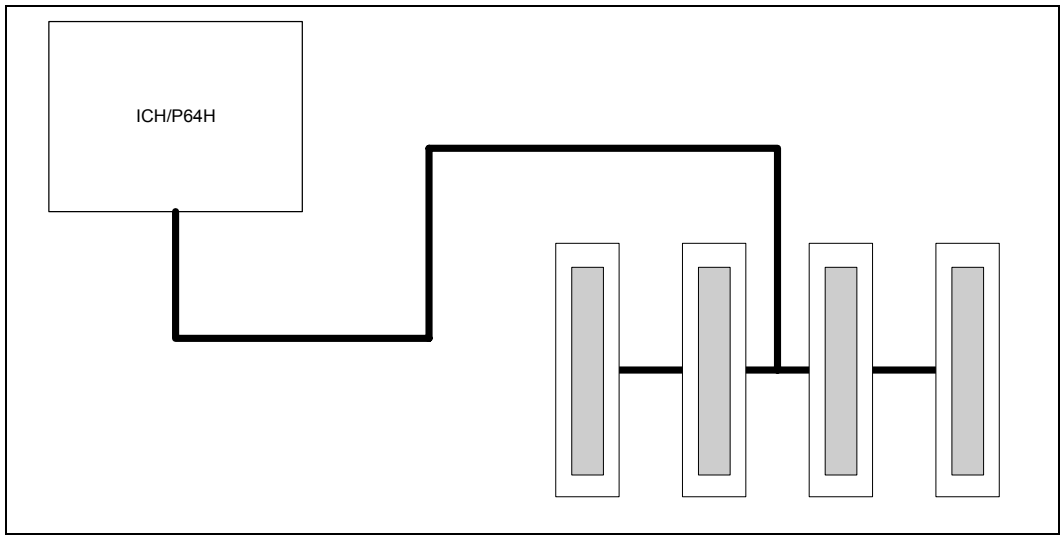
4.11 PCI

The Intel® 840 chipset offers support for both 33 MHz and 66 MHz PCI operations. The ICH supports 33 MHz while the P64H supports both 33/66 MHz PCI operations. The ICH and P64H each provide 6 pairs of REQ#/GNT# signals, supporting 6 PCI masters. In addition, the ICH supports 2 PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

4.11.1 PCI 33 MHz Guidelines

The ICH and P64H both provide PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. Their implementation is optimized for high-performance data streaming when either ICH or P64H is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

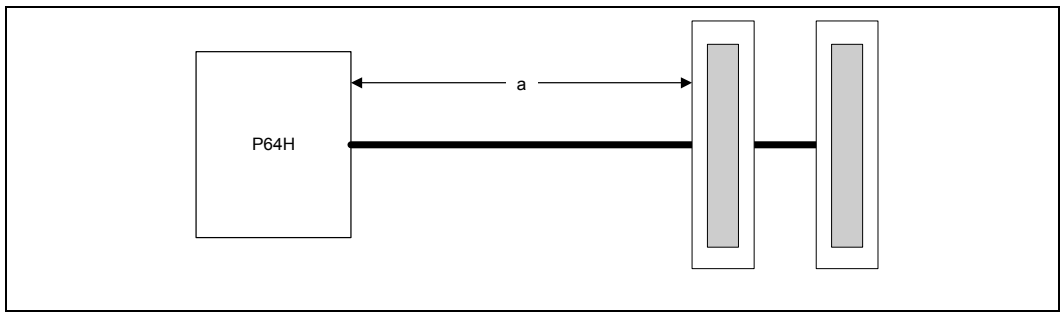
Figure 4-46. PCI 33 MHz Bus Layout Example



4.11.2 PCI 66 MHz Guidelines

The P64H provides PCI Bus interface that is compliant with *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the P64H is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Revision 2.2*.

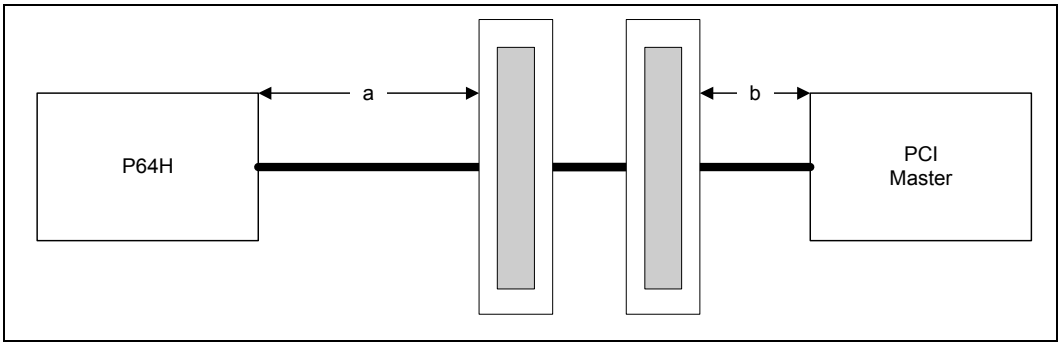
Figure 4-47. PCI 66 MHz- 2 Slots Only



All of the PCI 66 MHz signals can be routed using 5 mil traces with 7 mil spacing between the traces. The following guidelines apply to Figure 4-47:

- (a) P64H to 1st 66 MHz slot connector length: a ≤ 13”
- The typical spacing between PCI connectors is 0.8”

Figure 4-48. PCI 66 MHz-2 Slots w/ 1 Device Down



All of the PCI 66 MHz signals can be routed using 5 mil traces with 7 mil spacing between the traces. The following guidelines apply to Figure 4-48:

- (a) P64H to 1st 66 MHz slot connector length: 0” ≤ a ≤ 6”
- (b) 2nd 66 MHz slot to PCI device down length: 1” ≤ b ≤ 5”
- The typical spacing between PCI connectors is 0.8”

5

System Bus: AGTL+ Design Guidelines

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System Bus: AGTL+ Design Guidelines5

5.1 Methodology

Analog simulations are recommended for high speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working "solution space" that meets flight time and signal quality requirements. The layout recommendations in the previous sections are based on pre-layout simulations conducted at Intel. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulation can be reduced.

Intel recommends running simulations at the **device pads** for signal quality and at the **device pins** for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

Pre-layout analysis includes a sensitivity analysis using parametric sweeps. Parametric sweep analysis involves varying one or two system parameters while all others such as driver strength, package, Z_0, and S_0 are held constant. This way, the sensitivity of the proposed bus topology to varying parameters can be analyzed systematically. Sensitivity of the bus to minimum flight time, maximum flight time, and signal quality should be covered. Suggested sweep parameters include trace lengths, termination resistor values, and any other factors that may affect flight time, signal quality, and feasibility of layout. Minimum flight time and worst signal quality are typically analyzed using fast I/O buffers and interconnect. Maximum flight time is typically analyzed using slow I/O buffers and slow interconnects.

Outputs from each sweep should be analyzed to determine which regions meet timing and signal quality specifications. To establish the working solution space, find the common space across all the sweeps that result in passing timing and signal quality. The solution space should allow enough design flexibility for a feasible, cost-effective layout.

5.2 Simulation Criteria

Accurate simulations require that the actual range of parameters be used in the simulations. Intel has consistently measured the cross-sectional resistivity of the PCB copper to be approximately 1 ohm*mil^2/inch, not the 0.662 ohm*mil^2/inch value for annealed copper that is published in reference material. Using the 1 ohm*mil^2/inch value may increase the accuracy of lossy simulations.

Positioning drivers with faster edges closer to the middle of the network typically results in more noise than positioning them towards the ends. However, Intel has shown that drivers located in all positions (given appropriate variations in the other network parameters) can generate the worst-case noise margin. Therefore, Intel recommends simulating the networks from all driver locations, and analyzing each receiver for each possible driver.

Analysis has shown that **both fast and slow corner conditions** must be run for both rising and falling edge transitions. The fast corner is needed because the fast edge rate creates the most noise. The slow corner is needed because the buffer's drive capability will be a minimum, causing the V_{OL} to shift up, which may cause the noise from the slower edge to exceed the available budget. Slow corner models may produce minimum flight time violations on rising edges if the transition starts from a higher V_{OL}. So, Intel **highly recommends** checking for minimum and maximum

flight time violations with both the fast and slow corner models. The fast and slow corner I/O buffer models are contained in the processor and Intel 840 chipset electronic models provided by Intel.

The transmission line package models must be inserted between the output of the buffer and the net it is driving. Likewise, the package model must also be placed between a net and the input of a receiver model. Editing the simulator's net description or topology file generally does this.

Intel has found wide variation in noise margins when varying the stub impedance and the PCB's Z_0 and S_0. Intel therefore recommends that PCB parameters are controlled as tightly as possible, with a sampling of the allowable Z_0 and S_0 simulated. The Pentium® III processor nominal effective line Impedance is 60 Ω±15%. Intel recommends the baseboard nominal effective line impedance to be at 60 Ω±15% for the recommended layout guidelines to be effective. Intel also recommends running uncoupled simulations using the Z_0 of the package stubs; and performing fully coupled simulations if increased accuracy is needed or desired. Accounting for cross-talk within the device package by varying the stub impedance was investigated and was not found to be sufficiently accurate. This lead to the development of full package models for the component packages.

5.3 Place and Route Board

5.3.1 Estimate Component to Component Spacing for AGTL+ Signals

Estimate the number of layers that will be required. Then determine the expected interconnect distances between each of the components on the AGTL+ bus. Using the estimated interconnect distances, verify that the placement can support the system timing requirements.

The required bus frequency and the maximum flight time propagation delay on the PCB determine the maximum network length between the bus agents. The minimum network length is independent of the required bus frequency. Table 5-1 assumes values for CLK_{SKEW} and CLK_{JITTER} - parameters that are controlled by the system designer. In order to reduce system clock skew to a minimum, clock buffers that allow their outputs to be tied together are recommended. Intel strongly recommends running analog simulations to ensure that each design has adequate noise and timing margin.

5.3.2 Layout and Route Board

Route the board satisfying the estimated space and timing requirements. Also stay within the solution space set from the pre-layout sweeps. Estimate the printed circuit board parameters from the placement and other information including the following general guidelines:

- Distribute V_{TT} with a power plane or a partial power plane. If this cannot be accomplished, use as wide a trace as possible and route the V_{TT} trace with the same topology as the AGTL+ traces.
- Keep the overall length of the bus as short as possible (but don't forget minimum component-to-component distances to meet hold times).
- Plan to minimize cross-talk with the following guidelines developed for the example topology given (signal spacing recommendations were based on fully coupled simulations - spacing may be decreased based upon the amount of coupled length):
  - Use a spacing to line width to dielectric thickness ratio of at least 3:1:2. If $\varepsilon_r = 4.5$, this should limit coupling to 3.4%.
  - Minimize the dielectric process variation used in the PCB fabrication.
  - Eliminate parallel traces between layers not separated by a power or ground plane.

Table 5-1 contains the trace width:space ratios assumed for this topology. The cross-talk cases considered in this guideline involve three types: Intragroup AGTL+, Intergroup AGTL+, and AGTL+ to non-AGTL+. Intra-group AGTL+ cross-talk involves interference between AGTL+ signals within the same group (See section 4.4.1 for a description of the different AGTL+ group types). Intergroup AGTL+ cross-talk involves interference from AGTL+ signals in a particular group to AGTL+ signals in a different group. An example of AGTL+ to non-AGTL+ cross-talk is when CMOS and AGTL+ signals interfere with each other.

Table 5-1. Trace Width:Space Guidelines

Cross-talk Type	Trace Width:Space Ratio
Intragroup AGTL+ (same group AGTL+)	5:10 or 6:12
Intergroup AGTL+ (different group AGTL+)	5:15 or 6:18
AGTL+ to non-AGTL+	5:20 or 6:24

5.3.3 Post-Layout Simulation

Following layout, extract the interconnect information for the board from the CAD layout tools. Run simulations to verify that the layout meets timing and noise requirements. A small amount of "tuning" may be required; experience at Intel has shown that sensitivity analysis dramatically reduces the amount of tuning required. The post layout simulations should take into account the expected variation for all interconnect parameters.

Intel specifies signal integrity **at the device pads** and therefore recommends running simulations at the device pads for signal quality. However, Intel specifies core timings **at the device pins,** so simulation results at the device pins should be used later to correlate simulation performance against actual system measurements.

5.3.3.1 Intersymbol Interference

Intersymbol Interference (ISI) refers to the distortion or change in the waveform shape caused by the voltage and transient energy on the network when the driver begins its next transition.

Intersymbol Interference (ISI) occurs when transitions in the current cycle interfere with transitions in subsequent cycles. ISI can occur when the line is driven high, low, and then high in consecutive cycles (the opposite case is also valid). When the driver drives high on the first cycle and low on the second cycle, the signal may not settle to the minimum V_{OL} before the next rising edge is driven. This results in improved flight times in the third cycle. Intel performed ISI simulations for the topology given in this section by comparing flight times for the first and third cycle. ISI effects do not necessarily span only 3 cycles so it may be necessary to simulate beyond 3 cycles for certain designs. After simulating and quantifying ISI effects, adjust the timing budget accordingly to take these conditions into consideration.

5.3.3.2 Cross-Talk Analysis

AGTL+ cross-talk simulations can consider the processor core package, Intel 840 MCH package, and SC242 connectors as non-coupled. Treat the traces on the processor cartridge and baseboard as fully coupled for maximum cross-talk conditions. Simulate the traces as lossless for worst case cross-talk and lossy where more accuracy is needed. Evaluate both odd and even mode cross-talk conditions. AGTL+ Cross-talk simulation involves the following cases:

- Intra-group AGTL+ cross-talk
- Inter-group AGTL+ cross-talk
- Non-AGTL+ to AGTL+ cross-talk

5.3.3.3 Monte Carlo Analysis

Perform a Monte Carlo analysis on the extracted baseboard. Vary all parameters recommended for the pre-layout Monte Carlo analysis within the region that they are expected to vary. The range for some parameters will be reduced compared to the pre-layout simulations. For example, baseboard lengths L1 through L7 should no longer vary across the full min and max range on the final baseboard design. Instead, baseboard lengths should now have an actual route, with a length tolerance specified by the baseboard fabrication manufacturer.

5.3.4 Validation

Build systems and validate the design and simulation assumptions.

5.3.4.1 Measurements

Note that the AGTL+ specification for signal quality is at the **pad** of the component. The expected method of determining the signal quality is to run analog simulations for the pin and the pad. Then correlate the simulations at the pin against actual system measurements at the pin. Good correlation at the pin leads to confidence that the simulation at the pad is accurate. Controlling the temperature and voltage to correspond to the I/O buffer model extremes should enhance the correlation between simulations and the actual system.

5.3.4.2 Flight Time Simulation

As defined earlier, flight time is the time difference between a signal crossing V_{REF} at the input pin of the receiver, and the output pin of the driver crossing V_{REF} were it driving a ***test load***. The timings in the tables and topologies discussed in this guideline assume the actual system load is 50 and is **equal to the *test load***. While the DC loading of the AGTL+ bus in a DP mode is closer to 25 Ω, AC loading is approximately 29 Ω since the driver effectively "sees" a 56 Ω termination resistor in parallel with a 60 Ω transmission line on the cartridge.

Figure 5-1. Test Load vs. Actual System Load

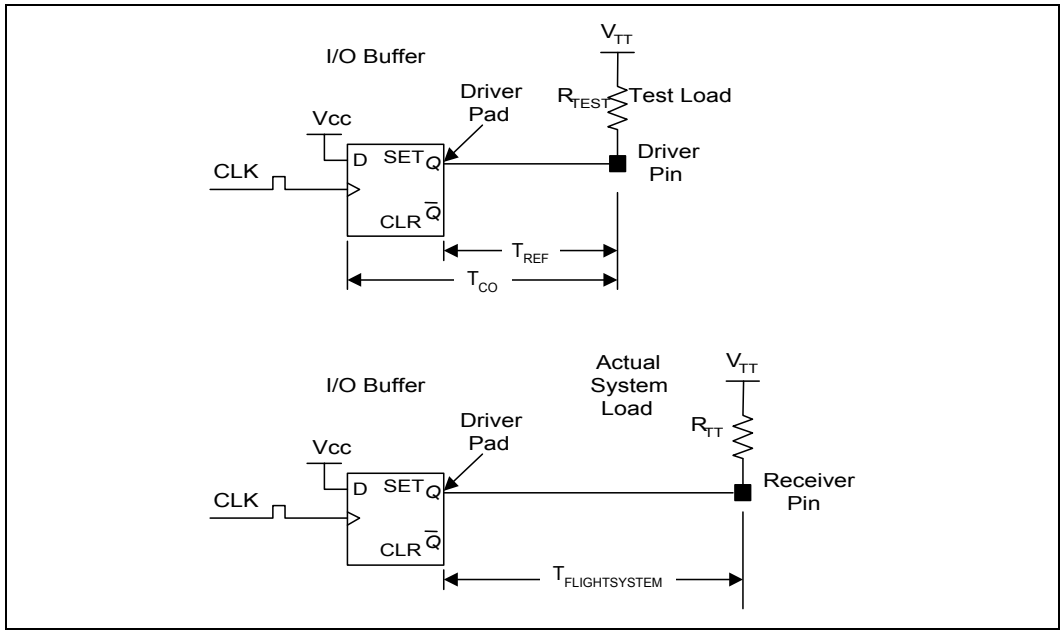


Figure 5-1 shows the different configurations for T_{CO} testing and flight time simulation. The flip-flop represents the logic input and driver stage of a typical AGTL+ I/O buffer. T_{CO} timings are specified at the driver pin output. $T_{FLIGHT\text{-}SYSTEM}$ is usually reported by a simulation tool as the time from the driver pad starting its transition to the time when the receiver's input pin sees a valid data input. Since both timing numbers (T_{CO} and $T_{FLIGHT\text{-}SYSTEM}$) will include propagation time from the pad to the pin, it is necessary to subtract this time (T_{REF}) from the reported flight time to avoid double counting. T_{REF} is defined as the time that it takes for the driver output pin to reach the

measurement voltage, V_{REF}, starting from the beginning of the driver transition at the pad. T_{REF} must be generated using the same test load for T_{CO}. Intel provides this timing value in the AGTL+ I/O buffer models.

In this manner, the following *valid delay* equation is satisfied:

Equation 5-1. Valid Delay Equation

$$\text{Valid Delay} = T_{CO} + T_{FLIGHT\text{-}SYS} - T_{REF} = T_{CO\text{-}MEASURED} + T_{FLIGHT\text{-}MEASURED}$$

This valid delay equation is the total time from when the driver sees a valid clock pulse to the time when the receiver sees a valid data input.

5.4 Theory

5.4.1 AGTL+

AGTL+ is the electrical bus technology used for the processor bus. This is an incident wave switching, open-drain bus with external pull-up resistors that provide both the high logic level and termination at each load. The processor AGTL+ drivers contain a full-cycle active pull-up device to improve system timings. The AGTL+ specification defines:

- Termination voltage (V_{TT}).
- Receiver reference voltage (V_{REF}) as a function of termination voltage (V_{TT}).
- processor termination resistance (R_{TT}).
- Input low voltage (V_{IL}).
- Input high voltage (V_{IH}).
- NMOS on resistance (R_{ONN}).
- PMOS on resistance (R_{ONP}).
- Edge rate specifications.
- Ringback specifications.
- Overshoot/Undershoot specifications.
- Settling Limit.

5.4.2 Timing Requirements

The system timing for AGTL+ is dependent on many things. Each of the following elements combine to determine the maximum and minimum frequency the AGTL+ bus can support:

- The range of timings for each of the agents in the system.
  - Clock to output [T_{CO}]. (Note that the system load is likely to be different from the "specification" load therefore the T_{CO} observed in the system might not be the same as the T_{CO} from the specification.)
  - The minimum required setup time to clock [T_{SU_MIN}] for each receiving agent.
- The range of flight time between each component. This includes:
  - The velocity of propagation for the loaded printed circuit board [S_{EFF}].
  - The board loading impact on the effective T_{CO} in the system.
- The amount of skew and jitter in the system clock generation and distribution.
- Changes in flight time due to cross-talk, noise, and other effects.

5.4.3 Cross-Talk Theory

AGTL+ signals swing across a smaller voltage range and have a correspondingly smaller noise margin than technologies that have traditionally been used in personal computer designs. This requires that designers using AGTL+ be more aware of cross-talk than they may have been in past designs.

Cross-talk is caused through capacitive and inductive coupling between networks. Cross-talk appears as both backward cross-talk and as forward cross-talk. Backward cross-talk creates an induced signal on a victim network that propagates in a direction opposite that of the aggressor's signal. Forward cross-talk creates a signal that propagates in the same direction as the aggressor's signal. On the AGTL+ bus, a driver on the aggressor network is not at the end of the network; therefore it sends signals in both directions on the aggressor's network. Figure 5-2 shows a driver on the aggressor network and a receiver on the victim network that are not at the ends of the network. The signal propagating in each direction causes cross-talk on the victim network.

Figure 5-2. Aggressor and Victim Networks

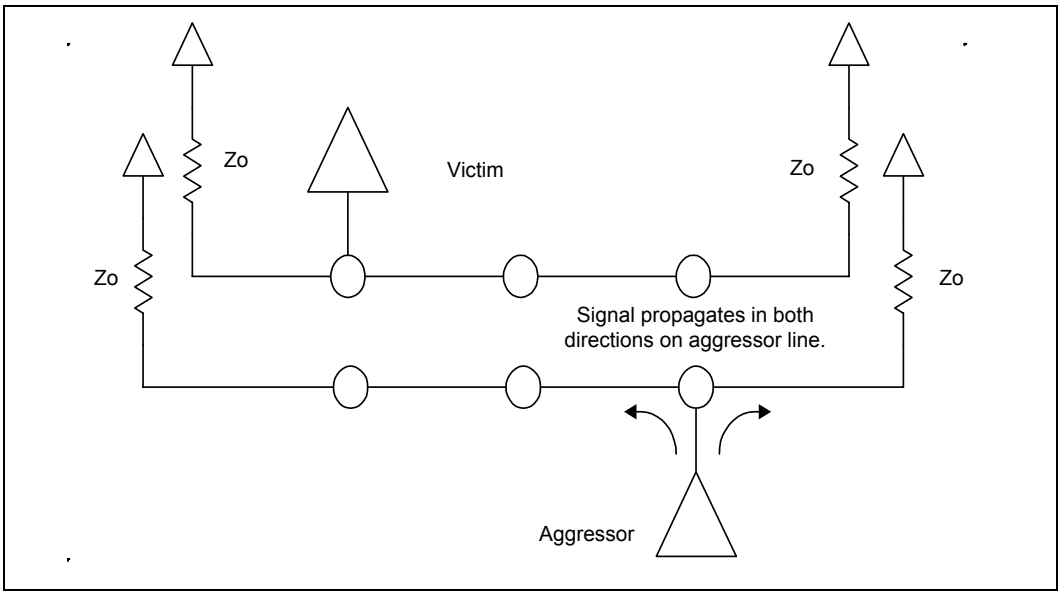
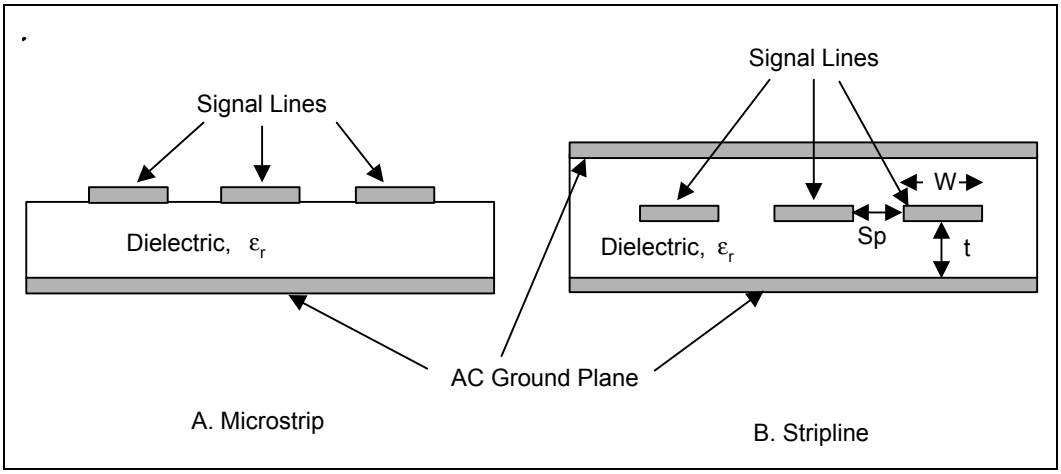


Figure 5-3. Transmission Line Geometry: (A) Microstrip (B) Stripline



Additional aggressors are possible in the z-direction, if adjacent signal layers are not routed in mutually perpendicular directions. Because cross-talk-coupling coefficients decrease rapidly with increasing separation, it is rarely necessary to consider aggressors that are at least five line widths separated from the victim. The maximum cross-talk occurs when all the aggressors are switching in the same direction at the same time. There is cross-talk internal to the IC packages, which can also affect the signal quality.

Backward cross-talk is present in both stripline and microstrip geometry's (see Figure 5-3). A way to remember which geometry is stripline and which is microstrip is that a stripline geometry requires **stripping** a layer away to see the signal lines. The backward coupled amplitude is proportional to the backward cross-talk coefficient, the aggressor's signal amplitude, and the coupled length of the network up to a maximum that is dependent on the rise/fall time of the aggressor's signal. Backward cross-talk reaches a maximum (and remains constant) when the

propagation time on the coupled network length exceeds one half of the rise time of the aggressor's signal. Assuming the ideal ramp on the aggressor from 0% to 100% voltage swing, and the fall time on an unloaded coupled network, then:

$$LengthforMaxBackwardCrosstalk = \frac{\frac{1}{2} \times FallTime}{BoardDelayPerUnitLength}$$

An example calculation if the fast corner fall time is 3 V/ns and board delay is 175 ps/inch (2.1 ns/foot) follows:

Fall time = 1.5 V/3 V/ns = 0.5 ns

Length for Max Backward Cross-talk

= ½ * 0.5 ns * 1000 ps/ns /175 ps/in

= 1.43 inches

Agents on the AGTL+ bus drive signals in each direction on the network. This causes backward cross-talk from segments on two sides of a driver. The pulses from the backward cross-talk travel toward each other and meet and **add** at certain moments and positions on the bus. This can cause the voltage (noise) from cross-talk to double.

5.4.3.1 Potential Termination Cross-Talk Problems

The use of commonly used "pull-up" resistor networks for AGTL+ termination may not be suitable. These networks have a common power or ground pin at the extreme end of the package, shared by 13 to 19 resistors (for 14- and 20-pin components). These packages generally have too much inductance to maintain the voltage/current needed at each resistive load. Intel recommends using discrete resistors, resistor networks with separate power/ground pins for each resistor, or working with a resistor network vendor to obtain resistor networks that have acceptable characteristics.

5.5 More Details and Insights

5.5.1 Textbook Timing Equations

The “textbook” equations used to calculate the propagation rate of a PCB are the basis for spreadsheet calculations for timing margin based on the component parameters. These equations are:

Equation 5-2. Intrinsic Impedance

$$Z_0 = \sqrt{\frac{L_0}{C_0}} \quad (\Omega)$$

Equation 5-3. Stripline Intrinsic Propagation Speed

$$S_{0\_STRIPLINE} = 1.017 * \sqrt{\varepsilon_r} \quad (\text{ns/ft})$$

Equation 5-4. Microstrip Intrinsic Propagation Speed

$$S_{0\_MICROSTRIP} = 1.017 * \sqrt{0.475 * \varepsilon_r + 0.67} \quad (\text{ns/ft})$$

Equation 5-5. Effective Propagation Speed

$$S_{EFF} = S_0 * \sqrt{1 + \frac{C_D}{C_0}} \quad (\text{ns/ft})$$

Equation 5-6. Effective Impedance

$$Z_{EFF} = \frac{Z_0}{\sqrt{1 + \frac{C_D}{C_0}}} \quad (\Omega)$$

Equation 5-7. Distributed Trace Capacitance

$$C_0 = \frac{S_0}{Z_0} \quad (\text{pF/ft})$$

Equation 5-8. Distributed Trace Inductance

$$L_0 = 12 * Z_0 * S_0 \quad (\text{nH/ft})$$

Symbols for Equation 5-2 through Equation 5-8:

- S_0 is the speed of the signal on an unloaded PCB in ns/ft. This is referred to as the board propagation constant.
- $S_{0\ MICROSTRIP}$ and $S_{0\ STRIPLINE}$ refer to the speed of the signal on an unloaded microstrip or stripline trace on the PCB in ns/ft.
- Z_0 is the intrinsic impedance of the line in Ω and is a function of the dielectric constant (ε_r), the line width, line height and line space from the plane(s). The equations for Z_0 are not included in this document. See the *MECL System Design Handbook* by William R. Blood, Jr. for these equations.
- C_0 is the distributed trace capacitance of the network in pF/ft.
- L_0 is the distributed trace inductance of the network in nH/ft.
- C_D is the sum of the capacitance of all devices and stubs divided by the length of the network's trunk, not including the portion connecting the end agents to the termination resistors in pF/ft.
- S_{EFF} and Z_{EFF} are the effective propagation constant and impedance of the PCB when the board is "loaded" with the components.

5.5.2 Effective Impedance and Tolerance/Variation

The impedance of the PCB needs to be controlled when the PCB is fabricated. The method of specifying control of the impedance needs to be determined to best suit each situation. Using stripline transmission lines (where the trace is between two reference planes) is likely to give better results than microstrip (where the trace is on an external layer using an adjacent plane for reference with solder mask and air on the other side of the trace). This is in part due to the difficulty of precise control of the dielectric constant of the solder mask, and the difficulty in limiting the plated thickness of microstrip conductors, which can substantially increase cross-talk.

The effective line impedance (Z_{EFF}) is recommended to be 60 Ω±15%, where Z_{EFF} is defined by Equation 6.

5.5.3 Clock Routing

Analog simulations are required to ensure clock net signal quality and skew is acceptable. The system clock skew must be kept to a minimum (The calculations and simulations for the example topology given in this document have a total clock skew of 200 ps and 150 ps of clock jitter). For a given design, the clock distribution system, including the clock components, must be evaluated to ensure these same values are valid assumptions. Each processor datasheet specifies the clock signal quality requirements. To help meet these specifications, follow these general guidelines:

- Tie clock driver outputs if clock buffer supports this mode of operation.
- Match the electrical length and type of traces on the PCB (microstrip and stripline may have different propagation velocities).
- Maintain consistent impedance for the clock traces.
  - — Minimize the number of vias in each trace.
  - — Minimize the number of different trace layers used to route the clocks.
  - — Keep other traces away from clock traces.
- Lump the loads **at the end** of the trace if multiple components are to be supported by a single clock output.
- Have equal loads at the end of each network.

The **ideal** way to route each clock trace is on the same single inner layer, next to a ground plane, isolated from other traces, with the same total trace length, to the same type of single load, with an equal length ground trace parallel to it, and driven by a zero skew clock driver. When deviations from ideal are required, going from a single layer to a pair of layers adjacent to power/ground planes would be a good compromise. The fewer number of layers the clocks are routed on, the smaller the impedance difference between each trace is likely to be. Maintaining an equal length and parallel ground trace for the **total length of each** clock ensures a low inductance ground return and produces the minimum current path loop area. (The parallel ground trace will have lower inductance than the ground plane because of the mutual inductance of the current in the clock trace.)

5.6 Conclusion

AGTL+ routing requires a significant amount of effort. Planning ahead and leaving the necessary time available for correctly designing a board layout will provide the designer with the best chance of avoiding the more difficult task of debugging inconsistent failures caused by poor signal integrity. Intel recommends planning a layout schedule that allows time for each of the tasks outlined in this document.

6

Clocking

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Clocking 6

There are three clock generator components required in a Intel® 840 chipset platform. Two Direct Rambus* Clock Generator (DRCG) generates clock for the RDRAM interface and a CK133W/S clock generator for the other platform components. Clock synthesizers that meet the CK98W/S Clock Synthesizer/Driver Specification and DRCG specification will be suitable for a Intel® 840 chipset system.

6.1 CK133W

The CK133W shares identical pinout as the CK133 but limits processor clock jitter of 150 ps. This clock generates the signals listed in Table 6-1.

Table 6-1. Intel® 840 Chipset System Clocks w/ CK133W

# of Clocks	Name	Routed to		Frequency	Voltage
4	CPUCLK[3:0]	2 processors	CLK	100/133 MHz	2.5V
		MCH	HCLKIN		
		ITP	BCLK		
3	APIC[2:0]	2 processors	PICCLK	16.667 MHz	2.5V
		P64H	APICCLK		
		ICH	APICCLK		
8	PCICLK[7:0]	PCI Devices	CLK	33 MHz	3.3V
		ICH	PCICLK		
		FWH Flash BIOS	CLK		
		LPC	CLK		
4	3V66[3:0]	MCH	CLK66	66 MHz	3.3V
		ICH	CLK66		
		P64H	CLK66		
		AGP	CLK		
2	REF[1:0]	ICH	CLK14	14.318 MHz	3.3V
		SIO			
1	48 MHz	ICH	CLK48	48 MHz	3.3V
2	CPU_DIV2[1:0]	DRCG	REFCLK	50/66 MHz	2.5V

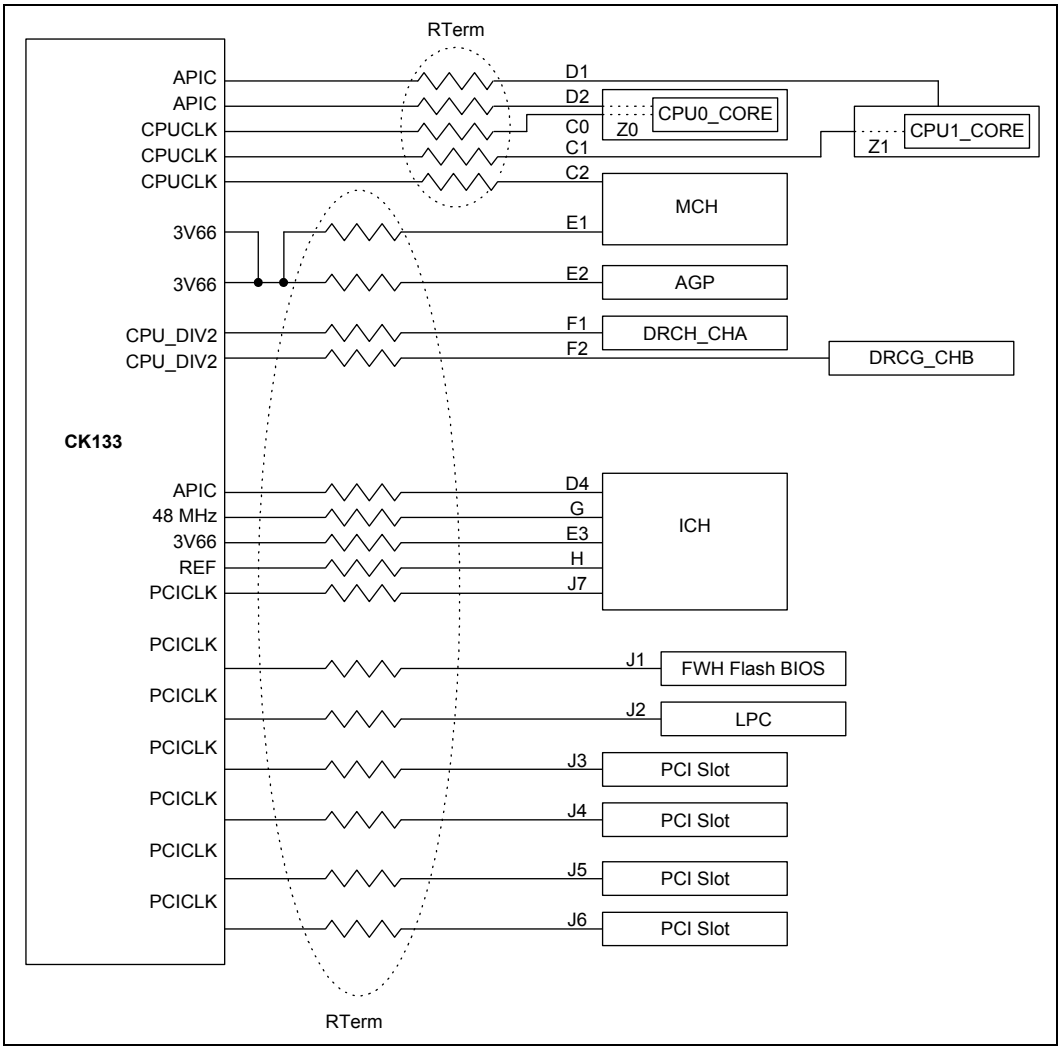
The CK-133W is a mixed voltage component. Some of the output clocks are 3.3V and some of the output clocks are 2.5V. As a result, the CK-133W device requires both 3.3V and 2.5V. These power supplies should be as “clean” as possible. Noise in the power delivery system for the clock driver can cause noise on the clock lines.

The MCH uses the same clock for hub interfaces and AGP. It is important that the hub interface/AGP clocks are routed to ensure the skew requirements are met between:

- MCH hub interface/AGP clock and the AGP connector (or device)
- MCH hub interface/AGP clock, ICH hub interface clock and P64H hub interface clock

6.1.1 Intel® Pentium® III Processors 2-Way

Figure 6-1. CK133 Clock Diagram—Intel® Pentium® III Processor / Intel® 840 Chipset



6.1.1.1 CK133W—Intel® Pentium® III Processor / Intel® 840 Chipset Clock Skew

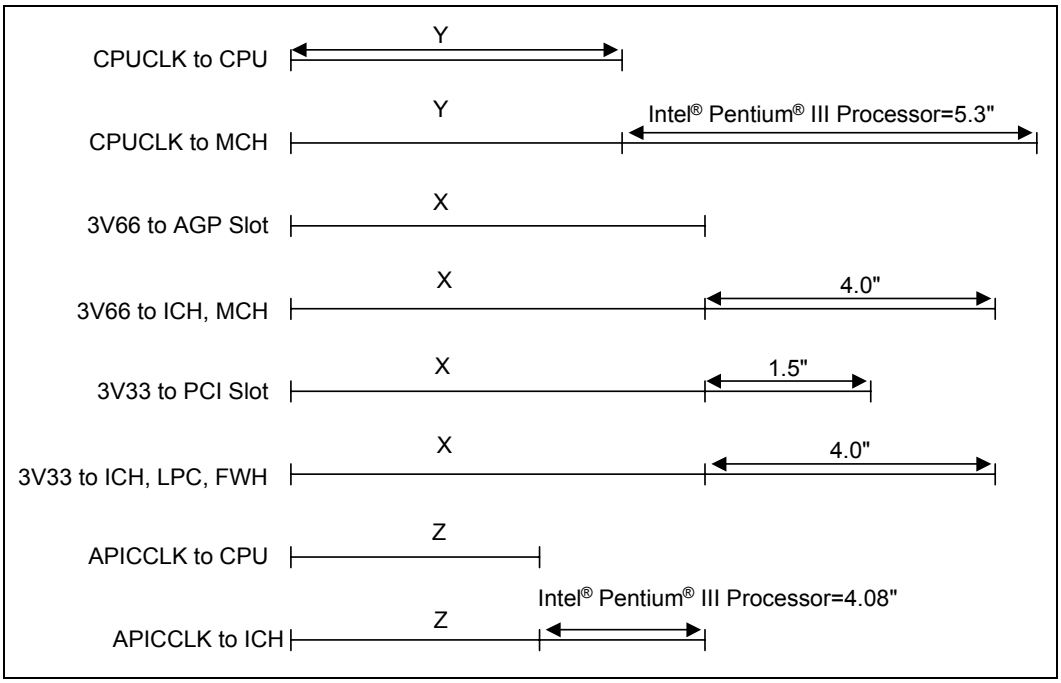
See Figure 6-1.

Table 6-2. CK133W—Intel® Pentium® III Processor / Intel® 840 Chipset Clock Skew

Clock Symbol	Relationship	Skew (Typical)			Notes
		Pin-Pin (ps)	Base Board (ps)	Total (ps)	
C0 - C1	SC242 CPUCLK **leads** SC242 CPUCLK	175	125	300	1
C0 - C1	SC242 CPUCLK **lags** SC242 CPUCLK	-175	-125	-300	1
(C0,C1) - C2	SC242 CPUCLK **leads** MCH HCLK	175	125	300	2, 3
(C0, C1) - C2	SC242 CPUCLK **lags** MCH HCLK	-175	-125	-300	2, 3
D1 - D2	CPU PICCLK **leads** CPU PICCLK	250	125	375	
D1 - D2	CPU PICCLK **lags** CPU PICCLK	-250	-125	-375	
(D1, D2) - D3	CPU PICCLK **leads** ICH APICCLK	250	125	375	4
(D1, D2) – D3	CPU PICCLK **lags** ICH APICCLK	-250	-125	-375	4
E1 - E2	MCH CLK66 **leads** AGP device AGPCLK	250	125	375	5, 6
E1 - E2	MCH CLK66 **lags** AGP device AGPCLK	-250	-125	-375	5, 6
E1 - E3	MCH CLK66 **leads** ICH CLK66	250	125	375	7
E1 - E3	MCH CLK66 **lags** ICH CLK66	-250	-125	-375	7
E3 - J7	ICH CLK66 **to** ICH PCICLK	1500-3500	±500	1000-4000	8, 9
J1, J2, J3, J4, J5, J6	PCICLK **lead** PCICLK	500	1500	2000	9
J1, J2, J3, J4, J5, J6	PCICLK **lags** PCICLK	-500	-1500	-2000	9

NOTES:
1. 2-way processor configuration only.
2. Additional board skew 795 ps (795 ps=5.3” at 150 ps/inch) must be added to MCH HCLK to compensate for the propagation delay to the Intel® Pentium® III processor cartridge. The ±125 ps board skew shown does not reflect this addition.
3. An additional ±40ps have been added, to the skew, to support SSC.
4. Additional board skew 612 ps (612 p s= 4.08” at 150 ps/inch) must be added to the ICH APICCLK to compensate for the propagation delay to the Pentium III processor cartridge. The ±125 ps board skew shown does not reflect this addition.
5. Clock drivers are tied together to reduce pin-to-pin skew, and the pin-pin skew must not exceed 250 ps.
6. Additional board skew (4.0” = 700 ps at 175 ps/inch) must be added to MCH CLK66 and ICH CLK66 if an AGP connector/card is used. This is stated in the AGP Specification. The ±125 ps board skew shown does not reflect this addition.
7. An additional ±60ps have been added, to the skew, to support SSC.
8. ICH CLK66 must lead ICH PCICLK.
9. Additional board skew must be added to ICH PCICLK and/or PCICLK if a PCI connector/card is used. This is stated in the PCI Specification. The ±1500 ps board skew shown does not reflect this addition.

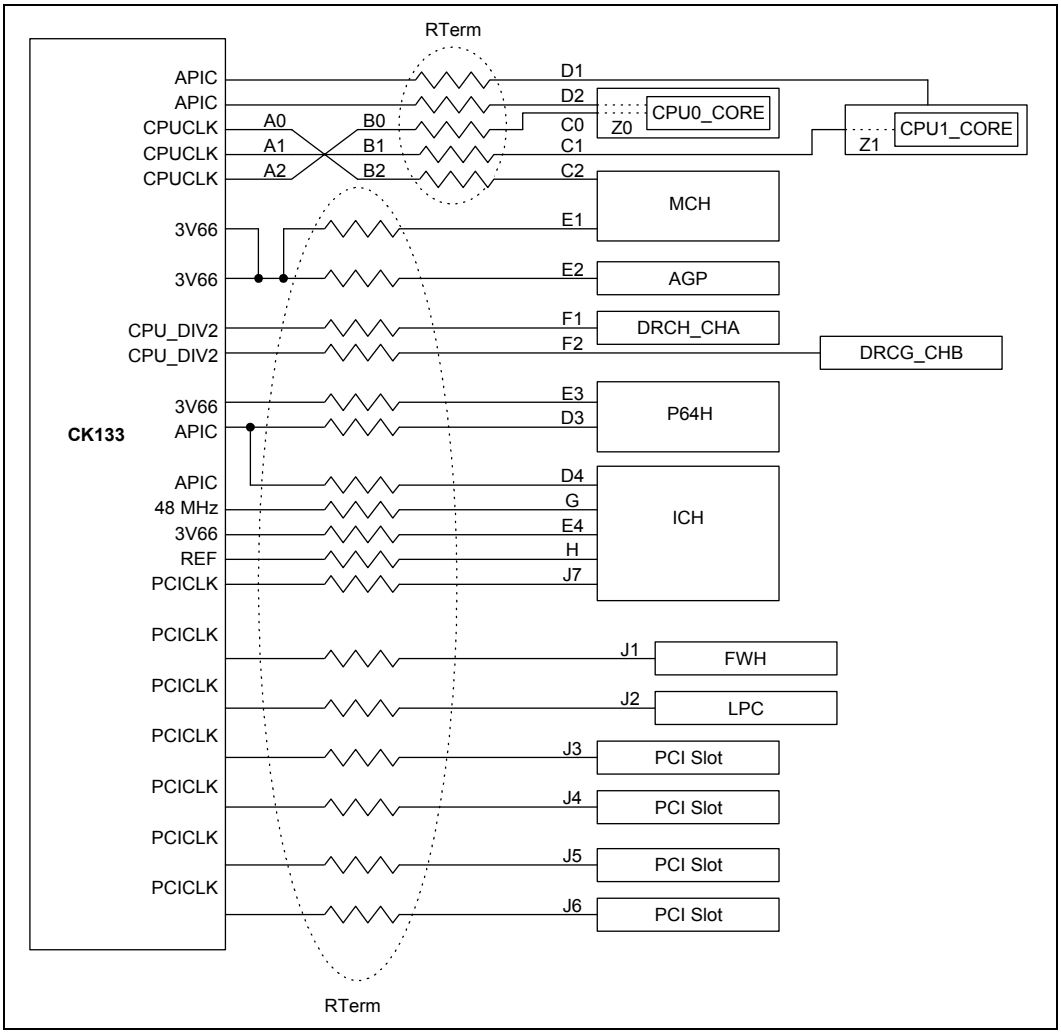
Figure 6-2. CK133W—Intel® Pentium® III Processor / Intel® 840 Chipset Guidelines



NOTES:
1. If any of the clock signals are stripline (being routed on inner layers), then the trace lengths given need to be adjusted for the ~30 ps/inch difference between the Microstrip and Stripline. Stripline is ~175 ps/inch.
2. There is no relationship between lengths X, Y and Z.

6.1.2 Intel® Pentium® III Xeon™ Processor at 600+ MHz 2-Way

Figure 6-3. 2-Way Intel® 840 Chipset CK-133W Clock Diagram



6.1.2.1 CK-133W—Intel® Pentium® III Xeon™ Processor at 600+ MHz / Intel® 840 Chipset Clock Skew

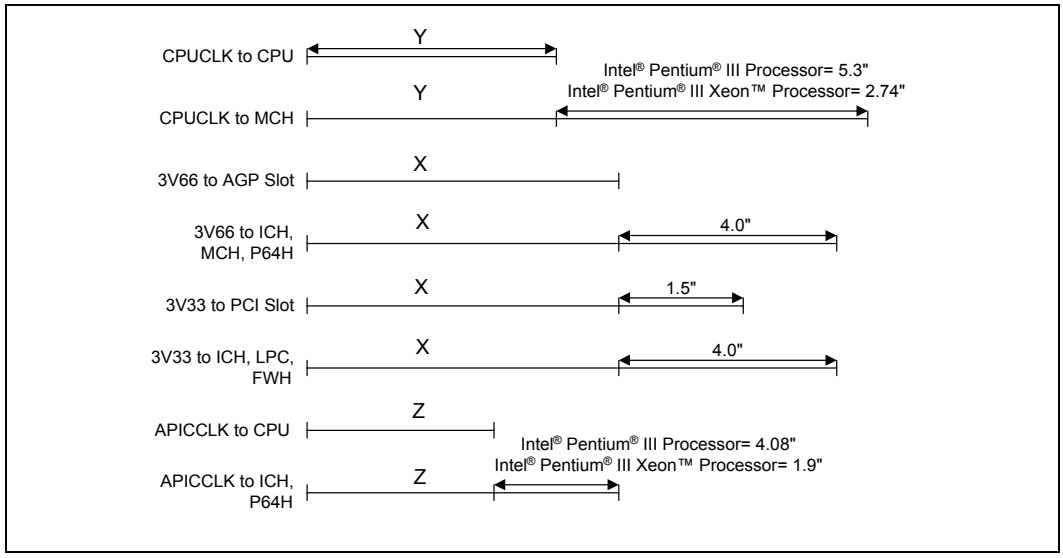
See Figure 6-3.

Table 6-3. 2-Way Intel® 840 Chipset Clock Skew

Clock Symbol	Relationship	Skew (Typical)			Notes
		Pin-Pin (ps)	Base Board (ps)	Total (ps)	
C0 - C1	SC330 CPUCLK **leads** SC330 CPUCLK	50	100	150	1, 2, 3
C0 - C1	SC330 CPUCLK **lags** SC330 CPUCLK	-50	-100	-150	1, 2, 3
(C0, C1) - C2	SC330 CPUCLK **leads** MCH CPUCLK	50	100	150	3, 4
(C0, C1) - C2	SC330 CPUCLK **lags** MCH CPUCLK	-50	-100	-150	3, 4
D1 - D2	CPU PICCLK **leads** CPU PICCLK	250	125	375	
D1 - D2	CPU PICCLK **lags** CPU PICCLK	-250	-125	-375	
(D1, D2) – (D3, D4)	CPU PICCLK **leads** ICH APICCLK and P64H APICCLK	250	125	375	5
(D1, D2) – (D3, D4)	CPU PICCLK **lags** ICH APICCLK and P64H APICCLK	-250	-125	-375	5
E1 – E2	MCH CLK66 **leads** AGP device AGPCLK	250	125	375	2, 6, 7
E1 - E2	MCH CLK66 **lags** AGP device AGPCLK	-250	-125	-375	2, 6, 7
E1 - (E3, E4)	MCH CLK66 **leads** ICH CLK66 and P64H CLK66	250	125	375	7
E1 - (E3, E4)	MCH CLK66 **lags** ICH CLK66 and P64H CLK66	-250	-125	-375	7
E4 - J7	ICH CLK66 **to** ICH PCICLK	1500–3500	±500	1000–4000	8, 9
J1, J2, J3, J4, J5, J6	PCICLK **leads** PCICLK	500	1500	2000	9
J1, J2, J3, J4, J5, J6	PCICLK **lags** PCICLK	-500	-1500	-2000	9

NOTES:
1. 2-way processor configuration only.
2. Clock driver output pins tied together to reduce pin-to-pin skew.
3. An additional ±40ps have been added, to the skew, to support SSC.
4. Additional board skew 480 ps (480 ps =2.74” at 175 ps/inch) must be added to the MCH HCLK to compensate for the propagation delay to the Intel® Pentium® III Xeon™ processor at 600+ MHz cartridge. The ±150 ps board skew shown does not reflect this addition. See Section 6.1.1, “Intel® Pentium® III Processors 2-Way” on page 6-2 for Intel® Pentium® III processor cartridge compensation.
5. Additional board skew 332.5 ps (332.5 ps=1.9” at 175 ps/inch) must be added to the ICH APICCLK and P64H APICCLK to compensate for the propagation delay to the Intel® Pentium® III Xeon™ processor at 600+ MHz cartridge. The ±250 ps board skew shown does not reflect this addition. See Section 6.1.1, “Intel® Pentium® III Processors 2-Way” on page 6-2 for Pentium III processor cartridge compensation.
6. An additional ±60ps have been added, to the skew, to support SSC.
7. Additional board skew (4.0” = 700 ps at 175 ps/inch) must be added to MCH CLK66, ICH CLK66 and P64H CLK66 if an AGP connector/card is used. This is stated in the AGP Specification. The ±125 ps board skew shown does not reflect this addition.
8. ICH CLK66 must lead ICH PCICLK.
9. Additional board skew must be added to ICH PCICLK if a PCI connector/card is used. This is stated in the PCI Specification. The ±1500 ps board skew shown does not reflect this addition

Figure 6-4. CK133W—Intel® Pentium® III Xeon™ Processor at 600+ MHz / Intel® 840 Chipset Guidelines



There is no relationship between lengths X, Y and Z.

6.1.3 Dual Processor Platform Processor Clocks Ganging Solution

Dual processor platform processor clocks ganging solution is an optional implementation. This implementation requires shorting the CPUCLK signals together to improve the output-to-output skew. It is important that the signal quality of the receiver clock meet the specified edge rate, jitter, skew and monotonicity under all loading conditions. Note all clock tables and length recommendation contained in this document assume clock outputs are ganged and meet the specification.

Figure 6-5. 2-way SC242/SC330 CPUCLK Ganging Diagram

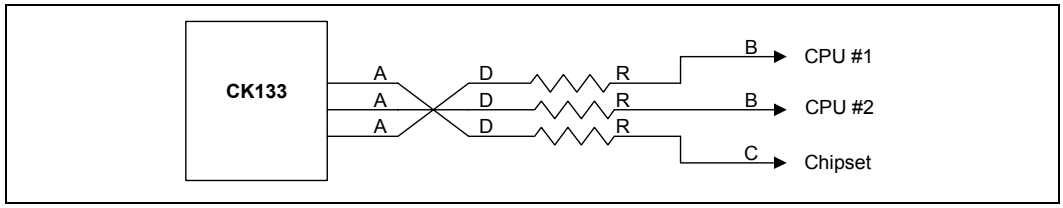


Table 6-4. CPUCLK Ganging Parameters

Symbol	Min. Trace Length (inches)	Max Trace Length (inches)
A	0.3”	0.3”
B	3”	6”
C	—	B + Δ^2
D	0.3”	0.3”

NOTES:
1. These guidelines assume 60 Ω board impedance and series resistor R is 33 Ω
2. For Intel® Pentium® III Xeon™ processor at 600+ MHz, Δ = 2.74"
   For Intel® Pentium® III processors, Δ = 5.3"

6.2 Series Termination Resistor for CK133W/WS Clock Outputs

All outputs require series termination resistors. The recommended resistor values are defined by simulation. The stub length to the CK133W of these resistors can be compromised to make room for decoupling caps. The rule is to keep all resistor stubs within 250 mils of the CK133W. If routing rules allow, Rpacks can be used assuming power dissipation is not exceeded for the Rpack.

6.3 Unused CK133W/WS Clock Outputs

All unused clock outputs shall be tied to ground through a series resistor approximately the impedance of the output buffer (Table 6-5). The intent of these resistors is to terminate the unused outputs to eliminate the EMI radiation.

Table 6-5. Unused CK133W/WS Clock Outputs

Buffer Name	VCC Range (V)	Impedance (Ohms)	If Unused Output Termination to VSS
CPU, CPU_Div2, IOAPIC	2.375–2.625	13.5–45	30 Ωs
48 MHz, REF	3.135–3.465	20–60	40 Ωs
PCI, 3V33, 3V66	3.135–3.465	12–55	33 Ωs

6.4 DRCG

The DRCG reference clock operates at one-half the processor clock frequency. It is an input into the DRCG and is used to generate the Direct RDRAM “Clock to Master” differential pair (CTM, CTM#). The DRCG generates one pair of differential Direct RDRAM Clocks (CTM, CTM#) from the DRCG reference clock generated by the CK133W/S. In addition, the DRCG uses phase information provided by the MCH to phase align the Direct RDRAM clock with the processor clocks.

This phase alignment information is sent to the DRCG SynclkN and PclkM pins from MCH RCLK and HCLK.

6.5 Component Placement and Layout Requirements

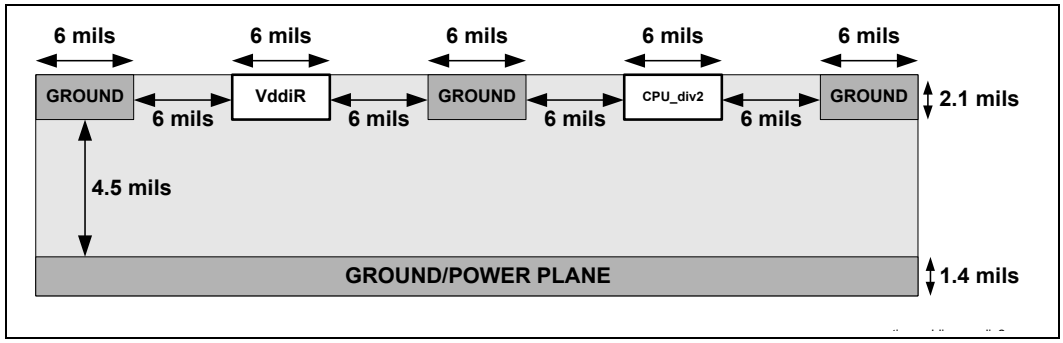
Figure 6-6 shows the conceptual overview of layout requirements among components. Detailed explanation of layout requirements for each interconnections are provided in the following sections:

- Crystal to CK133W/S
- CK133W/S to DRCG
- MCH to DRCG
- DRCG to RDRAM channel

6.5.1 14.318 MHz Crystal to CK133W/S

The distance between the crystal and the CK133 should be minimized. The maximum trace length is 500 mils.

Figure 6-6. VddIR and CPU_Dive2 Routing



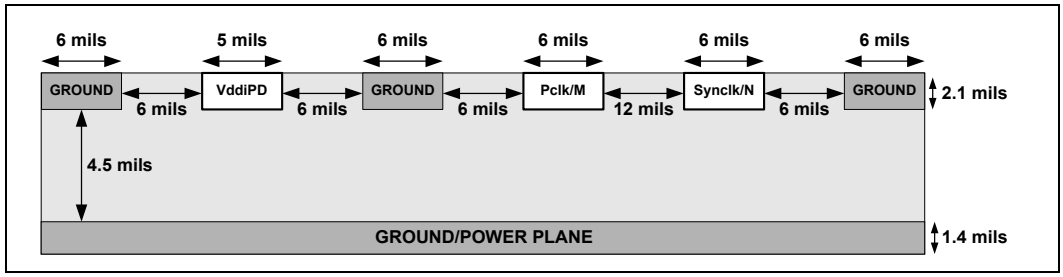
6.5.2 CK133W/S to DRCG

VddIR and CPU_div2 must be routed as shown below. Note that the VddiR pin can be connected directly to 2.5V near the DRCG if the 2.5V plane extends near the DRCG. However, if a 2.5V trace must be run as a trace, it should originate at the CK133W/S and routed as shown.

6.5.3 82840 MCH to DRCG

The Pclk/M, Synclk/N and VddIPD should be routed as shown in Figure 6-7. Note that VddIPD can be connected directly to 1.8V near the DRCG if the 1.8V plane extends near the DRCG. However, if a 1.8V trace must be run, it should originate at the CK133W/S and be routed as shown. If the VddIPD pin is connected to the 1.8V plane using a via (i.e., trace is not run from the CK133W/WS, PCLK/M and SYNCLK/N), HCLKOUT and RCLKOUT must still be routed differentially and ground isolated.

Figure 6-7. 82840 MCH to DRCG Routing Diagram



The maximum length for Pclk/M and Synclk/N is 6”. Additionally, Pclk/M and Synclk/N must be length matched within 50 mils. These signals should be routed on the same layer. If the signals must switch layers, then BOTH signals should change layers together.

6.5.4 DRCG to RDRAM Channels

The RDRAM clock signals (CTM/CTM# and CFM/CFM#) are high-speed, impedance matched transmission lines. The RDRAM clocks begin at the end of the RDRAM channel and propagate to the controller as CTM/CTM#, where they loop back as CFM/CFM# to the RDRAM devices and terminate at the end of the channel.

The CTM/CTM# signals must be ground referenced (with continuous ground island/plane) from the DRCG to the 2nd RIMM. If signals are routed either on top or bottom layer from the 2nd RIMM to the termination, then the ground reference island must extend to the ground of the termination capacitors.

Figure 6-8. RDRAM Clock Routing Dimension

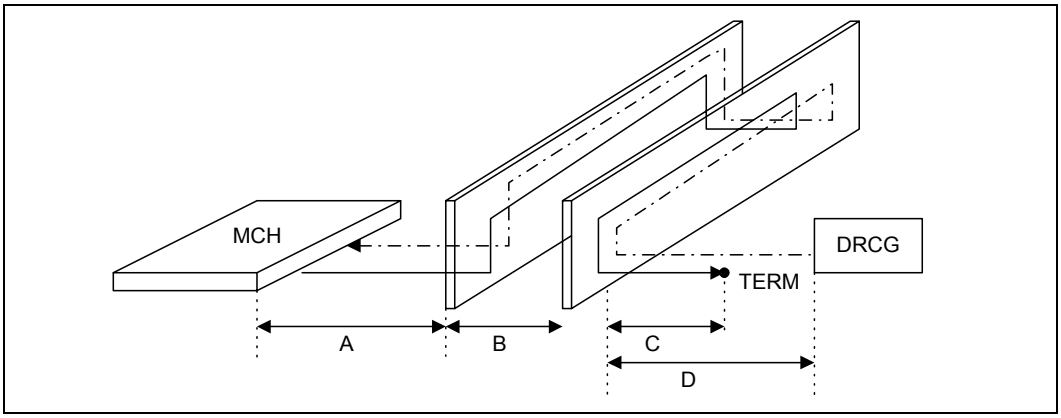


Table 6-6. RDRAM Clock Routing Guidelines

Clock	From	To	Length (inches)	Fig.84 Trace
CTM/CTM#	DRCG	2nd RIMM Connector	0.0–6.0	D
	RIMM	RIMM	0.4–0.45	B
	1st RIMM Connector	Chipset	0.0–6.0	A
CFM/CFM#	Chipset	1st RIMM Connector	0.0– 6.0	A
	RIMM	RIMM	0.4–0.45	B
	2nd RIMM Connector	Termination	0.0– 3.0	C

In line section ‘A’, ‘C’ and ‘D’, the clock signals should be routed differentially. The clock signals in section ‘B’ should be routed non-differentially.

For trace section ‘A’ and ‘D’, the clock signals (CTM/CTM# and CFM/CFM#) must be 14 mils wide and routed as shown in Figure 6-8. For all section ‘B’ and ‘C’, the clock signals must be routed with 18 mil wide traces. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. The 22 mil ground isolation traces must be connected to ground with a via per every 1”. A 6 mil gap is required between the clock signals and the ground isolation traces. In section ‘A’, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clock’s faster trace velocity on the outer layer. CTM/CTM# and CFM/CFM# must be matched within ±2 mils in line section ‘A’ and ‘B’ using the trace length matching method. In section ‘C’, CFM/CFM# must be length matched within ±2 mils. In section ‘D’, the CTM/CTM# must be length matched within ±2 mils.

6.5.5 Trace Lengths

For section ‘A’, CTM/CTM# and CFM/CFM# must be length matched within ±2 mils (although exact length matching is ideal). Package trace compensation, via compensation and RSL signal layer alteration must also be considered. Additionally, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clock’s faster trace velocity on the outer layer.

For trace section ‘B’, the clock signals must be routed with 18 mil wide traces. There must be a 10 mil ground isolation trace routed around the clock differential pair signals. The clock signals must be matched within ±2 mil to the RSL trace length. Exact matching is preferred.

For trace section ‘C’, the clock signals must be routed with 14 mil wide traces. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. A 6 mils gap is required between the clock signals and the ground isolation traces. CFM/CFM# must be matched within ±2 mils. Exact matching is preferred.

For trace section ‘D’, the clock signals must be routed with 14 mil wide traces. There must be a 22 mil ground isolation trace routed around the clock differential pair signals. A 6 mils gap is required between the clock signals and the ground isolation traces. CTM/CTM# must be matched within ±2 mils. Exact matching is preferred.

Figure 6-9. Differential Clock Routing Diagram

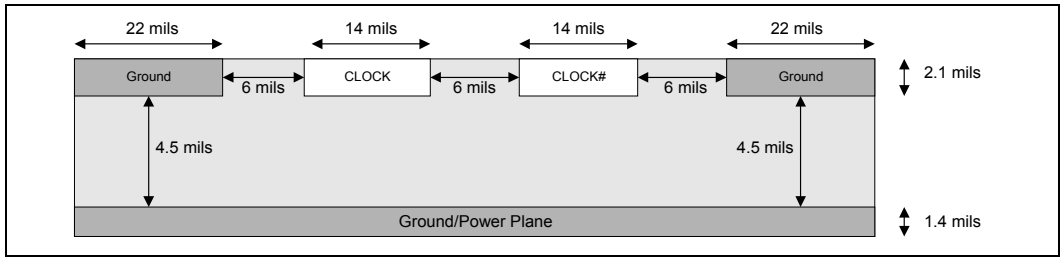
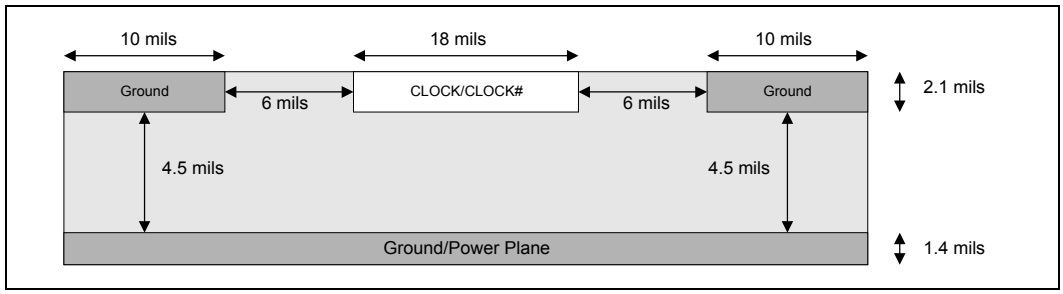
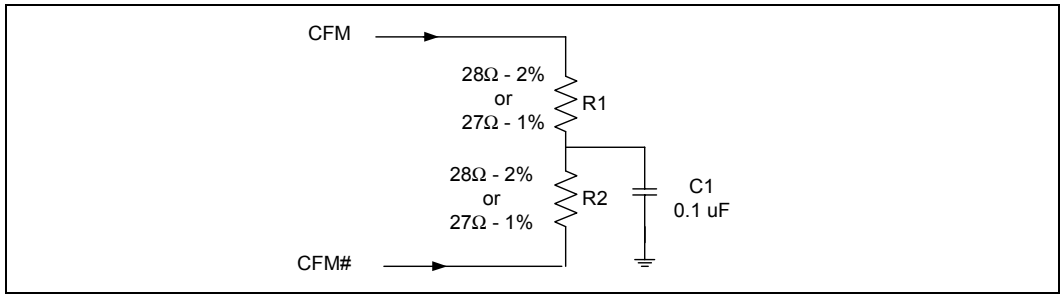


Figure 6-10. Non-Differential Clock Routing Diagram



The CFM/CFM# differential pair signals require termination using either 27 Ω 1% or 28 Ω 2% resistors and a 0.1 uF capacitor as shown.

Figure 6-11. CFM/CFM# Termination



6.5.6 DRCG Impedance Matching Circuit

The external DRCG impedance matching circuit is shown in Figure 6-12.

Figure 6-12. DRCG Impedance Matching Network

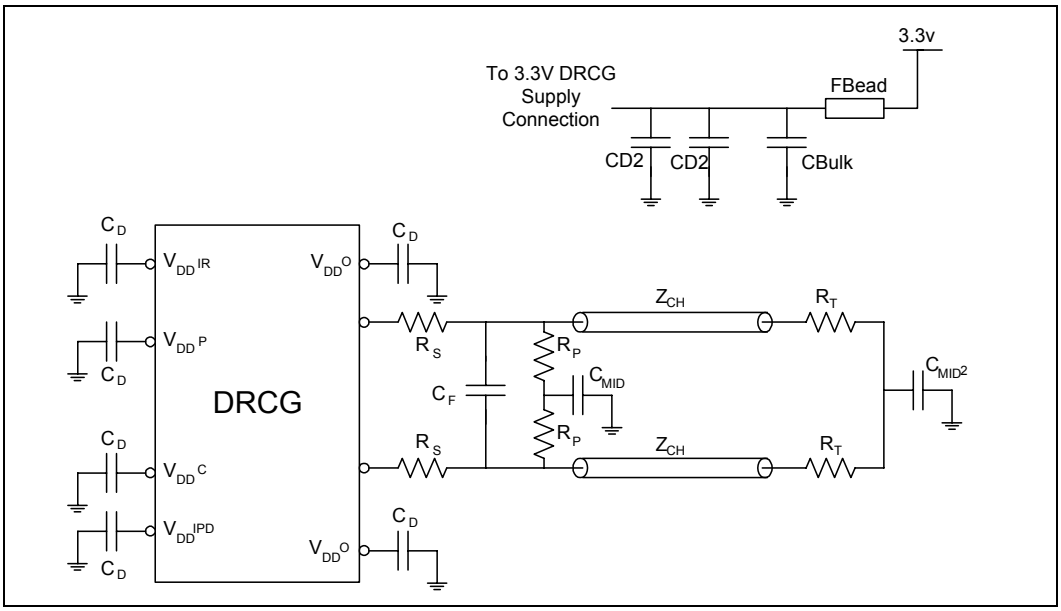


Table 6-7. DRCG Impedance Matching Network

Component	Nominal Value	Notes
C_D	0.1 uF	Decoupling caps to GND
R_S	39 Ωs	Series termination resistor
R_P	51 Ωs	Parallel termination resistor
C_{MID1}, C_{MID2}	0.1 uF	Virtual GND caps
R_T	27 Ωs	End of channel termination
C_F	4-15 pF	Do Not Stuff, leave pads for future use
FBead	50 Ωs at 100 MHz	Ferrite bead
CD2	0.1 uF	Additional 3.3V decoupling caps
CBulk	10 uF	Bulk cap on device side of ferrite bead

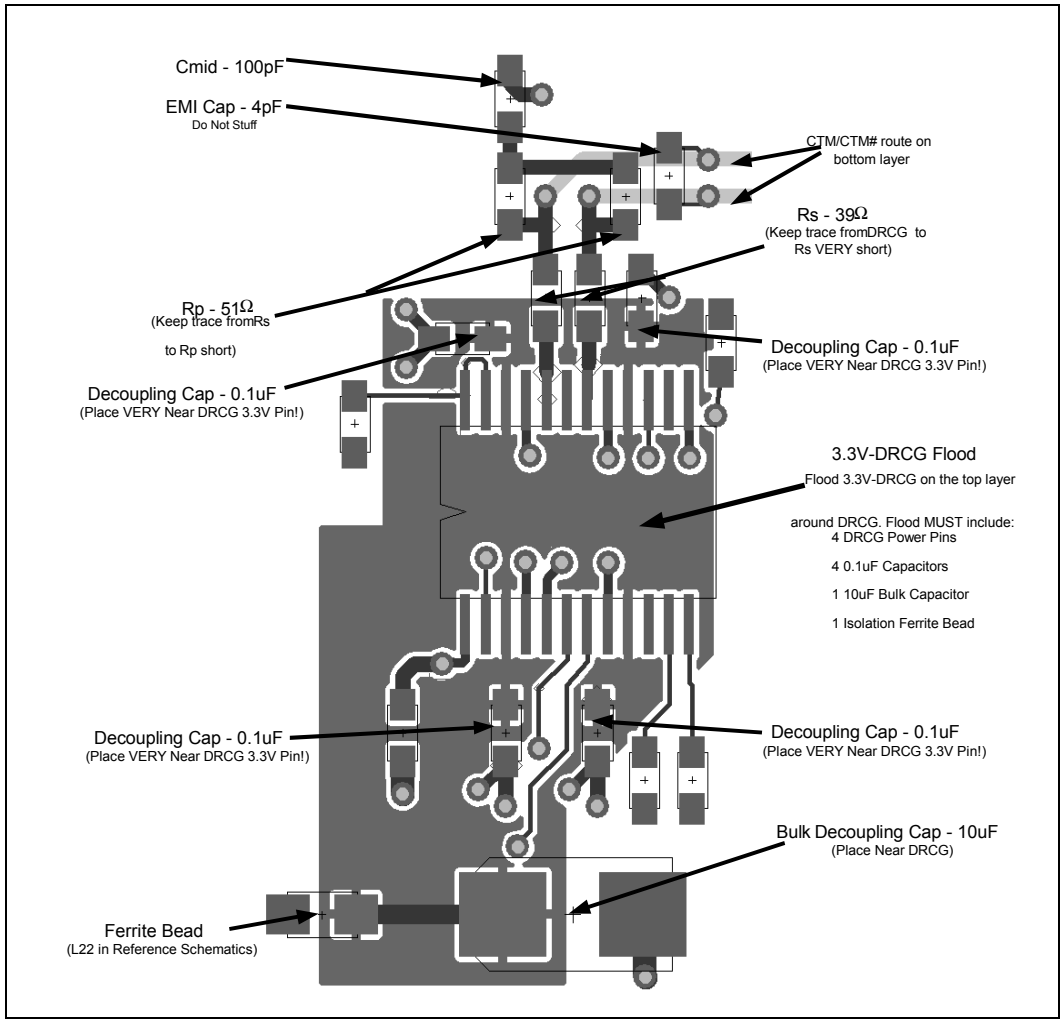
NOTES:
1. Note the removal of the original EMI capacitors between the junctions of R_S, R_P and ground. These capacitors had minimal impact on EMI and increased DRCG output jitter by approximately 2X.
2. The intent of component C_F is to decouple CLK and CLKB outputs to each other, but early data shows this actually increases device jitter. C_F should not be stuffed at this time.
3. The ferrite bead and 10 uF bulk cap combination improves jitter and helps to keep the clock noise away from the rest of the system. The additional 3.3V capacitors (CD2) have a minor positive impact, but the ideal values have not been extensively optimized. There is a possibility that one or both CD2 caps can be removed in future board revisions.
4. uF capacitors are better than 0.01 uF or 0.001 uF caps for DRCG decoupling. Most decoupling experiments that replaced 0.1 uF caps with higher frequency caps ended up with the same or worse jitter. Replacing existing 0.1 uF caps with higher frequency caps is not advised.
5. C_{mid} at 0.1 uF has improved jitter versus C_{mid} at 100 pF. However, this will increase the latency coming out of a stop clock or tri-state mode.
6. R_S, R_P, R_T were modified to improve channel signal integrity through increasing CTM/CTMN swing.

The circuit shown is required to match the impedance of the DRCG to the 28 Ω channel impedance. More detailed information can be found in the *Direct Rambus* Clock Generator Specification*.

The previously recommended 15 pF capacitors on CTM/CTM# should be removed. The 4 pF capacitor shown in the figure should not be assembled (“no-stuff”).

6.5.7 DRCG Layout Example

Figure 6-13. DRCG Layout Example



6.5.8 Decoupling Recommendation for CK133W/S and DRCG

Some CK133W/S vendors may integrate the XTAL_IN and XTAL_OUT frequency adjust capacitors. However, pads should be placed on the board for these external capacitors for testing/debug. To further reduce jitter and voltage supply noise, the addition of a ferrite filter with 2 caps (10 uF and 0.1 uF) on both the 2.5V and 3.3V planes close to the CK133W/S clock devices is recommended.

6.6 DRCG Frequency Selection and DRCG+

6.6.1 DRCG Frequency Selection Table

To provide further flexibility, Intel has enabled a variation of the DRCG labeled the *DRCG+*. The device has the same pin out and form-factor as the existing DRCG device document at *www.rambus.com*.

The DRCG+ Mult[1:0] select table has changed to modify two of the multiplier ratios. An additional 9/2 multiplier allows 133/300 MHz. Note that the 133/356 ratio is not support by the Intel® 840 chipset. Support for 300 MHz and 400 MHz memory bus remains unchanged.

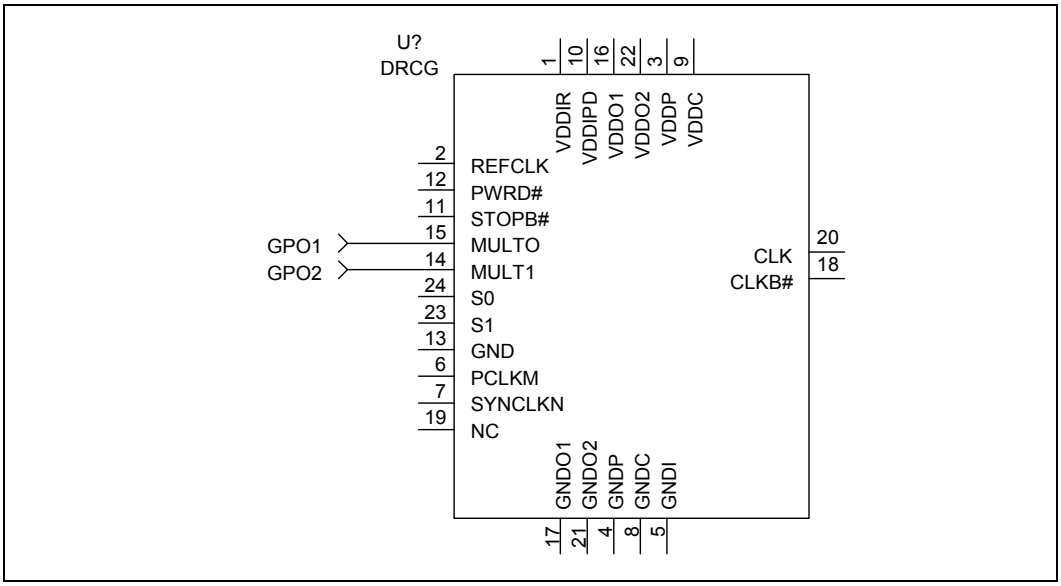
Table 6-8. Multiplier Ratios

Mult[1:0]	DRCG	DRCG+
0:0	4:1	9:2
0:1	6:1	6:1
1:0	8:3	16:3
1:1	8:1	8:1

6.6.2 DRCG+ Frequency Selection Schematic

DRCG+ frequency can be selected by connecting two GPIO's to the MULT[1:0] pins, as shown in Figure 6-14. This allows selection of all frequencies that are supported by the Intel® 840 chipset.

Figure 6-14. DRCG+ Frequency Selection



6.6.3 Jitter Specification

The jitter timing specifications are expanded to encompass both the component specification and the channel specification. Follow the component specification when measuring jitter at the DRCG output resistor. Follow the channel jitter guidelines when measuring jitter at the MCH or at the termination for CFM/CFM# on the RDRAM interface.

Table 6-9. Jitter Specification

Output Frequency (MHz)	Component Jitter Specification	Channel Jitter Guidelines
400	50 ps	100 ps
300	70 ps	120 ps

6.7 AGP Clock Routing Guidelines

The AGP clock must be routed with 20 mil spacing to all other signals. It must also meet the length guidelines shown in Figure 6-15 to Figure 6-18.

6.8 P64H PCI 33 MHz Clock Routing Guidelines

At 33 MHz, the P64H can support 4x33 MHz PCI slots. The P64H can provide 6 copies of the PCLKOUT to PCI devices on its primary PCI bus. PCLKFBOUT is used as the feedback clock and must be routed into PCLKFBIN of the P64H. The PCLKOUT routing guidelines are shown below.

Figure 6-15. P64H PCI 33 MHz Clock Routing

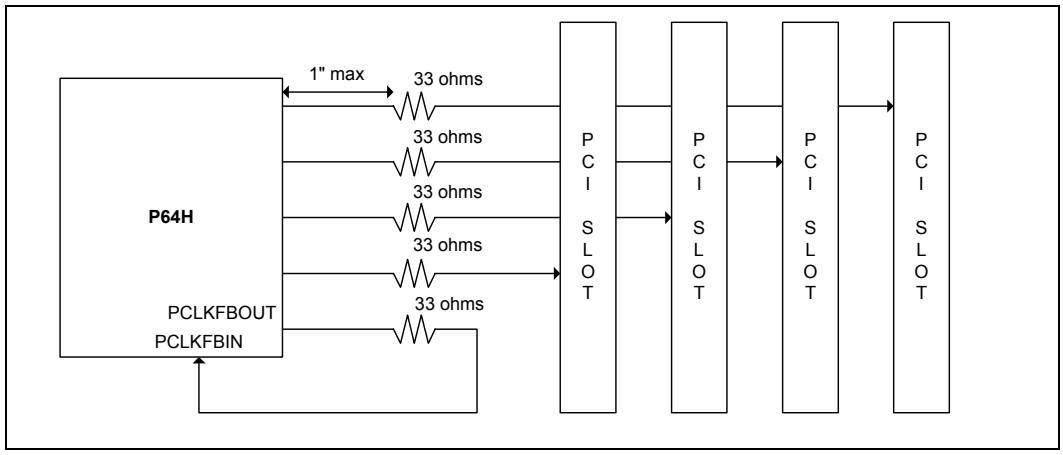
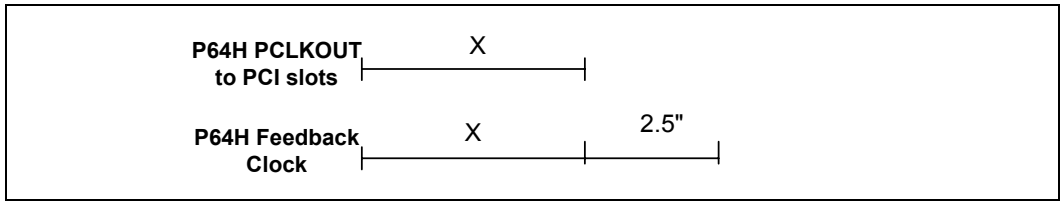


Figure 6-16. P64H PCI 33 MHz Clock Routing



Per the PCI Specification, the PCI CLK signal length from the expansion board edge connector to the PCI device should be 2.5” ±0.1 inches for 32-bit and 64-bit expansion boards.

6.9 P64H PCI 66 MHz Clock Routing Guidelines

At 66 MHz, the P64H can supports 2x66 MHz PCI slots and 1x66 MHz device down. The P64H can provide 3 copies of the PCLKOUT to PCI devices on its primary PCI bus. PCLKFBOUT is used as the feedback clock and must be routed into PCLKFBIN of the P64H. The PCLKOUT layout guidelines are shown below:

Figure 6-17. P64H PCI 66 MHz Clock Routing

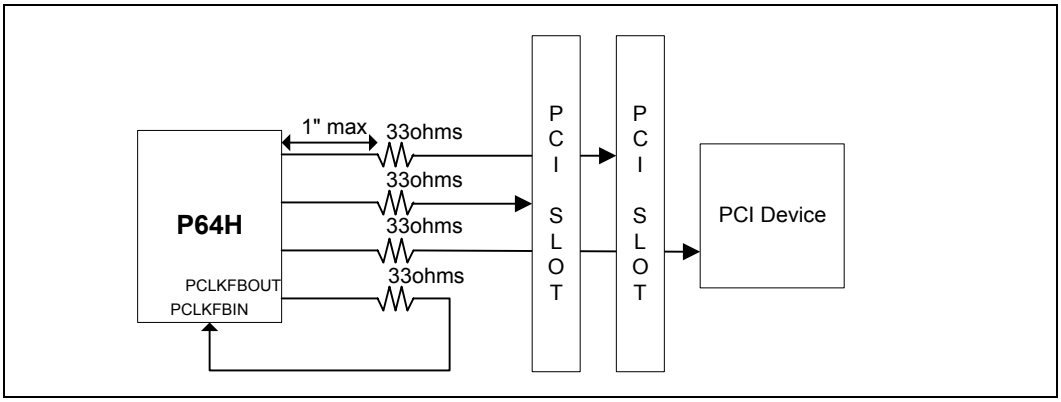
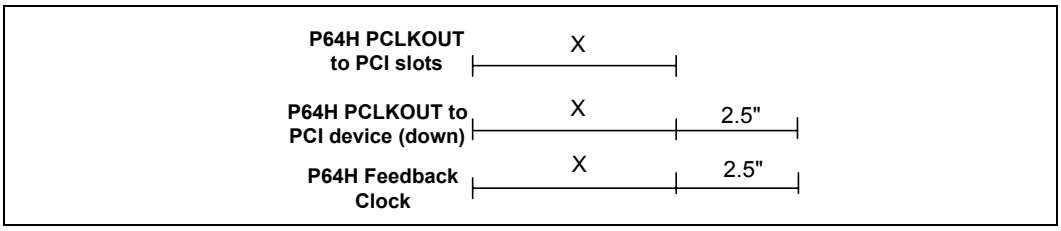


Figure 6-18. 66 MHz PCI Clock Routing



Per the PCI Specification, the PCI CLK signal length from the expansion board edge connector to the PCI device should be 2.5” ±0.1 inches for 32-bit and 64-bit expansion boards.

7

System Design Consideration

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System Design Consideration 7

7.1 Power Delivery

7.1.1 Definitions

Term	Definition
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.
Full-power operation	During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state and the S1 (processor stop grant state) state.
Suspend operation	During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).
Power rails	WTX power supply has 6 power rails: +5V, -5V, $+12V_{DIG}$, +12V, -12V, +3.3V, -3.3V, 3VSB, 5VSB. In addition to these power rails, other power rails can be created with voltage regulators.
Core power rail	A power rail that is only on during full-power operation.
Standby power rail	A power rail that in on during suspend operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rails that are distributed directly from the WTX power supply is: 3VSB and 5VSB (3V Standby and 5V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived power rail	A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, 1.8V can be derived (on the motherboard) from either the 3.3V or 5V using a voltage regulator.
Dual power rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation.

7.1.2 Intel® 840 Chipset Board Power Delivery

Figure 7-1. 2-Way SC242/Intel® 840 Chipset RIMMs Power Delivery Architecture

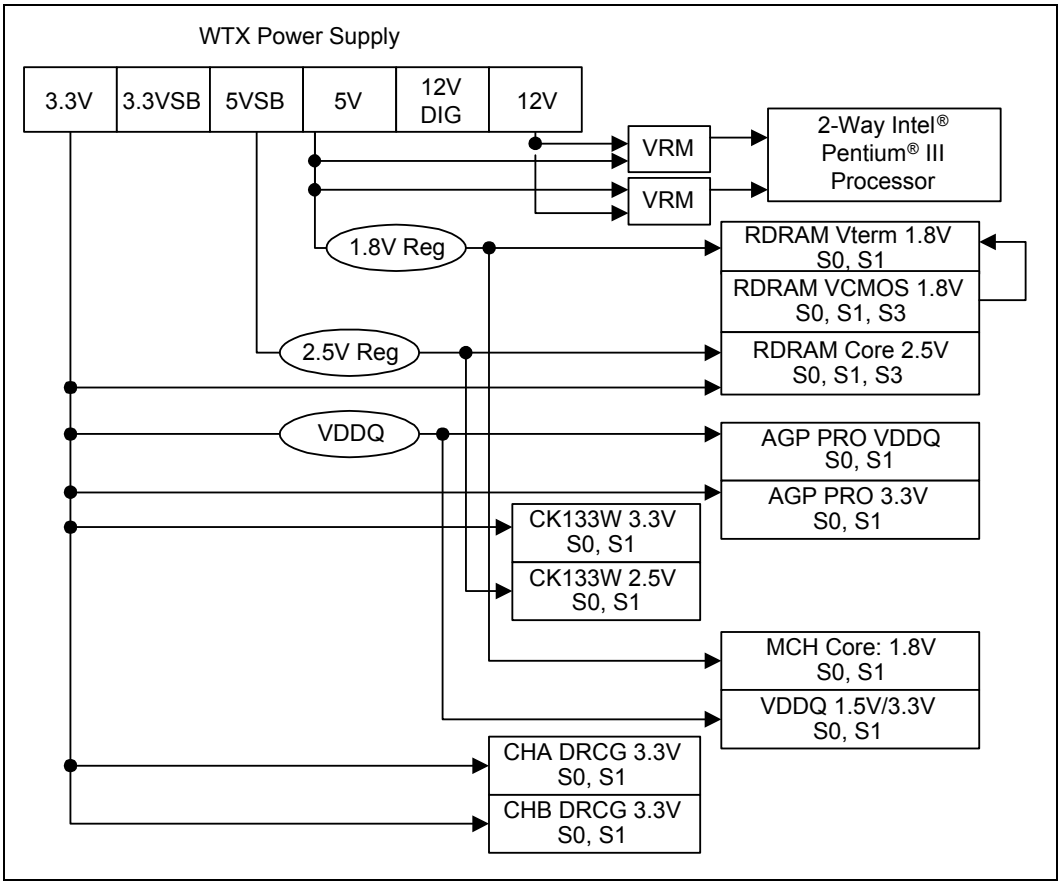


Figure 7-2. 2-Way SC242 Processors/Intel® 840 Chipset MRH-R MEC Power Delivery

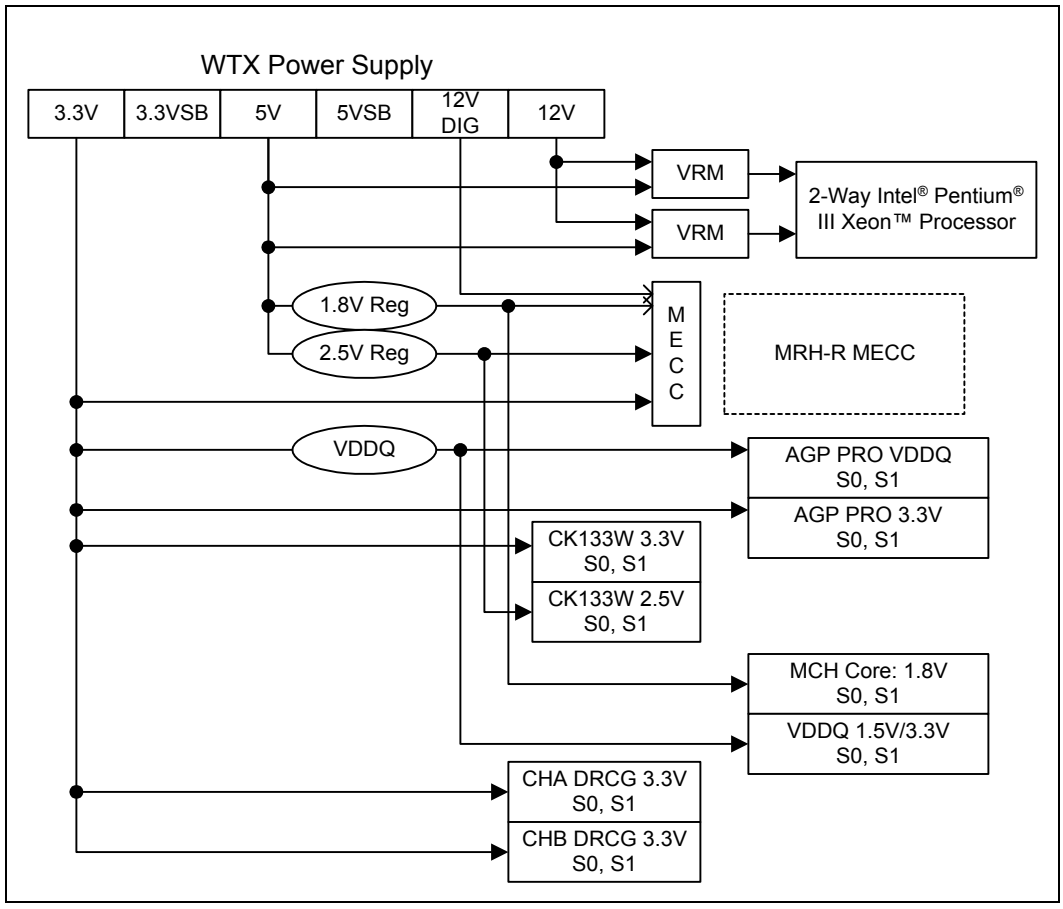
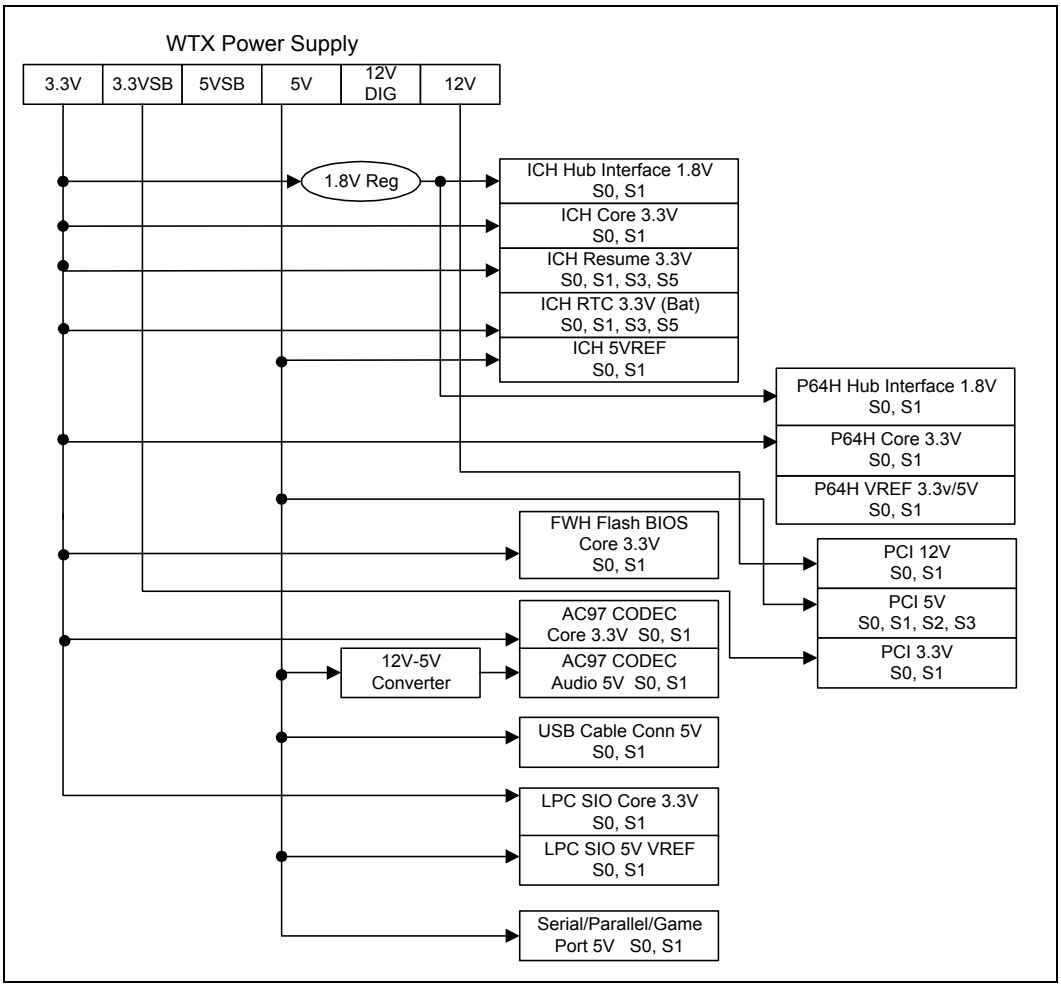


Figure 7-3. Intel® 840 Chipset System I/O Power Delivery



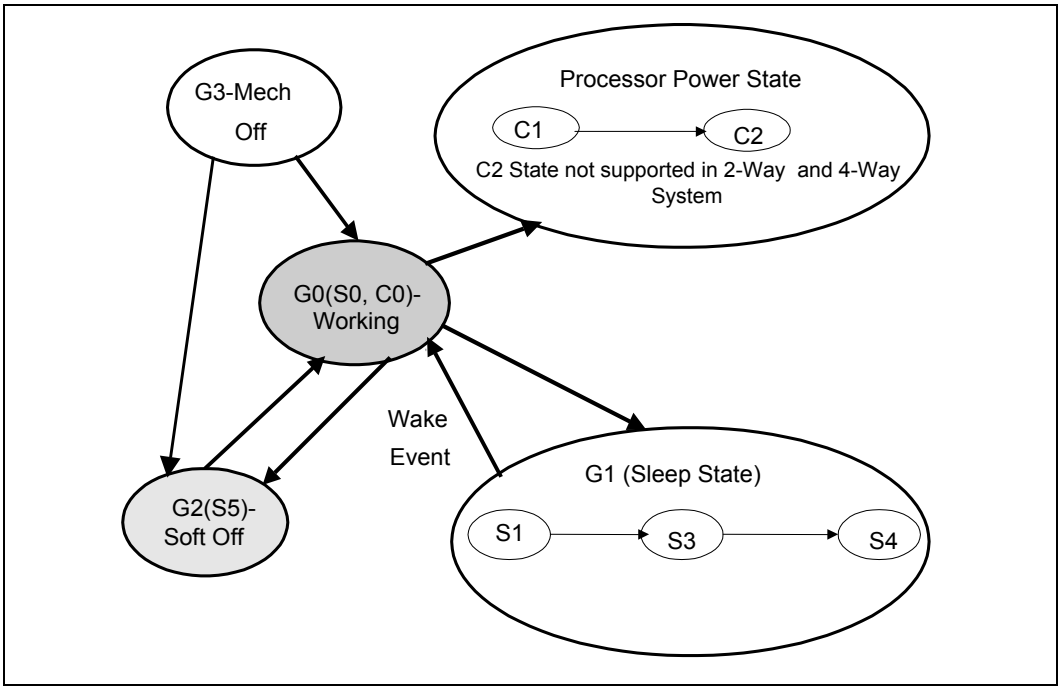
7.2 Power Management

The Intel® 840 chipset-based platform implements the ACPI mechanisms software and hardware that enables the system to minimize system power consumption, manage system thermal limits, and maximize the battery life. This implementation involves tradeoffs among system speed, noise.

7.3 ACPI Hardware Model

The Intel® 840 chipset-based workstation or server supports both legacy and ACPI operations which involves sequencing the platform between the various global system states (G0-G3). The following Figure 7-4 depicts global states and the transitions. For complete detail of the mechanisms involves in transition from any of the global states, refer to ACPI Interface specification 1.0a section 4.5.

Figure 7-4. Global System Power States and Transition



7.4 Thermal Design Power

The thermal design power numbers are estimation of the maximum expected power generated by a component in a realistic application. It is based on extrapolations in both hardware and software technology over the product life. It does not represent the expected power generated by a power virus. The ICC max sustained (WCRA) numbers are estimation of the maximum expected current generated within a die section in a realistic application. For example, an application that is doing only extensive memory reads/writes.

The numbers below should be used for power supply design and not thermal design. Refer to the Intel® 840 Chipset Thermal Application Note for thermal design details.

Table 7-1. Thermal Design Power

Parameter	Operating Voltage	Icc Max Sustained Current (mA)
MCH Max Thermal Design Power = 4.2 W		
Core	1.8V	1000
RAC Core	1.8V	340
RSL	1.8V	730[1]
Hub Interface	1.8V	360
AGP	3.3V	230
VDDQ -AGP	1.5V	200
P64H Max Thermal Design Power = @ 33 MHz = 1.8W / @ 66 MHz = 2.2 W		
Core @ 33 MHz	3.3V	650
Core @ 66 MHz	3.3V	820
PCI I/O @ 33 MHz—6 devices	3.3V	460
PCI I/O @ 66 MHz—2 devices	3.3V	310
HL I/O	1.8V	340
MRH-R Max Thermal Power = 2.2 W		
RAC Core	1.8V	1020
RSL RAC A	1.8V	730[2]
RAC B	1.8V	730[3]
RAC C	1.8V	730[3]
ICH Max Thermal Power = 1.4 W		
Core	3.3V	300
PCI I/O	3.3V	1500
HL I/O	1.8V	55

NOTES:
1. Could be shared between the MCH and RDRAM.
2. Could be shared between MCH and MRH-R.
3. Could be shared between MRH-R and RDRAM.
4. This is consumed by either RIMMs or MCH, and not by both.
5. The 1.8V RDRAM termination (MCH) is consumed by either RIMMs or MCH, and not by both.

7.5 64/72Mbit RDRAM Excessive Power Consumption

During initialization of RDRAM devices, all RDRAM devices on the channel responds incorrectly to device directed commands. These commands are the SET_FAST_CLOCK, SET_RESET, and CLEAR_RESET commands. This causes excessive current consumption on the 2.5V supply. The amount of excessive current depends on the number of devices and frequency used. The worst case current draw is 7.5 A, in a system with 32 devices and a frequency of 400 MHz. This issue will be present in initial production of 64/72Mbits RDRAM devices; however, 128Mbit device operation will be corrected. There are two potential options/solutions:

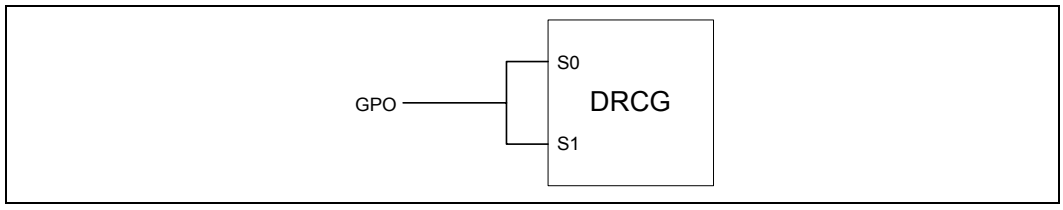
- Reduce the clock frequency during initialization
- Increase the current capability of the 2.5V voltage regulator.

For specific RDRAM impact, please contact the RDRAM vendors.

Option 1—Reduce the Clock Frequency During Initialization

Tie a single core well GPO with a default high state to both the S0 and S1 pins of the DRCG (i.e., tie S0 and S1 together and then connect to a GPO as shown in Figure 7-5. When the core power supply to the system is turned on, the DRCG will enter a test mode and the output frequency will match the input REFCLK frequency. For details on this DRCG mode, please refer to the latest DRCG specification. By slowing down the DRCG output clock, the power consumption from the 2.5V power supply will be reduced. After the SetR/ClrR commands have been issued, BIOS will drive the GPO low to bring the DRCG back to normal operation.

Figure 7-5. Use a GPO to reduce DRCG frequency



Note that if a default low GPO is used, on power up, all the devices may come up in the standby state at full speed, thus requiring more power.

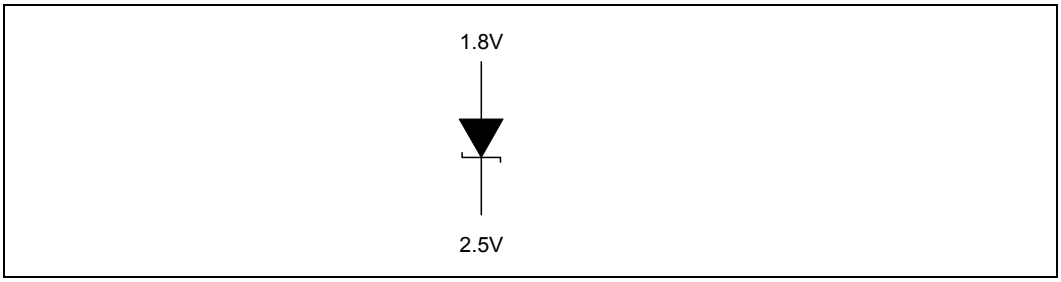
Option 2—Increase the Current Capability of the 2.5V Voltage Regulator

The second implementation option requires that the 2.5V power supply be modified to maintain the maximum amount of current required by a fully populated RDRAM channel (~7.5A).

7.6 Vterm/Vdd Power Sequencing Requirement

Power to the RDRAM termination resistors (Vterm) must follow the power to the RDRAM Core. A schottky diode can be placed between the 1.8V and 2.5V to ensure this power-up sequence.

Figure 7-6. 1.8V and 2.5V Power Sequence (Schottky Diode)

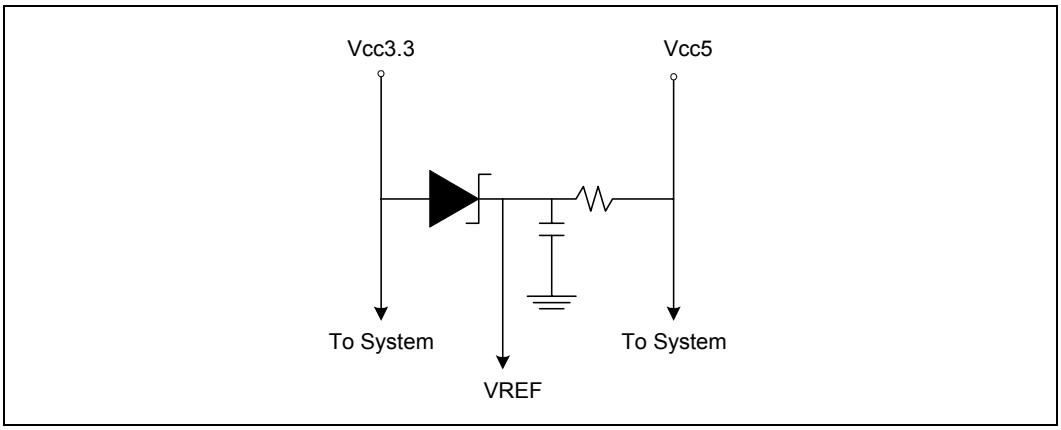


7.7 ICH/P64H 5VREF and VCC3_3 Sequencing Requirement

5VREF is the reference voltage for 5V tolerance on inputs to the ICH. 5VREF must be power up before or simultaneously to 3.3VCC. It must also power down after or simultaneous to 3.3VCC.

VCC5REF and PVCC5REF signals are reference voltage for 5V tolerance on P64H inputs. These signals share the same sequencing requirement as the ICH 5VREF signal. The following circuit demonstrates one possible method to ensure this power sequence requirement is met.

Figure 7-7. 5VREF Sequencing Circuit



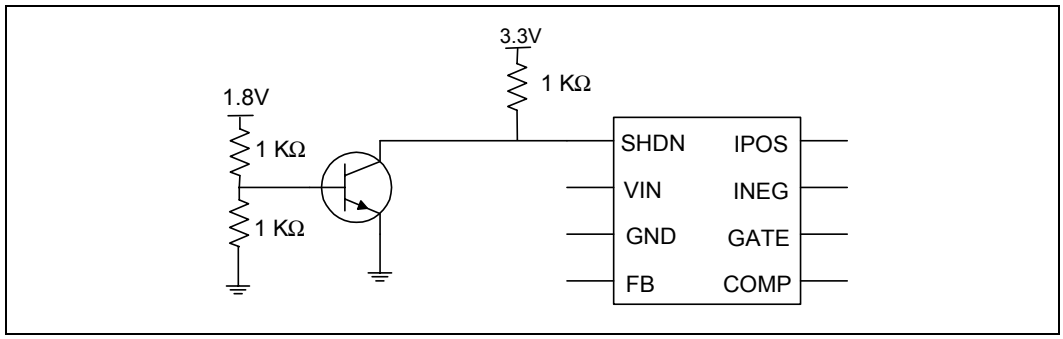
7.8 VDDQ/Vcc1_8 Power Sequencing

For the consideration of long term component reliability, the following power sequence is strongly recommended while the AGP interface of MCH is running at 3.3V. If the AGP interface is running at 1.5V, the following power sequence recommendation is no longer applicable. The power sequence recommendation is:

- During the power-up sequence, the 1.8V must ramp up to 1.0V BEFORE 3.3V ramps below 2.2V
- During the power-down sequence, the 1.8V CAN NOT ramp below 1.0V BEFORE 3.3V ramps below 2.2V
- The same power sequence recommendation also applies to the entrance and exit of S3 state

System designers need to be aware of this requirement while designing the voltage regulators and selecting the power supply.

Figure 7-8. VDDQ Power Sequencing Example



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8

Design Considerations/Checklist

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Design Considerations/Checklist 8

Pull-up and pull-down values are system dependent. The appropriate value is determined by AD/DC analysis of the pull-up voltage used, the current drive capability of the output driver, input leakage currents of all devices on the signal net, the pull-up voltage tolerance, the pull-up/pull-down resistor tolerance, the high/low voltage specification, the input timing specification (RC rise time), etc. Analysis should be done to determine the minimum/maximum values that may be used on the individual signal. Engineering judgement should be used to determine the optimal values. This determination can include cost concerns, commonality considerations, manufacturing issues, specifications, etc…

DC calculation for pull-up value:

$$R_{max} = (Vcc_{PU}\ MIN - V_{ih}\ MIN) / I_{leakage}\ MAX$$

$$R_{min} = (Vcc_{PU}\ MAX - V_{il}\ MAX) / I_{ol}\ MAX$$

Since $I_{leakage}$ MAX is normally very small, Rmax may not be meaningful. R_{max} is also determined by the maximum allowable rise time.

8.1 Design Considerations

The following design considerations are intended to be used for Intel® 840 chipset design reviews. This list should be used with the Intel® 840 Chipset Customer Reference Schematics (see Appendix A, “Reference Schematics”).

8.1.1 Intel® Pentium® III Xeon™ Processor at 600+ MHz

- Pay special attention to the high-speed layout of AERR#, BERR#, BINIT#, BNR#, HIT#, and HITM#. These "wired-OR" signals may be driven simultaneously by more than one agent and may be more susceptible to undershoot/ringback caused by falling edge transitions. Make sure **only ground planes** are used as reference planes for the entire path of these signals.
- The processor outputs, at the clock driver, should be shorted together if ganging is supported.
- Use the OCVR_OK#/VRM_PWRGD signal with the CPUPWRGOOD/RESET generation logic to ensure correct timings.
- PRDY# should be connected to the processor and ITP PRDYX# pin through a 240 Ω series resistor. A 50 Ω pull-up to VTT1.5 must also be added on the processor side of the series resistor.
- Pull up or pull down should be implemented in SA[2:0] to set the address bits accordingly.

8.1.2 82840 Memory Controller Hub (MCH)

8.1.2.1 System Bus Interface

- System bus frequency and system bus ECC straps require external network for proper enabling. HLA10 is used to determine the system bus frequency. ST0 (AGP) is used to enable ECC.
- BREQ0 is provided by the MCH and must be connected to the processors.
- GTL+ termination is recommended for the following signals: HD#[63:0], HA#[35:3], BREQ#[3:0], DEP#[7:0], BPRI#, DBSY#, DEFER#, DRDY#, BERR#, BNR#, ADS#, HIT#, HITM#, HLOCK#, CPURST#, HREQ#[4:0], HTRDY#, RSP#, RP#, AP#[1:0], RS#[2:0].
- GTLREF[B:A] can be generated with a 75 Ω and 150 Ω resistor divider circuit. The 75 Ω and 150 Ω resistors should be connected to VCC1.5 and GND, respectively. There should be one divider circuit for each GTLREF signal. Additionally, GTLREF signals should also be decoupled to GND with a 0.001 uF capacitor.

8.1.2.2 RDRAM Interface

- RDRAM channel termination should be pulled to a 1.8V source.
- Source generation circuit (RAMREF) is recommended when MECC's are implemented. This circuit should be placed near the MCH to generate RAMREF_FM to the MECC. An identical circuit should be placed on the MECC, to generate the RAMREF_TM signal to REF[1:0]. This is a typical resistor divider circuit and comprises of 160 Ω to Vterm and 560 Ω to GND.

8.1.2.3 Hub Interface A

- HLAREF reference voltage is ½ of 1.8V.
- HLACOMP can support either RCOMP or ZCOMP implementation. Reference Design Guide for design information.

8.1.2.4 AGP Interface

- AGP interrupts can be shared with PCI interrupts (PCI Specification, Revision.2.2). It is recommended that interrupts be staggered and each PIRQ should be programmed to a different IRQ.
- AGPREF can be generated with a voltage divider circuit to VDDQ.
- TYPEDET# must be connected to a flexible voltage regulator for VDDQ.
- All AGP pull-up resistors should be pulled to VDDQ.
- VREFCG should be tied to a resistor divider circuit, near the MCH.
- VREFGC should be connected to a FET switch that will supply either locally or source generated VREF to the MCH.

8.1.3 RDRAM Design Considerations

Ground Isolation Well Grounded

- Via to ground every ½ inch around edge of isolation island
- Via to ground every ½ inch between RIMMs
- Via to ground every ½ inch between RSL signals
- Via between every signal within 100 mils of the MCH edge and the RIMM/MEC connector edge
- No unconnected ground floods
- All ground isolation at lest 10 mils wide
- Ground isolation fills between *serpentines*
- Ground isolation not *broken* by C-TABs
- Ground isolation connects to the ground pins in the middle of the RIMM connectors
- Ground isolation vias connect on all layers and should NOT have thermal relieves
- Ground pins in RIMM connector connect on all layers

Vterm Layout Yields Low Noise (Proper Vterm decoupling is CRITICAL!)

- Solid Vterm-island is on top routing layer; DO NOT split this plane
- Ground island (for ground-side of Vterm caps) is on top routing layer
- Termination Resistors connect DIRECTLY to the Vterm island on the routing (without Vias)
- Decoupling capacitors connect to top layer Vterm-island and top routing layer ground island directly
- Use AT LEAST 2 Vias per decoupling capacitor in the top layer ground island
- Use 2 x 100uF TANTALUM capacitors to decouple Vterm (Aluminum/Electrolytic capacitors are too slow!)
- High-frequency decoupling capacitors MUST be spread-out across the termination-island so that all termination resistors are near high-frequency capacitors
- 100uF TANTALUM capacitors should be at each end of the Vterm-island
- 100uF TANTALUM capacitors must be connected to Vterm-island directly
- 100uF TANTALUM capacitors must have AT LEAST 2 vias/cap to ground
- Vterm-island should be 50 – 75 mils wide and should not be broken
- If any RSL signals are routed out of the 2nd RIMM (towards termination) on a plane referenced to power (even for a short distance), ensure that the Ground Reference Plane (on the power plane) is continuous under the termination resistors/capacitors
- Ensure current path for power delivery to the MRH-R does not go through the Vterm-island

CTM/CTM# Routed Properly

- CTM/CTM# are routed differentially from DRCG to 2nd RIMM
- CTM/CTM# are ground isolated from DRCG to 2nd RIMM
- CTM/CTM# are ground referenced from DRCG to 2nd RIMM
- Vias are placed in ground isolation and ground reference every ½”
- If CTM/CTM# serpentine together, they MUST maintain EXACTLY 6 mils spacing

Clean DRCG Power Supply

- 3.3V DRCG power flood on the top layer.
- High frequency (0.1 uF) capacitors should be placed near the DRCG power pins, with one capacitor next to each power pin.
- 10 uF bulk *tantalum* capacitor near DRCG connected directly to the 3.3V DRCG power flood on the top layer
- Ferrite bead isolating DRCG power flood from 3.3V main power also connecting directly to the 3.3VDRCG power flood on the top layer
- Use 2 vias on the ground-side of each

Good DRCG Output Network Layout

- Series resistors (39 Ω) should be VERY near CTM/CTM# pins and parallel resistors (51 Ω) should be very near series resistors
- CTM/CTM# should be 18 mils wide from the CTM/CTM# pins to the resistors
- CTM/CTM# should be 14 on 6 routed differential as soon as possible after the resistor network
- When not 14 on 6, the clocks should be 18 mils wide
- Ensure CTM/CTM# are ground referenced and the ground reference is connected to the ground plane every ½” to 1”. Also ensure CTM/CTM are ground isolated and the ground isolation is connected to the ground plane every ½” to 1”
- Ensure 15 pF EMI capacitors to ground are removed (the pads are not necessary and removing the pads provides more space for better placement of other components)
- Ensure the 4 pF EMI capacitor (but do not assemble the capacitor)

Good RSL Transmission Lines

- RSL traces are 18 mils wide
- Do NOT neckdown RSL traces to the RIMM connector
- If tight serpentine configuration is necessary, 10 mil ground isolation MUST be between serpentine segments (i.e., an RSL signal CAN NOT serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines).
- RSL traces do not cross power plane splits. RSL signals must also not be routed *on next to* a power plane splits
- Uniform ground isolation flood is exactly 6 mils from the RSL signals at all times
- ALL RSL, CMD/SCK, and CTM/CTM#/CFM/CFM# signals have C-Tabs on each RIMM connector pin
- All RSL signals are routed adjacent to a ground reference plane. This includes all signals from the 2nd RIMM to the termination. If signals are routed referenced to ground from the 2nd RIMM to the termination, the ground reference plane MUST extend under these signals AND include the ground side of the Vterm decoupling capacitors.
- C-Tabs must not cross (or be on top of) power plane splits. They must be ENTIRELY referenced to ground.
- At least 10 mils ground flood isolation required around ALL RSL signals (ground isolation must be exactly 6 mils from RSL signals). Ground flood recommended for isolation. This ground flood should be as close to the MRH-R (and the 1st RIMM) as possible. If possible, connect the flood to the ground balls/pins on the MRH-R/connector.

Clean V_{REF} Routing

- Do not route V_{REF} near high-speed signals and ensure 1 x 0.1 uF capacitor on V_{REF} at each connector
- Use 10 mil wide trace (6 mils minimum)

RSL Routing

- All signals must be length matched within ± 10 mils of the Nominal RSL Length as described in the *Intel® Workstation/Server MEC Design Guide*. Ensure that signals with a dummy via are compensated correctly.
- ALL RSL signals must have 1 via near the MRH-R BGA pad. Signals routed on the bottom layer of the MB will have a “real via” while signals routed on the top layer will have a “dummy via”. Additionally, all signals with a dummy via must have an additional trace length of 25 mils.
- Signals must “alternate” layers as shown in Section 4.2, “Memory Interface” on page 4-6.

RDRAM Clock Routing

- Clock signals must be routed as a differential pair. The traces must be 14 mils wide and 6 mils apart (with no ground isolation.
- Clock signals must be length compensated (using the 1.021 length factor described in Section 4.2, “Memory Interface” on page 4-6). Ensure that each clock pair is length matched within ±2 mils.
- If clock signals serpentine, they must serpentine together (to maintain differential 14:6 routing).
- 22 mils ground isolation required on each side of the differential pair.

8.1.4 I/O Controller Hub (ICH)

8.1.4.1 AC'97 Interface

- ACSDIN[1:0] require external 8.2 KΩ pull-down if a CODEC is not present or if the codec is not powered in suspend.

8.1.4.2 APIC Interface

- If the APIC is not used, 150 Ω pull-ups are required on APICD[1:0] and APICCLK must be tied to GND. The APICCLK can also be connected to CK133W/S if unused but it can not be left floating.

8.1.4.3 FWH Flash BIOS Interface

- The FWH Flash BIOS INIT pin should be connected directly to the processors. This pin must be tied to the FWH Flash BIOS to allow the FWH Flash BIOS to abort its programming sequence in the event that the processor is reset during programming stage.
- ID[3:0] should be tied to GND is only one FWH Flash BIOS is implemented.

8.1.4.4 Hub Interface A

- Initial stepping of the ICH requires a 110 Ω ±1% pull-up to 3.3V on HLAZCOMP. All production stepping requires 40 Ω 1% pull-up to 1.8V on HLAZCOMP.
- There are two options for HLAZCOMP:
  - RCOMP: Connect 40 Ω 1% pull-up resistor to 1.8V.
  - ZCOMP: Connect this signal to a 10 mil wide trace that is 18" long. This trace must be not be terminated and my not cross power planes.

8.1.4.5 IDE

- The ICH should be placed as close as possible to the ATA connector(s). The total signal length, from the IDE drivers to the end of the IDE cable, should be less than 26".
- The capacitance of each of the IDE connector (on the host) pins should be less than 25 pF when the cable is disconnected from the host.
- The following signals do not require series termination resistors: PDD[15:0], SDD[15:0], PDIOW#, SDIOW#, PDIOR#, SDIOR#, PDREQ#, SDREQ#, PDDACK#, SDDACK#, PIORDY, SIORDY, PDA[2:0], SDA[2:0], PDCS1#, SDCS1#, PDCS3#, SDCS3#, IRQ14, IRQ15.
- To allow the host to recognize the absence of a device during power-up, a 10 KΩ pull-down resistor should be placed on unused PDD7 or SDD7. Also if IDE is not implemented, xDREQ and xIORDY should be grounded and other IDE output signals can be left as no connects.
- PCI_RST# should be use as the IDE reset signal and should be connected to pin 1 of the IDE connector(s). The PCIRST# should be buffered to the IDE connector. The IDE reset signal requires series termination.
- Primary IDE connector uses IRQ14 and secondary IDE connector uses IRQ15. These IRQ signals require additional 8.2 KΩ pull-up to 5V.
- Pin 34 of the IDE connector should be connected to a GPI. This allows Ultra ATA/66 cable detection. This pin is sampled low if an 80-pin cable is installed, and is sampled high if a 40-pin cable is installed.

8.1.4.6 LPC SIO

- The SIO PME# should be connected to an ICH resume-well GPI. The SIO PME# should not be connected to the PCI PME# because this would violate the ACPI specification.
- The LPC_SMI# signal can be connected to any ICH GPI. The GPI_ROUTE register provides the ability to generate an SMI# from a GPI assertion.
- Additional pull-up resistors are not require on LFRAME#, LAD[3:0] and LDREQ0#.

8.1.4.7 PCI Interface

- PCI control signals require pull-up resistors to ensure that they contain stable values when no agent is actively driving the bus. Pull-up required: FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, INTD#, REQ64#and ACK64#. SBO# and SDONE must be separately pulled-up with a ~5 KΩ resistor if unused. Also, if boundary scan is not used, TMS and TDI must be independently pulled-up, and TRST# and TCK must be independently pulled-down via 5 KΩ resistors. TDO must be left open.
- 100 Ω series resistor is recommended on IDSEL signals.
- All unused core well inputs must be pulled-up to 3.3V, and unused resume well inputs must be pulled-up to 3.3VSBY.
- The following signals do not require additional pull-up resistors: PME#, PWRBTN#, GNT#[A:B]
- PCI GNT# pull-ups should not be implemented. The GNT# lines are actively driven by the ICH.
- PCIRST# rise time should be evaluated in large I/O systems, buffering may be needed. This signal must be buffered to the IDE connectors.

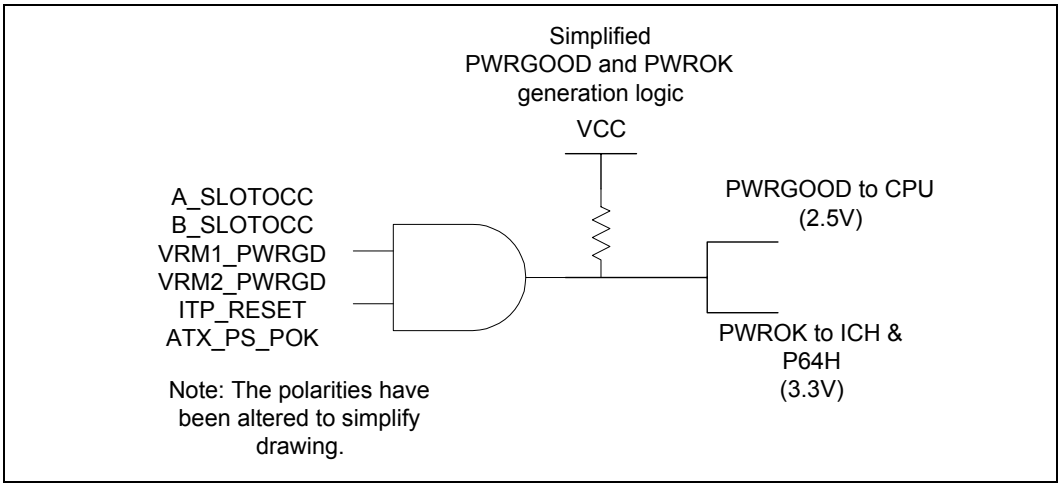
8.1.4.8 Power and Ground

- 5VREF must be tied to 5V in a 5V tolerant or non-tolerant system. This signal must be power up before or simultaneous to VCC5, and it must be power down after or simultaneous to VCC5. In a STR system, 5VREF can be tied to the VCC5 since there will be no 5V signals active during the STR state.
- A Schottky diode in the 5Vref circuit for a minimum voltage drop from VCC3_3 to 5VREF because there is an internal diode in parallel to the Schottky diode that does not have high current capability. The Schottky diode will begin to conduct first, therefore carrying the high current.

8.1.4.9 Power Management

- A power button is required by the ACPI specification. PWRBTN# is connected to the front panel on/off power button. The ICH integrates 16msec debounce logic on this pin and AC power loss circuitry has been integrated into the ICH to detect power failure.
- It is recommended that the PS_POK signal from the power supply connector be routed through a schmitt trigger to square-off and maintain its signal integrity, and not be connected directly to logic on the board. PS_POK logic from the power supply connector can be powered from the core voltage supply.
- RSMRST# logic should be powered by a standby supply, making sure that the input to the ICH is at a 3V level. The RSMST# signal requires a minimum time delay of 1 ms from the rising edge of the standby power supply voltage. A Schmitt trigger circuit is recommended to drive the RSMRST# signal. To provide the required rise time, the 1 ms delay should be placed before the Schmitt trigger circuit. The reference design implements a 20 ms delay at the input of the Schmitt trigger to ensure the Schmitt trigger inverters have sufficiently powered up before switching the input. Also, ensure that voltage on RSMRST# does not exceed VCC (RTC). It is recommended that 3.3V logic be used to drive RSMRST# to alleviate rise time problems when using a resistor divider from VCC5.
- The PWROK signal to the chipset is a 3V signal. The core well power valid to PWROK asserted at the chipset is a minimum of 1 ms. PWROK to the chipset must be deasserted a minimum of 0 ns after RSMRST#.
- PWRGOOD signal to processor is driven with an open collector buffer pulled up to 2.5V using a 330 ohm resistor.
- Figure 8-1 is a simplified diagram of the PWRGOOD and PWROK logic, connected to the processor slots and ICH respectively in a DP system. The circuitry checks for both slots occupied, both processor VRMs powered up, and the PS_POK signal from the ATX power supply connector before asserting PWRGOOD and PWROK to the processor, ICH and P64H.

Figure 8-1. PWRGOOD and PWROK Logic



- RI# can be connected to the serial port if this feature is used. To implement ring indicate as a wake event, the RS232 transceiver driving the RI# signal must be powered when the ICH suspend well is powered. This can be achieved with a serial port transceiver powered from the standby well that implements a shut-down feature.
- The SLP_S3# signal from the ICH must be inverted and then connected to SLEEP of the WTX power supply connector to control the state of the core well during sleep states.
- The PS_ON of the WTX power supply connector is controlled by ICH SLP_S5# and P0/P1_PRES signals.

8.1.4.10 RTC

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1". It is recommended to minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them), and place a ground plane under all of the external RTC circuitry. Do not route any switching signals under the external components (unless on the other side of the ground plane)
- Provide a 1 uF 805 X5R dielectric, monolithic, ceramic capacitor on the VCCRTC pin. The cap +ve connection should not be stubbed off the trace run and must be as close as possible to the ICH. If a stub is required, it should be within a few mm of the maximum length. The ground connection must be made through a via to the plane with no trace between the capacitor pad and the via.
- Place the battery, 1 KΩ series current limit resistor, and the common-cathode isolation diode very close to the ICH. If this is not possible, place the common-cathode diode and the 1 KΩ resistor as close to the 1 uF capacitor as possible. Do not place these components between the cap and the ICH. The battery can be placed remotely from the ICH.
- On boards that have chassis-intrusion utilizing inverters powered by the VCCRTC pin, place the inverters as close to the common-cathode diode as possible. If this is not possible, keep the trace run near the center of the board.

8.1.4.11 SMBus/Alert Bus

- If the Alert-on-LAN signals are used, then 4.7 KΩ pull-up resistors to 3.3VSBY are required. Otherwise, if the Alert-on-LAN signals are used as GPIOs, pull-up resistors to 3.3VSBY are required. The signals must be allowed to change states on power-up. The pull-up resistor values depend on the loading on the GPIO signals.
- ALERTCLK and ALERTDATA requires 4.7 KΩ pull-up resistors to 3.3VSBY if unused.
- SMBus implementation needs to provide proper isolation if there are SMBus devices that are both powered by VCC and VCCSBY. SMBus devices powered by 3.3VCCSBY requires pull-up resistors.
- The value if the SMBus pull-up resistors should reflect the number of loads on the bus. For implementation with 4-5 loads, 4.7 KΩ are recommended. OEMs should complete simulation to determine the exact value.

8.1.4.12 USB Interface

- The AGP OVRCNT# pin should be pulled-up with a 330 KΩ resistor to 3.3V, on the motherboard, to prevent this line from floating when add-in card is not present.
- 15 Ω resistors should be used on D-/D+ data lines.
- VCC USB (cable power) should be power off the 5V source, rather than 5VSBY.
- The resistive component of the fuses, ferrite beads and traces must be considered when choosing components and power/GND trace width. This must be done such that the resistance between the 5VCC power supply and the host USB port is minimized. Minimizing the resistance will also minimize voltage drop seen along the path.
- Sufficient bypass capacitance should be located near the host USB receptacles. This is to minimize the voltage droop that occurs upon hot attach of new devices.

8.1.5 FWH Flash BIOS

- If an ATE is used to program the FWH Flash BIOS, it is recommended that pull-up resistors be added to the FGPI pins. Otherwise, unused FGPI pins can be tied to VCC or GND.
- FWH Flash BIOS INIT# should be connected to processor INIT#.
- FWH Flash BIOS RST# must be connected to ICH PCIRST#.

8.1.6 PCI 64-bit Hub (P64H)

8.1.6.1 APIC Interface

- All I/O APIC IRQs are wired OR to BT_INTR#. The BT_INTR# signal should be connected to ICH PCI interrupt to support boot devices on the P64H PCI segment. This signal is internally disabled once the I/O APIC is enabled.
- External pull-up resistors are required on APICCLK and APICD[1:0] if P64H APIC is not used.
- Additional pull-up resistors are recommended on all IRQ signals.

8.1.6.2 Hub Interface B

- HUBREF reference voltage is 2/3 1.8V.
- HLBRCOMP requires a 30 ohm pull-down resistor to GND.

8.1.6.3 PCI Interface

- Per the PCI Specification, pull-up resistor must be added to AD[63:32], C/BE[7:4]#, and PAR64. This prevent floating input if a 32-bit PCI card is installed into a 64-bit PCI connector.
- PCI GNT# pull-up resistor should not be implemented. These signals are actively driven by the P64H.

8.1.6.4 PCI Clocks

- Unused clock outputs (PCLKOUT) can be left as N/C. These clock outputs must be disable via the P64H Configuration register.

8.1.6.5 Power and Ground

- PCI 66 MHz operates with 3.3V signaling only.
- PVCC5REF and VCC5REF are P64H voltage reference pins. For a 3.3V-only environment, these signals can be tied together to a 3.3V source. For a 5V tolerant environment, a Schottky diode should be used to ensure that the 5V reference voltage powers up before or simultaneous to the 3.3V source.
- VCC5REF (ball P7) is used for the hot plug interface and RSTIN#.
- VCC5REF (ball H17) is used for the IRQs, TEST# and BT_INTR#.
- PVCC5REF (ball F4) is used for the PCI interface.

8.1.7 CK133W/S Clock Synthesizer

- All unused clock outputs should be tied to GDN through a series resistor. The resistor value should be the approximately the impedance of the output buffer. The intent of these termination resistors is to eliminate the EMI radiation.
- 33 Ω series resistors are recommended on all clock outputs.
- Ganging the CPUCLK signals improves the output-to-output skew. This implementation requires that all CPUCLK signals be tied (short) together.
- If power-down mode is not supported, it is recommended that PWRDWN# be pulled-up with to 3.3V via a 10 KΩ resistor.
- SEL pins can be used to select special functionality using 10 KΩ pull-up resistors:

SEL133/100#	SEL1	SEL0	Function
0	0	0	Tri-state
0	0	1	RESERVED
0	1	0	Active 100 MHz, 48 MHz PLL inactive
0	1	1	Active 100 MHz, 48 MHz PLL active
1	0	0	Test Mode
1	0	1	RESERVED
1	1	0	Active 133 MHz, 48 MHz PLL inactive
1	1	1	Active 133 MHz, 48 MHz PLL active

Check with the clock vendor and reference schematics for decoupling considerations.

8.2 Design Checklist

The following checklist is intended to be use for Intel® 840 chipset design schematic reviews. This checklist should be use with the Intel® 840 Chipset Customer Reference Schematics in Appendix A, “Reference Schematics”. This checklist represents only one possible system configuration and will be revised as new information becomes available.

Note: VCC, VSS, and GND signals are not included into the below connectivity checklist.

8.3 Intel® Pentium® III Processor Checklist

The following checklist is intended to be use for Intel® 840 Chipset design schematic reviews. This checklist represents dual processor- Intel® Pentium® III processor design ONLY. This checklist supports Intel Pentium® II processors that use a 100 MHz system bus, Intel Pentium III processors to a FMB guideline of 19.3A, and Intel Pentium III SECC2 (SC242) processors to the current FMB guideline of 18.4 A.

For UP designs, the “UP PIN CONNECTION (CPU0)” column should be used. For DP designs, the “UP PIN CONNECTION (CPU0)” and “DP PIN CONNECTION (CPU1)” columns should both be used.

Table 8-1. 2-Way SC242 Connectivity (AGTL+)

AGTL+	CPU0 Pin Connection	CPU1 Pin Connection
A[35:3]#	Connect to MCH	Connect to CPU0
ADS#	Connect to MCH	Connect to CPU0
AERR#	Leave as N/C (not supported by chipset)	Leave as N/C (not supported by chipset)
AP[1:0]#	Connect to MCH	Connect to CPU0
BERR#	Connect to MCH	Connect to CPU0
BINIT#	Leave as N/C (not supported by chipset)	Leave as N/C (not supported by chipset)
BNR#	Connect to MCH	Connect to CPU0
BP[3:2]#	Leave as N/C	Leave as N/C
BPM[1:0]	Leave as N/C	Leave as N/C
BPRI#	Connect to MCH	Connect to CPU0
BR0#	Connect to MCH (BREQ0#) and CPU1 (BR1#)	Connect to CPU0 (BR1#)
BR1#	Connect to CPU1 (BR0#)	Connect to MCH (BREQ0#) and CPU0 (BR0#)
D[63:0]#	Connect to MCH	Connect to CPU0
DBSY#	Connect to MCH	Connect to CPU0
DEFER#	Connect to MCH	Connect to CPU0
DEP[7:0]#	Connect to MCH	Connect to CPU0
DRDY#	Connect to MCH	Connect to CPU0
HIT#	Connect to MCH	Connect to CPU0
HITM#	Connect to MCH	Connect to CPU0
LOCK#	Connect to MCH	Connect to CPU0
REQ[4:0]#	Connect to MCH	Connect to CPU0
RESET#	Connect to MCH and connect to ITP pin 1 (RESET#) with 240Ω series resistor	Connect to CPU0
RP#	Connect to MCH	Connect to CPU0
RS[2:0]#	Connect to MCH	Connect to CPU0
RSP#	Connect to MCH	Connect to CPU0
TRDY#	Connect to MCH	Connect to CPU0

Table 8-2. 2-Way SC242 Connectivity (CMOS)

CMOS	CPU0 PIN CONNECTION	CPU1 PIN CONNECTION
A20M#	Connect to ICH with 150 Ω pull-up to $VCC_{2.5}$	Connect to CPU0
FERR#	Connect to ICH with 150Ω pull-up to $VCC_{2.5}$	Connect to CPU0
FLUSH#	150 Ω pull-up to $VCC_{2.5}$ (not used by chipset)	Connect to CPU0
IERR#	Connect to MCH IERR#	Connect to MCH IERR#
IGNNE#	Connect to ICH with 150 Ω pull-up to $VCC_{2.5}$	Connect to CPU0
INIT#	Connect to ICH and FWH Flash BIOS with 150 Ω pull-up to $VCC_{2.5}$	Connect to CPU0
LINT0/INTR	Connect to ICH with 150 Ω pull-up to $VCC_{2.5}$	Connect to CPU0
LINT1/NMI	Connect to ICH with 150 Ω pull-up to $VCC_{2.5}$	Connect to CPU0
PICD[1:0]	Connect to ICH	Connect to CPU0 with two 300–330 Ω pull-ups to $VCC_{2.5}$ located at opposite ends of the trace. If used, connect to P64H (APICD[1:0]) and terminate at the P64H rather than the ICH.
PWRGOOD	Connect to PWRGOOD logic with 150-330 Ω pull-up to $VCC_{2.5}$	Connect to CPU0
SLP#	Connect to ICH with 150 Ω pull-up to $VCC_{2.5}$	Connect to CPU0
SMI#	Connect to ICH with 150 Ω pull-up to $VCC_{2.5}$	Connect to CPU0
STPCLK#	Connect to ICH with 150 Ω pull-up to $VCC_{2.5}$	Connect to CPU0
THERMTRIP#	Connect to power-off logic or ASIC with 150Ω pull-up to $VCC_{2.5}$, or leave as N/C	Connect to CPU0, or could tie to a separate monitoring ASIC with 150Ω pull-up to $VCC_{2.5}$, or leave as N/C

Figure 8-2. Routing Topology Example for PICD[1:0]

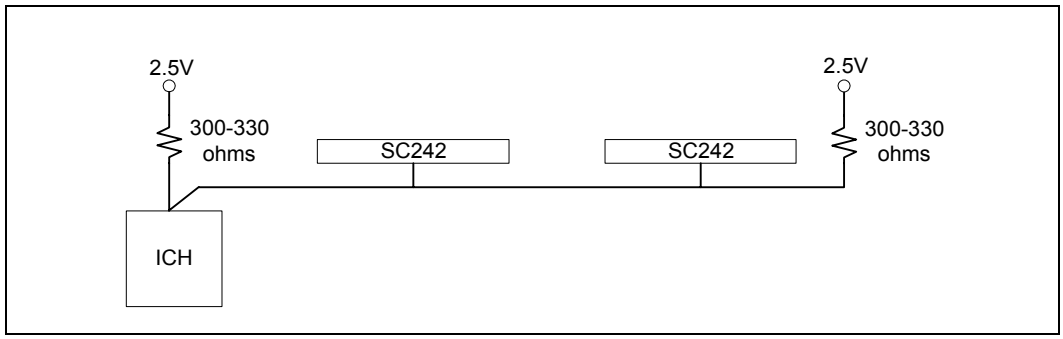


Figure 8-3. Routing Topology Example for PICD[1:0] with P64H

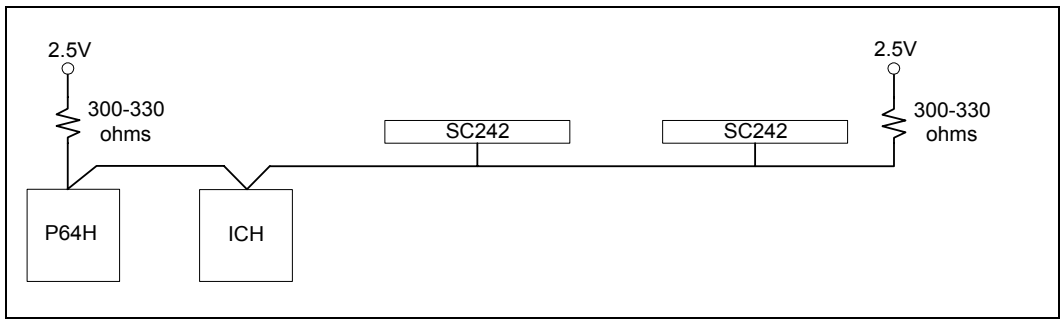


Table 8-3. 2-Way SC242 Connectivity (TAP)

TAP	CPU0 Pin Connection	CPU1 Pin Connection
PRDY#	Connect to ITP pin 18 (PRDY0#) with 240 Ω series resistor and 150 Ω pull-up to VTT (series resistor needs to be placed next to the debug port with the termination resistor on the processor side)	Connect to ITP pin 22 (PRDY1#) with 240 Ω series resistor and 150 Ω pull-up to VTT (series resistor needs to be placed next to the debug port with the termination resistor on the processor side)
PREQ#	Connect to ITP pin 16 (PREQ0#) with 200-330 Ω pull-up to $VCC_{2.5}$	Connect to ITP pin 20 (PREQ1#) with 200-330 Ω pull-up to $VCC_{2.5}$
TCK	Each processor should receive a separately buffered copy of TCK from ITP pin 5 (TCK), where the given capacitance and inductance values are for illustration and must be determined by simulation)	
TDO	Connect to CPU1 (TDI) with 150 Ω pull-up to $VCC_{2.5}$	Connect to ITP pin 10 (TDO) with 150 Ω pull-up to $VCC_{2.5}$
TDI	Connect to ITP pin 8 (TDI) with 150–330 Ω pull-up to $VCC_{2.5}$	Connect to CPU0 (TDO) with 150 Ω pull-up to $VCC_{2.5}$
TMS	Each processor should receive a separately buffered copy of TCK from ITP pin 7 (TMS), where the given capacitance and inductance values are for illustration and must be determined by simulation)	
TRST#	Connect to ITP pin 12 (TRST#)	Connect to CPU0 with ~680 Ω pull-down to GND

Figure 8-4. TCK/TMS Implementation Example for DP Designs

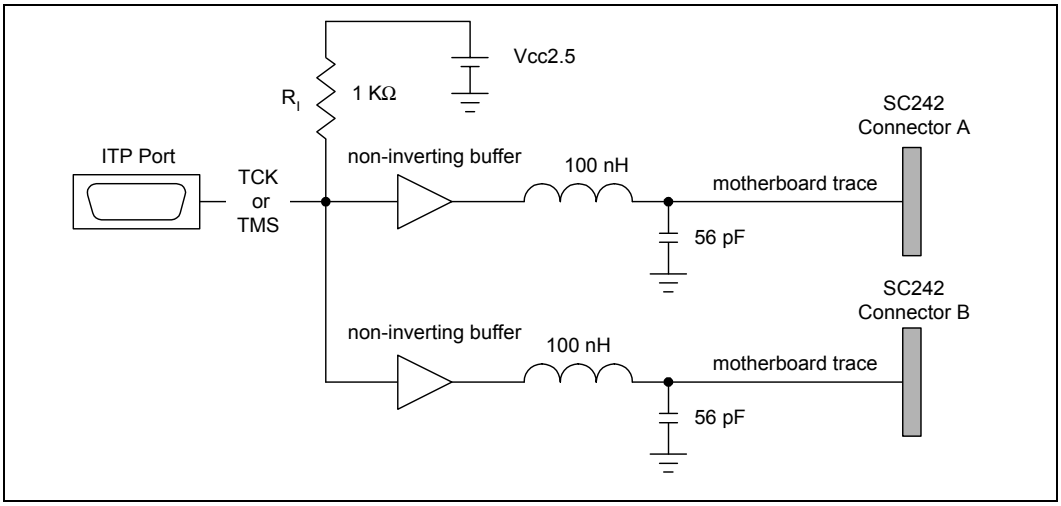


Figure 8-5. ITP Diagram

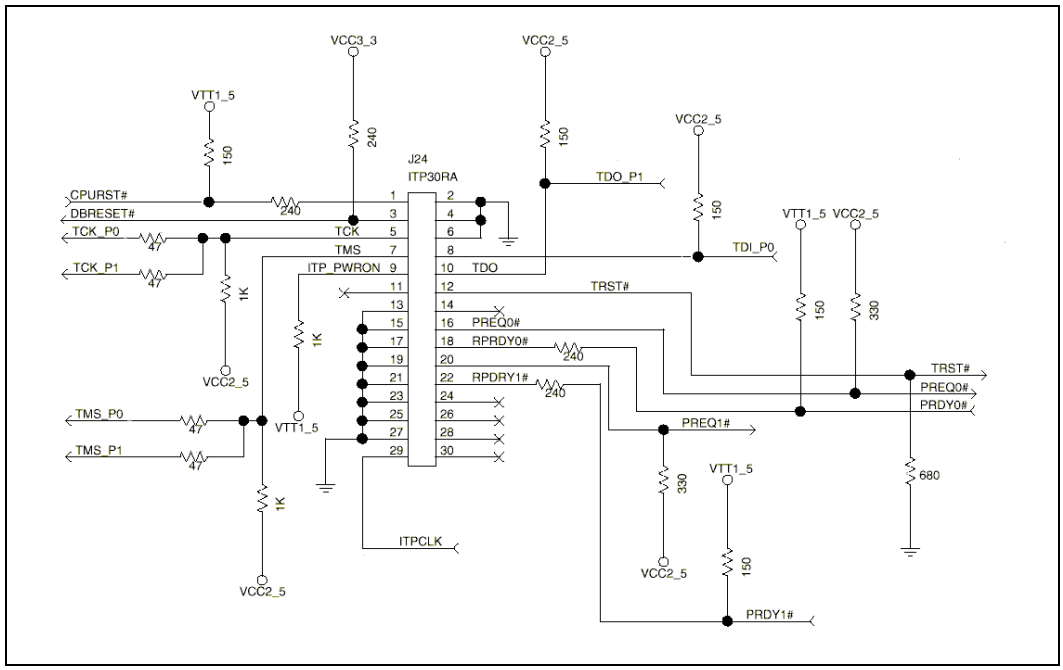


Table 8-4. 2-Way SC242 Connectivity (Clocks)

Clock	CPU0 Pin Connection	CPU1 Pin Connection
BCLK	Connect to CK133W with 22–33 Ω series resistor (based on clock driver characteristics) To reduce pin-to-pin skew, tie all host clock outputs together at the clock driver then route to the MCH and processors	Use a separate BCLK from CPU0 and gang/terminate as described
PICCLK	Connect to CK133W with 22–33 Ω series resistor (though OEM needs to simulate based on driver characteristics)	Use separate PICCLK from CPU0 and terminate as described

Table 8-5. 2-Way SC242 Connectivity (Power/Other)

Power/Other	CPU0 Pin Connection	CPU1 Pin Connection
BSEL0	Connect to PWRGOOD logic with 220 Ω pull-up to 3.3V, where a logic-low will ground PWRGOOD	Connect to CPU0
BSEL1	Connect to CK133W (133/100#) with 220 Ω pull-up to 3.3V and connect to MCH (HL10) with 8.2 kΩ series resistor	Connect to CPU0
EMI[4:0]	Pull-down to GND with 0 Ω resistor	Implement in same manner as CPU0
SLOTOCC#	Connect to PWRGOOD logic (to prevent system from powering up if no processor is present), GND, or leave as N/C If used, 1 KΩ–10 KΩ pull-up to any voltage	Implement in same manner as CPU0
TESTHI	1k-100 KΩ pull-up to $VCC_{2.5}$ If a legacy design pulls this up to VCC_{CORE}, use a 1 KΩ – 10 KΩ pull-up	Implement in same manner as CPU0
VCC_{CORE}	Connect to core voltage regulator and provide low frequency decoupling	Implement in same manner as CPU0
VID[4:0]	Connect to core voltage regulator (may require 10 KΩ pull-up if regulator does not have internal pull-ups) Optional override (jumpers, ASIC, etc) could be used for debug purposes May also connect to system monitoring device	Implement in same manner as CPU0 where CPU0 and CPU1 have different regulators
V_{TT}	Connect to 1.5V regulator and provide high and low frequency decoupling	Implement in same manner as CPU0
Reserved	The following pins must be left as no-connects: A16, A47, A88, A113, A116, B12, B20, B76, and B112	Implement in same manner as CPU0

8.3.1 Intel® Pentium® III Xeon™ Processor at 600+ MHz Checklist

The following checklist is intended to be use for Intel® 840 chipset design schematic reviews. This checklist should be use with the *Intel® 840 Chipset Customer Reference Schematics*. This checklist represents only one possible system configuration, and it will be revised as new information becomes available. Note that VCC, VSS, and GND signals are not included in the following connectivity checklist.

Table 8-6. 2-Way SC330 Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
A20M#	Two 300 Ω PU to VCC2.5	Connect to CPUs and ICH.
ADS#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
AERR#	N/C	
AP#[1:0]	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
BCLK		Connect to clock synthesizer, CPU and MCH
BERR#	85 Ω/15 0Ω PU to VTT1.5	Connect to CPUs and MCH.
BINIT#	N/C	
BNR#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
BP#[3:2]	N/C	
BPM#[1:0]	N/C	
BPRI#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
BREQ#[1:0]	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
BREQ#[3:2]	N/C	See Table 9
CPURST#	85 Ω/150 Ω PU to VCC1.5	Connect to ITP connector, CPUs, and MCH.
DBSY#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
DEFER#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
DEP#[7:0]	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
DRDY#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
FERR#	Two 300 Ω PU to VCC2.5	Connect to CPUs and ICH.
FLUSH#	Two 300 Ω PU to VCC2.5	Connect to CPUs.
FRCERR	N/C	
HA#[35:3]	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
HD#[63:0]	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
HIT#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
HITM#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
HLOCK#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
HREQ#[4:0]	85 Ω/150Ω PU to VTT1.5	Connect CPUs and MCH.
IERR#	Two 300Ω PU to VCC2.5	Connect to CPUs and MCH.
IGNNE#	Two 300 Ω PU to VCC2.5	Connect to CPUs and ICH.
INIT#	Two 300 Ω PU to VCC2.5	Connect to CPUs, ICH and FWH Flash BIOS.
LINT[1:0]	Two 300 Ω PU to VCC2.5	Connect to CPUs and ICH.
OCVR_EN		Connect to CPUs and processor VRM.
OCVR_OK#/ VRM_PWRGD		Connect to CPUs, processor VRM and system logic.
PICCLK		Connect to clock synthesizer and APIC agents.

Table 8-6. 2-Way SC330 Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
PICD[1:0]	Two 300 Ω PU to VCC2.5	Connect to CPUs, ICH and P64H. Connect to CPUs and ICH only if P64H is not used.
PO_VID_CORE [4:0]	10 KΩ PU to VCC5	Connect to processor VRM
PO_VID_L2[4:0]	10 KΩ PU to VCC5	Connect to L2 cache VRM
PRDY#	50 Ω PU to VTT1.5	Connect to ITP connector.
PREQ#	330 Ω PU to VCC2.5	Connect to ITP connector.
PWR_EN[1:0]	10 KΩ PU to VCC3.3STBY	Connect to system logic that detects presence of processor or termination card in each slot.
PWRGOOD	330 Ω PU to VCC2.5	Connect to processors and PWRGOOD circuitry.
RP#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
RS#[2:0]	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
RSP#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
SA[2:0]		For SMBus address.
SELFSB0	1KΩ PU to VCC2.5	Connect to CPUs.
SELFSB1	2KΩ PU to VCC2.5	Connect to CPUs, MCH, and clock circuitry. PU value may change depending on implementation.
SLP#	300 Ω PU to VCC2.5	Connect to CPUs and ICH.
SMBALERT#		Connect to CPUs and ICH
SMBCLK		Connect to CPUs and ICH.
SMBDATA		Connect to CPUs and ICH.
SMI#	Two 300 Ω PU to VCC2.5	Connect to CPUs and ICH.
STPCLK#	Two 300 Ω PU to VCC2.5	Connect to CPUs and ICH.
TCK		Connect to ITP connector.
TDO		Connect CPU1 TDO to CPU2 TDI. Connect CPU2 TDO to ITP TDO.
TDI	150 Ω PU to VCC2.5 only necessary on last device in scan chain.	Connect to CPU1 TDO to CPU2 TDI. Connect to ITP TDI to CPU0 TDI.
THERMTRIP#	N/C (if not used) 300 Ω pull-up resistor to VCC2.5 (if used)	
TMS	1 KΩ PU to VCC2.5	Connect to ITP connector and CPUs.
TRDY#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and MCH.
TRST#	680 Ω PD to GND	Connect to ITP and CPUs.
WP		Connect to CPUs, ICH, and MECC.

8.3.2 82840 Memory Controller Hub (MCH)

Table 8-7. MCH Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
ADS#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
ADSTB0	8.2 KΩ PU to VDDQ	Connect to AGP device.
ADSTB0#	8.2 KΩ PD to GND	Connect to AGP device.
ADSTB1	8.2 KΩ PU to VDDQ	Connect to AGP device.
ADSTB1#	8.2 KΩ PD to GND	Connect to AGP device.
AGPRCOMP	40.2 Ω PD to GND	
AGPREF		Connect to AGP voltage reference circuit.
AP0#	85 Ω/150 Ω PU to VTT1_5	Connect to CPUs.
AP1#	85 Ω/150 Ω PU to VTT1_5	Connect to CPUs.
BERR#	85 Ω/150 Ω PU to VTT1_5	Connect to CPUs.
BNR#	85 Ω/150 Ω PU to VTT1_5	Connect to CPUs.
BPRI#	85 Ω/150 Ω PU to VTT1_5	Connect to CPUs.
BREQ0#	85 Ω/150 Ω PU to VTT1_5	Connect to CPUs.
CHA_CFM		Connect to MECC.
CHA_CFM#		Connect to MECC.
CHA_CMD		Connect to MECC.
CHA_CTM		Connect to MECC.
CHA_CTM#		Connect to MECC.
CHA_DQA[8:0]		Connect to MECC.
CHA_DQB[8:0]		Connect to MECC.
CHA_EXP0		Connect to MECC.
CHA_EXP1		Connect to MECC.
CHA_REF0		Connect to CHA_REF noise filter/ reference circuit.
CHA_REF1		Connect to CHA_REF noise filter/ reference circuit.
CHA_RQ[7:0]		Connect to MECC.
CHA_SCK		Connect to MECC.
CHA_SIO		Connect to MECC.
CHB_CFM		Connect to MECC.
CHB_CFM#		Connect to MECC.
CHB_CMD		Connect to MECC.
CHB_CTM		Connect to MECC.
CHB_CTM#		Connect to MECC.
CHB_DQA[8:0]		Connect to MECC.
CHB_DQB[8:0]		Connect to MECC.

Table 8-7. MCH Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
CHB_EXP0		Connect to MECC.
CHB_EXP1		Connect to MECC.
CHB_REF0		Connect to CHB_REF noise filter/ reference circuit.
CHB_REF1		Connect to CHB_REF noise filter/ reference circuit.
CHB_RQ[7:0]		Connect to MECC.
CHB_SCK		Connect to MECC.
CHB_SIO		Connect to MECC.
CLK66		Connect to clock synthesizer.
CPURST#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs and ITP connector.
DBSY#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
DEFER#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
DEP[7:0]#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
DRDY#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
GAD[31:0]		Connect to AGP device.
GC/BE[3:0]#		Connect to AGP device.
GDEVSEL#	8.2 KΩ PU to VDDQ	Connect to AGP device.
GFRAME#	8.2 KΩ PU to VDDQ	Connect to AGP device.
GGNT#	8.2 KΩ PU to VDDQ	Connect to AGP device.
GIRDY#	8.2 KΩ PU to VDDQ	Connect to AGP device.
GPAR	8.2 KΩ PU to VDDQ	Connect to AGP device.
GREQ#	8.2 KΩ PU to VDDQ	Connect to AGP device.
GSERR#	8.2 KΩ PU to VDDQ	Connect to AGP device.
GSTOP#	8.2 KΩ PU to VDDQ	Connect to AGP device.
GTLREFA	75 Ω/150 Ω	Connect to resistor divider circuit.
GTLREFB	75 Ω/150 Ω	Connect to resistor divider circuit.
GTRDY#	8.2 KΩ PU to VDDQ	Connect to AGP device.
HA[35:3]#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
HCLKIN		Connect to clock synthesizer.
HCLKOUTA		Connect to DRCG.
HCLKOUTB		Connect to DRCG
HD[63:0]#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
HIT#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
HITM#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
HLA[11:0]		Connect to ICH.
HLA_REF		Connect to HLA HUBREF generation circuit.
HLA_STB		Connect to ICH.
HLA_STB#		Connect to ICH.

Table 8-7. MCH Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
HLA_RCOMP	40.2 Ω PU to VCC1.8	
HLB[19:0]		Connect to P64H.
HLBREF		Connect to HLB HUBREF generation circuit.
HLB_STB0		Connect to P64H.
HLB_STB0#		Connect to P64H.
HLB_STB1		Connect to P64H.
HLB_STB1#		Connect to P64H.
HLB_ZCOMP	30 Ω PD to GND	
HLOCK#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
HREQ[4:0]#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
HTRDY#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
IERR#	300 Ω PU to VCC2.5	Connect to CPUs.
OVERT#	10 KΩ PU to VCC1.8	
PIPE#	8.2 KΩ PU to VDDQ	Connect to AGP device.
RBF#	8.2 KΩ PU to VDDQ	Connect to AGP device.
RCLKOUTA		Connect to DRCG
RCLKOUTB		Connect to DRCG
RP#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
RS[2:0]#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
RSP#	85 Ω/150 Ω PU to VTT1.5	Connect to CPUs.
RSTIN#		Connect to ICH.
SBA[7:0]		Connect to AGP device.
SBSTB	8.2 KΩ PU to VDDQ	Connect to AGP device.
SBSTB#	8.2 KΩ PD to GND	Connect to AGP device.
ST[2:0]	8.2 KΩ PU to VDDQ	Connect to AGP device.
TEST#	10 KΩ P/U to VCC1.8	
WBF#	8.2 KΩ PU to VDDQ	Connect to AGP device.

8.3.3 I/O Controller Hub (ICH)

Table 8-8. ICH Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
A20GATE	8.2 KΩ PU to VCC3.3	Connect to SIO.
A20M#	Two 300Ω PU to VCC2.5	Connect to CPUs.
AC_BITCLK		Connect to audio codec
AC_RST#		Connect to audio codec
AC_SDIN0		Connect to audio codec
AC_SDIN1/GPIO9	8.2 KΩ PD to GND	
AC_SDOUT		Connect to audio codec
AC_SYNC		Connect to audio codec
AD[31:0]		Connect to all PCI connectors/ devices.
APICCLK		Connect to clock synthesizer.
APICD0	Two 300 Ω PU to VCC2.5	Connect to CPUs, ICH and P64H.
APICD1	Two 300 Ω PU to VCC2.5	Connect to CPUs, ICH and P64H.
C/BE[3:0]#		Connect to all PCI connectors/ devices.
CLK14		Connect to clock synthesizer.
CLK48		Connect to clock synthesizer
CLK66		Connect to clock synthesizer
CPUSLP#	300 Ω PU to VCC2.5	Connect to CPUs.
DEVSEL#	8.2 KΩ PU to VCC3.3	Connect to all PCI connectors/ devices.
FERR#	Two 300 Ω PU to VCC2.5	Connect to CPUs.
FRAME#	8.2 KΩ PU to VCC3.3	Connect to all PCI connectors/ devices.
GNT[4:0]#		Connect to PCI connectors/devices.
GPIO0/ REQA#	8.2 KΩ PU to VCC3.3	
GPIO1/REQB#/ REQ5#	8.2 KΩ PU to VCC3.3	Connect to PCI connector/device.
GPIO10/ INTRUDER#	8.2 KΩ PU to VCC3.3SBY	
GPIO11/ SMBALERT#	8.2 KΩ PU to VCC3.3SBY	
GPIO12	8.2 KΩ PU to VCC3.3SBY	
GPIO13	8.2 KΩ PU to VCC3.3SBY	
GPIO16/ GNTA#	N/C	
GPIO17/ GNTB#/ GNT5#		Connect to PCI device.
GPIO21/ WP_EEPROM		Connect to CPUs and MECC.
GPIO22	N/C	
GPIO23	4.7 KΩ PD to GND	Connect to front panel LEDs.

Table 8-8. ICH Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
GPIO24/ SLP_S3#		Connect to power connector.
GPIO25/ SUSSTAT#		
GPIO27/ ALERTCLK	4.7 KΩ PU to VCC3.3SBY	Connect to 82559.
GPIO28/ ALERTDATA	4.7 KΩ PU to VCC3.3SBY	Connect to 82559.
GPIO5	8.2 KΩ PU to VCC3.3	Connect to LPC SIO device.
GPIO6	8.2 KΩ PU to VCC3.3	Connect to LPC SIO device.
GPIO8/ LDRQ1#	8.2 KΩ PU to VCC3.3SBY	
GPIO9/ AC_SDIN1	8.2 KΩ PD to GND	
HLA[11:0]		Connect to MCH.
HL_STB		Connect to MCH.
HL_STB#		Connect to MCH.
HLCOMP	40.2 Ω PU to VCC1.8	
HUBREF		Connect to HUBREF generation circuit.
IGNNE#	Two 300 Ω PU to VCC2.5	Connect to CPUs.
INIT#	Two 300 Ω PU to VCC2.5	Connect to CPUs, FWH Flash BIOS.
INTR	Two 300 Ω PU to VCC2.5	Connect to CPUs.
IRDY#	8.2 KΩ PU to VCC3.3	Connect to PCI devices, 82559 and ICH.
IRQ14	8.2 KΩ PU to VCC5	Connect to IDE connector.
IRQ15	8.2 KΩ PU to VCC5	Connect to IDE connector.
LAD0/ FWH0		Connect to FWH Flash BIOS and LPC SIO device.
LAD1/ FWH1		Connect to FWH Flash BIOS and LPC SIO device.
LAD2/ FWH2		Connect to FWH Flash BIOS and LPC SIO device.
LAD3/ FWH3		Connect to FWH Flash BIOS and LPC SIO device.
LDRQ0#		Connect to LPC SIO device.
LFRAME#/ FWH4		Connect to FWH Flash BIOS and LPC SIO device.
NMI	Two 300 Ω PU to VCC2.5	Connect to CPUs.
OC0#		Connect to USB connector.
OC1#		Connect to USB connector.
PAR		Connect to all PCI devices.
PCICLK		Connect to clock synthesizer.
PCIRST#	33 Ω series resistor to IDE connector.	Connect through buffer logic to MCH, P64H, FWH Flash BIOS, LPC SIO, MECC, AGP and all PCI devices.
PDA[2:0]		Connect to primary IDE connector.
PDCS1#		Connect to primary IDE connector.

Table 8-8. ICH Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
PDCS3#		Connect to primary IDE connector.
PDD[15:0]	10 KΩ PD to GND on PDD7.	Connect to primary IDE connector.
PDDACK#		Connect to primary IDE connector.
PDDREQ	5.6KΩ PD to GND	Connect to primary IDE connector.
PDIOR#		Connect to primary IDE connector.
PDIOW#		Connect to primary IDE connector.
PERR#/ GPIO7	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
PIORDY	1 KΩ PU to VCC5	Connect to primary IDE connector.
PIRQA#	8.2 KΩ PU to VCC3.3	Connect to AGP and all PCI devices.
PIRQB#	8.2 KΩ PU to VCC3.3	Connect to AGP and all PCI devices.
PIRQC#	8.2 KΩ PU to VCC3.3	Connect to AGP and all PCI devices.
PIRQD#	8.2 KΩ PU to VCC3.3	Connect to AGP and all PCI devices.
PLOCK#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
PME#		Connect to AGP and all PCI devices.
PWRBTN#		Connect VCC3.3SBY.
PWROK		Connect to PWROK logic.
RCIN#	8.2 KΩ PU to VCC3.3	Connect to LPC SIO.
REQ[4:0]#	8.2 KΩ PU to VCC3.3	Connect to PCI devices.
RI#		Connect to serial port and RI logic.
RTCRST#	CLR CMOS: 1 KΩ to GND.	NORMAL: generated from VCC3.3SBY
RTCX1		Connect to clock crystal.
RTCX2		Connect to clock crystal.
SDA[2:0]		Connect to secondary IDE connector.
SDCS1#		Connect to secondary IDE connector.
SDCS3#		Connect to secondary IDE connector.
SDD[15:0]	10 KΩ PD to GND on SDD7.	Connect to secondary IDE connector.
SDDACK#		Connect to secondary IDE connector.
SDDREQ	5.6 KΩ PD to GND	Connect to secondary IDE connector.
SDIOR#		Connect to secondary IDE connector.
SDIOW#		Connect to secondary IDE connector.
SERIRQ	8.2 KΩ PU to VCC3.3	Connect to LPC SIO.
SERR#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
SIORDY	1 KΩ PU to VCC5	Connect to secondary IDE connector.
SLP_S5#		Connect to Power Connectors
SMBCLK	4.7 KΩ PU to VCC3.3	Connect to CPUs and MECC.
SMBDATA	4.7 KΩ PU to VCC3.3	Connect to CPUs and MECC.
SMI#	Two 300 Ω PU to VCC2.5	Connect to CPUs.

Table 8-8. ICH Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
SPKR		Connect to audio codec or speaker circuit.
STOP#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
STPCLK#	Two 300 Ω PU to VCC2.5	Connect to CPUs.
SUSCLK/ GPIO26		Connect to LEDs.
THRM#	8.2 KΩ PU to VCC3.3	Connect to CPUs.
TRDY#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
USBP0-		Connect to USB port.
USBP0+		Connect to USB port.
USBP1-		Connect to USB port.
USBP1+		Connect to USB port.
VBIAS		Connect to RTCX1 through a 10 MΩ resistor and to VCCRTC through a 0.047 µF capacitor.
VCCRTC		Connect to VCC3.3SBY.
VCCSUS0/1		Connect to VCC3.3SBY.
VCC5REF	1 KΩ PU to VCC5.	Connect to VCC3.3 via a schottky diode.

8.3.4 FWH Flash BIOS – 40Lead TSOP

Table 8-9. FWH Flash BIOS Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
CLK		Connect to clock synthesizer.
FGP[14:10]	8.2 KΩ PD to GND	
FWH[3:0]		Connect to ICH and LPC SIO.
FWH4		Connect to ICH and LPC SIO.
IC	8.2 KΩ PD to GND	
ID[3:0]		Connect to GND.
INIT#	Two 300 Ω PU to VCC2.5	Connect to processors and ICH.
NC[6:3]	N/C	
NC1	N/C	
NC[14:13]	N/C	
NC8	N/C	
RFU[36:32]	N/C	
RST#		Connect to all PCI devices off of the ICH.
TBL#		Connect to VCC3.3.
VPP		Connect to VCC3.3.
WP#	4.7 KΩ PU to VCC3.3	

8.3.5 PCI 64-bit Hub (P64H)

This checklist section corresponds to the Intel® 840 chipset Customer Reference Schematics (see Appendix A, "Reference Schematics").

Table 8-10. P64H Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
ACK64#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
AD[63:0]	8.2 KΩ PU to VCC3.3 on [64:32]	Connect to all PCI devices.
APICCLK		Connect to clock synthesizer.
APICD[1:0]	Two 300 Ω PU to VCC2.5	Connect to processors and ICH
BT_INTR#		Connect to ICH and PCI devices.
C/BE#[7:0]	8.2 KΩ PU to VCC3.3	Connect to PCI devices.
CLK66		Connect to clock synthesizer
DEVSEL#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
FRAME#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
GNT#[1:0]		Connect to all PCI devices.
GNT[5:2]	N/C	
HLB[19:0]		Connect to MCH.
HLB_STB0		Connect to MCH
HLB_STB0#		Connect to MCH
HLB_STB1		Connect to MCH
HLB_STB1#		Connect to MCH
HLBRCOMP	30 Ω 1% PD to GND	
HUBREF		Connected to 2/3Vterm HUBREF circuit.
IRDY#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
IRQ[23:0]	8.2 KΩ PU to VCC3.3	Connect to PCI devices.
M66EN	8.2 KΩ PU to VCC3.3	Connect to PCI devices.
PAR		Connect to all PCI devices.
PAR64	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
PCIRST#	N/C	
PCLKFBIN		Connect to PCLKFBOUT.
PCLKFBOUT		Connect to PCLKFBIN via 33Ω series resistor.
PCLKOUT[1:0]		Connect to all PCI devices via 33Ω series resistor.
PCLKOUT[2:5]	N/C (unused)	
PERR#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
PLOCK#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
PVCC5REF	(5V) 1 KΩ PU to VCC5.	(5V)Connect to VCC3.3 via a schottky diode. (3V) Connect to VCC3.3.
REQ#[5:0]	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
REQ64#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.

Table 8-10. P64H Connectivity

Pin	Pull-up(PU)/Pull-down(PD) Requirement	Pin Connection/Comment
RSTIN#		Connect to ICH.
SERR#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
STOP#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
TEST#	10 KΩ PU to VCC3.3	Connect to all PCI devices.
TRDY#	8.2 KΩ PU to VCC3.3	Connect to all PCI devices.
VCC5REF	(5V) 1 KΩ PU to VCC5.	(5V)Connect to VCC3.3 via a schottky diode. (3V) Connect to VCC3.3.

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A

Customer Reference Schematics

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Reference Schematics A

This appendix contains the Intel® 840 chipset Customer Reference Schematics. The reference schematics include the following features:

- Dual processor, SC330
- Intel® 840 chipset MCH, ICH, FWH Flash BIOS, and P64H
- Memory Expansion Card Connector (MECC)
- AGP Pro connector
- 4x33 MHz/32 bit PCI (ICH) and 2x66 MHz/64 bit PCI (P64H)
- UltraDMA/66
- RAID
- Audio
- 82559
- SIO
- CK133W

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