Intel® Pentium® 4 Processor in the 423 pin package / Intel® 850 Chipset Platform

Design Guide

February 2002

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Contents

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Revision History

Rev.	Description	Date
-001	• Initial Release	Nov 2000
-002	• Added latest ICH2 Spec Updates	May 2001
-003	• Added latest ICH2 Spec Updates	Aug 2001
-004	• Added Section 9.8.9 ICH2 Power Supply PS_ON Consideration • Revised Section 16.7.12 ICH2 RTC Checklist, SUSCLK • Revised Section 16.7.15 ICH2 Power Checklist, V5REF • Revised Section 12.5 ICH2 5VREF and VCC3_3 Sequencing Requirement • Corrected Figure 103 in Section 9.9.2 General LAN Routing Guidelines and Considerations • Revised Update #3, Section 12.5, ICH2 5VREF and VCC3_3 Sequencing Requirement • Replaced Figure 98 in Section 9.8.8 ICH2 Power-well Isolation Control Guidelines	Jan 2002
-005	• Revised paragraph 3 in Section 12.4 ICH2 V5REF and VCC3_3 Sequencing Requirement • Revised APIC in Section 16.7.6 Interrupt Interface in the Schematics Checklist • Revised V5REF_SUS in Section 16.7.15 Power in the Schematics Checklist	Feb 2002

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1. Introduction

This design guide documents Intel's design recommendations for systems based on the Intel® Pentium® 4 processor and Intel® 850 chipset. Design issues such as thermal considerations should be addressed using specific design guides or applications notes for the Pentium 4 processor and 850 chipset.

Carefully follow the design information, board schematics, debug recommendations and system checklist presented in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two categories below.

- *Design Recommendations* are items based on Intel's simulations and lab experience to date and are strongly recommended, if not necessary, to meet the timing and signal quality specifications.
- *Design Considerations* are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as an example, but may not be applicable to particular designs.

Note: The guidelines recommended in this document are based on experience and simulation work done at Intel while developing the Pentium 4 processor and 850 chipset-based systems.

The Pentium 4 processor / 850 chipset platform schematics are provided in Appendix A and are intended as a reference for board designers. While the schematics may cover a specific design, the core schematics will remain the same for most platforms. The schematic set provides a reference schematic for each platform component as well as common system board options. Additional flexibility is possible through other permutations of these options and components.

1.1. Related Documentation

Reference the following documents or models for more information. The specific revision numbers referenced should be used for all documents not released by Intel.

- *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet
- *Intel® Pentium® 4 Processor I/O Buffer and FloTherm Models*
- *CKOO Clock Synthesizer/Driver Design Guidelines*
- *Intel® Pentium® 4 Processor EMI Guidelines*
- *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel 82801BAM I/O Controller Hub 2 Mobile (ICH2-M)* datasheet (Ref Number: 290687)
- *Intel® 850 Chipset: 82850 Memory Controller Hub (MCH) (*Ref Number: *290691)*
- *Intel® 850 Chipset Specification Update*
- *Intel® 850 I/O Buffer Model Documentation*
- *Intel® 850 Chipset: Thermal Considerations; Application Note (AP-720) (*Ref Number: *292268)*
- *I/O Controller Hub 2 (ICH2) I/O Buffer Model Documentation*
- *AC '97 Component Specification,Rev.2.1*
- *Accelerated Graphics Port Interface Specification, Rev.2.0*
- *Low Pin Count Interface Specification, Rev.1.0*
- *PCI Local Bus Specification,Rev.2.2*
- *PCI-PCI Bridge Specification, Rev.1.0*
- *PCI Bus Power Management Interface Specification, Rev.1.0*
- *Universal Serial Bus Specification, Rev. 1.0*
- *RAMBUS* Direct RAMBUS* documentation*
- *Advanced Configuration and Power Interface Specification (ACPI), Rev. 1.0b*
- *PC 99/2001 Specification*

Notes:
1. The I/O Buffer Models are in IBIS format.

1.2. Conventions and Terminology

Convention/ Terminology	Definition
Aggressor	A network that transmits a coupled signal to another network is called the aggressor network.
AGTL+	The processor System Bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors that provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Corner	Describes how a component performs when all parameters that could impact performance are adjusted simultaneously to have the best or worst impact on performance. Examples of these parameters include variations in manufacturing process, operating temperature, and operating voltage. Performance of an electronic component may change as a result of (including, but not limited to): clock to output time, output driver edge rate, output drive current, and input drive current. The “slow” corner is defined as a component operating at its slowest, weakest drive strength performance. The “fast” corner is defined as a component operating at its fastest, strongest drive strength performance. Operation or simulation of a component at its slow corner and fast corner is expected to bound the extremes between slowest, weakest performance and fastest, strongest performance.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk – coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal. • Forward Crosstalk – coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal. • Even Mode Crosstalk – coupling from single or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk – coupling from single or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Convention/ Terminology	Definition
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the T_{CO} of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, *flight time* is defined to be: • Time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; e.g., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings. • Maximum and Minimum Flight Time – Flight time variations can be caused by many different variables. The causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage and manufacturing process. Some other causes include effects of Simultaneous Switching Output (SSO) and packaging effects. • Maximum flight time is the largest acceptable flight time a network will experience under all variations of conditions. • Minimum flight time is the smallest acceptable flight time a network will experience under all variations of conditions.
GTL+	GTL+ is the bus technology used by the Intel® Pentium® Pro processor. This is an incident wave switching, open-drain bus with pull-up resistors that provide both the high logic level and termination. It is an enhancement to the GTL (Gunning Transceiver Logic) bus technology.
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.
Network Length	The distance between one agent pin and the corresponding agent pin at the far end of the bus.
Overshoot	Maximum voltage observed for a signal at the device pad.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulation.
Pin	The contact point of a component package to the traces on a substrate, like the system board. Signal quality and timings can be measured at the pin.
Ringback	The voltage that a signal rings back to after achieving its maximum absolute value. Ringback may be due to reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the microprocessor bus of the Intel® Pentium® 4 processor. The System Bus is not compatible with the P6 bus protocol.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.

Convention/ Terminology	Definition
SSO	Simultaneous Switching Output (SSO) effects refers to the difference in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels (e.g., high-to-low) in the opposite direction from a single signal (e.g., low-to-high) or in the same direction (e.g., high-to-low). These are respectively called odd-mode switching and even-mode switching. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay (or "push-out"), or a decrease in propagation delay (or "pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Test Load	Intel uses a 50 Ω test load for specifying its components.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	Minimum voltage observed for a signal to extend below V_{SS} at the device pad.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.
V_{REF} Guardband	A guardband defined above and below V_{REF} to provide a more realistic model accounting for noise such as V_{TT} and V_{REF} variation.

1.3. System Overview

The Pentium 4 processor with the 850 chipset delivers Intel's highest performance desktop platform to date. The processor, chipset, and memory are balanced to provide the best possible performing systems.

1.3.1. Intel® Pentium® 4 Processor

The Pentium 4 processor is the next generation IA-32 processor. This processor has a number of features that significantly increase its performance from previous generation IA-32 processors. The Intel® NetBurst™ microarchitecture includes a number of new features as well as some improvements on existing features.

Intel NetBurst microarchitecture features include hyper-pipelined technology, rapid execution engine, 400 MHz system bus, and execution trace cache. The hyper-pipelined technology doubles the pipeline depth in the Pentium 4 processor allowing the processor to reach much higher core frequencies. The rapid execution engine allows the 2 integer ALUs in the processor to run at twice the core frequency, which allows many integer instructions to execute in 1/2 clock tick. The 400 MHz system bus is a quad-pumped bus running off a 100 MHz system clock making 3.2 GB/sec data transfer rates possible. The execution trace cache is a level 1 cache that stores approximately 12k decoded micro-operations, which removes the decoder from the main execution path, thereby increasing performance.

Improved features within the Intel NetBurst microarchitecture include the advanced dynamic execution, advanced transfer cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The advanced dynamic execution improves speculative execution and branch prediction internal to the processor. The advanced transfer cache is a 256 KB, on-die level 2 cache with an increased bandwidth over previous micro-architectures. The floating point and multi-media units have been improved by making the registers 128 bits wide and adding a separate register for data movement.

Finally, SSE2 adds 144 new instructions for double precision floating point, SIMD integer, and memory management.

The Pentium 4 processor supports uni-processor configurations only. The same manageability features, which are included in Intel® Pentium® III processors, are included on Pentium 4 processors with the addition of thermal monitor. Thermal monitor allows systems to be designed for anticipated processor thermals as opposed to worst-case with no performance degradation expected.

Table 1. Intel® Pentium® 4 Processor Feature Set Overview

Feature	Intel® Pentium® 4 Processor
L1 Cache	On-die
L2 Cache	256 KB on-die
System Bus Frequency	400 MHz
Manageability Features	Thermal Monitor
Package Pin Configuration	423 pin, 0.10 inches interstitial PGA

1.3.2. Intel® 850 Chipset

The 850 chipset consists of two main components: 82850 Memory Controller Hub (MCH) and the 82801BA I/O Controller Hub 2 (ICH2). These components are interconnected via an Intel proprietary interface called hub interface. The hub interface is designed into the 850 chipset to provide efficient communication between components.

Additional hardware platform features include AGP 4x mode, Rambus* Direct RDRAM* device, Ultra ATA/100, Low Pin Count interface (LPC), integrated LAN* and Universal Serial Bus (USB). The platform is also ACPI compliant and supports *Full-on*, *Stop Grant*, *Suspend to RAM*, *Suspend to Disk*, and *Soft-off* power management states. Through the use of an appropriate LAN* connect, the platform supports *Wake-on-LAN** for remote administration and troubleshooting.

1.3.2.1. 82850 Memory Controller Hub (MCH)

The MCH provides the processor interface, Direct RDRAM device interface, AGP interface, and hub interfaces in an 850 chipset platform. The processor interface is optimized for the System Bus Protocol in order to support the Pentium 4 processor.

The MCH is in a 615 ball OLGA package and has the following functionality:

- Supports a single Pentium 4 processor with a data transfer rate of 400 MHz
- Dual Rambus* channels support 300 MHz and 400 MHz RDRAM device operation
- AGTL+ host bus with integrated termination supporting 32-bit host addressing
- 1.5 V AGP interface with 4x SBA/data transfer and 2x/4x fast write capability
- 8-bit, 66 MHz 4x hub interface to ICH2

1.3.2.2. I/O Controller Hub 2 (ICH2)

The ICH2 provides the I/O subsystem with access to the rest of the system. Additionally, it integrates many widely utilized I/O functions.

The ICH2 is in a 360-ball EBGA package and contains the following functionality:

- PCI bus interface at 33 MHz, 133 MB/s maximum throughput
- Supports up to six PCI master devices
- LAN* controller with 10/100 Mbit/s Ethernet and 1 Mbit/s HomePDA* support
- Low pin count (LPC) interface
- Firmware Hub (FWH) Flash BIOS interface
- 82C54 based timer
- IDE controller with support for Ultra ATA 100/66/33
- Two USB controllers for a total of four ports
- Enhanced DMA controller with support for REQ#/GNT# pairs, LPC DMA, Type F DMA
- SMBus interface
- AC-link for external audio and telephony Codec's

1.3.3. Bandwidth Summary

The table below shows the theoretical maximum bandwidth of critical 850 chipset platform interfaces.

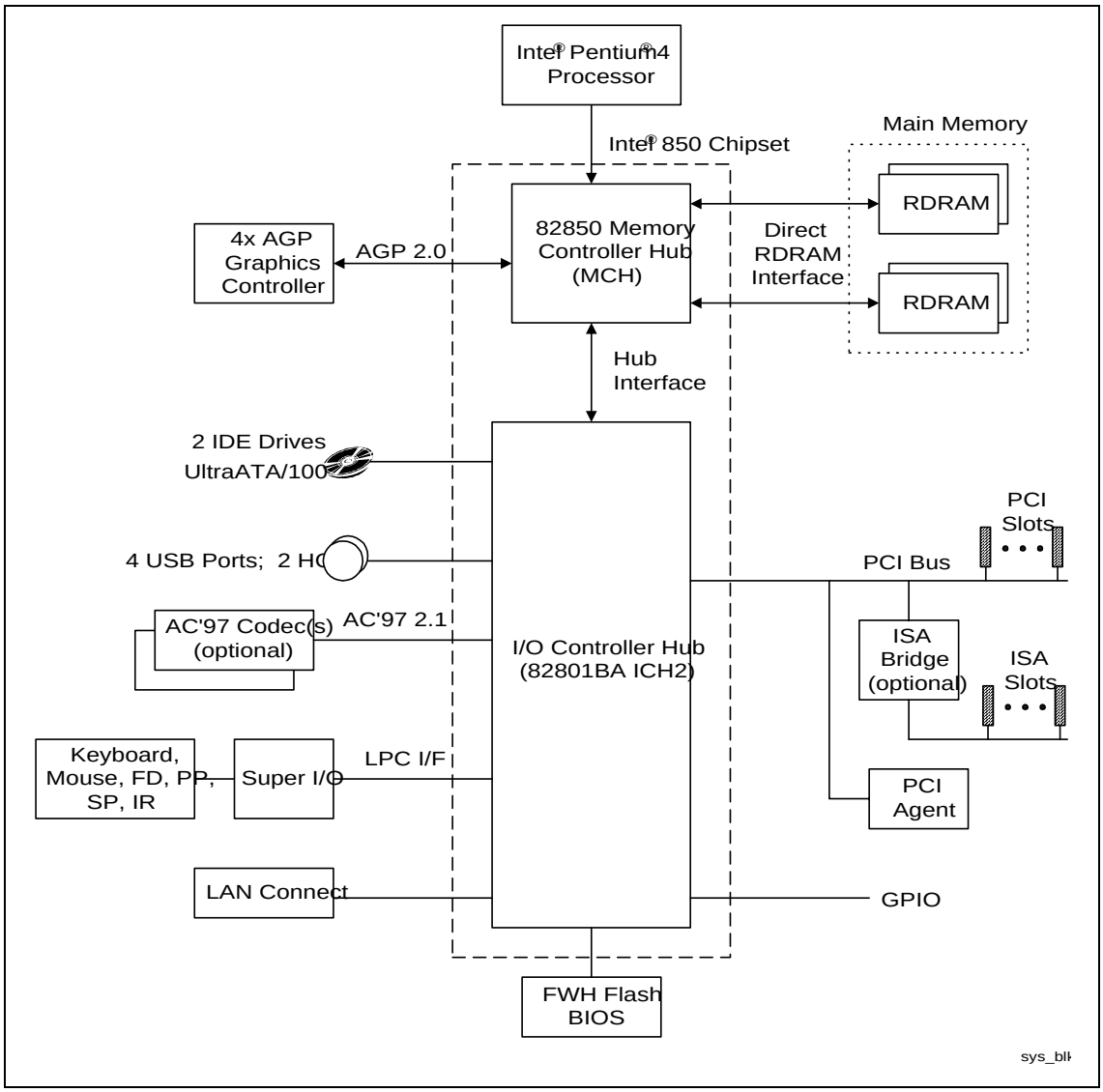
Table 2. Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth (MB/s)
System Bus	100	4	8	3200
AGP	66	4	4	1066
Hub interface A	66	4	1	266
PCI	33	1	4	133
RDRAM* devices	400	2	4	3200

1.3.4. System Configurations

The following figure illustrates a typical Pentium 4 processor and 850 chipset based system configuration for professional and high performance desktops using the Pentium 4 processor.

Figure 1. Typical System Configuration Using the Intel® Pentium® 4 Processor and Intel® 850 Chipset



1.4. Platform Initiatives

1.4.1. Intel® 850 Chipset

1.4.1.1. Rambus* Direct RDRAM* Device Interface

The Direct RDRAM device interface provides the necessary memory bandwidth to obtain optimal performance from the Pentium 4 processor as well as a high performance AGP graphics controller. The MCH RDRAM device interface supports 300/400 MHz operations, delivering 3.2 GB/s of theoretical maximum memory bandwidth using two Rambus channels operating in lock step. This is twice the memory bandwidth of 100 MHz SDRAM systems. Coupled with the greater bandwidth, the heavily pipelined RDRAM device protocol, a substantially more efficient data transfer is achieved. The RDRAM device memory interface can achieve greater than 95% utilization of the 3.2 GB/s theoretical maximum bandwidth.

In addition to the RDRAM device's performance features, this new memory architecture provides enhanced power management capabilities. The *powerdown* mode of operation will enable 850 chipset-based systems to cost effectively support the *suspend-to-RAM* sleep state.

Industry leading DRAM vendors have agreed to develop RDRAM devices and module vendors will be developing Rambus* RIMM* modules, which are approximately the same form factor as SDRAM DIMMs.

The 128-Mb and 256-Mb Direct RDRAM device technologies will be supported by 850 chipset -based platforms.

1.4.1.2. Accelerated Graphics Port (AGP)

AGP is a high performance, component level interconnect targeted at 3D graphical display applications. AGP is based on a set of performance extensions or enhancements to the PCI bus. The 850 chipset employs an AGP interface that is optimized for a point-to-point topology using 1.5 V signaling in 4x mode. The 4x mode provides a peak bandwidth of 1066 MB/s.

For additional information, refer to the *Accelerated Graphics Port Interface Specification, Rev. 2.0*, which is located at the following URL: http://www.agpforum.org/specs_specs.htm.

1.4.2. 82801BA ICH2

1.4.2.1. Integrated LAN* Controller

The ICH2 incorporates an integrated LAN* controller. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers processor utilization by off-loading communication tasks from the processor.

The ICH2 functions with several options of LAN* connect components to target the desired market segment. The *82562EH* component provides a *HomePNA* 1Mbit/sec connection. The *82562ET* component provides a basic Ethernet 10/100 connection. The *82562EM* component provides an Ethernet 10/100 connection with the added flexibility of *Alert on LAN**. More advanced LAN* solutions can be implemented with the 82550 or other PCI based product offerings.

1.4.2.2. AC ’97 6-Channel Support

The *AC ’97 Component Specification, Revision 2.1* defines a digital link that can be used to attach an audio codec (AC), a modem codec (MC), an audio/modem codec (AMC), or both an AC and an MC. The *AC ’97 Component Specification, Revision 2.1* defines the interface between the system logic and the audio or modem codec known as the AC-link.

The Intel® ICH2 AC ’97 (with the appropriate codecs) not only replaces ISA audio and modem functionality, but also improves overall platform integration by incorporating the AC ’97 digital link. Using the ICH2 integrated AC-link reduces cost and eases migration from ISA.

By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio on the 850 chipset platform. In addition, an AC ’97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC ’97. ICH2’s integrated digital link allows two external codecs to be connected to the ICH2 in several configurations. Reference the following table for the various AC ’97 codec implementations.

Table 3. ICH2 Codec Options

Primary	Secondary
Audio (AC)	None
Modem (MC)	None
Audio/Modem (AMC)	None
Audio (AC)	Modem (MC)
Audio (AC)	Audio (AC)
Audio (AC)	Audio/Modem (AMC)

Modem implementation for different countries must be considered as telephone systems may vary. By using a split design, the audio codec can be on-board and the modem codec can be placed on a riser. Intel is developing an AC-link connector. With a single integrated codec, or AMC, both audio and modem can be routed to a connector near the rear panel where the external ports can be located.

The digital link in the ICH2 *AC ’97 Component Specification, Revision 2.1* compliant, supporting two codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec. The 850 chipset-based platform expands audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center and Woofer for a complete surround sound effect.

Refer to the *AC ’97 Component Specification, Revision 2.1* at http://developer.intel.com/pc-supp/platform/ac97/ for complete details.

1.4.2.3. Low Pin Count (LPC) Interface

In the platform, the super I/O component has migrated to the Low Pin Count (LPC) interface. Migration to the LPC interface allows for lower cost super I/O designs. The LPC super I/O component requires the same feature set as traditional super I/O components. It should include a keyboard and mouse controller, floppy disk controller, and serial and parallel ports. In addition to the standard super I/O features, an integrated game port is recommended because the AC '97 interface does not provide support for a game port. In a system with ISA audio, the game port typically existed on the audio card. The fifteen-pin game port connector provides for two joysticks and a two-wire MPU-401 MIDI interface.

For further information, refer to the *Low Pin Count Interface Specification, Rev. 1.0*, which is located at the following URL: http://developer.intel.com/design/pcisets/lpc/INDEX.HTM. Consult your super I/O vendor for a comprehensive list of devices offered and features supported.

1.4.2.4. Ultra ATA

Ultra ATA "widens" the path to the hard drive by transferring twice as much data per clock cycle. The net effect is that the maximum burst data transfer rate from the disk drive increases from 16.6 MB/s to 100 MB/s. Hard disk drive manufacturers can now bring higher performance products to market that scale with the rest of the PC platform (faster hard drives to feed faster processors, memory and graphics).

The Ultra ATA protocol allows 850 chipset-based systems to send and retrieve data faster, removing bottlenecks associated with data transfers — especially during sequential operations. Users of new 850 chipset-based systems will need less time to boot their systems and open applications, a direct result of the improved throughput provided by Ultra ATA. Current disk drive technology has been optimized to perform within the limits of the legacy protocol (16.6 MB/s). Raising the data transfer headroom results in moderate performance gains with today's drive technology. Even greater performance improvements will emerge as drive manufacturers introduce products that generate a faster data stream.

The ICH2 supports the IDE controller with two sets of interface signals (Primary and Secondary) that can be independently enabled, tri-stated or driven low. It supports the Ultra ATA/33, Ultra ATA/66 and Ultra ATA/100 protocol transfer rates. Ultra ATA/66 and ATA/100 are similar to the Ultra ATA/33 scheme and are intended to be device driver compatible. The Ultra ATA/66 logic is clocked at 66 MHz and can move 16 bits of data every two clocks (for a maximum of 66 MB/s transfers). The Ultra ATA/100 logic is clocked at 100 MHz and can move 16 bits of data every two clocks (for a maximum of 100 MB/s transfers).

1.4.2.5. Universal Serial Bus (USB)

Universal Serial Bus (USB) simplifies the peripheral attaching and accessing process to the computer. It also eases the system configuration process from an end-user's perspective. The USB specification outlines a single connector-type for all PC peripherals, automatic detection/configuration of the USB devices and transfer types allowed on the bus.

In the 850 chipset based platform, the ICH2 integrates two USB Host Controllers. The Host Controllers include the root hub with two separate USB ports, resulting in a total of four USB ports. The ICH2 Host Controller supports the standard *Universal Host Controller Interface (UHCI), Rev. 1.0*.

Refer to the *USB Specification, Rev. 1.0* at http://www.usb.org for further information.

1.4.3. Platform Manageability

The 850 chipset platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system and recover from system lockups without the aid of an external micro-controller.

Interrupt Controller: The interrupt capabilities of the ICH2 in an 850 chipset-based platform expands support for up to eight PCI interrupt pins and PCI 2.2 Message-Based Interrupts. In addition, the ICH2 supports system bus interrupt delivery.

TCO Timer: The ICH2 integrates a programmable TCO timer. This timer is used to detect system locks. The first expiration of the timer generates an SMI# which the system can use to recover from a software lock. The second expiration of the timer causes a system reset to recover from a hardware lock.

Processor Present Indicator: The ICH2 looks for the processor to fetch the first instruction after reset. If the processor does not fetch the first instruction the ICH2 has the ability to blink a GPIO and reboot the system.

ECC Error Reporting: The MCH has the ability to send one of several messages to the ICH2 when an ECC error is detected. The MCH can tell the ICH2 to generate either an SMI#, SCI, or SERR# interrupt.

Function Disable: The ICH2 provides the ability to disable the following functions: AC ’97 Modem, AC ’97 Audio, IDE, USB or SMBus. Once disabled, these functions no longer decode I/O, memory, or PCI configuration space. Also, no interrupts or power management events are generated from the disabled functions.

Intruder Detect: The ICH2 provides an input signal, INTRUDER#, that can be attached to a switch that is activated by the system case being opened. The ICH2 can be programmed to generate an SMI# or TCO interrupt due to an active INTRUDER# signal.

SMBus: The ICH2 integrates an SMBus controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RIMM modules and thermal probes. A slave interface is also provided to enable additional platform manageability. This interface allows and external microcontroller to access system resources, as well as external system devices the ability to check the system power state, watchdog timer, and system status bits and generate a system reset and other platform messages.

Alert-On-LAN*: The ICH2 supports *Alert-On-LAN**. In response to a TCO event (intruder detect, thermal event, processor not booting) the ICH2 will send a hard-coded message over the SMLink. Refer to the Wired for Management (WfM) Design Guide at http://www.intel.com/ial/wfm/design/ for additional information.

1.5. PC 99/2001 Platform Compliance

PC 99/2001 is intended to provide guidelines for hardware design that will result in optimal user experience, particularly when the hardware is used with the Microsoft Windows* family of operating systems. This document includes PC 99/2001 requirements and recommendations for basic consumer and office implementations, such as desktop, mobile, and workstation systems, and entertainment PC's. This document includes guidelines to address the following design issues:

- Design requirements for specific types of system that will run either Microsoft Windows* 98, Windows* 2000 or Windows* Millennium Edition (ME) operating systems.
- Design requirements related to OnNow design initiative, including requirements related to ACPI, Plug and Play device configuration, and power management in PC systems.
- Manageability requirements that focus on improving Windows 98, Windows 2000 and Windows Millennium Edition with the end goal of reducing TCO.
- Clarification and additional design requirements for devices supported under Windows 98, Windows 2000 and Windows Millennium Edition including new graphics and video device capabilities, DVD, scanners and digital cameras, and other devices.

Refer to the *PC 99/2001 System Design Guide* at http://www.microsoft.com/windows/ for additional information.

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2. Component Quadrant Layout

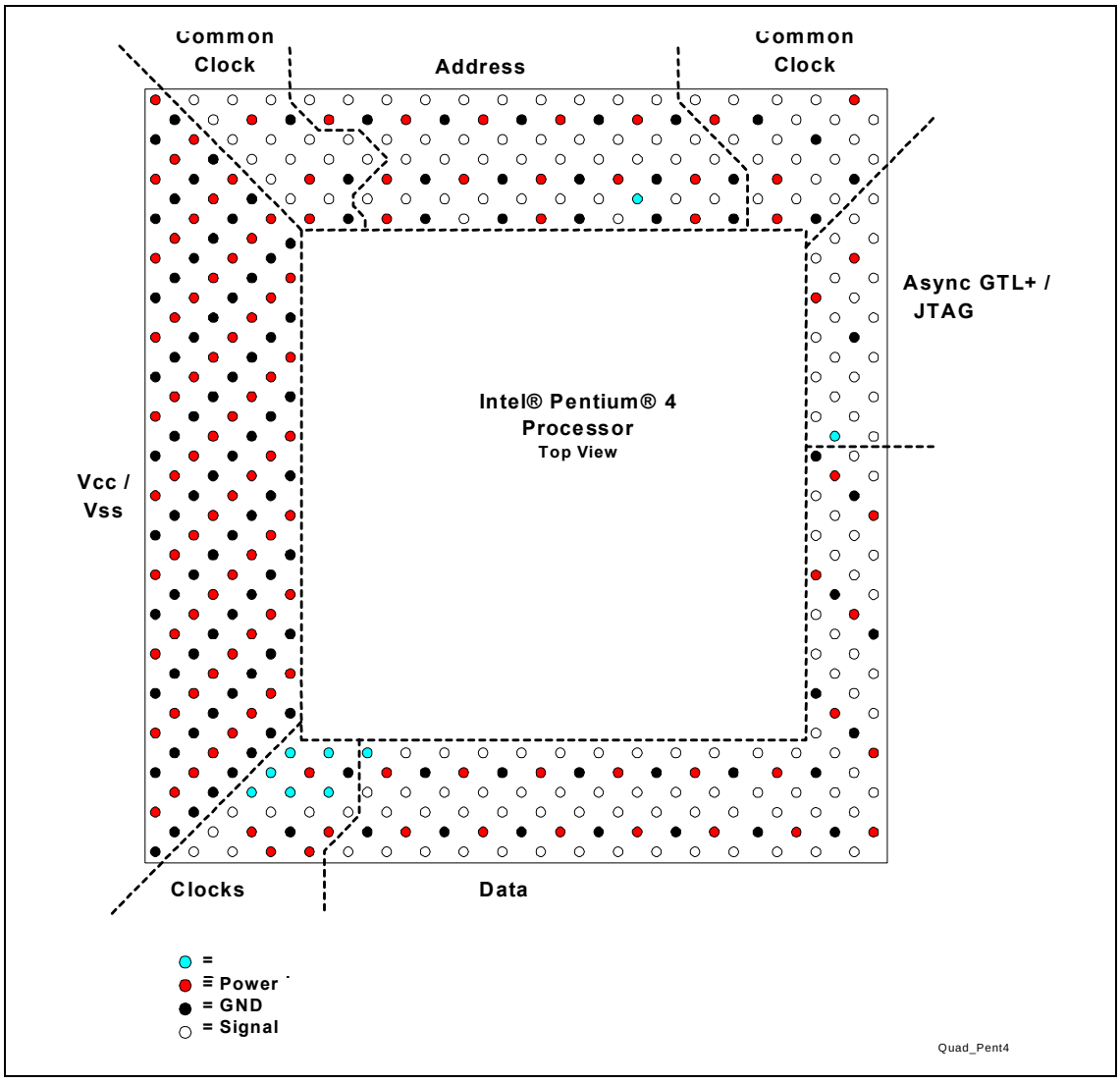
The preliminary quadrant layouts shown are approximations. The quadrant layout figures do not show the exact component ball count; only general quadrant information is presented and is intended for reference while using this document. Only the exact pin or ball assignment should be used to conduct routing analysis. Reference the following documents for pin or ball assignment information.

- *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet
- *Intel® 850 Chipset: 82850 Memory Controller Hub (MCH)* datasheet

2.1. Intel® Pentium® 4 Processor Component Quadrant Layout

The following figure illustrates the quadrant layout of the Pentium 4 processor. In the event that this information conflicts with the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet, the datasheet data should be considered correct.

Figure 2. Intel® Pentium® 4 Processor Socket Quadrant Layout (topside)



2.2. Intel® 850 Chipset Component Quadrant Layout

The following two figures show the quadrant layouts for the 850 chipset components. These are preliminary and subject to change.

Figure 3. Intel® 850 Chipset Quadrant Layout (topside)

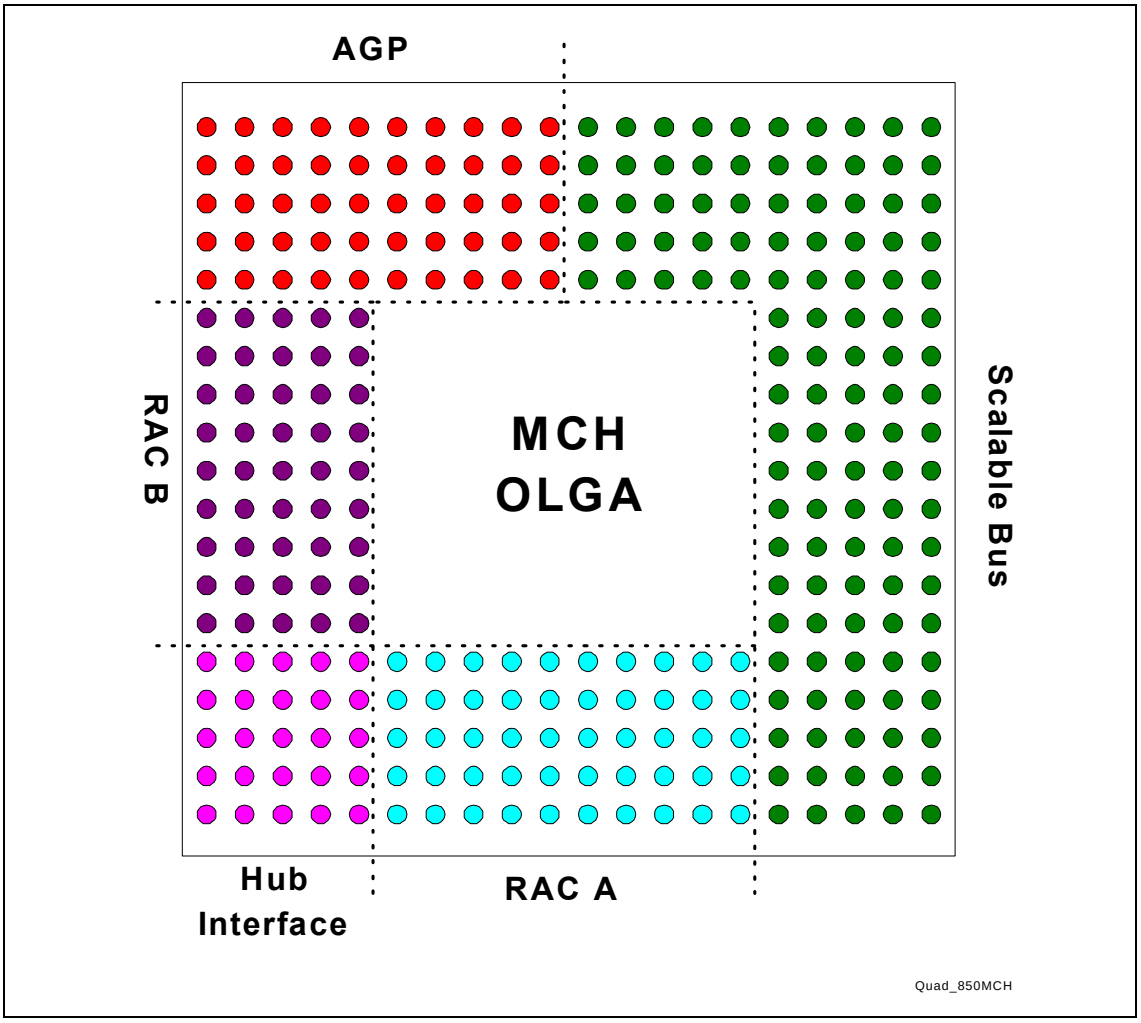
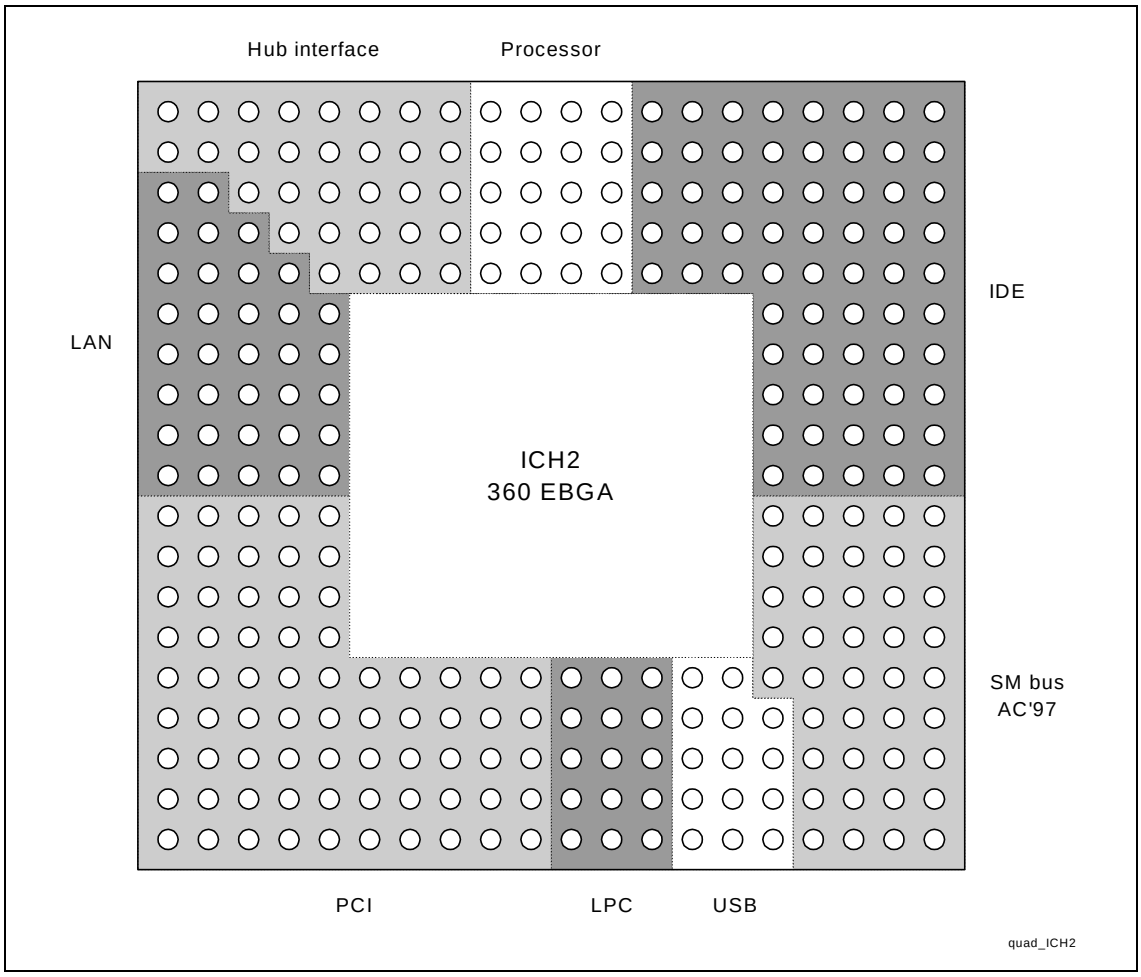


Figure 4. ICH2 Quadrant Layout (topside)



3. Platform Placement and Stack-Up Overview

In this section, an example of an 850 chipset platform component placement and stack-up is presented for a desktop system in an ATX board form factor.

3.1. Platform Component Placement

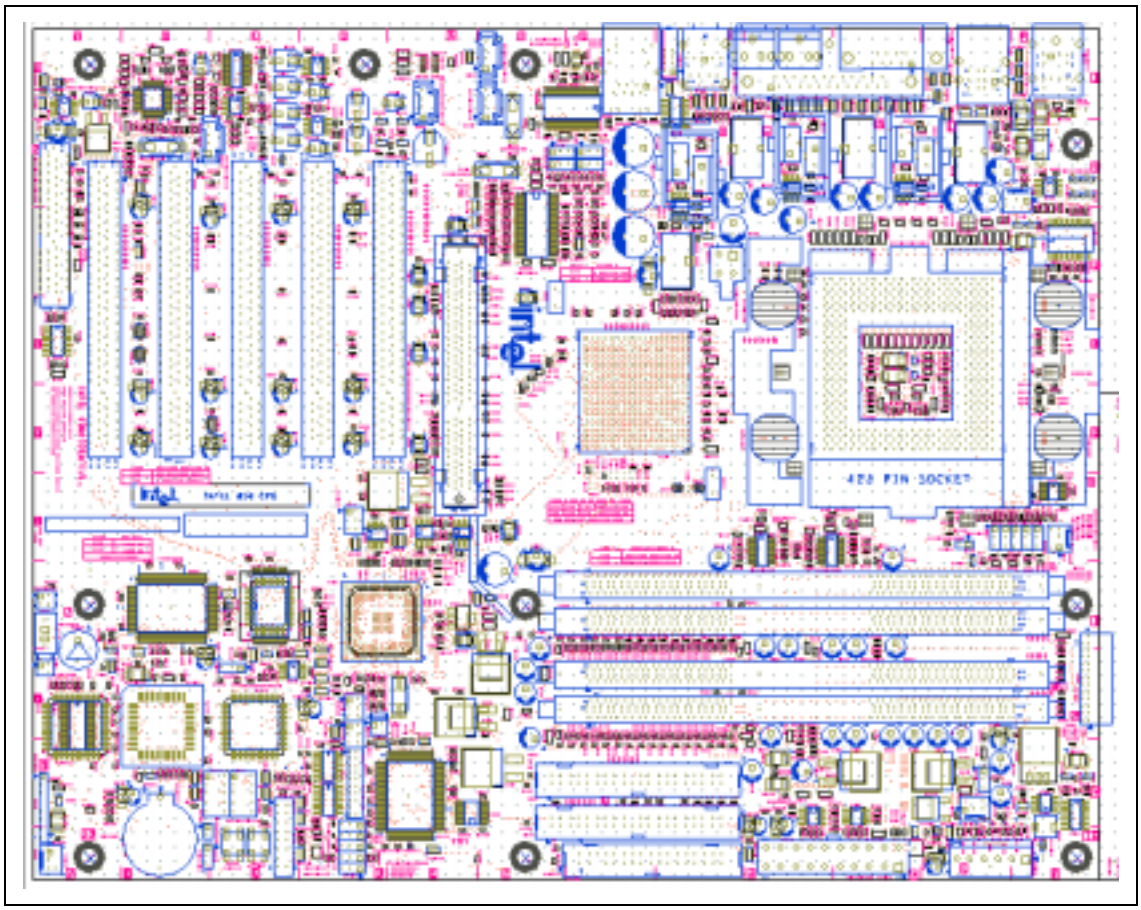
The following figure illustrates general component placement for a Pentium 4 processor and 850 chipset-based desktop motherboard system. The assumptions used for the component placement are documented in the following table and are consistent with the customer reference board (CRB) schematics.

Note: The Pentium 4 processor supports uni-processor configurations only.

Table 4. Placement Assumptions for the Desktop Configuration

System Configuration	Assumptions		
	Form Factor	Number of Layers for Routing	Assembly
Uni-processor	ATX	6 Layers	Single Sided

Figure 5. Desktop Component Placement Example

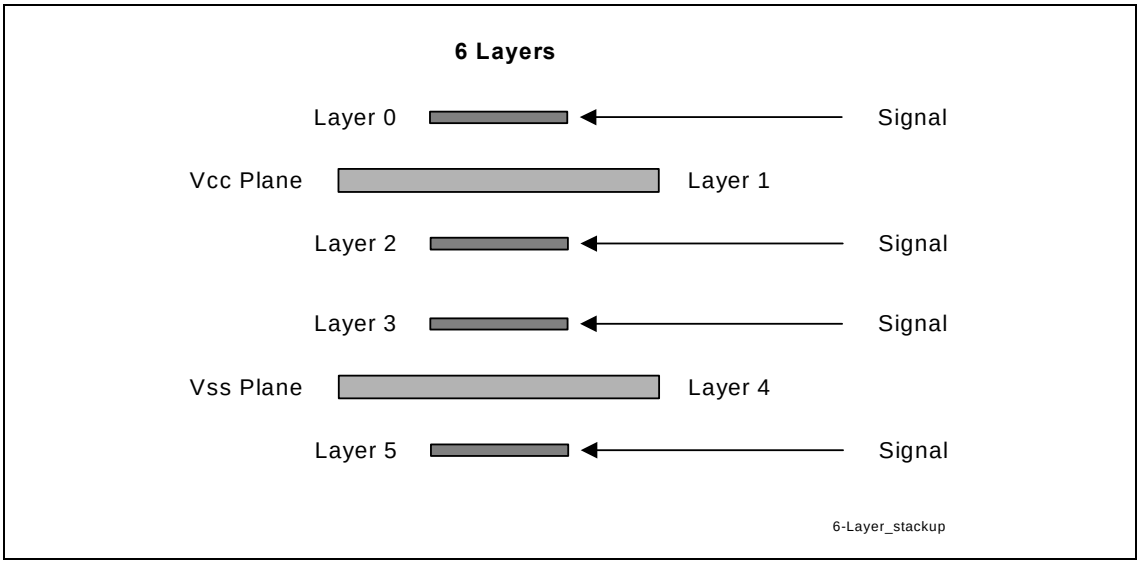


3.2. Motherboard Layer Stack-Up

The following two figures show a six-layer stack-up for a Pentium 4 processor system, it is for reference only and the actual board stack-up may vary depending on the following considerations.

- The separation between layers 2 and 3 should be kept as large as possible. A distance greater than 2x should be kept between signals on layers 2 and signals on layer 3.
- Additionally, traces on layer 2 should be routed orthogonally to traces on layer 3. If traces on layer 2 are unable to be routed orthogonally to traces on layer 3, then the distance between layer 2 and layer 3 should be greater than 4x.
- If possible, signals should be referenced to a V_{SS} plane.

Figure 6. Six-Layer Stack-Up for Intel® Pentium® 4 Processor Based Systems



Design Recommendations

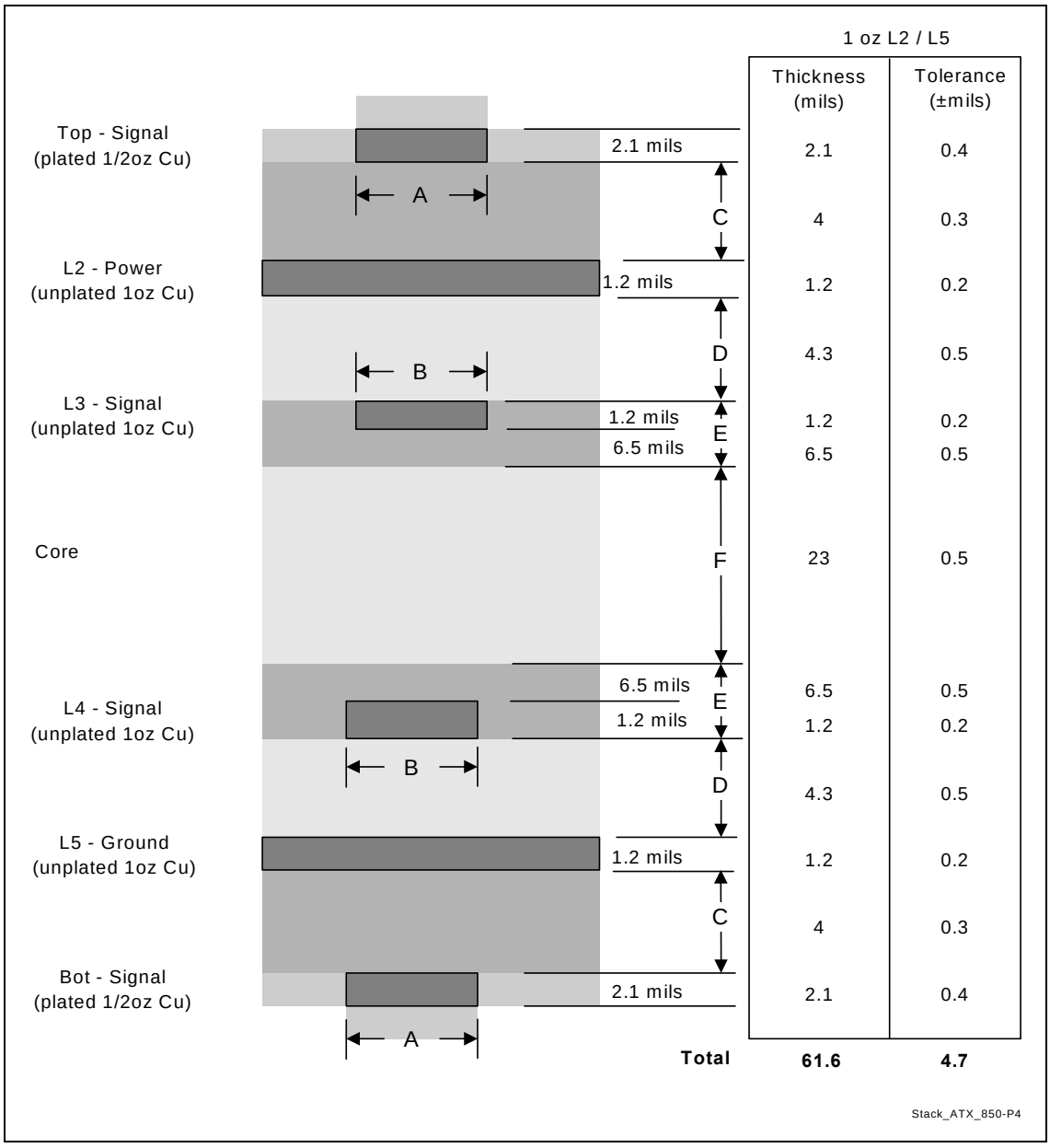
It is recommended that an equivalent of 2-oz. copper be used for power delivery to the processor. This could be a 2-oz. power plane, or a combination of 1 oz. copper from a power/ground plane and 1 oz. copper from a power/ground island on a signal plane. For more details, refer to Section 11, *Intel® Pentium® 4 Processor Power Distribution Guidelines*.

Design Considerations

Intel has found that the following recommendations aid in the design of a Pentium 4 processor-based platform.

- Standard vias should be a 14 mil hole with a 26 mil pad.
- There must be the equivalent total of 2 oz of copper on power/ground planes for power delivery to the processor.
- The islands and/or planes in the power pin area of the Pentium 4 processor should **not** contain signal routing through them.

Figure 7. Intel® Pentium® 4 Processor / Intel® 850 Chipset Example Stack-Up for ATX Form Factor

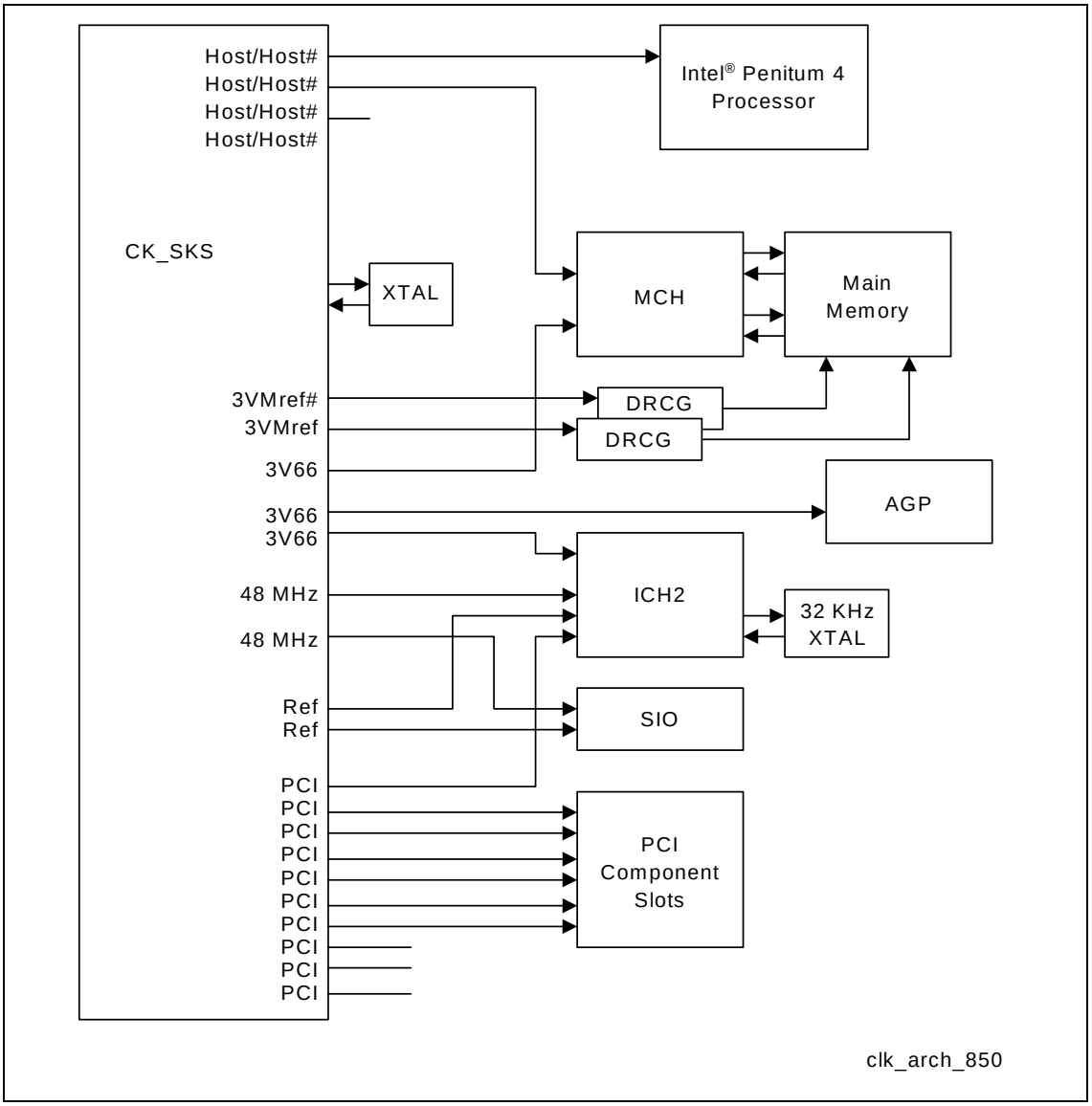


4. Platform Clock Routing Guidelines

Intel recommends CK00 compliant clocking for Pentium 4 processor-based platforms. For more information on CK00 compliance, refer to the *CK00 Clock Synthesizer/Driver Design Guidelines*.

The CK00 Clock Synthesizer/Driver Design Guidelines specify the platform clocking solution that can be used in a Pentium 4 processor and 850 chipset-based design – the CK_SKS clock synthesizer.

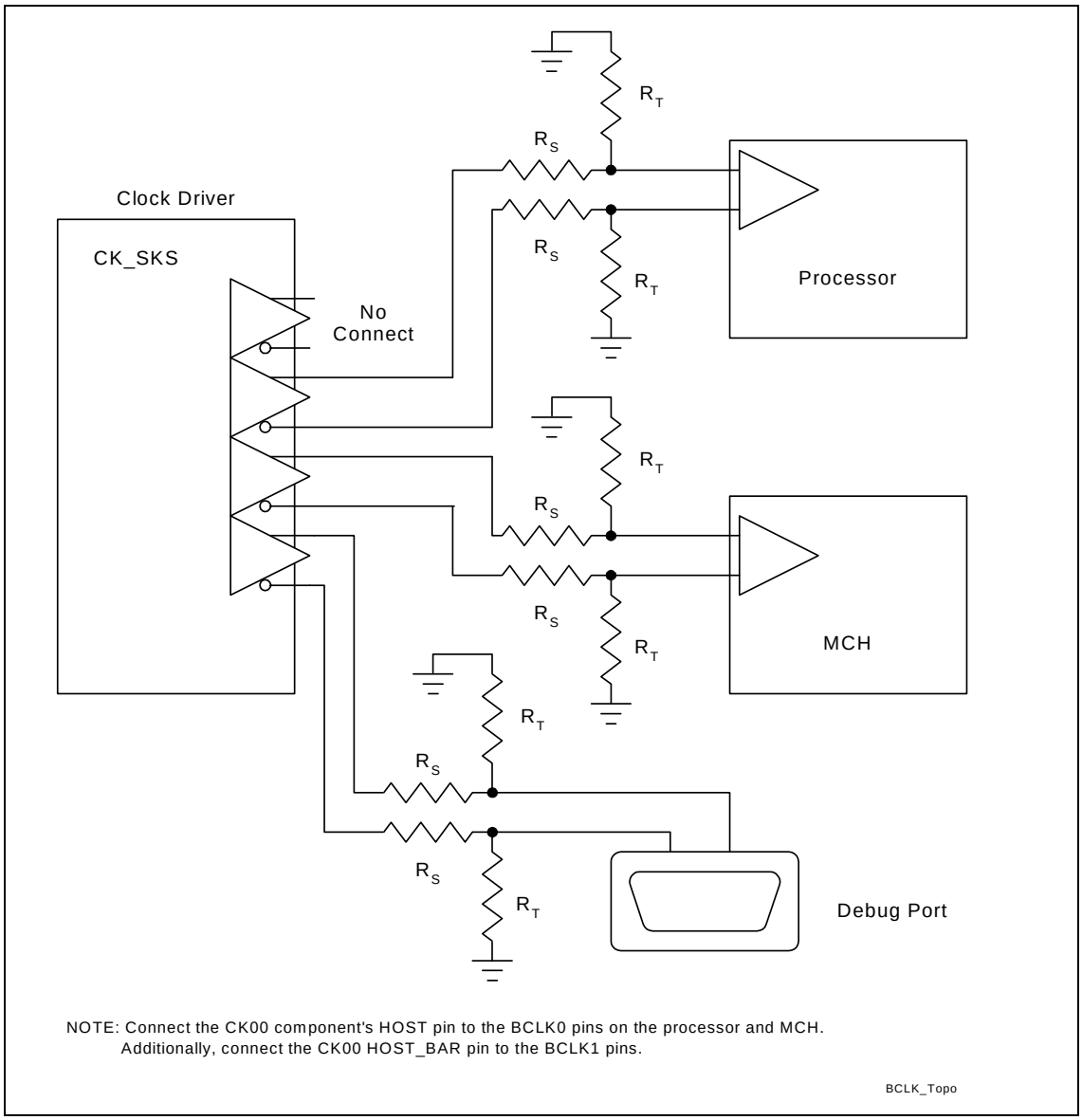
Figure 8. Clocking Architecture Using the CK_SKS



4.1. Routing Guidelines for System Bus Clocks

The CK_SKS clock synthesizer provides four sets of 100 MHz differential clock outputs. The 100 MHz differential clocks are driven to the Pentium 4 processor and MCH as shown in the following figure.

Figure 9. Intel® Pentium® 4 Processor BCLK Topology

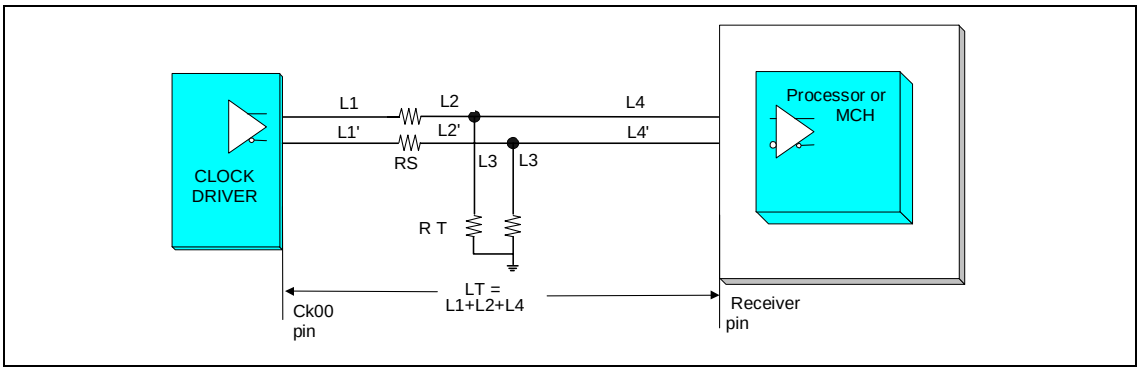


The CK00 clock driver differential bus output structure is a “Current Mode Current Steering” output that develops a clock signal by alternately steering a programmable constant current to the external termination resistors Rt. The resulting amplitude is determined by multiplying I_{OUT} by the value of Rt. The current I_{OUT} is programmable by a resistor and an internal multiplication factor so the amplitude of the clock signal can be adjusted for different values of Rt to match impedance or to accommodate future load requirements.

The recommended termination for the CK00 differential bus clock is a “Shunt Source termination.” Refer to the following figure for an illustration of this terminology scheme. Parallel Rt resistors perform a dual function, converting the current output of the CK00 to a voltage and matching the driver output impedance to the transmission line. The series resistors Rs provide isolation from the clock driver’s output parasitics, which would otherwise appear in parallel with the termination resistor Rt.

The value of Rt should be selected to match the characteristic impedance of the system board and Rs should be between 20 Ω and 33 Ω. Simulations have shown that Rs values above 33 Ω provide no benefit to signal integrity but only degrade the edge rate.

Figure 10. Source Shunt Termination



The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in dielectric constant and the impedance variations due to physical tolerances of circuit board material. Routing on internal layers provides the least amount of dielectric constant and impedance variation.

- **Requirement:** Do not split up the two halves of a differential clock pair between layers
- **Goal:** Route clocks to all agents on the same physical routing layer

General Routing Guidelines

- If layer transition is required, make sure that skew induced by the vias used to transition between routing layers is compensated in the traces to other agents
- Layer transitions should only be made between routing layers of the same configuration i.e., stripline layer to stripline layer
- Keep routes to all agents as short as possible to minimize the cumulative effects of dielectric constant variations on clock skew
- Do not place vias between adjacent complementary clock traces.
- Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and RS, if needed to shorten length L1.

EMI Constraints

Clocks are a significant contributor to EMI and should be treated with care. The following recommendations can aid in EMI reduction:

- Route clocks on inner layers.
- On internal signals layers maintain a minimum of 100 mils from the edge of the clock traces to the edge of the system board.
- Maintain uniform spacing between the two halves of differential clocks
- Route clocks on physical layer adjacent to the V_{SS} reference plane only
- Spread spectrum clocking should be enabled.

The following table describes the routing guidelines for the bus clock signals.

Table 5. BCLK [1:0]# Routing Guidelines

Layout Guideline	Value	Illustration	Notes
BCLK Skew between agents	400 ps total Budget: 150 ps for Clock driver 250 ps for interconnect	Figure 9	1, 2, 3, 4
Differential pair spacing	4 x W min. to 5 x W max.	Figure 12	5, 6
Spacing to other traces	25 mils	Figure 12	—
Line width	7.0 mils	Figure 12	7
System board Impedance – Differential	100 Ω	—	8
System board Impedance – single ended	50 Ω ±15%	—	9
Processor routing length – L1, L1': Clock driver to Rs	0.5 inches max	Figure 10	13
Processor routing length – L2, L2': Rs to Rs-Rt node	0 inches – 0.2 inches	Figure 10	13
Processor routing length – L3: RS-RT node to Rt	0 inches – 0.2 inches	Figure 10	13
Processor routing length – L4, L4': RS-RT Node to Load	0 inches – 12 inches	Figure 10	
MCH routing length – L1: Clock Driver to RS	0.5 inches max	Figure 10	13
MCH routing length – L2, L2': Rs to Rs-Rt node	0 inches – 0.2 inches	Figure 10	13
MCH routing length – L3: RS-RT node to Rt	0 inches – 0.2 inches	Figure 10	13
MCH routing length – L4, L4': RS-RT Node to Load	0 inches – 12 inches	Figure 10	
Clock driver to Processor and clock driver to Chipset length matching (LT)	0.850 inches ±0.010 inches (Add to MCH trace length)	Figure 9	10
BCLK0 – BCLK1 length matching	±10 mils	Figure 9	—

Layout Guideline	Value	Illustration	Notes
Rs Series termination value	33 Ω ±5%	Figure 9	11
Rt Shunt termination value	49.9 Ω ±1% (for 50 Ω MB impedance)	Figure 9	12

NOTES:

1. The skew budget includes clock driver output pair to output pair jitter (differential jitter), and skew, clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes clock pairs are routed on multiple routing layers and routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.
5. Edge-to-edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing, as this will degrade the noise rejection of the network.
7. Set line width to meet correct system board impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack-up.
8. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1-2*Kb) where Kb is the backwards cross-talk coefficient. For the recommended trace spacing, Kb is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the BCLK traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the system board trace length for the chipset will be longer than that for the processor. Details of this additional length will be included in a future revision of the processor package files.
11. Rs values between 20 Ω – 33 Ω have been shown to be effective.
12. Rt shunt termination value should match the system board impedance.
13. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination and contribute to ring back.

Figure 11. Clock Skew As Measured from Agent to Agent

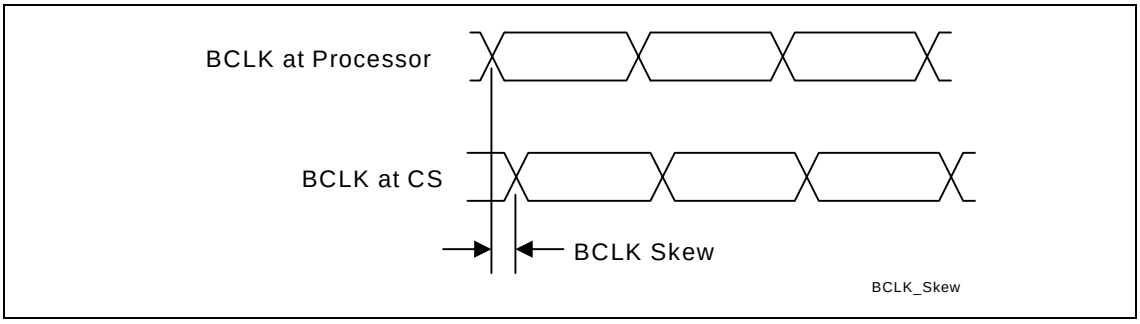
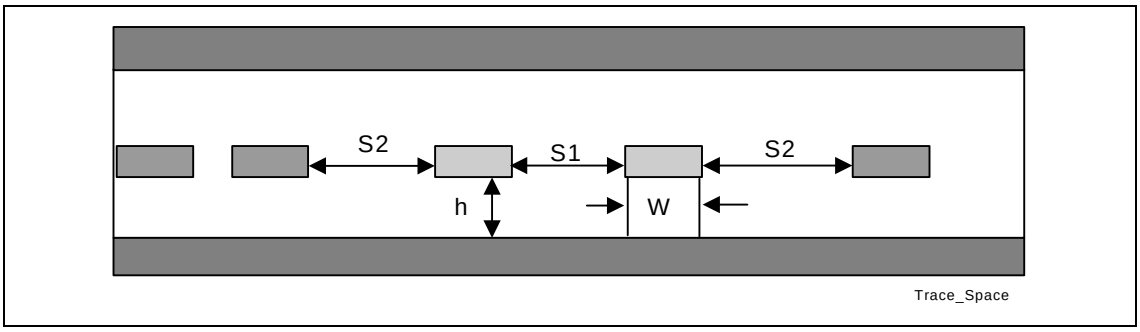


Figure 12. Trace Spacing



4.2. Routing Guidelines for Rambus* RDRAM* Device Clocks

The CK_SKS clock synthesizer provides two 3.3 V clock reference outputs (3VMRef and 3VMRef#) for the memory clock drivers, DRCGs (Direct RAMBUS* Clock Generator). Two DRCGs are required in an 850 chipset dual-Rambus channel interface.

The DRCG reference clock operates at one-half the processor clock frequency. The reference clocks are inputs into the DRCGs and are used to generate the Direct RDRAM device “Clock to Master” differential pair (CTM, CTM#) clocks on each Rambus channel.

In addition, the DRCG uses phase information provided by the MCH via the RCLKOUT and HCLKOUT phase aligning signals.

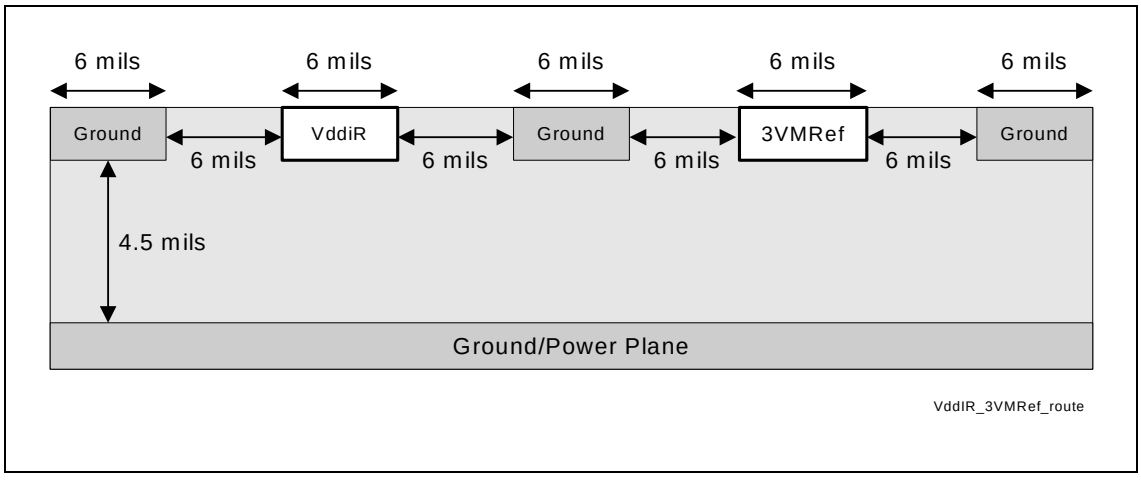
4.2.1. CK_SKS to DRCG (Reference Clocks)

The 3VMRef clock output must be routed as shown in the following figure. Note that the VddIR power pin on the DRCG can be connected directly to 3.3 V near the DRCG if the 3.3 V plane extends near the DRCG. However, if a 3.3 V trace must be used, it should originate at the clock synthesizer and routed as shown in the following figure.

The maximum routing length for the 3VMRef and 3VMRef# signals is 8 inches.

Note: The following recommendations assume routing of the reference clocks on microstrip.

Figure 13. VddIR and 3VMRef Routing



Note: 3VMRef# should be routed in a similar manner as 3VMRef.

4.2.2. MCH to DRCG (Phase Aligning Clocks)

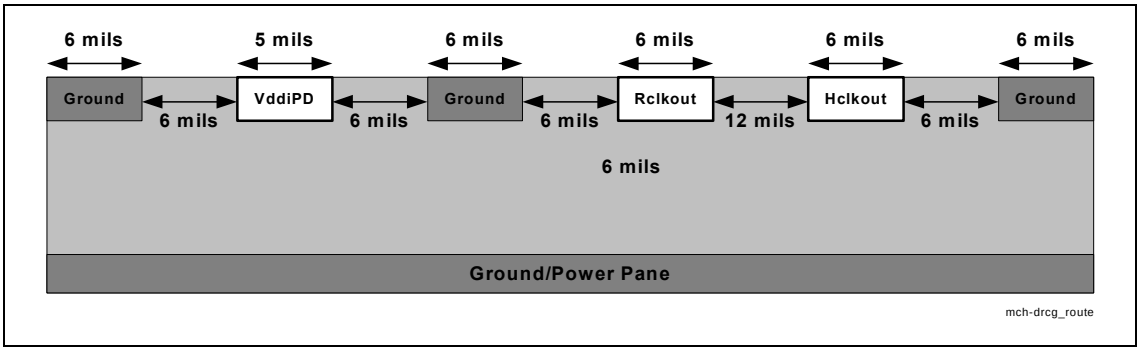
The RCLKOUT and HCLKOUT signals from the MCH should be routed to the SYNCLKN and PCLKM signals on the DRCG, respectively, as shown in the following figure Note that the VddiPD power pin on the DRCG can be connected directly to 1.8 V near the DRCG if the 1.8 V plane extends near the DRCG. However, if a 1.8 V trace must be run, it should originate at the CK00 clock synthesizer and be routed as shown with respect to RCLKOUT and HCLKOUT.

The maximum length for RCLKOUT and HCLKOUT is 6 inches. Additionally, these signals must be length matched within 50 mils. These signals should be routed on the same layer. If these signals must switch layers, then BOTH signals should change layers together.

If the VddIPD pin is connected to the 1.8 V plane using a via (i.e., trace is not run from the CK00 clock synthesizers), then HCLKOUT and RCLKOUT must still be routed as shown below and ground isolated.

Note: The following recommendations assume routing of the phase alignment clocks on microstrip.

Figure 14. MCH to DRCG Routing Diagram



Note: The signals Rclkout and Pclkout are channel specific, and their exact names are CHx_RCLKOUT and CHx_PCLKOUT, where x is the channel, either A or B. Consult the 850 chipset ballout document for more information.

4.2.3. DRCG to Rambus* Channels (300 MHz / 400 MHz Clocks)

The RDRAM device clock signals (CTM/CTM# and CFM/CFM#) are high-speed, impedance matched transmission lines that require strict routing recommendations to insure that the memory timings are met. The following RDRAM device clock recommendations should be strictly followed. Any deviations from the recommendations should be properly simulated.

4.2.3.1. Trace Lengths

The following figure shows the critical RDRAM device clock routing sections, with the routing lengths for each section defined in the following table.

Figure 15. Rambus* RDRAM* Device Clock Routing Dimension

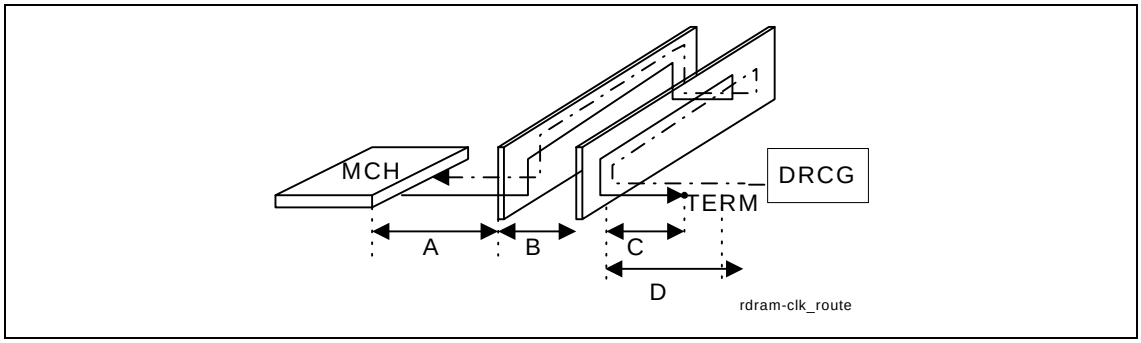


Table 6. Rambus* RDRAM* Device Clock Routing Guidelines

Clock	From	To	Length (inches)	Figure 15 Trace
CTM/CTM# (1)	DRCG	2nd RIMM Connector	0.0 – 6.0	D
	RIMM Connector	RIMM Connector	0.4 – 1.0	B
	1st RIMM Connector	MCH	1.0 – 6.0	A
CFM/CFM# (2)	MCH	1st RIMM Connector	1.0 – 6.0	A
	RIMM Connector	RIMM Connector	0.4 – 1.0	B
	2nd RIMM Connector	Termination	0.0 – 2.0	C

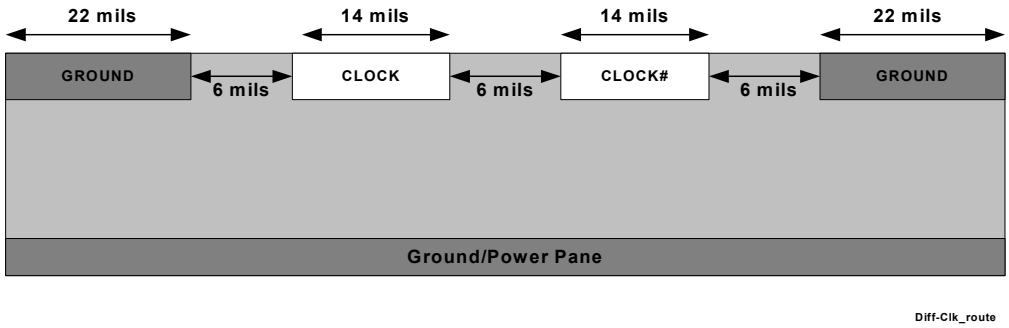
NOTES:
1. 1st RIMM connector to MCH:
   Trace length needs to be compensated to match the RSL signals from MCH to 1st RIMM connector.
2. MCH to 1st RIMM Connector:
   Trace length needs to be compensated to mach the RSL signals from 1st RIMM connector to MCH.

In clock routing sections “A” and “D,” it is recommended that the clock signals (CTM/CTM# and CFM/CFM#) be routed differentially. An example recommended topology for microstrip differential clock routing is shown in the following figure

Note: Clock trace widths and spacing may change with different prepreg thickness.

The clock signals shown in the example topology are 14 mils wide and routed differentially. There must be a 22-mil ground isolation trace routed around the clock differential pair signals. The 22 mil ground isolation traces must be connected to ground with a via per every 1 inch. A via must be placed within less than 0.5 inches of the beginning and end of the ground isolation trace. A 6-mil gap is required between the clock signals and between the clocks and ground isolation traces.

Figure 16. Differential Clock Routing Diagram



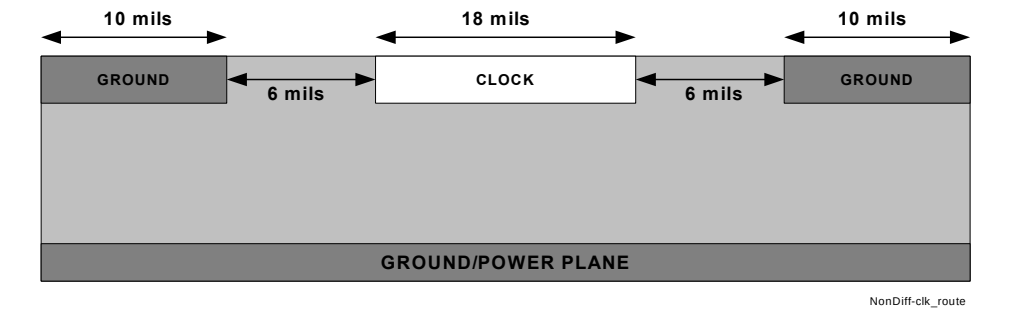
Note: "CLOCK" stands for the signals CTM and CFM and "CLOCK#" stands for the signals CTM# and CFM#.

In clock routing section "B," it is recommended that the clock signals (CTM/CTM# and CFM/CFM#) be routed non-differentially due to the short routing lengths between RIMM connectors. An example recommended topology for microstrip non-differential clock routing is shown in Figure 17.

Note: Clock trace widths and spacing may change for different prepreg thickness.

The clock signals shown in the example topology are routed with 18 mil wide traces. When routing the clocks non- differentially, there must be a 10-mil ground isolation trace routed around the single ended clock signals. The 10 mil ground isolation traces must be connected to ground with a via per every 1 inch. A 6-mil gap is required between the clock signals and the ground isolation traces.

Figure 17. Non-Differential Clock Routing Diagram



Note: "CLOCK" stands for the signals CTM, CTM#, CFM and CFM#.

Note: The CTM/CTM# and CFM/CFM# clock signals must be ground referenced (with continuous ground island/plane) at all times.

4.2.3.2. Topology Considerations

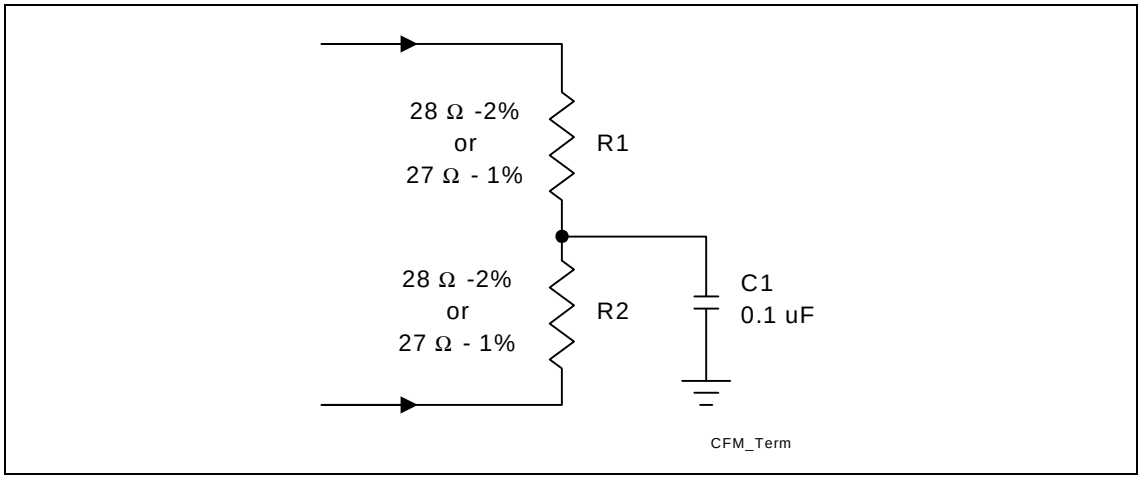
Package trace compensation, via compensation and Rambus* Signaling Level (RSL) signal layer alteration must also be considered when routing the RDRAM device clocks. Additionally, 0.021 inches of CLK per 1 inch of RSL trace length must be added to compensate for the clock's faster trace velocity when routing on microstrip layers.

- For clock routing section "A," the CTM/CTM# and CFM/CFM# clocks must be length matched within ±2 mils to the RSL channel trace length. Exact matching is preferred.
- For clock routing section "B," the CTM/CTM# and CFM/CFM# clocks must be length matched within ±2 mils to the RSL channel trace length. Exact matching is preferred.
- For trace section "C," the CFM/CFM# clocks must be length matched within ±2 mils to the RSL channel trace length. Exact matching is preferred.
- For trace section "D," the CTM/CTM# clocks must be length matched within ±2 mils to the RSL channel trace length. Exact matching is preferred.

4.2.3.3. Rambus* RDRAM* Device Clock Termination

The CFM/CFM# differential pair signals require termination using either 27 Ω 1% or 28 Ω 2% resistors and a 0.1 µF capacitor as shown in the following figure.

Figure 18. CFM/CFM# Termination



4.2.4. DRCG Impedance Matching Circuit

The external DRCG impedance matching circuit is shown below.

Figure 19. DRCG Impedance Matching Network

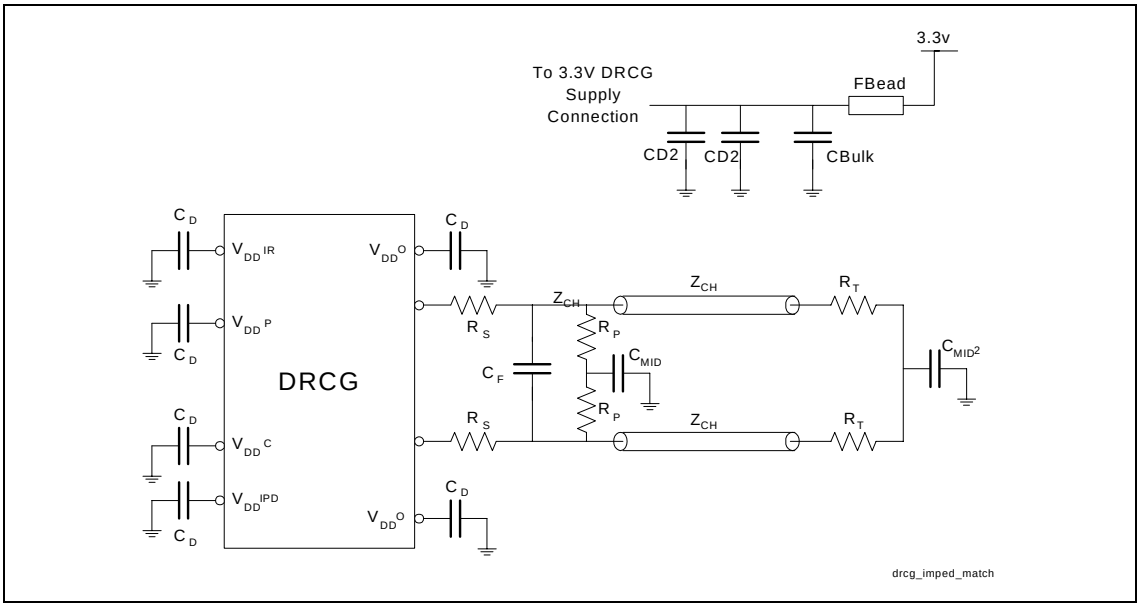


Table 7. DRCG Impedance Matching Network Values

Component	Nominal Value	Notes
C_D	0.1 µF	Decoupling caps to GND
R_S	39 Ω	Series termination resistor
R_P	51 Ω	Parallel termination resistor
C_{MID1}, C_{MID2}	0.1 µF	Virtual GND caps
R_T	27 Ω	End of channel termination
C_F	4-15 pF	Do Not Stuff, leave pads for future use
FBead	50 Ω @ 100 MHz	Ferrite bead
CD2	0.1 µF	Additional 3.3 V decoupling caps
CBulk	10 µF	Bulk cap on device side of ferrite bead

NOTES:

1. Note the removal of the original EMI capacitors between the junctions of RS, RP and ground. These capacitors had minimal impact on EMI and increased DRCG output jitter by approximately 2X.
2. The intent of component CF is to decouple CLK and CLKB outputs to each other, but data shows this actually increases device jitter. CF should not be stuffed at this time.
3. The ferrite bead and 10 µF bulk cap combination improves jitter and helps to keep the clock noise away from the rest of the system. The additional 3.3 V capacitors (CD2) have a minor positive impact, but the ideal values have not been extensively optimized.
4. 0.1 µF capacitors are better than 0.01 µF or 0.001 µF capacitors for DRCG decoupling. Most decoupling experiments that replaced 0.1 µF capacitors with higher frequency caps ended up with the same or worse jitter. Replacing existing 0.1 µF capacitors with higher frequency capacitors is not advised.
5. Cmid at 0.1 µF has improved jitter versus Cmid at 100 pF. However, this will increase the latency coming out of a stop clock or tri-state mode.

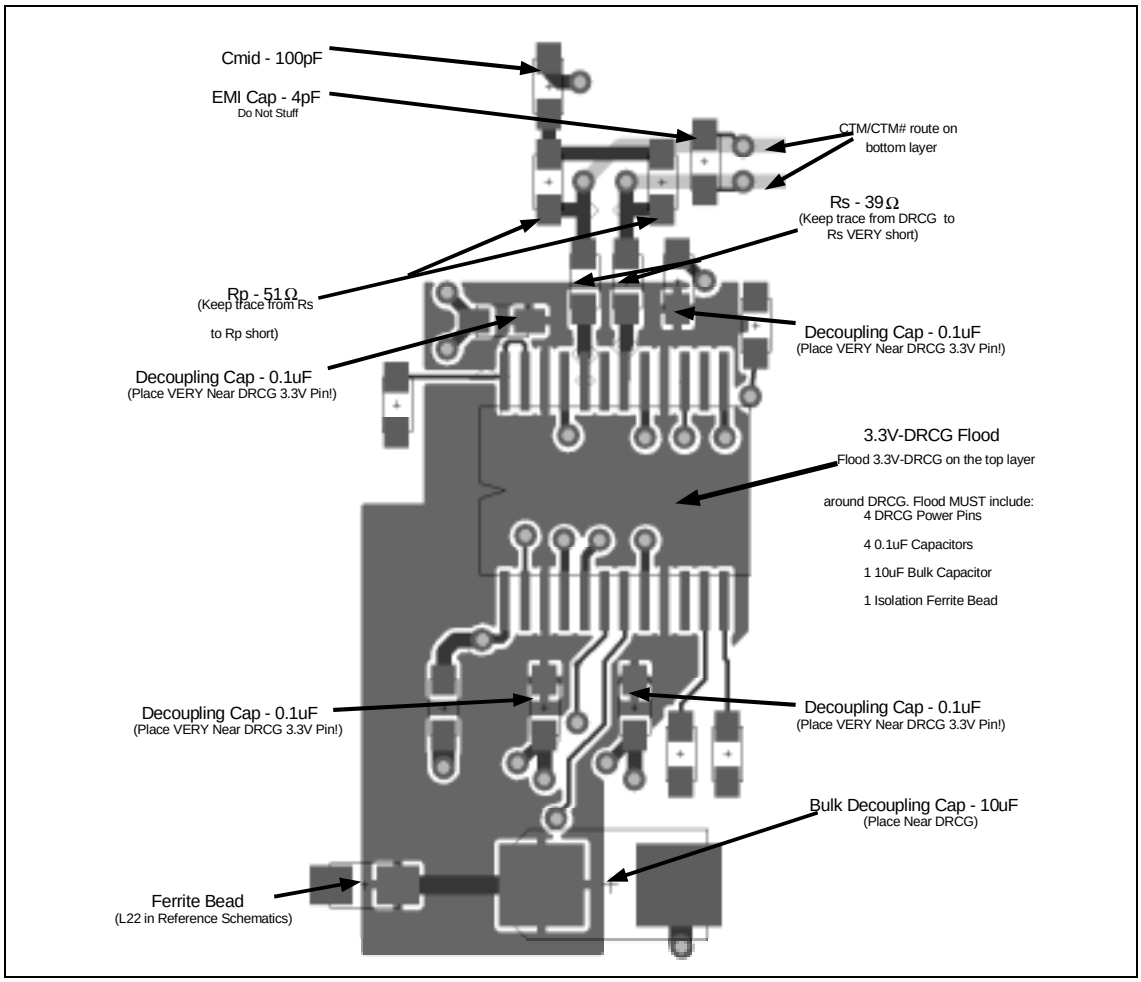
6. RS, RP, RT were modified to improve channel signal integrity through increasing CTM/CTMN swing.

The circuit shown is required to match the impedance of the DRCG to the 28 Ω channel impedance. More detailed information can be found in the Direct RAMBUS* Clock Generator Specification.

The previously recommended 15 pF capacitors on CTM/CTM# should be removed. The 4 pF capacitor shown in the figure should not be assembled ("no-stuff").

4.2.5. DRCG Layout Example

Figure 20. DRCG Layout Example

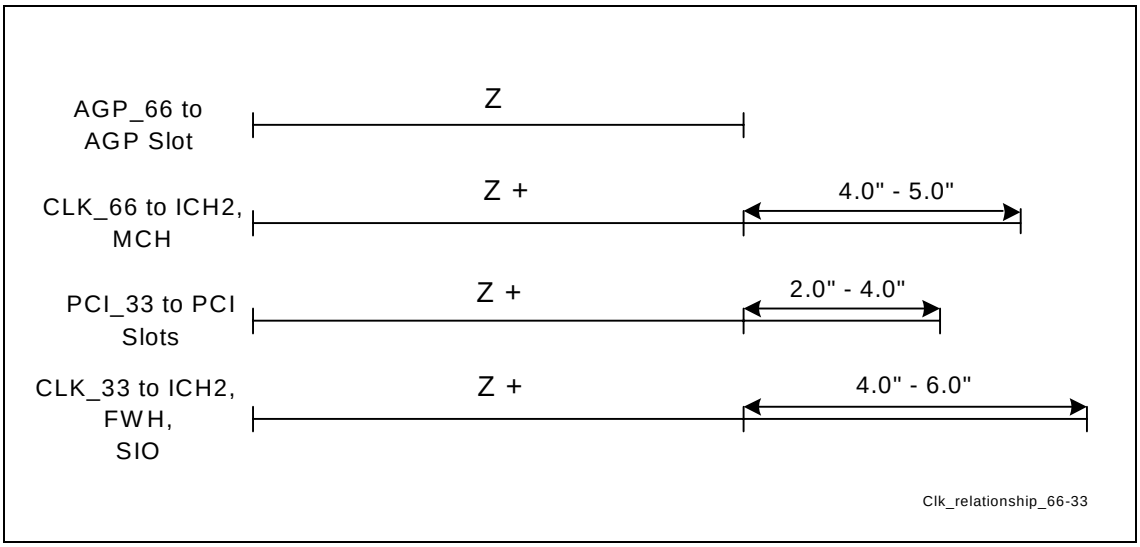


4.3. Routing Guidelines for 66 MHz and 33 MHz Clocks

4.3.1. 66 MHz / 33 MHz Clock Relationships

The following figure shows the clock routing relationships between the 66 MHz clocks and the 33 MHz clocks. The routing guidelines and the topologies for these clocks are also documented.

Figure 21. 66 MHz / 33 MHz Clock Relationships



The following table summarizes the layout recommendations between the CK00 clock synthesizer and the AGP connector, MCH and ICH2 components, which require a 66 MHz clock.

4.3.2. 66 MHz Clock Routing Length Guidelines

Table 8. 66 MHz Clock Routing Length Guidelines

Clock Group	Length of Trace A (in)	Length of Trace B (in)	R1 (Ω)
AGP_66	0 inches to 0.5 inches	Z	33
CLK_66	0 inches to 0.5 inches	Z + (4 inches – 5 inches)	33

Note: The routing length value of Z is 5 inches to 9 inches.

The following two figures show the recommended clock routing topologies for the 66 MHz clocks.

Figure 22. AGP_66 Clock Routing Topology

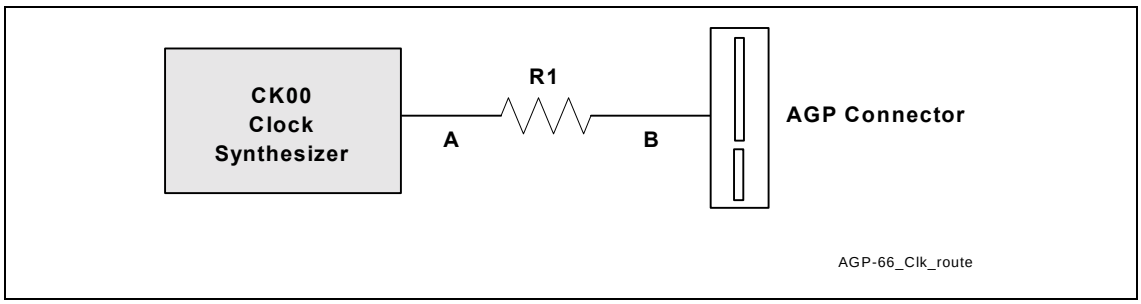
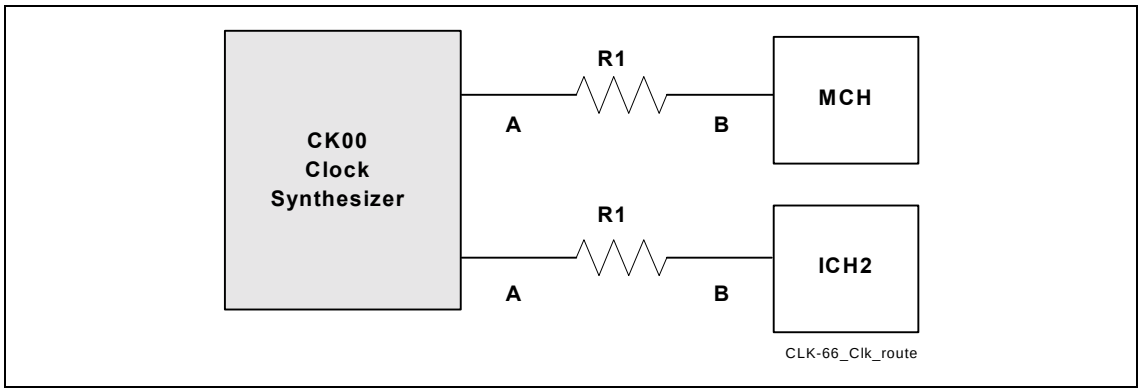


Figure 23. CLK_66 Clock Routing Topology



4.3.3. 33 MHz Clock Routing Length Guidelines

The following table summarizes the layout recommendations between the CK00 clock synthesizer and PCI connectors, ICH2, FWH and SIO components, which require a 33 MHz clock.

Table 9. 33 MHz Clock Routing Guidelines

Clock Group	Length of Trace A (in)	Length of Trace B (in)	R1 (Ω)
PCI_33	0 inches to 0.5 inches	Z + (2 inches – 4 inches)	33
CLK_33	0 inches to 0.5 inches	Z + (4 inches – 6 inches)	33

Note: The routing length value of Z is 5 inches to 9 inches.

The following two figures show the recommended clock routing topologies for the 33 MHz clocks.

Figure 24. PCI_33 Clock Routing Topology

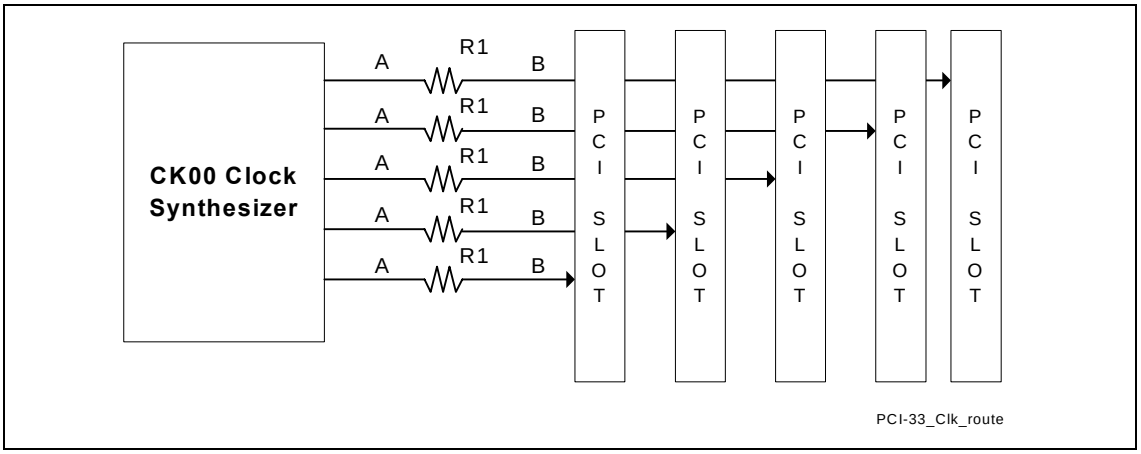
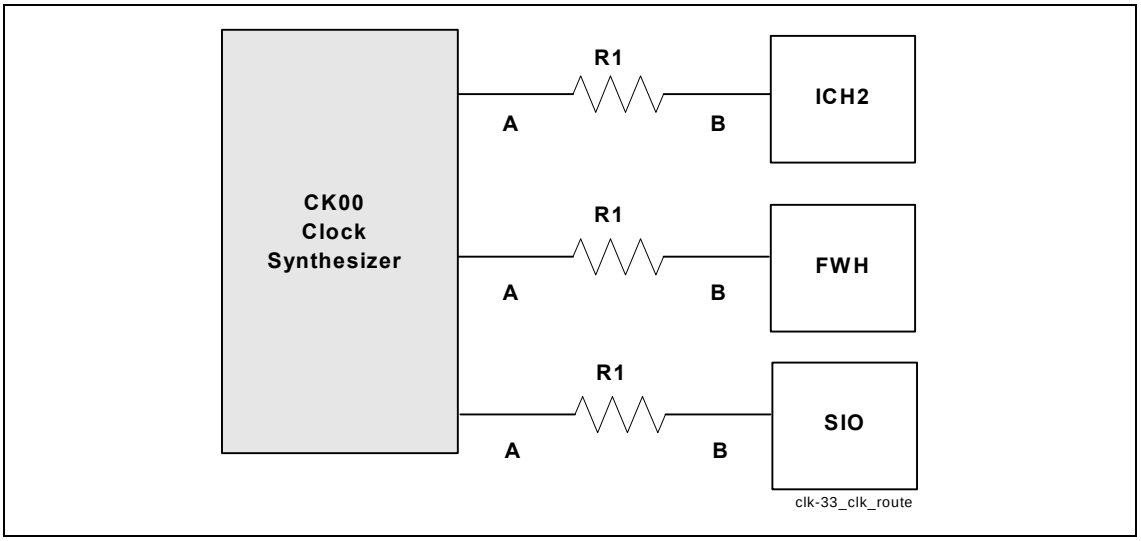


Figure 25. CLK_33 Clock Routing Topology



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5. System Bus Routing

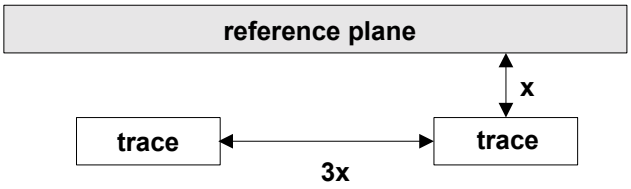
The following table summarizes the layout recommendations for Pentium 4 processor configurations and expands on specific design issues and their recommendations.

Table 10. System Bus Routing Summary for Intel® Pentium® 4 Processor

Parameter	Intel® Pentium® 4 Processor Routing Guidelines
Line to line spacing	Greater than 3:1 edge-to-edge spacing versus trace to reference plane height ratio. See Figure 26 for an illustration of this recommendation.
Data Line lengths (agent to agent spacing)	2 inches – 10 inches from pin-to-pin Data signals of the same source synchronous group should be routed to the same pad-to-pad length ±100 mils. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. These package lengths and a worksheet to aid in length compensation can be found in the *Intel® Pentium® 4 Signal Integrity Models*.
DSTBn/p[3:0]#	DSTBn/p# should be routed to the same length as their corresponding data signals' mean pad-to-pad length ±25 mils. A data strobe and its complement should be routed within ±25 mils of the same pad-to-pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. These package lengths and a worksheet to aid in length compensation can be found in the *Intel® Pentium® 4 Signal Integrity Models*.
Address line lengths (agent to agent spacing)	2 inches – 10 inches Address signals of the same source synchronous group should be routed to the same pad-to-pad length ±100 mils. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. These package lengths and a worksheet to aid in length compensation can be found in the *Intel® Pentium® 4 Signal Integrity Models*.
ADSTBn/p[3:0]#	ADSTBn/p# should be routed to the same length as their corresponding address signals' mean pad-to-pad length ±25 mils. An address strobe and its complement should be routed within ±25 mils of the same pad-to-pad length. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. These package lengths and a worksheet to aid in length compensation can be found in the *Intel® Pentium® 4 Signal Integrity Models*.
Common Clock line lengths	6.2 inches – 10 inches pin-to-pin No length compensation is necessary.
Topology	Point to point (chipset to processor).
Routing priorities	All associated signals and strobes should be routed on same layer for entire length of bus. Ideally, layer changes should not occur for any signals. If a layer change must occur, reference plane must remain the same. Refer to Section 5.3 for specific details.

Parameter	Intel® Pentium® 4 Processor Routing Guidelines
Serpentine spacing	S/H ratio greater than or equal to 4. Keep parallel sections as short as possible. Minimize 90° bends. Make 45° bends if possible. See Figure 27 for an illustration of this recommendation.
Clock and strobe keepout zones	A spacing requirement of 25 mils should be maintained around all clock and strobe traces.
System board Impedance	50 Ω ± 15%

Figure 26. Cross-Sectional View of 3:1 Ratio



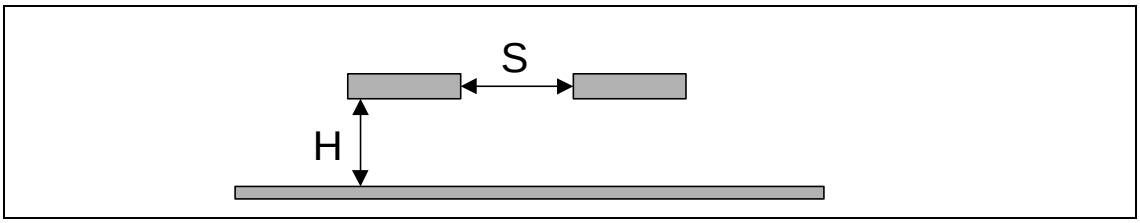
Note: This is the edge-to-edge trace spacing versus trace to reference plane height.

A trace spacing to height above reference plane ratio of 3 to 1 ensures a low crosstalk coefficient. Intel has performed extensive simulation and experimentation on the effects of crosstalk to more accurately predict these effects. The timing and layout guidelines for the Pentium 4 processor have been created with the assumption of a 3:1 trace spacing to height above reference plane ratio.

A serpentine net is a transmission line that is routed in such a manner so that sections of the net double back and forth and purposefully take a longer path. Serpentining a transmission line is sometimes necessary to properly match lengths between nets. It is important to properly control the serpentine in order to avoid signal integrity and timing problems that result from the expected coupled behavior of a serpentined net. The primary impact is an observed decrease in the flight time when compared to a straight trace of equal length. This decrease in the flight time is a result of the crosstalk between parallel sections of the serpentined net. As the signal travels down the transmission line, a component of the signal will follow the transmission line and behave as though it were a straight line with no serpentine. However, another portion of the energy will propagate perpendicular to the parallel routed portions of the serpentined net via the mutual capacitance and mutual inductance. This creates an extra mode that will arrive at the receiver significantly earlier than the other component of the signal. If the coupling between parallel sections is high, this will cause significant timing skew when attempting to match trace lengths. Furthermore, if the coupling is very high, significant signal integrity problems can result.

The serpentine guidelines included in this document were based on simulations with different spacing between parallel sections. The guidelines were chosen to significantly limit the effect of serpentining. The following illustrates the serpentine edge-to-edge spacing versus trace to reference plane height ratio.

Figure 27. Serpentine Spacing (Spacing to Reference Plane Height Ratio)



5.1. Return Path

The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, vias, VRMs etc. It is useful to think of the return path as following a path of least resistance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths need to be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance will be.

The following sets of return path rules apply to all designs:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near System Bus signals.
- Do not make signal layer changes that force the return path to make a reference plane change even if it is from one V_{SS} layer to another V_{SS} layer.
- Do not route over via anti-pads or socket anti-pads

5.2. System Bus Decoupling Requirements

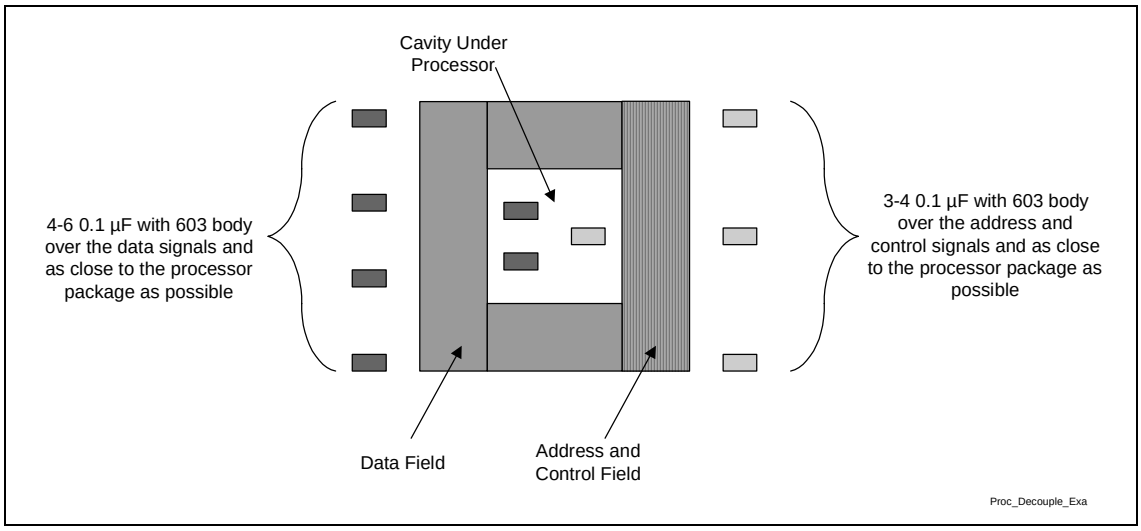
This section contains the system board decoupling recommendations that are needed for providing robust I/O power delivery along with minimizing any anticipated return path discontinuities. These are decoupling requirements for the System Bus I/O *only*. For decoupling requirements for the processor, refer to *Section 11, Intel® Pentium® 4 Processor Power Distribution Guidelines*.

The primary objective of the processor decoupling guidelines is to minimize the impact of return path discontinuities. The power delivery guidelines for the processor insures that the System Bus achieves adequate power decoupling. The primary return path discontinuity anticipated is for systems that use traces that have only one reference plane, such as microstrip structures on the system board. The Pentium 4 processor package utilizes symmetric stripline configurations with V_{CC} as one reference plane and V_{SS} as the other reference plane. If the system board uses striplines with V_{CC} and V_{SS} references, then a discontinuity does not exist and additional decoupling is not necessary. If the system board uses microstrip or embedded microstrip configurations for the System Bus signals, then a return path discontinuity exists between the processor and the system board and decoupling capacitors are required, as illustrated in the following figure.

If a stripline to microstrip discontinuity exists, the decoupling requirements for each processor are:

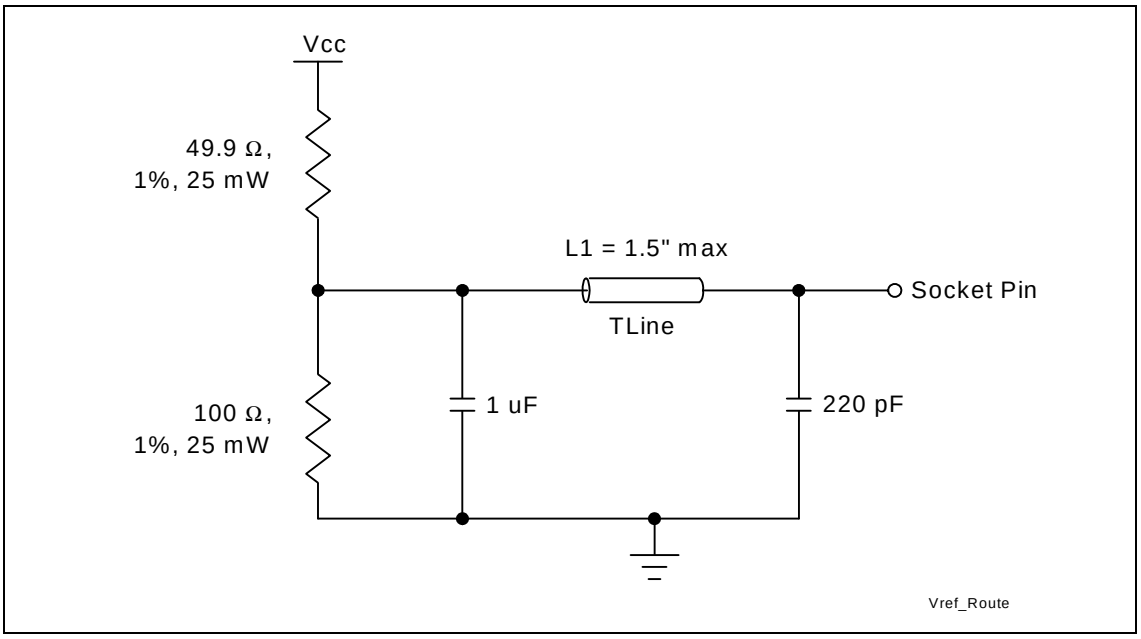
- Four minimum, six preferred 0.1 µF capacitors with 603 packages distributed evenly over the system bus data lines
- Three minimum, four preferred 0.1 µF capacitors with 603 packages distributed evenly over the system bus address and control lines
- All capacitors placed as close to the processor package as the processor keep-out zone allows

Figure 28. Example of Processor Decoupling for a Return Path Discontinuity



There are four AGTL+ GTLREF pins on the Pentium 4 processor that are used to set the reference voltage level for the AGTL+ signals (V_{REF}). The 850 chipset has HDVREF[3:0] pins for V_{REF} for the data signals, HAVREF[1:0] pins for V_{REF} for the address signals, and CCVREF for the common clock signals. The guidelines provided below for the generation of the V_{REF} voltage apply to all these pins.

Figure 29. V_{REF} Routing



- The processor must have at least two dedicated voltage dividers.
- Decouple each voltage divider with a 1 µF capacitor.
- Keep the voltage dividers within 1.5 inches of the first V_{REF} pin
- Decouple each pin with a high frequency capacitor (e.g., a 220 pF, 603) as close to each pin as possible
- Keep signal routing at least 20 mils separated from the V_{REF} routes
- Trace width should be kept at 25 mils apart.
- Do not allow signal lines to use the V_{REF} routing as part of their return path (i.e., do not allow the V_{REF} routing to create splits or discontinuities in the reference planes of the system bus signals.)

Due to the placement of the V_{REF} pins on the Pentium 4 processor, it may not be possible to route all four pins from two voltage dividers. It is acceptable to use more than two voltage dividers with decoupling at each processor and the chipset. The following figures illustrate some of the options for connecting V_{REF} to the four-processor V_{REF} pins.

Figure 30. Dual V_{REF} Daisy Chain Routing Example

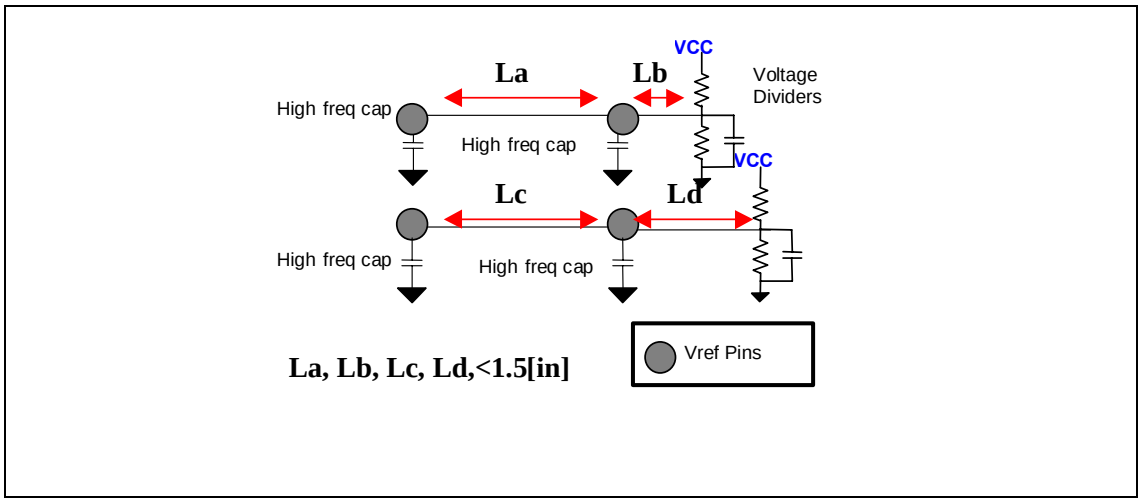


Figure 31. Dual V_{REF} Voltage Dividers Routing Example

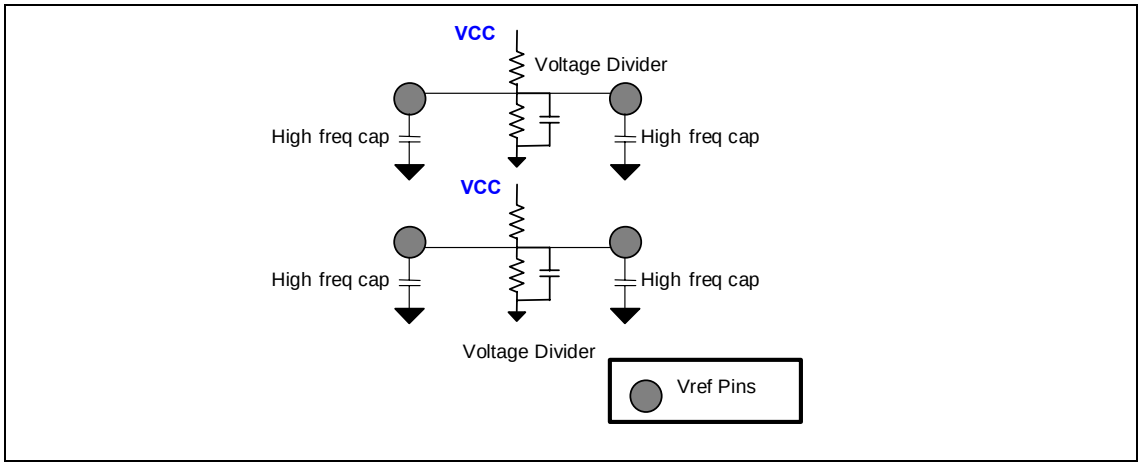
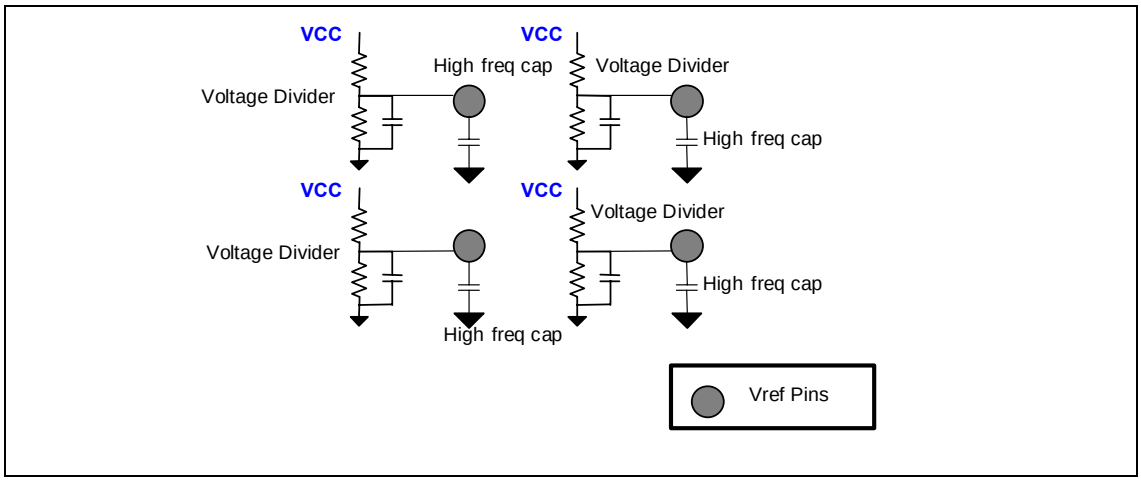


Figure 32. Four V_{REF} Voltage Dividers



5.2.1. Technology Assumptions

It is important to check return paths to insure that signals are not routed over via anti-pads.

5.3. Intel® Pentium® 4 Processor Configuration

This section provides more details for routing Pentium 4 processor based systems. For proper operation of the Pentium 4 processor and the 850 chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation. The most accurate way to understand the signal integrity and timing of the system bus in your platform is by performing a comprehensive simulation analysis.

A schematic of the Pentium 4 processor topology is shown in the figure titled *Intel® Pentium® 4 Single Processor Topology*. The trace impedance should be 50 Ω ± 15%. The traces should maintain a greater than three to one edge-to-edge spacing versus trace to reference plane height ratio (see Figure 33). Simulations performed at Intel have assumed, for nominal conditions, a 7-mil wide trace and 13 mil edge-to-edge spacing. As the traces pass through the pin fields the 3:1 requirement may not be achievable. In these areas where the 3:1 ratio is not possible, the separation should be maximized and the distance should be minimized.

Refer to the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet for a system bus signal list, signal types and definitions.

5.3.1. Topology and Routing

Table 11. Source Synchronous Signal Groups and the Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	ADSTB0#
A[32:17]#	ADSTB1#
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#

Design Recommendations are presented first, followed by Design Considerations.

5.3.1.1. Design Recommendations

Below are the design recommendations for the data, address, strobes, and common clock signals. The pad is defined as the attach point of the silicon die to the package substrate.

Data

- The pin-to-pin distance from the processor to the chipset should be between 2.0 inches to 10 inches (i.e., 2.0inches < L1 < 10 inches). Data signals of the same source synchronous group should be routed to the same pad-to-pad length ±100 mils. As a result, additional trace will be added to some data signals on the system board in order for all trace lengths within the same data group to be the same length (±100 mils) from the pad of the processor to the pad of the chipset. This length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without the length compensation the flight times between a data signal and its strobe will be different, which results in an inequity between the setup and hold times. Since the strobe typically has a shorter package length there will be favoritism toward hold time and, thus, the setup requirement may not be able to be met without length compensation on the system board.
- Source synchronous groups and associated strobes should be routed on the same layer for the entire length of the bus. This results in a significant reduction of the flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stack-up.

Equation 1. Calculation to Determine Package Delta Addition to System Board Length for UP Systems

$$delta_{net,group} = (max\_cpu\_pkglen_{group} - cpu\_pkglen_{net}) + (max\_cs\_pkglen_{group} - cs\_pkglen_{net})$$

Address

- Address signals follow the same rules as data signals. However, address signals may change layers if reference plane remains the same and V_{CC} and/or V_{SS} vias are placed as close to the signal via as possible.

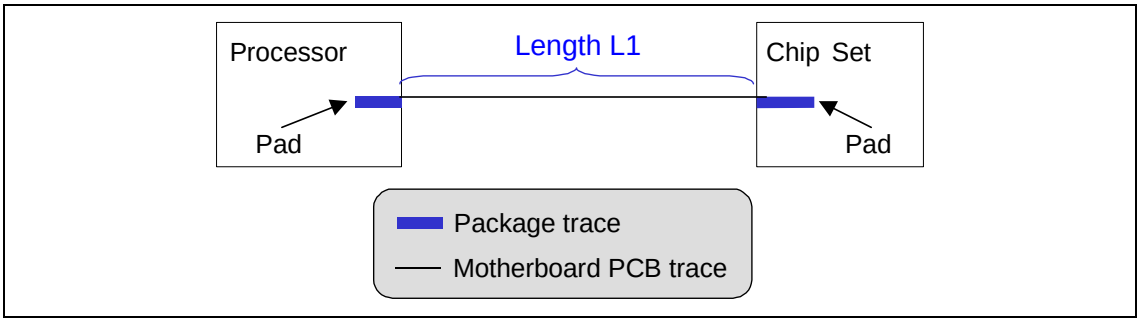
Strobe

- A strobe and its complement should be routed to a length equal to their corresponding data group's mean pad-to-pad length ±25 mils. This causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. A strobe and its complement (xSTBp/n) should be routed to ±25 mils of the same length. It is recommended to simulate skew in order to determine the length that best centers the strobe for a given system.

Common Clock

- Common clock signals should be routed to a minimum pin-to-pin system board length of 6.2 inches and a maximum system board length of 10 inches.

Figure 33. Intel® Pentium® 4 Processor: Single Processor Topology



5.3.1.2. Design Considerations

Intel has found that the following recommendations aid in the routing of the Pentium 4 processor, given the example stack-up shown in *Section 3.2*.

- Line width is 7.0 mil (~5 mils in the pin field region).
- Trace to trace spacing is 13.0 mil (except in component breakout where spacing is constrained)

5.4. Routing Guidelines for Asynchronous GTL+ and Other Signals

This section describes layout recommendations for signals other than data, strobe and address. The following table lists the signals covered in this section.

Table 12. Miscellaneous Signals (Signals that are Not Data, Address, or Strobe)[1]

Signal Name	Type	Direction	Topology	Driven by	Received by	Notes
A20M#	Asynchronous GTL+	I	2	ICH2	Processor	
BR0#	AGTL+	I/O	5	Processor		
COMP[1:0]	analog	I	6	External logic	Processor	
FERR#	Asynchronous GTL+	O	1	Processor	ICH2	
IGNNE#	Asynchronous GTL+	I	2	ICH2	Processor	
INIT#	Asynchronous GTL+	I	2	ICH2	Processor	
LINT0/INTR LINT1/NMI	Asynchronous GTL+	I	2	ICH2	Processor	
PROCHOT#	Asynchronous GTL+ OD	O	1	Processor	External logic	
PWRGOOD	Asynchronous GTL+ OD	I	2-A	ICH2	Processor	
RESET#	AGTL+ OD	I	7	MCH	Processor	
SLP#	Asynchronous GTL+	I	2	ICH2	Processor	
SMI#	Asynchronous GTL+	I	2	ICH2	Processor	
STPCLK#	Asynchronous GTL+	I	2	ICH2	Processor	
THERMTRIP#	Asynchronous GTL+	O	3	Processor	External logic	
V_{CCA}	power	I	4	External logic	Processor	
$V_{CCIOPLL}$	power	I	4	External logic	Processor	
$V_{CCSENSE}$	other	O		Processor	V_{REG}/external logic	2
V_{ID}[4:0]	other	O		Processor	V_{REG}	2
V_{SSA}	power	I	4	Ground	Processor	
$V_{SSSENSE}$	other	O		Processor	V_{REG}/external logic	2

NOTES:
1. Not included are the debug port signals TCK, TDO, TDI, TMS, and TRST#. Refer to the chapter titled *Debug Port Specifications* in the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet.
2. For more information on these signals, refer to the *Intel® Pentium® 4 Power Distribution Guidelines.*
3. All miscellaneous signals that require a pull-up should be pulled up to V_{CC_CPU}.

All signals must meet the AC and DC specifications as documented in the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet.

5.4.1. Topologies

The figures in this section show the possible topologies for the miscellaneous signals and list the layout recommendations. Table 13 through Table 17 detail the layout recommendations for each corresponding topology. Table 12 lists the signals and specifies the topology for each. The topologies are described in the following sections.

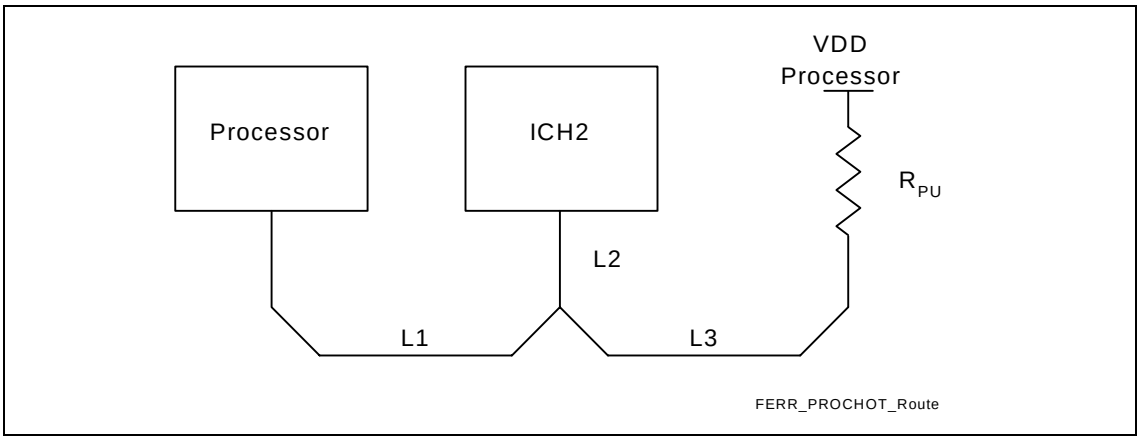
5.4.1.1. Topology 1: Asynchronous GTL+ Signals Driven by Intel® Pentium® 4 Processor

These signals (FERR# and PROCHOT#) should adhere to the following routing and layout recommendations. The following figure illustrates the recommended topology. Do not create a stub to connect to the socket pins.

Table 13. Layout Recommendations for Miscellaneous Signals (Topology 1)

Trace Zo	Trace Spacing	L1	L2	L3	Rpu
50 Ω	10 mil	1 inch– 12 inches	1.1 inches max	3 inches max	56 ±5% Ω

Figure 34. Routing Illustration for FERR# and PROCHOT#



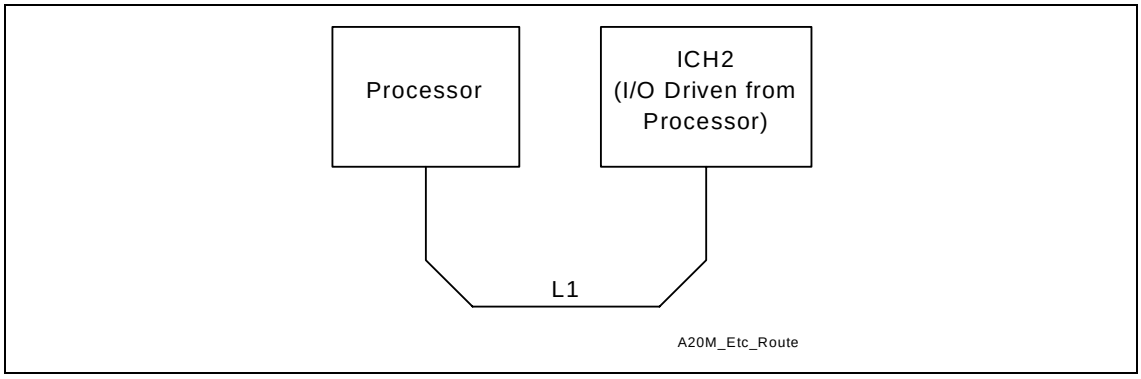
5.4.1.2. Topology 2: Asynchronous GTL+ Signals Driven by ICH2

These signals (A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, and STPCLK#) should adhere to the following routing and layout recommendations. The Figure 35 illustrates the recommended topology. Do not create a stub to connect to the socket pins.

Table 14. Layout Recommendations for Miscellaneous Signals (Topology 2)

Trace Zo	Trace Spacing	L1	Rpu
50 Ω	10 mil	12 inches max	None

Figure 35. Routing Illustration for A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, and STPCLK#



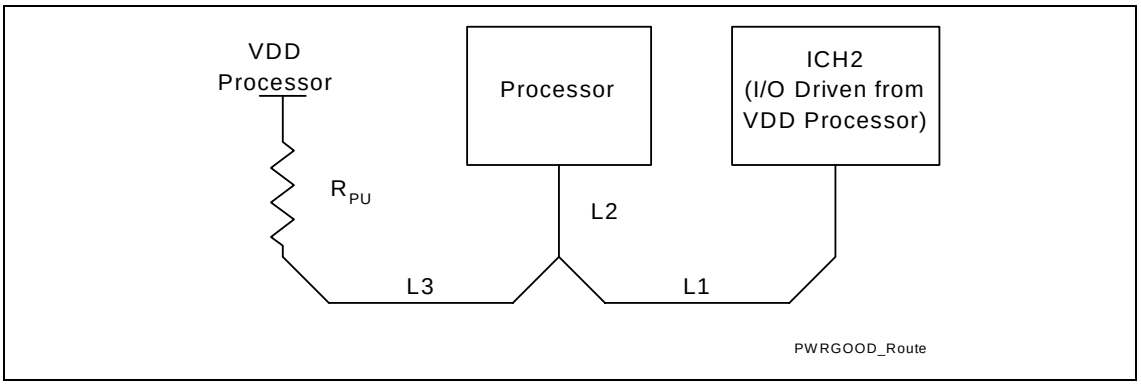
5.4.1.3. Topology 2A: Asynchronous GTL+ Signals Driven by ICH2 Open Drain

This signal (PWRGOOD) should adhere to the following routing and layout recommendations. The following figure illustrates the recommended topology. Do not create a stub to connect to the socket pins.

Table 15. Layout Recommendations for Miscellaneous Signals (Topology 2A)

Trace Zo	Trace Spacing	L1	L2	L3	Rpu
50 Ω	10 mil	1 inch– 12 inches	1.1 inches max	3 inches max	300 Ω ±5%

Figure 36. Routing Illustration for PWRGOOD



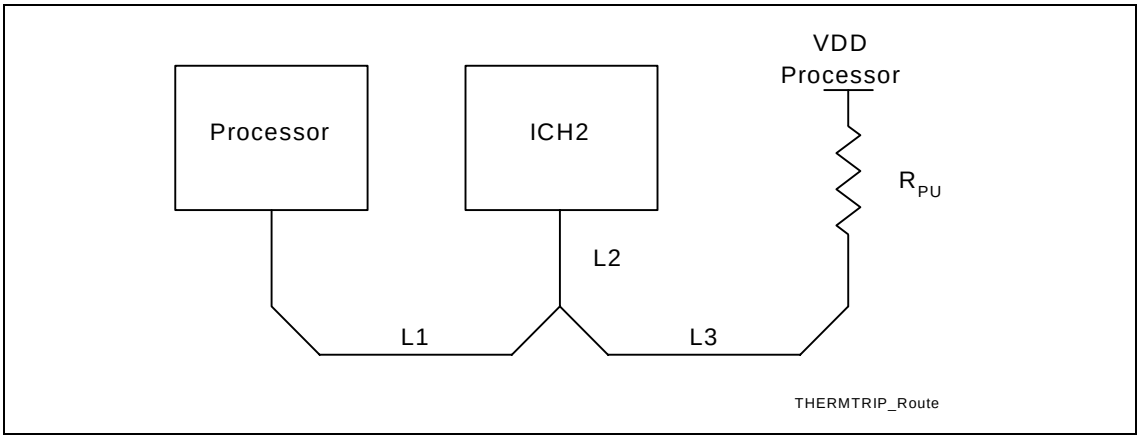
5.4.1.4. Topology 3: Asynchronous GTL+ Signals Driven by Intel® Pentium® 4 Processor

The signal in this topology is THERMTRIP#. Below are the routing and layout recommendations for the THERMTRIP# signal. Each signal must be terminated. The following figure illustrates the recommended topology.

Table 16. Layout Recommendations for Miscellaneous Signals (Topology 3)

Trace Zo	Trace Spacing	L1	L2	L3	Rpu
50 Ω	10 mil	1 inch–12 inches	1.1 inches max	3 inches max	56 ±5% Ω

Figure 37. Routing Illustration for THERMTRIP#



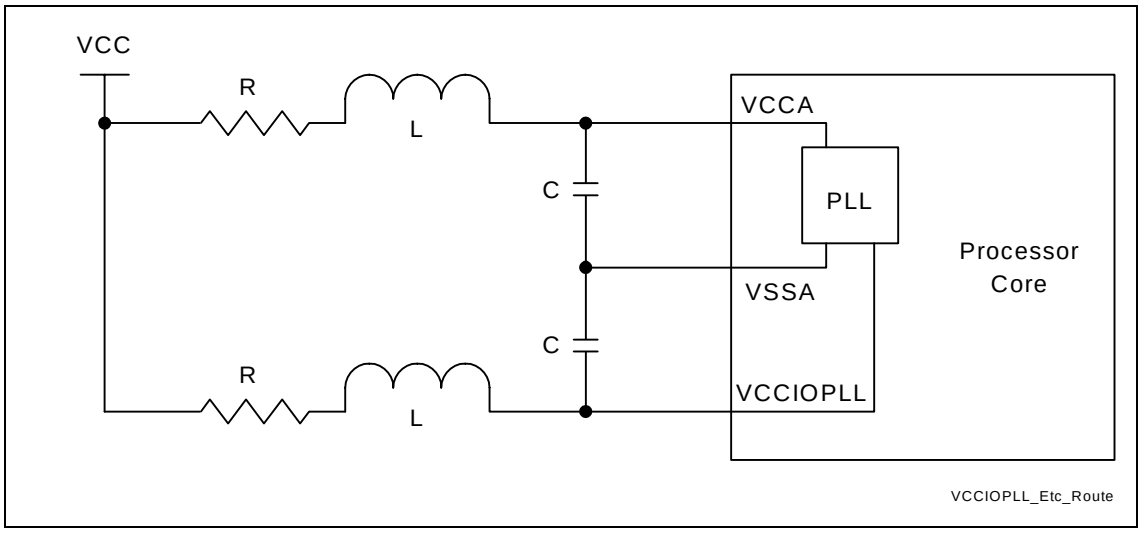
5.4.1.5. Topology 4: $V_{CCIOPLL}$, V_{CCA} and V_{SSA}

$V_{CCIOPLL}$ and V_{CCA} are isolated power for internal PLLs. It is critical that they have clean, noiseless power on their input pins. Keep these signals away from noisy or high frequency signals. Keep their traces as short as possible. Follow the recommendations in the following figure for layout guidelines. V_{SSA} should not be connected to ground on the system board. Further details can be found in the *Intel® Pentium® 4 Processor Power Distribution Guidelines*.

Table 17. Layout Recommendations for Miscellaneous Signals – Topology 4

R	L	C
1 Ω	4.7 uH	33 µF

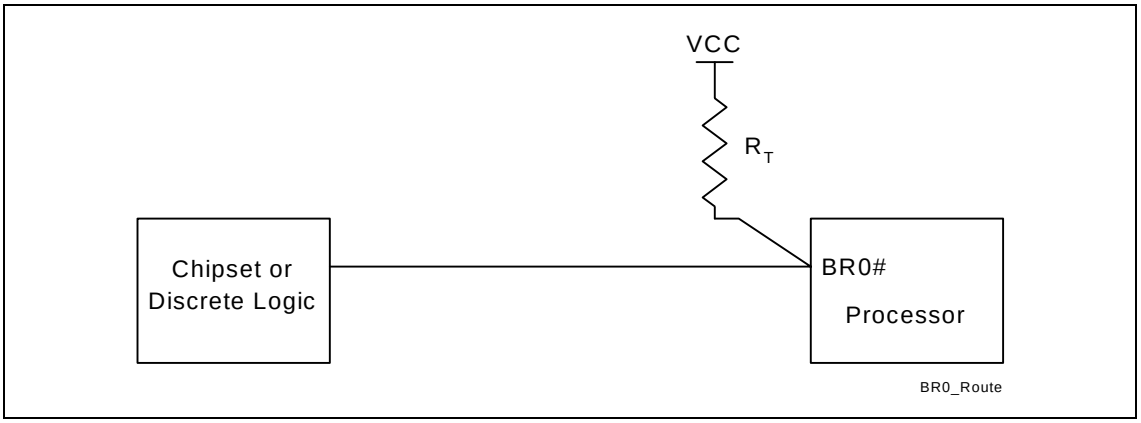
Figure 38. Routing Illustration for $V_{CCIOPLL}$, V_{CCA} and V_{SSA}



5.4.1.6. Topology 5: BR0# Signal Driven by Intel® Pentium® 4 Processor

Since the Pentium 4 processor **does not have on-die termination on the BR0# signal**, it is necessary to terminate using discrete components on the system board. Connect the BR0# signal between the components as shown in the following figure. The 850 chipset has on-die termination for BR0# and, thus, it is necessary to terminate only at the processor end. The value of Rt should equal the value of Rtt specified in the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet (36 Ω to 46 Ω).

Figure 39. Routing Illustration for BR0#



5.4.1.7. Topology 6: COMP[1:0] Signals

Terminate the COMP[1:0] pins to ground through a 43.2-Ω ±1% resistor as close as possible to the pin. Do not wire COMP[1:0] pins together; connect each pin to its own termination resistor. The R_{COMP} value can be adjusted to set external drive strength of I/O and to control the edge rate.

5.4.1.8. Topology 7: Recommendation for RESET#

Connect to MCH and pull-up to V_{CC} with 43 Ω ±5% resistor at the processor end. This signal does not have on die termination.

5.4.1.9. Topology 8: THERMDA/THERMDC Routing Guidelines

The Pentium 4 processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the Pentium 4 processor for thermal management/long term die temperature change monitoring purpose. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Routing Guidelines for THERMDA/THERMDC

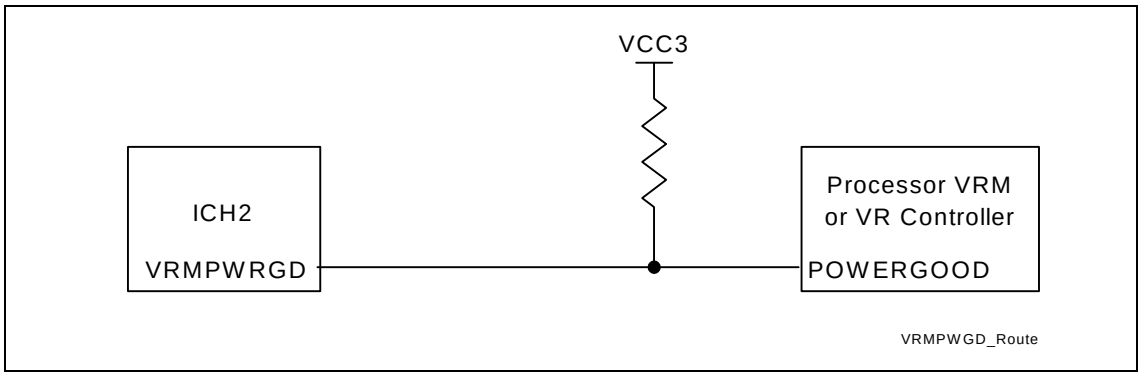
Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. Below are some guidelines:

- Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be around 4 to 8 inches away as long as the worst noise sources such as clock generator, data and address buses etc. are avoided.
- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.
- Leakage currents due to PC board contamination must be considered. Error can be introduced by the leakage current.
- Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. The width of 10 mil and space of 10 mil is recommended.
- A shielded twisted pair is recommended for a long distance remote sensor.

5.4.1.10. Topology 9: VRMPWRGD Routing

The VRMPWRGD signal on the ICH2 should be connected to the powergood signal on the processor VRM. This signal also requires a 10 kΩ pull-up to V_{CC3} on the system board.

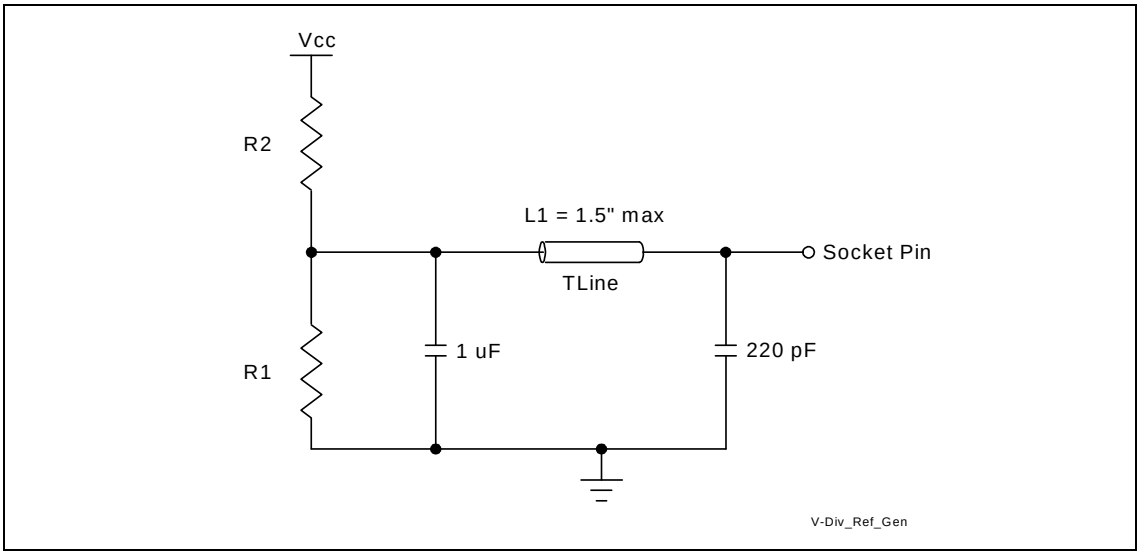
Figure 40. Routing Illustration for VRMPWRGD



5.5. Intel® 850 Chipset MCH System Bus Interface

A voltage divider network should supply host interface reference voltages locally as shown in the following two figures and as specified by the following table.

Figure 41. Voltage Divider Network for Reference Voltage Generation



- The 82850 MCH has only one dedicated voltage divider.
- Decouple the voltage divider with a 1 µF capacitor.
- Keep the voltage divider within 1.5 inches of the MCH V_{REF} ball

Figure 42. Pull-Down Circuit

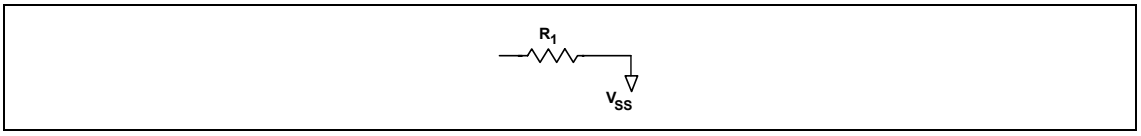


Table 18. Reference Voltage Network Values

Signal	R1	R2	Tolerance	Figure	Notes
HDVREF[3:0]	100 Ω	50 Ω	±1%	Figure 41	1,2
HAVREF[1:0]	100 Ω	50 Ω	±1%	Figure 41	1,2
CCVREF	100 Ω	50 Ω	±1%	Figure 41	1,2
HRCOMP[1:0]	20.75 Ω	—	±1%	Figure 42	3
HSWNG[1:0]	150 Ω	301 Ω	±1%		4

NOTES:
1. 2/3 V_{TT} Resistor Network
2. Single voltage divider for these signals.
3. Independent of board impedance.
4. 1/3 V_{TT} Resistor Network

5.5.1. 82850 MCH System Bus I/O Decoupling Requirements

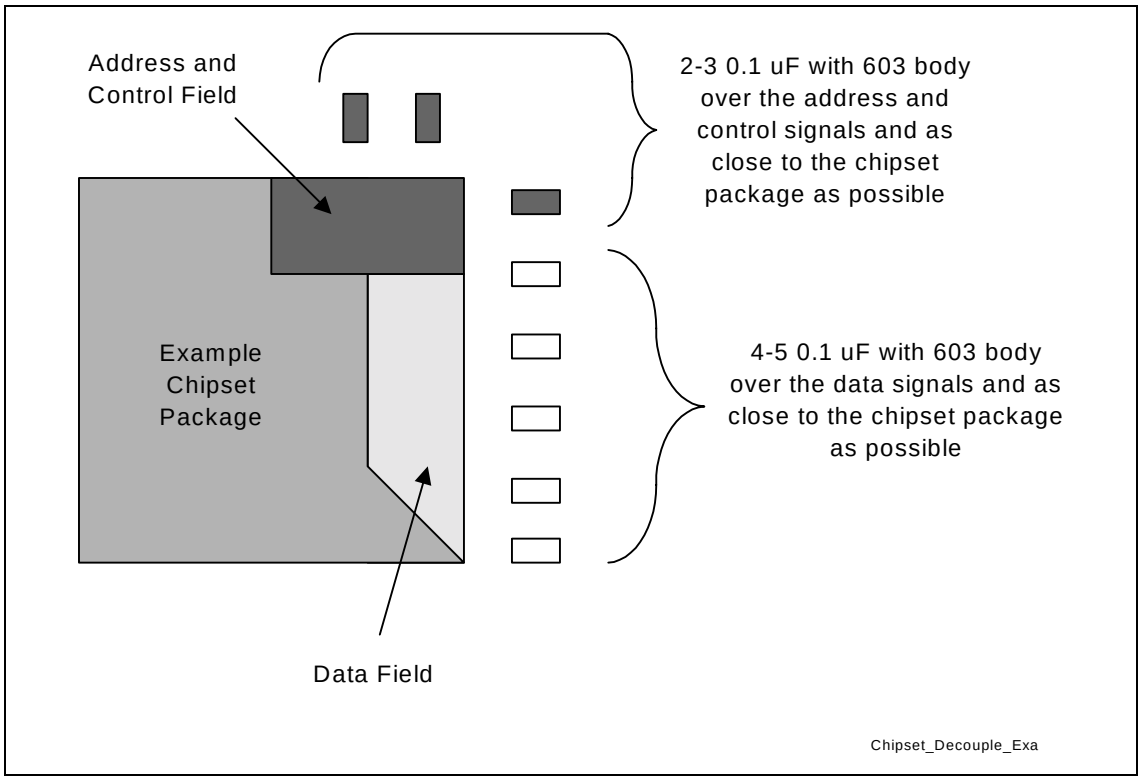
The primary objective of the decoupling requirements for the chipset is to provide clean power delivery to the System Bus I/O ring. The split plane nature of chipsets creates this power delivery concern.

The secondary objective of decoupling at the chipset is to minimize the impact of return path discontinuities that may occur between the chipset package and the system board. A return path discontinuity occurs in systems whose signals reference either power or ground, but not both. While the chipset uses symmetric stripline interconnects that reference the signal to both V_{CC} and V_{SS}. Systems that have this type of referencing should use the larger number of decoupling capacitors listed in the below guidelines for the chipset.

The requirements for the chipset are:

- Four minimum, five preferred 0.1 µF capacitors with 603 packages distributed evenly over the System Bus data lines
- Two minimum, three preferred 0.1 µF capacitors with 603 packages distributed evenly over the System Bus address and control lines
- All capacitors placed as close as possible to the MCH package (within 150 mils)

Figure 43. Example MCH Decoupling Guidelines for Chipset



6. Memory Interface Routing

The Rambus channel is a multi-symbol interconnect. Due to the length of interconnect and frequency of operation, this bus is designed to allow multiple command and data packets to be present on a signal wire at any given instant. For example, the driving device can send the next data out before the previous data has left the bus.

The nature of the multi-symbol interconnect forces many requirements on the bus design and topology. First and foremost, a drastic reduction in reflected voltage levels is required. The interconnect transmission lines must be terminated at their characteristic impedance. Else, the reflected voltage resulting from a mismatch in impedance will degrade signal quality. These reflections reduce noise, timing margins and the maximum operating frequency of the bus. Second, coupled noise can greatly affect the performance of high-speed interfaces. Just as in source synchronous designs, odd and even mode propagation velocity change can create skew between the clock and data or command lines which reduces the maximum operating frequency of the bus. Efforts must be made to significantly decrease crosstalk, as well as the other sources of skew.

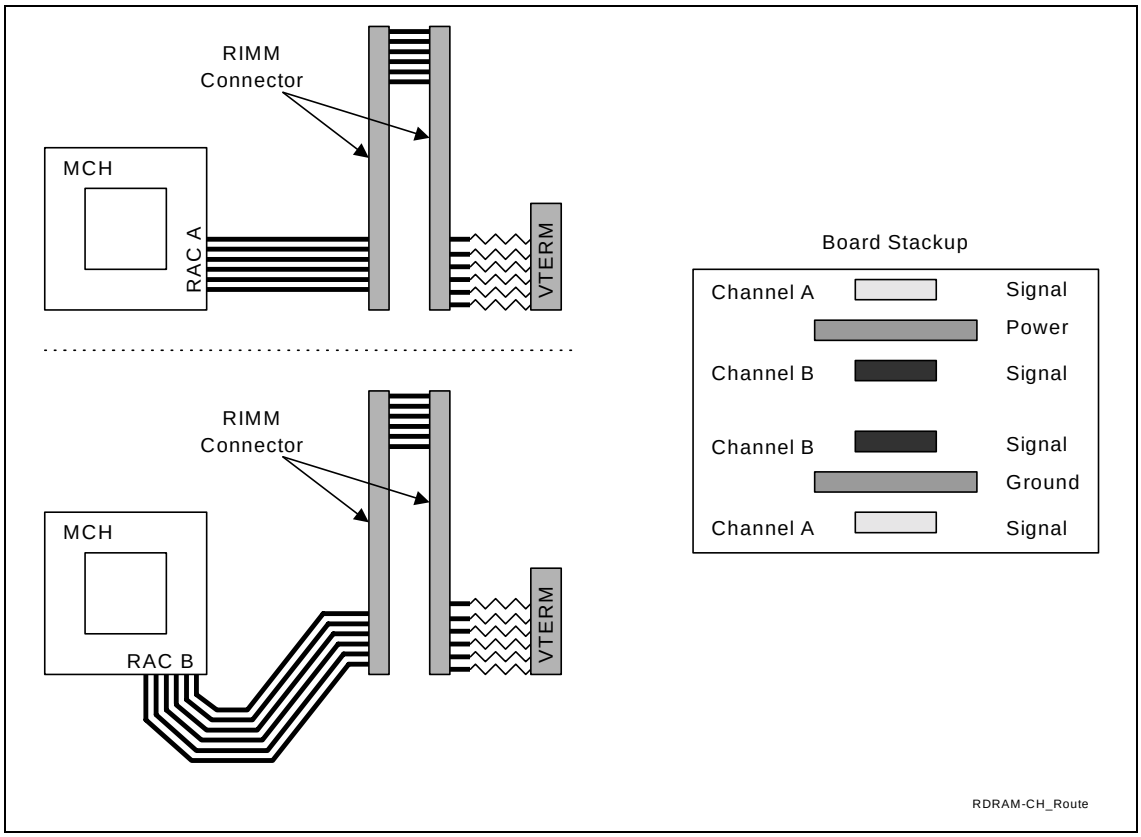
To achieve these bus requirements, the Rambus channel is designed to operate as a transmission line; all components, including the individual RDRAM devices, are incorporated into the design to create a uniform bus structure that can support up to 33 devices (including the MCH) running at 800 MegaTransfers/second (MT/s). The following sections will document the design guidelines to help ensure a robust Rambus* channel design.

Refer http://www.rambus.com for more information regarding Direct RDRAM device technology.

6.1. Direct RDRAM* Device Routing Guidelines

The Intel 850 MCH has two Rambus channels. The layout guidelines presented below are applicable for each channel. Because of routing and timing margin, one channel should be routed entirely microstrip (outer layers) or stripline (inner layers). The following figure illustrates an example routing topology for the 82850 MCH.

Figure 44. MCH Rambus* Channel Routing Example



The signals on the Rambus channel are broken into three groups: Rambus* Signaling Level (RSL) signals, CMOS signals and clocking signals. The signal groups are documented in the following table.

Table 19. Direct Rambus* Channel Signal Groups

Group	Signal
RSL Signals	DQA[8:0]
	DQB[8:0]
	RQ[7:0]
CMOS Signals	CMD(1)
	SCK(1)
	SIO
Clocking Signals	CTM
	CTM#
	CFM
	CFM#

NOTES:
1. These are high-speed CMOS signals.

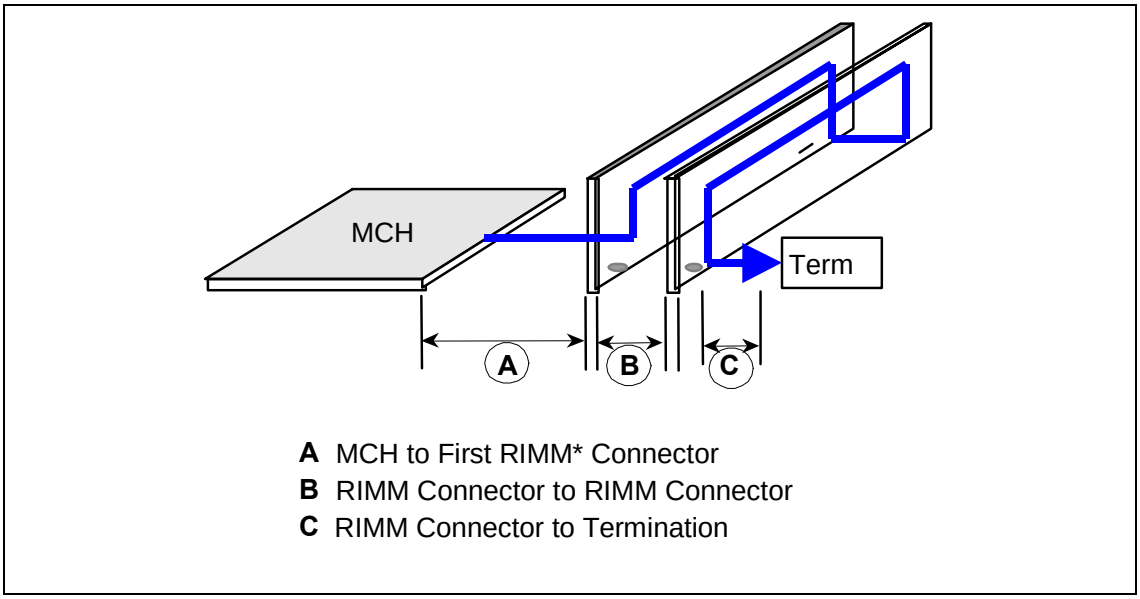
6.1.1. Rambus* Signaling Level (RSL) Signals

The Rambus channel RSL signals are high-speed signals that transmit data between the MCH and RDRAM component at speeds up 400 MHz. These signals start at the MCH, enter the first RIMM connector on either side, propagate through the RIMM connectors, and then exit on the opposite side. The RSL signals continue through the second RIMM connector until they are terminated at V_{TERM}. All unpopulated RIMM connectors must have continuity modules in place to ensure signals propagate to the termination at the end of the Rambus channel.

The perfect matching of transmission line impedance and uniform trace length are essential for the Direct RDRAM device interface to work properly. Maintaining 28 Ω ± 10% loaded impedance for every RSL signal requires some changes to the standard trace width and board prepreg thickness. Typically, to achieve 28 Ω nominal impedance with 7 mil prepreg, it will require 28 mil wide traces. The 28 mils wide traces are too wide to break out of the rows of RSL signals on the MCH. To reduce the trace width, a thinner prepreg is required. For example, a prepreg thickness of 4.0 to 4.5 mils allows 18 mil wide traces to meet the 28 Ω ± 10% nominal impedance requirement.

The figure and table below document the Rambus channel topology for a 28 Ω channel.

Figure 45. Example Rambus* Channel Routing



Note: This diagram only illustrates the routing of one Rambus channel. However, the example routing shown can be applied to both channels.

Table 20. Preliminary Rambus* Direct RDRAM* RSL Signal Lengths for Rambus* RIMM* Connectors on Motherboard

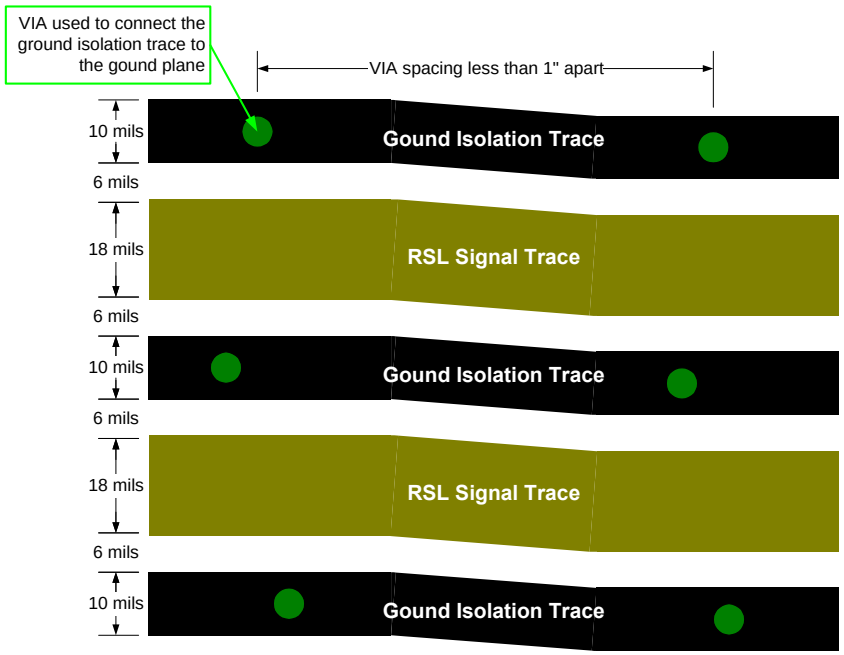
Reference Section	Trace Description	Trace Length
A	MCH to first RIMM for Channel A or first RIMM for Channel B	1 inch to 6 inches
B	RIMM connector to RIMM connector for the same channel.	0.4 inches to 1 inch
C	RIMM to Termination	0 inches to 2 inches(1)

NOTES:
1. Place termination resistors between RIMM connectors of the same channel to decrease trace length if possible.

To ensure a solid memory subsystem design, the RSL signals routing rules need to be followed. Below is a break down of the key areas to watch when design your platform.

- To control crosstalk and odd/even mode velocity deltas, there must be a 10 mil ground isolation trace between adjacent RSL signals (see Figure 46). The 10 mil ground isolation traces must be connected to ground with vias distributed less than every 1 inch. A via must be placed within less than 0.5 inches of the beginning and end of the ground isolation trace. A 6 mil gap is required between RSL signals and ground isolation trace.
- RSL signals must be length matched to ±10 mils in section “A” and ±2 mils in sections “B” using the trace length matching methods described in the next section. There is no trace length-matching requirement for traces in section “C.” If signals are routed on inner and outer layers, the trace velocity differences needs to be accounted for to minimize channel skew.
- RSL signals must have the same number of vias. It may be necessary to place additional vias (dummy vias) on certain RSL signals, even if vias are not needed, to meet the via loading (equal number of vias) requirement.

Figure 46. Rambus* Signaling Level (RSL) Routing Diagram Showing Ground Isolation Traces with Via around RSL Signals



Note: For the Intel® 850 chipset Customer Reference Board (CRB), both inner and outer layer RSL trace width is 18 mils. Inner layer RSL trace width may vary depending on the board stack-up used. RSL signals should be no wider than 18 mils to prevent neck-down in the RIMM connector pin field.

6.1.2. Rambus* Signaling Level (RSL) Channel Compensation

The RSL and clocking signals requires special compensation for any discontinuities introduced in the channel. Since the Rambus channel only allows for 125 ps of interconnect skew, it is critical to minimize skew and to match the skew on RSL and clocking signals within a given channel. The next few sections will show how to compensate for skew due to package trace differences, vias, differential clock routing and connector.

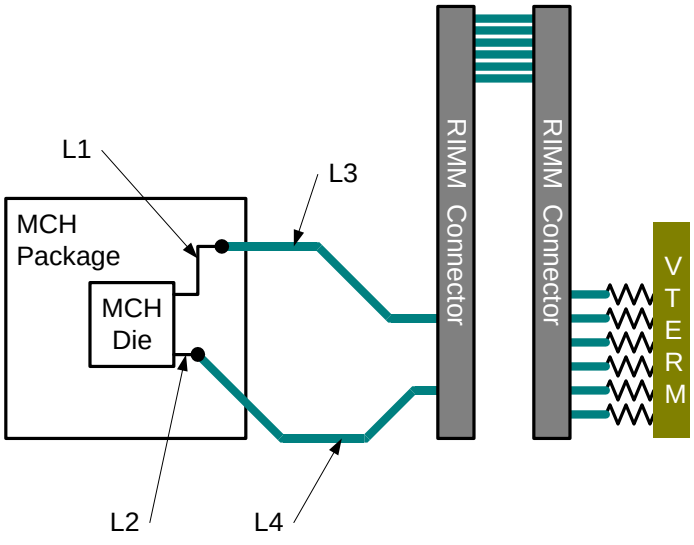
When compensating a channel, the compensating techniques must be performed in the following layout order:

1. Package trace compensation
2. Via compensation
3. Differential clock compensation
4. Alternating signal layer for RIMM connector pin compensation
5. RIMM connector impedance compensation

6.1.2.1. Package Trace Compensation (Rambus* Signaling Level and Clocking Signals)

All RSL and clocking signals require pad-to-pin length matching between the MCH to the first RIMM connector to minimize skew. All RSL and clocking signals for a given channel required pad-to-pin trace matching within ±10 mils. The RIMM connector -to- RIMM connector trace length match requirement is ±2 mils.

Figure 47. Rambus* RDRAM* Device Trace Length Matching Example



Note: This diagram only illustrates the routing of one Rambus* channel. However, the example routing shown can be applied to both channels.

Listed below are a few definitions.

- **Package Dimension (ΔL_{PKG}):** a representation of the length from the pad to the ball.
- **Board Trace Length (L_{MB}):** the trace length on the board.
- **Nominal Length:** the length to which all signals are matched.

As the Figure 47 shows, L1 plus L3 must be length matched to L2 plus L4 within ±10 mils.

Equation 2. Compensated Trace Length Calculation

$$\Delta L_{PCB} = (\Delta L_{PKG} * \text{Package}_{\text{TRACE VELOCITY}}) / PCB_{\text{TRACE VELOCITY}}$$

The PCB trace length for each signal is a calculated value, and may vary with designs. The nominal MCH package trace velocity is 167.64 ps/in. The $PCB_{\text{TRACE VELOCITY}}$ is board and layer dependent. $PCB_{\text{TRACE VELOCITY}}$ can change depending on which layer the board designer plans to route the RSL channel. Below is the $PCB_{\text{TRACE VELOCITY}}$ for stripline and microstrip routing used on the 850 chipset customer reference board (CRB).

- Stripline velocity typically equals 172 ps/in
- Microstrip velocity typically equals 154 ps/in

The MCH package trace length information is contained in the *Intel® 850 Chipset: 82850 Memory Controller Hub (MCH)* datasheet. The package trace length information presented in this document is normalized to the longest package trace length. The RSL and clocking signal lengths (ΔL_{PKG}) can be renormalized to any signal using Equation 3.

Equation 3. Normalized Trace Length Calculation

$$\text{New } \Delta L_{PKG} = \Delta L_{PKG} - \Delta L_{\text{NORMALIZED RSL}}$$

It is not necessary to account for CMOS signals package compensation. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be kept as minimum as possible.

6.1.2.2. Via Compensation

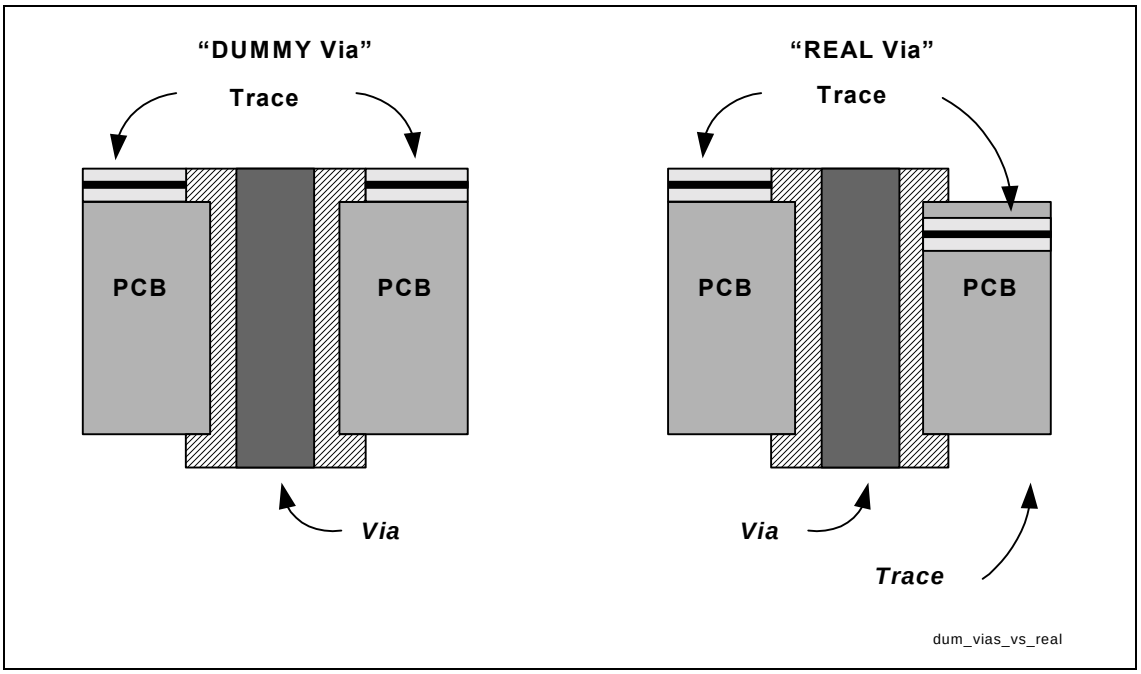
All RSL and clocking signals must have the same number of vias. As a result, each trace will have at least one via because some of the RSL signals must be routed on other layers of the motherboard. The via should be placed as close as possible to the MCH package ball. For the channel routed on outer layers (microstrip), it will be necessary to place “dummy” via on all signals routed on the top layer. The electrical characteristics between “dummy” and “real” vias are not exact, so additional compensation is needed on each signal that has “dummy” via.

“Dummy” vias are not required on the channel routed on the inner layers (stripline) because all signals will require a “real” via.

Each signal with a dummy via must have 25 mils of additional trace length. The additional 25 mils trace length must be added to the signal routed on the top layer, after length matching. Therefore:

“Real” via = “Dummy” via + 25 mils of trace length

Figure 48. "Dummy" vs. "Real" Vias



6.1.2.3. Differential Clock Compensation

If the RDRAM device clocks (CTM, CTM#, CFM and CFM#) are routed differential, the clock signals must be longer than the RSL signals due to their increased trace velocity because they are routed as a differential pair. To calculate the length for each clock, use Equation 4 for microstrip and Equation 5 for stripline routing.

Equation 4. Clock Trace Length Calculation for Microstrip

Clock Length = Nominal RSL Signal Length (package + board)* 1.030

Note: This compensation factor is based on the 850 chipset customer reference board (CRB) stack-up.

Equation 5. Clock Trace Length Calculation for Stripline

Clock Length = Nominal RSL Signal Length (package + board)* 1.009

Note: This compensation factor is based on the 850 chipset customer reference board (CRB) stack-up.

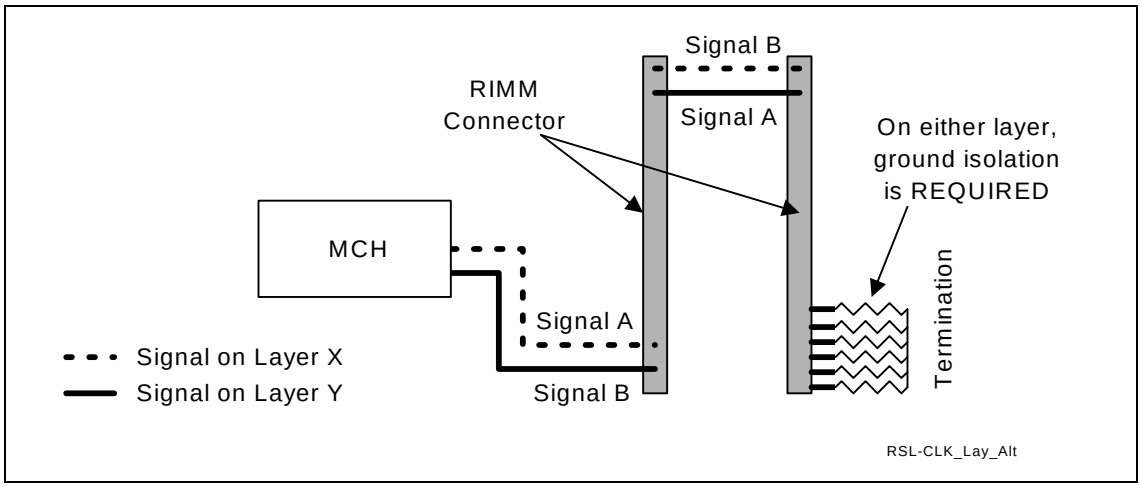
The lengthening of the clock signals, to compensate for their trace velocity change, only applies to routing between the MCH and first RIMM connector. The clock signals should be matched in length to the RSL signals between RIMM connectors.

6.1.2.4. Signal Layer Alternation for Rambus* RIMM* Connector Pin Compensation

RSL and clocking signals must alternate layers as they are routed through the channel to compensate for signals on bottom layer having to travel a longer distance through the pin connector. This is illustrated in the following figure. For example if a signal is routed on the top layer from the MCH to the first RIMM connector, it must be routed on the bottom layer from the first RIMM connector to the second RIMM connector. This rule also holds true for inner layer routing. If a signal is routed on the top inner layer from the MCH to the first RIMM connector, it must be routed on the bottom inner layer from the first RIMM connector to the second RIMM connector.

All RSL and clocking signals from the second RIMM connector to the termination resistor should be routed on the top layer.

Figure 49. Rambus* Signaling Level (RSL) and Clocking Signal Layer Alteration



6.1.2.5. Rambus*RIMM* Connector Impedance Compensation

The RIMM connector inductance has been shown to cause an impedance discontinuity on the Rambus channel. This can reduce voltage and timing margin. To compensate for the inductance of the connector, a compensating capacitance is required on each RSL and clocking connector pin. This compensating capacitance must be added to the following connector pins at each connector

- LCTM
- LCTM#
- RCTM
- RCTM#
- CMD
- LCFM
- LCFM#
- RCFM
- RCFM#
- SCK
- LROW[2:0]
- RROW[2:0]
- LCOL[4:0]
- RCOL[4:0]
- RDQA[8:0]
- LDQA[8:0]
- RDQB[8:0]
- LDQB[8:0]

The amount of capacitance needed depend on the length the signals have to travel though the RIMM connector pin (i.e., a signal on the bottom layer has to travel though more of the RIMM connector pin than a signal on the top layer). This can be achieved on the motherboard by adding a copper tab to the specified RSL pins at each connector.

Table 21. Rambus* Signaling Level (RSL) and Clocking Signal Rambus* RIMM* Connector Capacitance Requirement

RSL and Clocking Signal Routing Layer	Capacitance (pF)(1)
Top	0.8
Inner 1	0.9
Inner 2	1.23
Bottom	1.35

NOTES:
1. These numbers are based on a six layer stack-up.

The copper tab area for the recommended stack-up was determined through simulation. The amount of capacitance required is determined by the layer the RSL or clocking signal is routed on. The placement of the copper tabs can be on any signal layer, independent of the layer on which the RSL signal is routed.

Capacitance for a different stack-up assuming a 62-mil board thickness can be computed by linear interpolation. The equation for determining the amount of capacitance needed on any stripline layer can be found by Equation 6.

Equation 6. Calculation for a Stripline C-tab

$$Ctab_{Layer} = .8pf + (1.35pf - .8pf)(X/62)$$

Where:

— X is the distance in mils from the top of the board to the stripline signal layer in which the RSL or clocking signals are routed on.

Equation 7 is an approximation that can be used for calculating copper tab area on the outer layer.

Equation 7. Copper Tab Capacitance Calculation

$$Length * Width = Area = [C_{plate} * Thickness\ of\ prepreg] / [\varepsilon_0 * \varepsilon_r * 1.1]$$

Where:

— C_{plate} = Capacitance of the plates
— $\varepsilon_0 = 2.25 \times 10^{-16}$ Farads/mil
— ε_r = Relative dielectric constant of prepreg material
— Thickness of prepreg = Stack-up dependent
— Length, Width = Dimensions in mils of copper plate to be added
— Factor of 1.1 accounts for fringe capacitance.

The following example calculation is for a board where ε_r is 4.2 and thickness of prepreg is 4.5. Note these numbers will vary with differences in prepreg thicknesses.

Table 22. Copper Tab Area Calculation

Layer	Dielectric Thickness	Separation Between Signal Traces & Copper Tab	Minimum Ground Flood	Air Gap between Signal & GND Flood	Compensating Capacitance in Cplate (pF)(1)	CTAB Area in sq mils
Top	4.5	6	10	6	0.8	~3460
Inner 1	4.5	6	10	6	0.9	~3900
Inner 2	4.5	6	10	6	1.23	~5300
Bottom	4.5	6	10	6	1.35	~5800

NOTES:
1. These numbers are based on a six layer stack-up.

Note: More than one copper tab shape may be used as shown in the following figure. The dimensions are based on copper area over the ground plane. The actual length and width of the tabs may be different due to routing constraints (e.g., if tab must extend to center of hole or anti-pad) .The following figures show a routing example of tab compensation capacitors.

Note: The capacitor tabs must not interrupt ground floods around the RIMM connector pins, and they must be connected to avoid discontinuity in the ground plane as shown.

Figure 50. Top Layer CTAB with Rambus* Signaling Level (RSL) Signal Routed on the Same Layer (Ceff = 0.8 pF)

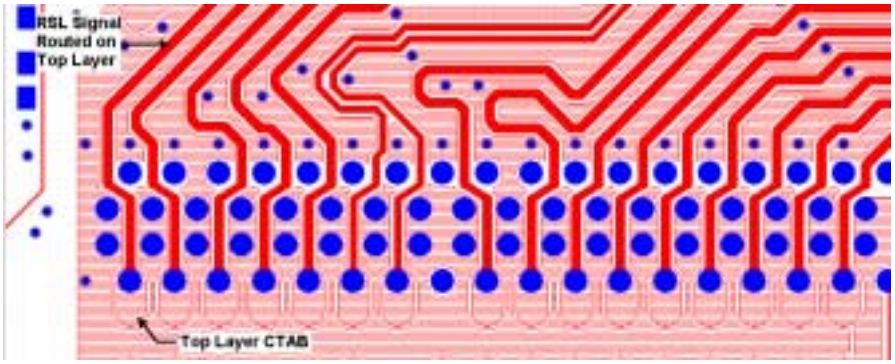
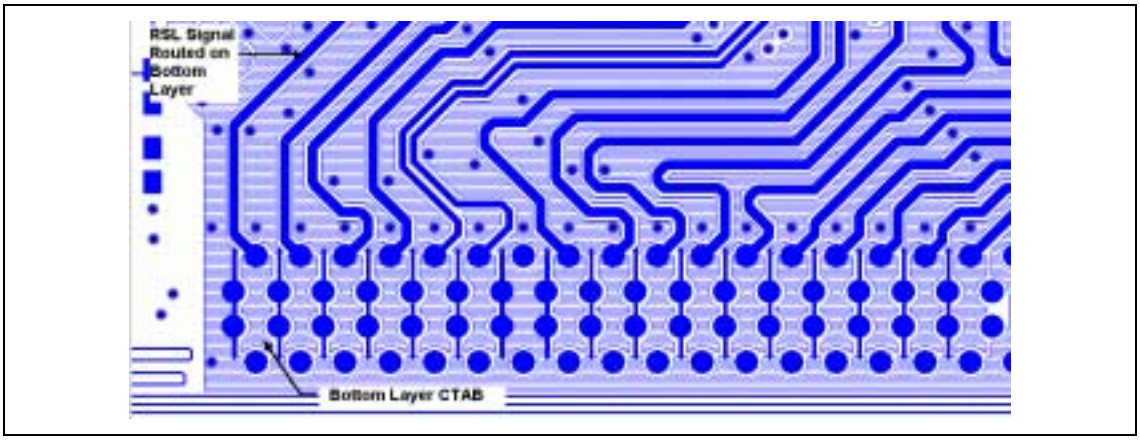
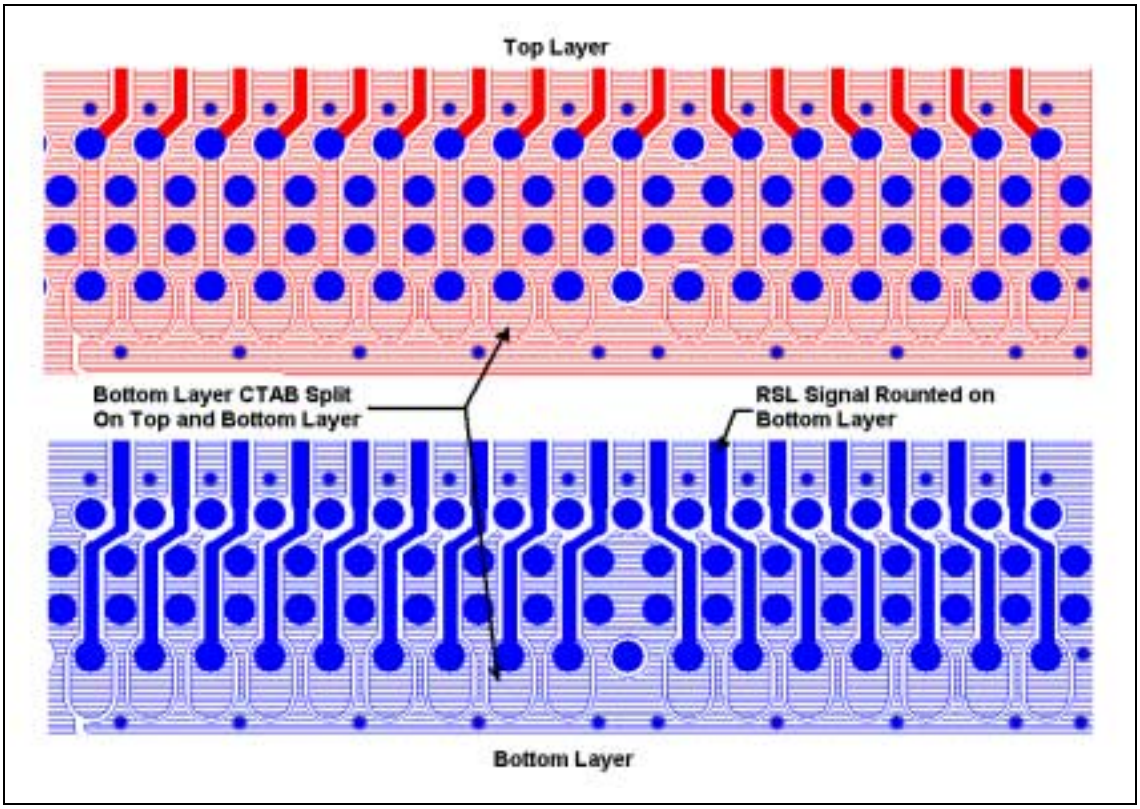


Figure 51. Bottom Layer CTAB with Rambus* Signaling Level (RSL) Signal Routed on the Same Layer (Ceff = 1.35 pF)



The CTAB can be implemented on the multiple layers to minimize routing and space constrains. The figure below issues the use of CTABs on the top and bottom layer for bottom layer RSL and clocking signals routed between RIMM connectors.

Figure 52. Bottom Layer CTABs Split Across the Top and Bottom Layer to Achieve an Effect Ceff ~1.35 pF



6.1.3. Rambus* Signaling Level (RSL) Signal Termination

All RSL signals must be terminated to 1.8 V (V_{TERM}) using 27 Ω 1% or 28 Ω 2% resistors at the end of the channel opposite the MCH. Resistor packs are acceptable, however discrete resistors are recommended for increase margin and control. The RSL and clocking signals from the last RIMM connector to termination should be routed on the top layer. V_{TERM} must be decoupled using high-speed bypass capacitors (one 0.1 µF ceramic chip capacitor per two RSL lines) near the terminating resistors. Additionally, bulk capacitance is required. Assuming a linear regulator with approximate 20 µs response time, two 100 µF tantalum capacitors are recommended. The trace length between the last RIMM connector and the termination resistors should be less than 2 inches. Length matching in this section of the channel is not required. The V_{TERM} power island should be AT LEAST 50 mils wide. This voltage is not required during Suspend-to-RAM (STR).

Figure 53. Direct RDRAM* Device Termination (Discrete Resistors Are Recommended)

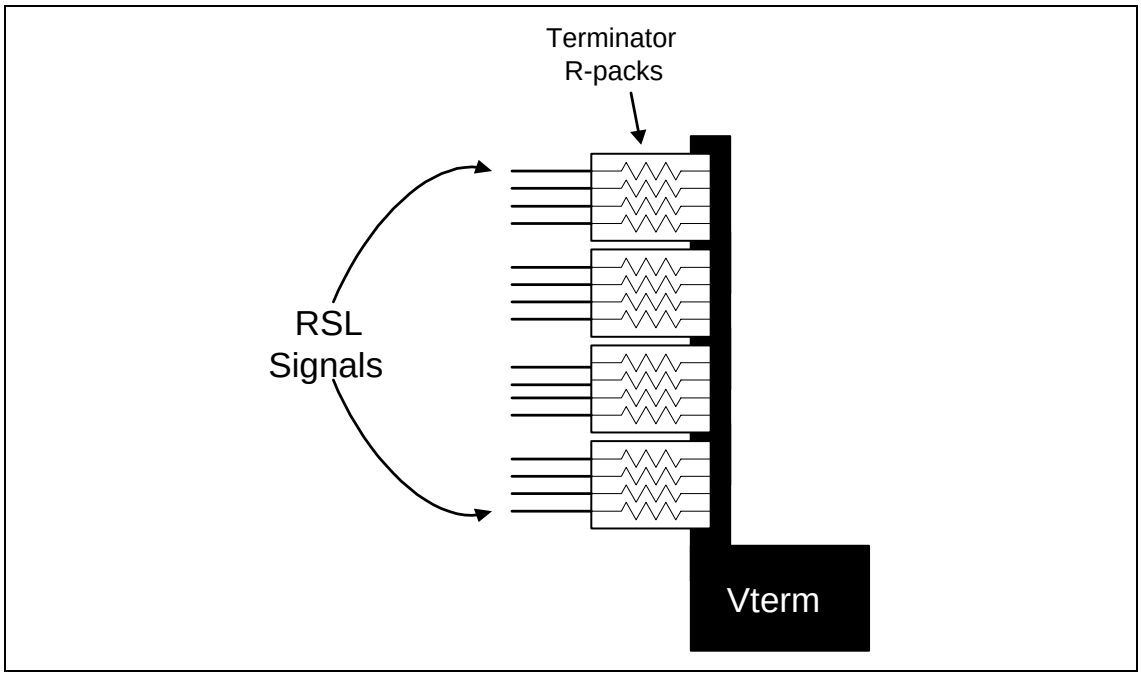
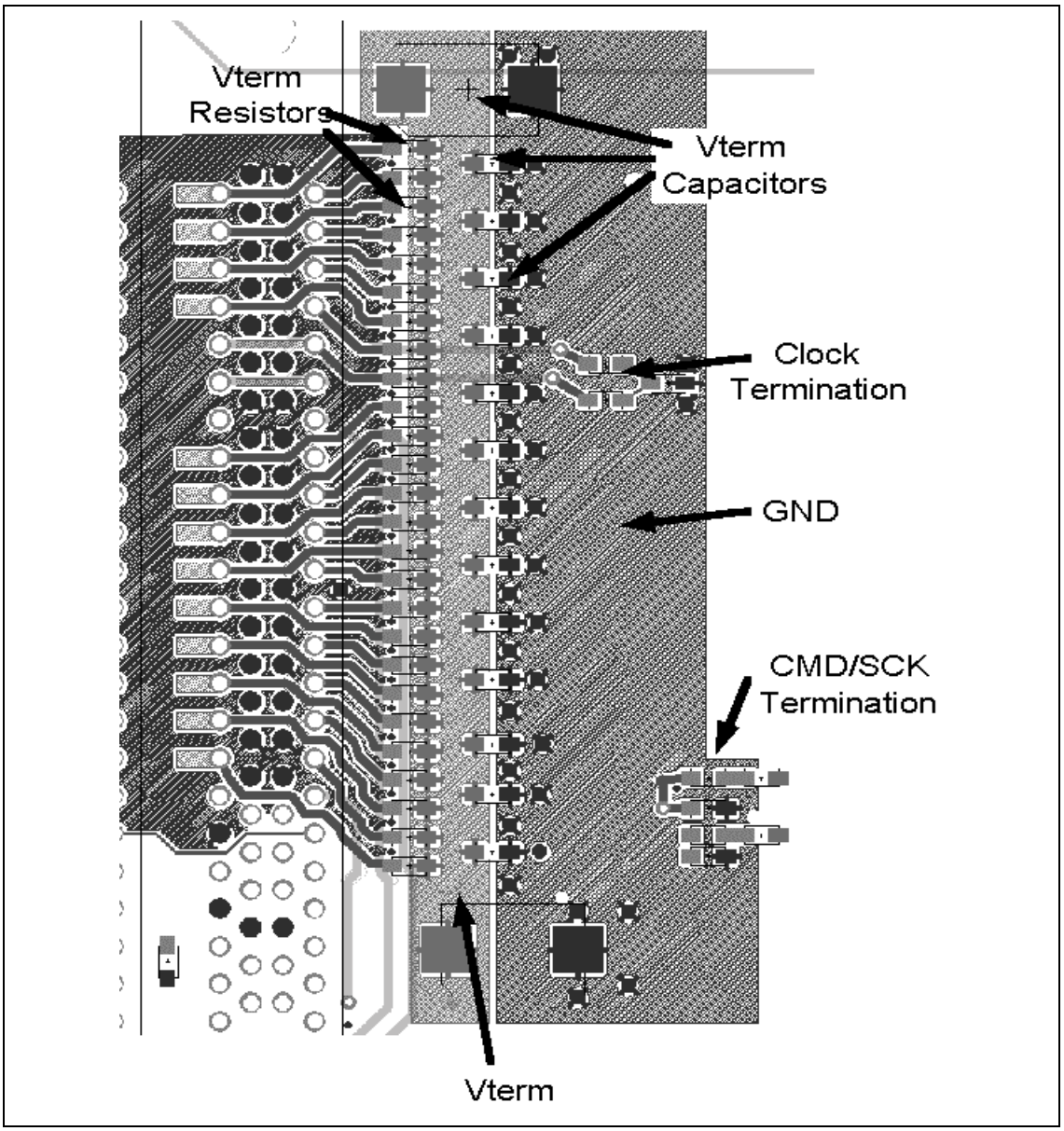


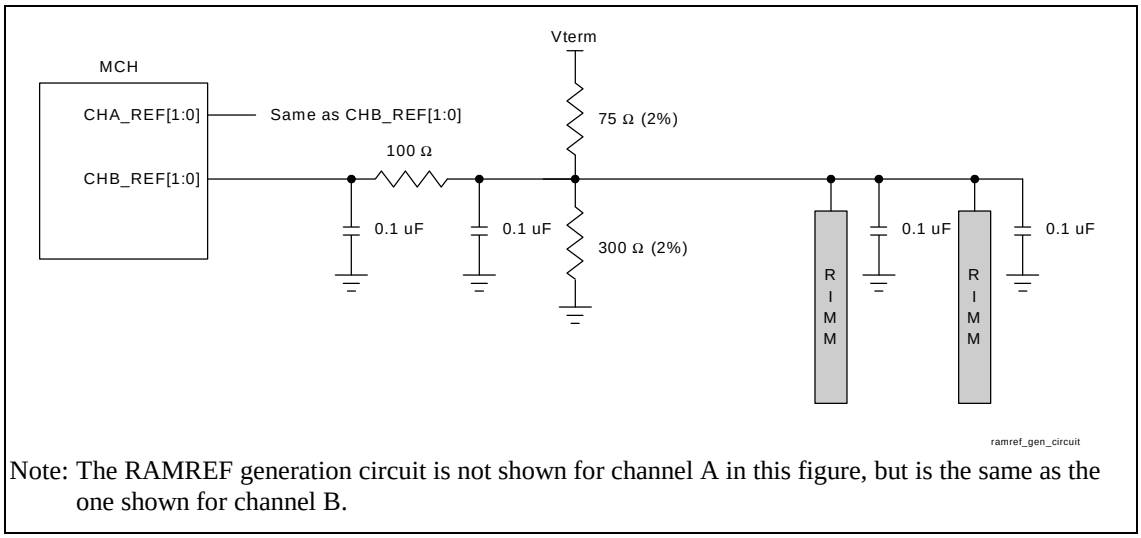
Figure 54. Direct RDRAM* Device Termination Example



6.1.4. Direct RDRAM* Device Reference Voltage

The RDRAM device reference voltage (RAMREF) must be generated as shown in the following table. RAMREF should be generated from a typical resistor divider using 2% tolerant resistors. Additionally, RAMREF must be decoupled locally at each RIMM connector, at the resistor divider network, and at the MCH. Finally, a 100 Ω series resistor is required near the MCH. The RAMREF signal should be routed with 10 mils wide traces.

Figure 55. RAMREF Generation Example Circuit

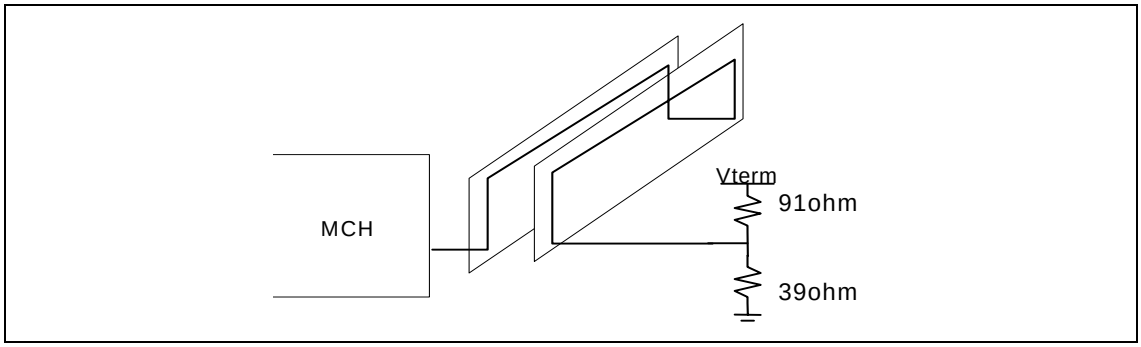


Note: The RAMREF generation circuit is not shown for channel A in this figure, but is the same as the one shown for channel B.

6.1.5. High Speed CMOS Routing

Due to the synchronous requirements between RSL signals and high-speed CMOS signals, the CMOS signals should be routed as part of the RSL channel. They must be impedance matched and properly terminated (using a different termination scheme than the RSL signals). It is not necessary to perform the length match calculation for high-speed CMOS signals. For PCB routing, the mismatch between the CMOS signals (CMD, SCK) and the RSL signals should be kept as minimal as possible.

Figure 56. High-Speed CMOS RC Termination



A CMOS voltage must be supplied to each RIMM connector. This CMOS voltage is used by the Direct RDRAM device CMOS interface. This voltage (V_{CMOS}) must be 1.8 V, and the maximum load is 3 mA. Additionally, this voltage must be supplied during *Suspend to RAM*. Therefore, V_{TERM} and V_{CMOS} cannot be generated from the same source. Due to the low power requirements of V_{CMOS}, it can be generated by a 36 / 100 Ω resistor divider from 2.5 V.

The high-speed CMOS signals require AC termination as shown in the above figure with a 91 Ω pull-up and 39 Ω pull-down resistors.

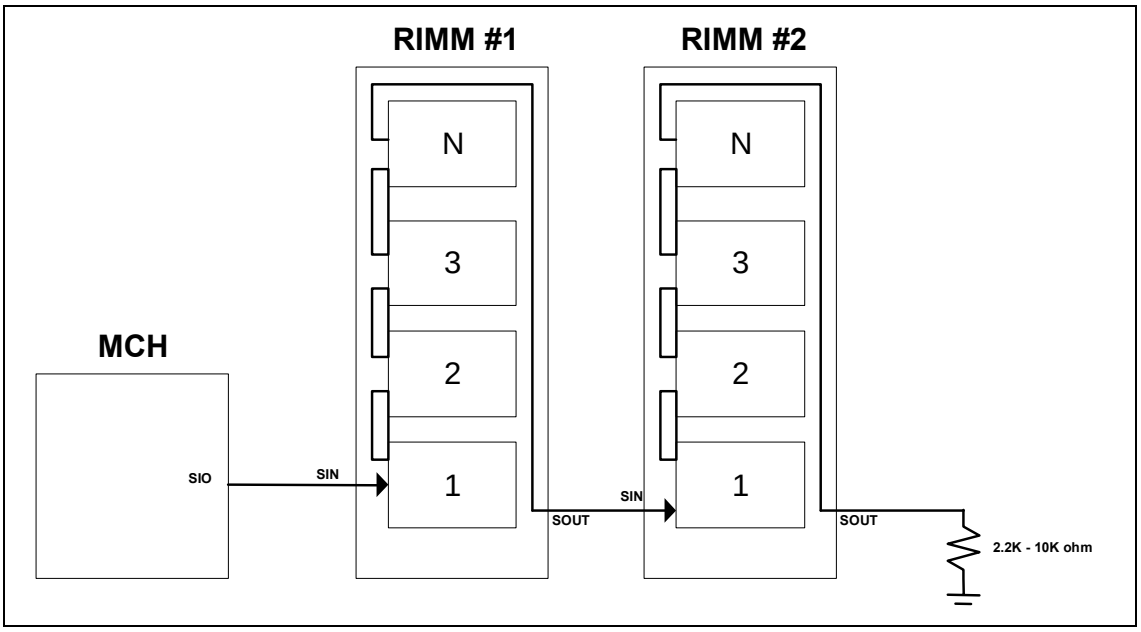
6.1.6. SIO Routing

The SIO signal is a bi-directional signal that operates at 1 MHz. This signal must be routed from MCH to RIMM connector to RIMM connectors as documented below and shown in the following figure.

- MCH SIO ball to the first RIMM connector's SIN pin (RIMM connector #1 – Pin B36)
- First RIMM connector's SOUT pin (RIMM connector #1 – Pin A36) to the second RIMM connector's SIN pin (RIMM connector #2 – Pin B36)
- Second RIMM connector's SOUT pin (RIMM connector #1 – Pin A36) to terminating resistor that is tied to GND

The SIO signal enters the first RIMM connector, propagates through all the devices (this signal is buffered by each device) on the RIMM connector and then exits the RIMM connector. A 2.2 kΩ–10 kΩ terminating resistor is required on the last RIMM connector's SOUT pin. This resistor needs to be tied to GND. The SIO is routed with a 5 mil wide, 60 Ω trace.

Figure 57. SIO Routing



6.1.7. Suspend-to-RAM Shunt Transistor

When the system enters or exits Suspend-to-RAM, power will be ramping to the MCH (i.e., it will be powering-up or powering-down). When power is ramping, the state of the MCH outputs is not guaranteed. Therefore, the MCH may drive the CMOS signals and issue CMOS commands. The only command RDRAM device would respond to is the power-down exit command. To avoid the MCH inadvertently taking the RDRAM devices out of power-down due to the CMOS interface being driven during power ramp, the SCK (CMOS clock) signal should be shunted to ground when the MCH is entering and exiting Suspend-to-RAM. This shunting can be accomplished using the NPN transistor having a sinking capability of 300 mA at 400 mV. The transistor should also have a Cobo of 15 pF or less with a signal switching range of 0.1 V–1.5 V. Lastly, shunting transistors must not be having their bases tied directly together. Please see Figure 58 for the SCK/CMD circuitry

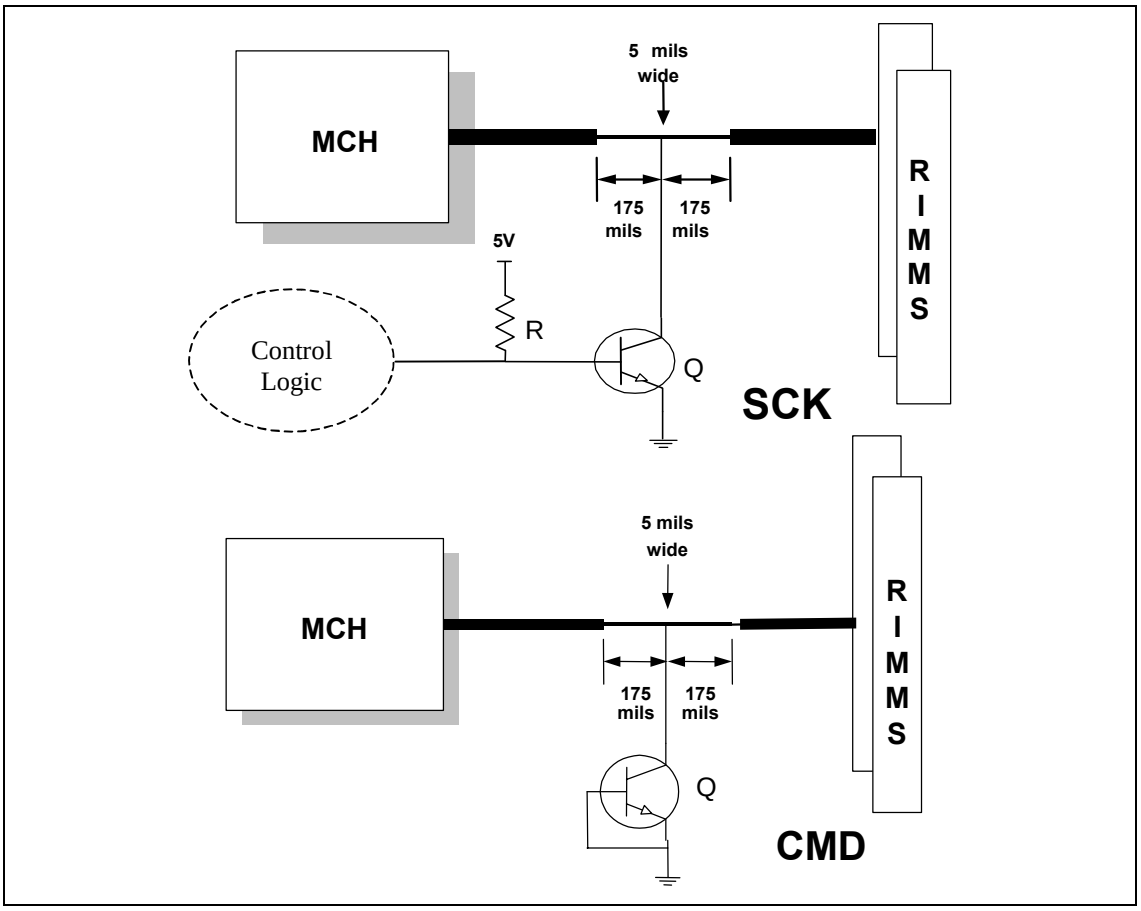
Below are sample transistors that can be utilized.

Single Package (Q)	Series Resistor (R)	Power
MMBT2222LT1D	1 kΩ	5 V
MMBT100A	300 Ω	5 V
Dual Package		
MMDT2222A	1 kΩ	5 V

Note: The use of these transistors alone does not guarantee the above conditions will be met. Each design must ensure that the transistor can sink the appropriate amount of current by properly driving the base. Resistances should include source impedance driver.

To match the electrical characteristics on the SCK signal, the CMD signal needs a dummy transistor. This transistor's base should be tied to ground (i.e., always turned off). To minimize impedance discontinuities, the traces for CMD and SCK must have a neck down from 18 mil traces to 5 mil traces for 175 mils on either side of the SCK/CMD attach point as shown below.

Figure 58. RDRAM* Device CMOS Shunt Transistor

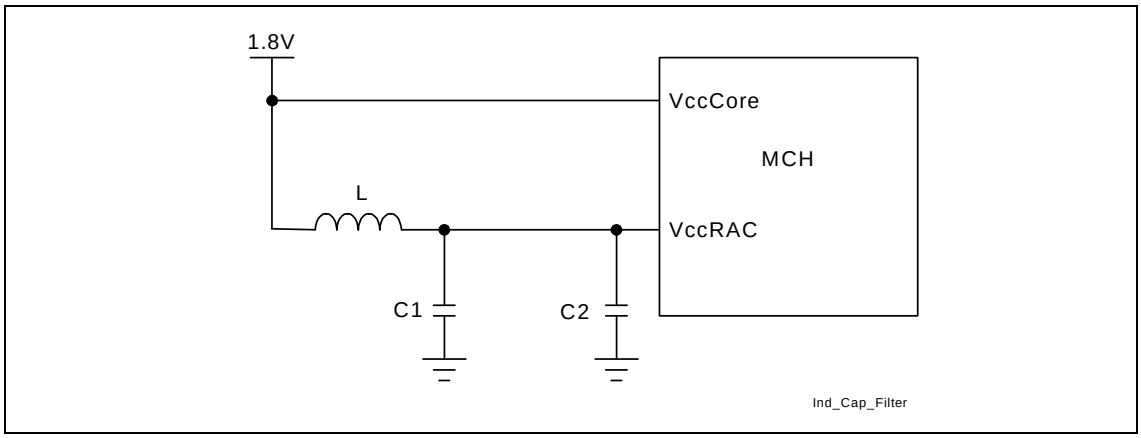


This implementation is applicable for RIMM modules down solution only and is not needed on the repeater channels. Also, this implementation is not necessary if Suspend-to-RAM is not supported within the system

6.2. 1.8 V Rambus* ASIC Cell (RAC) Isolation Solution

The 82850 MCH requires a low-pass filter on the V_{CC}RAC pins to meet clock jitter specifications. The two possible filter solutions may be configured as either an inductor-capacitor (LC) or ferrite bead-capacitor filters. For more details, see the following two figures. The inductor or ferrite bead must have a minimum current capacity of 500 mA **and** a maximum DC resistance of 100 mΩ. DC drop is a concern due to the series element between the RAC and 1.8 V supply. The V_{CC}RAC pins for the 82850 MCH are given in Table 23.

Figure 58. Inductor-Capacitor Filter Circuit

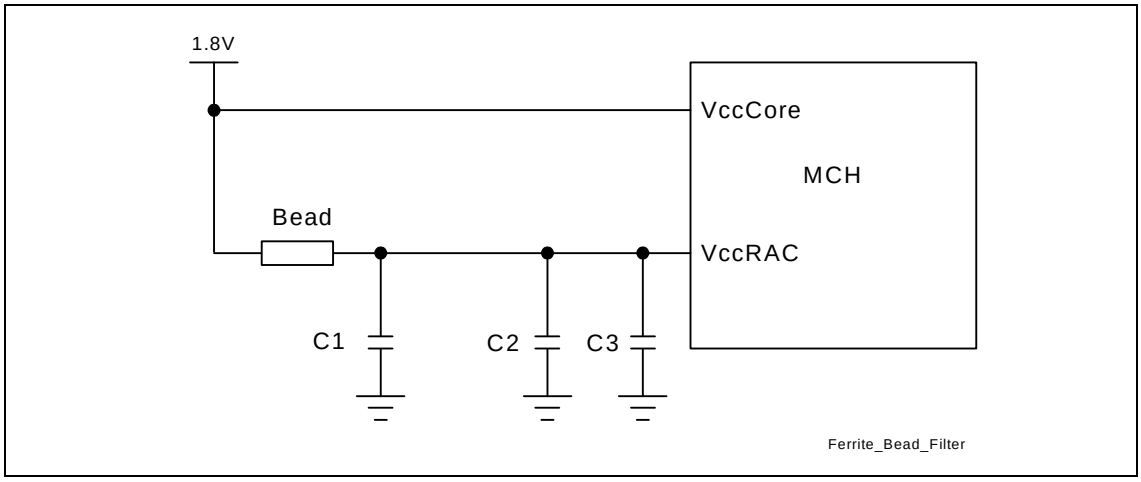


Simulations and validations indicate that L = 3.3 nH and C1 = 3.3 µF forms an adequate inductor-capacitor filter. The filter must be located within 2-inches of the device and the layout of V_{CC}RAC connections should follow high-speed design practices.

In addition to the low-pass filter, the RAC requires local decoupling capacitors. These decoupling capacitors should be located close to the RAC pins to control self-induced RAC noise. For the inductor-capacitor filter, two to three 0.1 µF capacitors (C2) for both RACs should provide adequate decoupling between V_{CC}RAC and V_{SS}.

The inductor-capacitor filter and its associated decoupling capacitors can be implemented using 0805 size components.

Figure 59. Ferrite Bead Filter Circuit



As an alternate solution, a 10 Ω (@ 100 MHz) and 10 µF form an adequate ferrite bead-capacitor filter. The filter must be located within 2-inches of the device and the layout of V_{CC}RAC connections should follow high-speed design practices.

In addition to the ferrite bead filter, the RAC requires local decoupling capacitors. These decoupling capacitors should be located close to the RAC pins to control self-induced RAC noise. For the ferrite bead filter, use a minimum number of two 0.1 µF capacitors (C2) per RAC, and a minimum of one 1.0 µF capacitor (C3) for both RACs should be sufficient. The layout of the capacitor connections should follow high-speed design practices.

The ferrite bead filter and its associated decoupling capacitors can also be implemented using 0805 components except for the 10 µF capacitor, which is a 1206 size component.

Table 23. 82850 MCH 1.8 V Rambus* ASIC Cell (RAC) Pinout

82850 MCH 1.8 V RAC Pinout Location	Channel A	Channel B
Ball	T22	C16
	N22	F15
	J22	F14
	J20	C13
	R19	E9
	P19	C9

Figure 60. Customer Reference Board Layout Example

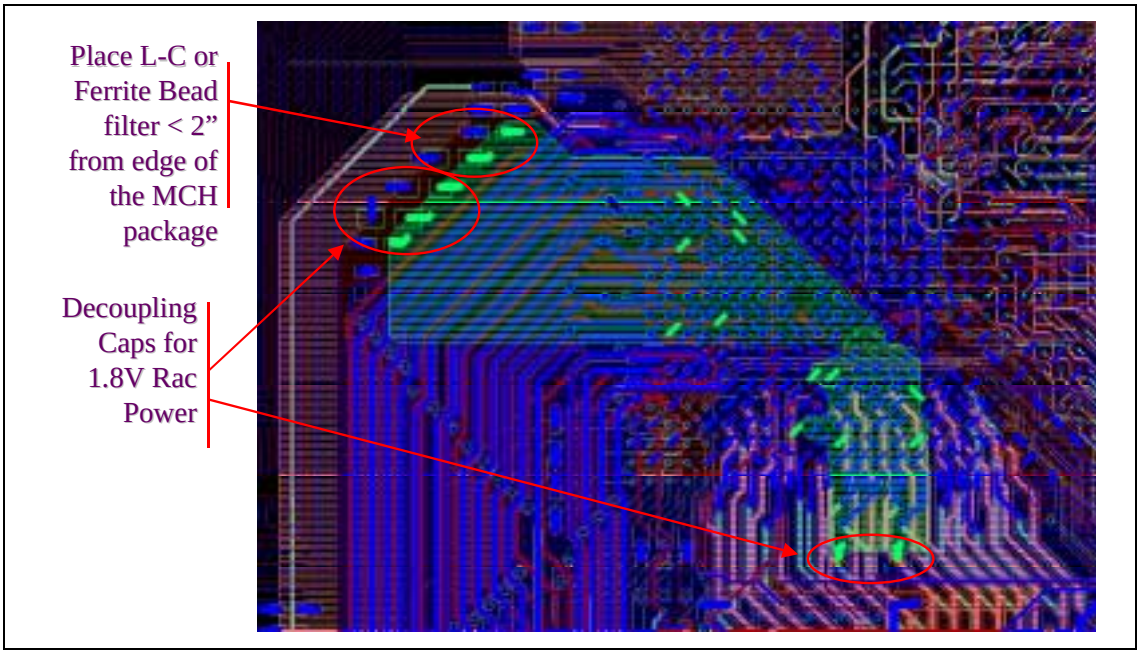


Figure 61. Customer Reference Board Layout Example (cont.) (Bottom – Layer 6)

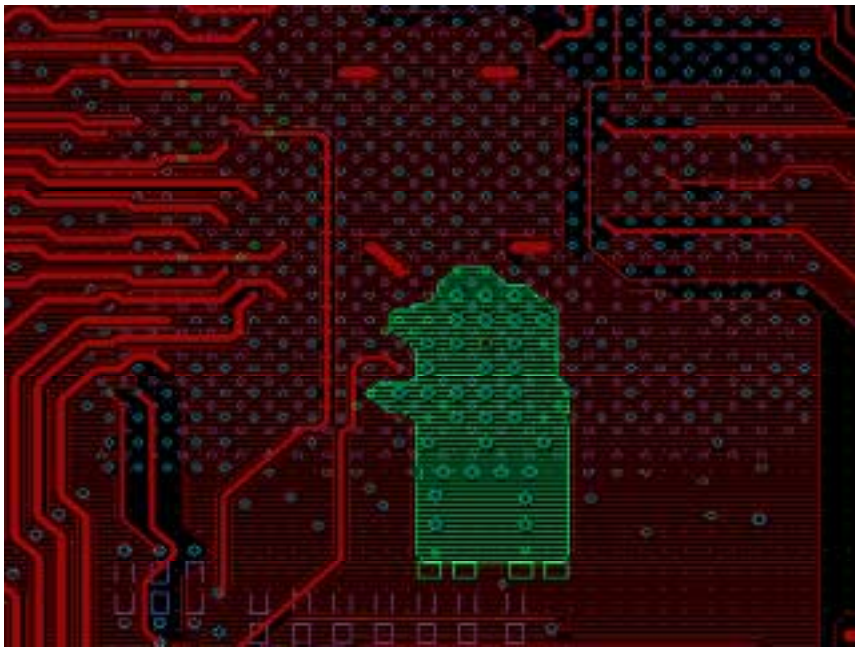


Figure 62. Customer Reference Board Layout Example (cont.) (Signal 2 – Layer 4)

7. AGP Interface Routing

For detailed AGP Interface functionality (protocols, rules and signaling mechanisms, etc.) refer to the *AGP Interface Specification, Rev. 2.0*, which can be obtained from http://www.agpforum.org. This design guide focuses only on specific 850 chipset-based platform recommendations.

The latest *AGP Interface Specification* enhances the functionality of the original *AGP Interface Specification, Rev. 1.0* by allowing 4x data transfers and 1.5 V operation. In addition to these enhancements, additional performance enhancement and clarifications, such as fast write capability, are included in the *AGP Interface Specification, Rev. 2.0*. The 850 chipset supports these enhanced features and 1.5 V signaling only.

The 4x mode of operation on the AGP interface provides for "quad-sampling" of the AGP AD (Address/Data) and SBA (Side-band Addressing) buses. This means data is sampled four times during each 66 MHz AGP clock cycle or each data cycle is ¼ of 15 ns or 3.75 ns. Note that 3.75 ns is the data cycle time, not the clock cycle time. During 2x mode, data is sampled twice during a 66 MHz clock cycle; therefore, the data cycle time is 7.5ns. These high-speed data transfers are accomplished using source synchronous data strobing for 2x mode and differential source synchronous data strobing for 4x mode.

With data cycle times as small as 3.75 ns and setup/hold times of 1 ns, it is important to minimize noise and propagation delay mismatch. Noise on the data lines will cause the settling time to be large. If the mismatch between a data line and the associated strobe is too great or there is noise on the interface, incorrect data will be sampled.

The AGP signals are broken into three groups: 1x timing domain and 2x/4x timing domain signals. In addition, the 2x/4x timing domain signals are divided into three sets of signals (#1–#3). All signals must meet the minimum and maximum trace length, width and spacing requirements. The trace length matching requirements are only applicable between the 2x/4x timing domain signal sets.

Table 24. AGP 2.0 Signal Groups

1x Timing Domain	2x/4x Timing Domain		Miscellaneous Signals
CLK	SET #1	AD[15:0]	USB+
RBF#		C/BE[1:0]#	USB-
WBF#		AD_STB0	OVRCNT#
ST[2:0]		AD_STB0#	PME#
PIPE#	SET #2	AD[31:16]	TYPDET#
REQ#		C/BE[3:2]#	PERR#
GNT#		AD_STB1	SERR#
PAR		AD_STB1#	INTA#
FRAME#	SET #3	SBA[7:0]	INTB#
IRDY#		SB_STB	
TRDY#		SB_STB#	
STOP#			
DEVSEL#			

Strobe signals are not used in the 1x AGP mode. In 2x AGP mode, AD[15:0] and C/BE[1:0]# are associated with AD_STB0, AD[31:16] and C/BE[3:2]# are associated with AD_STB1, and SBA[7:0] is associated with SB_STB. In 4X AGP mode, AD[15:0] and C/BE[1:0]# are associated with AD_STB0 and AD_STB0#, AD[31:16] and C/BE[3:2]# are associated with AD_STB1 and AD_STB1#, and SBA[7:0] is associated with SB_STB and SB_STB#.

7.1. AGP Routing Guidelines

The following section documents the recommended routing guidelines for 850 chipset-based designs. All aspects of the interface will be covered from signal trace length to decoupling. These trace length guidelines apply to ALL of the signals listed as 2X/4X timing domain signals. These signals should be routed using 5 mil (60 Ω) traces.

These guidelines are not intended to replace thorough system simulations and validation.

7.1.1. 1X Timing Domain Signal Routing Guidelines

1x signals should adhere to the follow routing guidelines:

- All 1X timing domain signals maximum trace length is 7.5 inches
- 1X timing domain signals can be routed with 5 mil minimum trace separation
- No trace length matching requirements for 1X timing domain signals

7.1.2. 2X/4X Timing Domain Signal Routing Guidelines

The maximum line length and mismatch requirements are dependent on the routing rules used on the motherboard. These routing rules were created to give design freedom by making tradeoffs between signal coupling (trace spacing) and line lengths. The maximum length of the AGP interface defines which set of routing guidelines must be used. Guidelines for short AGP interfaces (e.g., < 6 inches) and the long AGP interfaces (e.g., > 6 inches and < 7.25 inches) are documented separately. The maximum length allowed for the AGP interface is 7.25 inches.

7.1.2.1. Trace Lengths Less Than 6 Inches

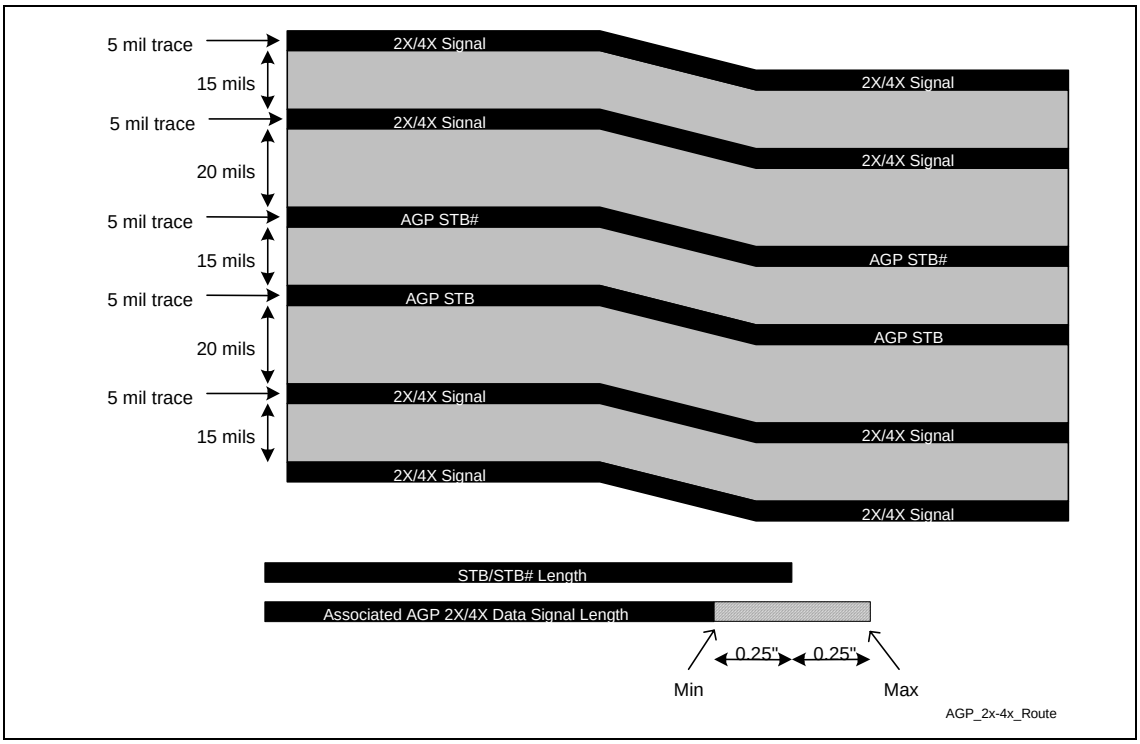
If the AGP interface is less than 6 inches with 60 Ω ±10% board impedance, at least 5 mil traces with at least 15 mils of space (1:3) between signals is required for 2X/4X lines (data and strobes). These 2X/4X signals must be matched to their associated strobe within ±0.25 inches. For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 5.3 inches long, the data signals associated to those strobe signals (e.g., AD[15:0] and C/BE#[2:0]), can be 5.05 inches to 5.55 inches long. While another strobe set (e.g., SB_STB and SB_STB#) could be 4.2 inches long and the data signals associated to those strobe signals (e.g., SBA[7:0]) can be 3.95 inches to 4.45 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore, special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 15 mils of space (1:3) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair

must be length matched to less than ±0.1 (that is, a strobe and its compliment must be the same length within 0.1 inches).

If the board impedance is 15%, the trace spacing increases to 20 mils. See the AGP interfaces trace length summary section for detailed information regarding 15% tolerance signals.

Figure 63. AGP 2X/4X Routing Example for Interfaces < 6 Inches



7.1.2.2. Trace Lengths Greater Than 6 Inches and Less Than 7.25 Inches

Longer lines have more crosstalk. Therefore, to reduce skew, longer line lengths require a greater amount of spacing between traces. For line lengths greater than 6 inches and less than 7.25 inches, 1:4 routing is required for all data lines and strobes with a 10% tolerance impedance. For these designs, the line length mismatch must be less than ±0.125 inches within each signal group (between all data signals and the strobe signals).

For example, if a set of strobe signals (e.g., AD_STB0 and AD_STB0#) are 6.5 inches long, the data signals that are associated to those strobe signals (e.g., AD[15:0] and C/BE[2:0]#) can be 6.475 inches to 6.625 inches long. Another strobe set (e.g., SB_STB and SB_STB#) could be 6.2 inches long, and the data signals that are associated to those strobe signals (e.g., SBA[7:0]) can be 6.075 inches to 6.325 inches long.

The strobe signals (AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB and SB_STB#) act as clocks on the source synchronous AGP interface; therefore special care must be taken when routing these signals. Because each strobe pair is truly a differential pair, the pair should be routed together (e.g., AD_STB0 and AD_STB0# should be routed next to each other). The two strobes in a strobe pair should be routed on 5 mil traces with at least 20 mils of space (1:4) between them. This pair should be separated from the rest of the AGP signals (and all other signals) by at least 20 mils (1:4). The strobe pair must be length matched to less than ±0.1 inches (i.e., a strobe and its compliment must be the same length within 0.1 inches).

7.1.3. AGP Interfaces Trace Length Summary

The 2X/4X timing domain signals can be routed with 5-mil spacing when breaking out of the MCH. The routing must widen to the documented requirements within 0.3 inches of the MCH package.

When matching trace length for the AGP 4X interface, all traces should be matched from the ball of the MCH to the pin on the AGP connector. It is not necessary to compensate for the length of the AGP signals on the MCH package.

Reduce line length mismatch to insure added margin. To reduce trace-to-trace coupling (crosstalk), separate the traces as much as possible. All signals in a signal group should be routed on the same layer. The trace length and trace spacing requirements must not be violated by any signal. Trace length mismatch for all signals within a signal group should be as close to zero as possible to provide timing margin.

Table 25. AGP 2.0 Routing Summary

Signal	Maximum Length	Trace Spacing (5 mil traces)	Length Mismatch	Relative To
1X Timing Domain	7.5 inches	5 mils	No requirement	N/A
2X/4X Timing Domain Set #1	7.25 inches	20 mils [3]	±0.125 inches [2]	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set #2	7.25 inches	20 mils [3]	±0.125 inches [2]	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set #3	7.25 inches	20 mils [3]	±0.125 inches [2]	SB_STB and SB_STB#
2X/4X Timing Domain Set #1	6 inches	15 mils [1,3]	±0.25 inches [2]	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set #2	6 inches	15 mils [1,3]	±0.25 inches [2]	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set #3	6 inches	15 mils [1,3]	±0.25 inches [2]	SB_STB and SB_STB#
2X/4X Timing Domain Set #1	6 inches	20 mils [1,4]	±0.25 inches [2]	AD_STB0 and AD_STB0#
2X/4X Timing Domain Set #2	6 inches	20 mils [1,4]	±0.25 inches [2]	AD_STB1 and AD_STB1#
2X/4X Timing Domain Set #3	6 inches	20 mils [1,4]	±0.25 inches [2]	SB_STB and SB_STB#

NOTES:
1. Each strobe pair must be separated from other signals by at least 20 mils.
2. Each strobe pair must be the same length.
3. These guidelines apply to board stack-ups with 10% impedance tolerance.
4. These guidelines apply to board stack-ups with 15% impedance tolerance

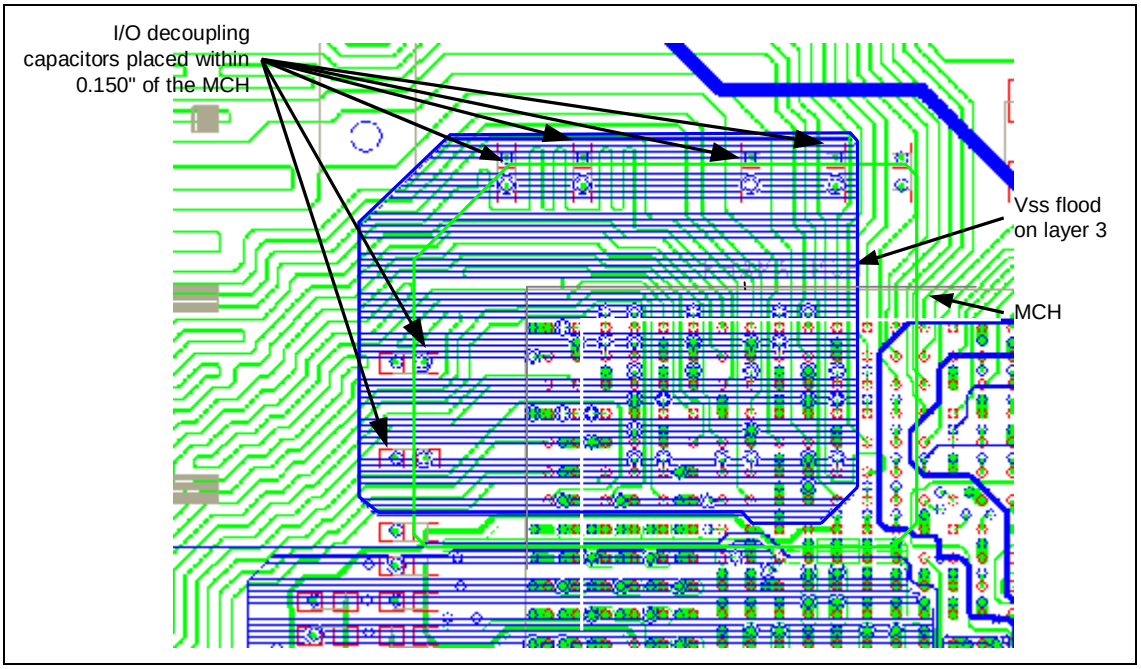
7.1.4. I/O Decoupling Guidelines

A minimum of six 0.01 µF capacitors are required for I/O decoupling. The designer should evenly distribute placement of decoupling capacitors among the AGP interface signal field and placed as close to the MCH as possible (no further than 0.15 inches from the edge of the MCH package). It is recommended that the designer use a low ESL ceramic capacitor, such as a 0603 body type, X7R dielectric.

To help lower the inductive path from the decoupling capacitor, pour a solid V_{SS} plane under the V_{DDQ} plane on layer 3 from the decoupling capacitors to the MCH.

The following figure illustrates an example AGP decoupling layout with a V_{SS} flood. This V_{SS} flood that is referenced to V_{DDQ} optimizes the mutual inductance between the two planes. The mutual inductance helps cancel out the self-inductance from the power balls on the package to the decoupling caps.

Figure 64. AGP I/O Decoupling Example with a V_{SS} Flood to Improve Power Delivery to the MCH



In addition to the minimum decoupling capacitors, the designer should place bypass capacitors at vias that transition AGP signal from one reference signal plane to another. One extra 0.01 µF capacitor is required per 10 vias. The capacitor should be placed as close to the center of the via field as possible.

The designer should ensure that the AGP connector is well decoupled as described in the revision 1.0 of the *AGP Design Guide*, Section 1.5.3.3.

7.1.5. Signal Power/Ground Referencing Recommendations

It is strongly recommended that, at a minimum, the following critical signals be referenced to ground from the MCH to an AGP connector utilizing a minimum number of vias on each net; AD_STB0, AD_STB0#, AD_STB1, AD_STB1#, SB_STB, SB_STB#, G_GTRY#, G_IRDY#, G_GNT# and ST[2:0].

In addition to the minimum signal set listed above, it is strongly recommended that half of all your AGP signals be reference to ground depending on board layout. An ideal design would have the complete AGP interface signal field referenced to ground.

The recommendations above are not specific to any particular PCB stack-up, but are applicable to all Intel chipset designs.

7.1.6. V_{DDQ} and TYPEDET#

AGP specifies two separate power planes: V_{CC} and V_{DDQ}. V_{CC} is the core power for the graphics controller and is always 3.3 V. V_{DDQ} is the interface voltage. The 850 chipset only supports an interface voltage of 1.5 V.

AGP 2.0 specification requires V_{CC} and V_{DDQ} to be tied to separate power planes and implements a TYPEDET# (type detect) signal on the AGP connector that determines the interface operating voltage (V_{DDQ}). However, a motherboard based on the 850 chipset only will only support 1.5 V add-in card. The 3 V add-in cards are not supported. Therefore, TYPEDET# detection on the motherboard is not required.

7.1.7. V_{REF} Generation

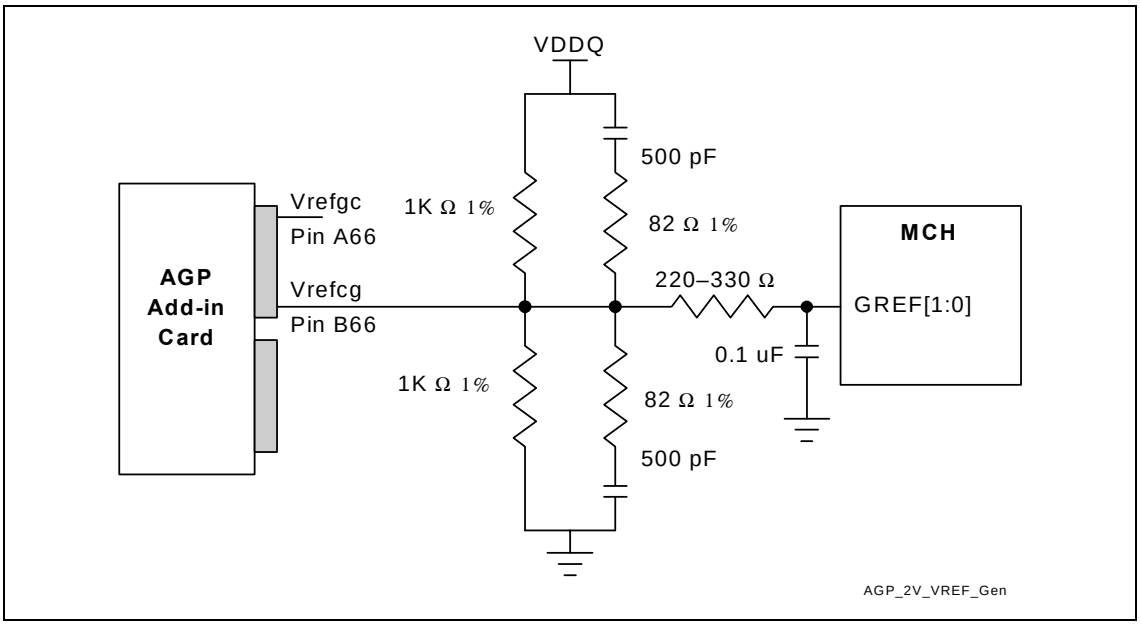
For 1.5 V add-in cards, both the graphics controller and MCH are required to generate V_{REF} and distribute it through the connector. Two signals have been defined on the 1.5 V connector to allow V_{REF} delivery:

- V_{REFGC} – V_{REF} from the graphics controller to the chipset
- V_{REFCG} – V_{REF} from the chipset to the graphics controller

However, the usage of the source generated V_{REF} at the MCH is not required per the *AGP Interface Specification, Rev 2.0*. Given this and the fact that the MCH requires the presence of V_{REF} when an AGP add-in card is present and not present, the following circuit is recommended for V_{REF} generation.

The V_{REF} divider network should be placed near the AGP interface. The minimum trace spacing around the V_{REF} signal must be 25 mils, in order to reduce cross talk and maintain signal integrity. Also, a 0.1µF bypass capacitor should be placed within 150 mils of the MCH's GREF pins. The two GREF pins on the MCH (GREF[0:1]) should be tied together before connecting to the bypass capacitor. V_{REF} voltage must be 0.5 x V_{DDQ} for 1.5 V operation.

Figure 65. AGP 2.0 V_{REF} Generation and Distribution for 1.5 V Cards



7.1.8. MCH AGP Interface Buffer Compensation

The MCH AGP interface supports resistive buffer compensation (GRCOMP[1:0]). The GRCOMP[1:0] signals must be tied to a 40 Ω ± 2% or 39 Ω ± 1% pull-down resistor to ground. This trace should be kept to 10 mils wide and less than 0.5 inches long.

7.1.9. AGP Pull-Ups/Pull-Down on AGP Signals

Some of the AGP signals may require either a pull-up resistor to V_{DDQ} (not $V_{CC3.3}$) or pull-down resistor to GND. This is to ensure stable values are maintained when agents are not actively driving the bus. The recommended AGP pull-up/pull-down resistor value is 8.2 kΩ at 10% tolerance ($4\ k\Omega \leq R_{value} \leq 16\ k\Omega$). The AGP interface does not require external termination.

The trace stub length to the pull-up/pull-down resistor should be kept to a minimal to avoid signal reflection. This trace length is different for 1x and 2x/4x modes. Below are the recommended stub lengths for 1x and 2x/4x modes.

- 1x mode, trace stub to pull-up resistor should be kept to less than 0.5 inches
- 2x/4x mode, trace stub to pull-up resistor should be kept to less than 0.1 inches

Short stub lengths help minimize signal reflections from the stub. The strobe signals require pull-up/pull-down on the motherboard to ensure stable values when there are no agents driving the bus.

Note: The G_GNT# and G_PAR signals require pull-ups to V_{DDQ}.

The MCH G_GNT# output signal will be tri-stated during RSTIN# assertion. This signal must have an external pull-up resistor to keep it from floating during the RSTIN# assertion. The recommended value is the same as the other AGP common clock signals.

The MCH G_PAR signal also needs an external pull-up resistor. This signal must have an external pull-up resistor to ensure that G_PAR remains at a valid logic level during AGP protocol transactions.

Table 26. AGP Pull-Up/Pull-Down Resistors

Signals	PU/PD Requirement
1x Timing Domain	
FRAME#	pull-up resistor to V_{DDQ}
TRDY#	pull-up resistor to V_{DDQ}
IRDY#	pull-up resistor to V_{DDQ}
DEVSEL#	pull-up resistor to V_{DDQ}
STOP#	pull-up resistor to V_{DDQ}
SERR#	pull-up resistor to V_{DDQ}
PERR#	pull-up resistor to V_{DDQ}
RBF#	pull-up resistor to V_{DDQ}
PIPE#	pull-up resistor to V_{DDQ}
REQ#	pull-up resistor to V_{DDQ}
GNT#	pull-up resistor to V_{DDQ}
WBF#	pull-up resistor to VDDQ
PAR#	pull-up resistor to V_{DDQ}
INTA#	pull-up resistor to 3.3 V
INTB#	pull-up resistor to 3.3 V
2x/4x Timing Domain	
AD_STB[1:0]	pull-up resistor to V_{DDQ}
SB_STB	pull-up resistor to V_{DDQ}
AD_STB[1:0]#	pull-down resistor to GND
SB_STB#	pull-down resistor to GND

7.1.10. AGP Signal Voltage Tolerance List

The table below documents 3.3 V tolerant signals and 5 V tolerant signals (refer to the AGP Specification for more details) on the AGP interface. All other signals, in the V_{DDQ} group, are not 3.3 V tolerant during 1.5 V AGP operation.

Table 27. 3.3 V and 5 V Tolerant Signals during 1.5 V Operation

3.3 V Tolerant Signals	5 V Tolerant Signals
PME#	USB+
INTA#	USB-
INTB#	OVRCNT#
PERR#	
SERR#	
CLK	
RST	

7.1.11. AGP Connector

Only 1.5 V add-in cards are supported. The 1.5 V uses the AGP 3 V connector and rotates it 180° on the planar. Therefore, the key of the connector moves to the opposite side of the planar away from the I/O panel and will not allow 3 V add-in cards.

The designer should ensure that the AGP connector is well decoupled as described in the revision 1.0 of the *AGP Design Guide*, Section 1.5.3.3 (i.e., use a 0.01 µF capacitor for each power pin and a bulk 10 µF tantalum capacitor on V_{DDQ} and 20 µF tantalum capacitor on V_{CC3_3} plane near the connector).

7.2. AGP Universal Retention Mechanism (RM)

Environmental testing and field reports indicate that AGP cards and AGP In Line Memory Module (AIMM) cards may come unseated during system shipping and handling without proper retention. In order to avoid disengaged AGP cards and AIMM modules, Intel recommends that AGP based platforms use the AGP retention mechanism (RM).

The AGP RM is a mounting bracket that is used to properly locate the card with respect to the chassis and to assist with card retention. The AGP RM is available in two different handle orientations; left-handed (see Figure 66) and right-handed. Most system boards accommodate the left-handed AGP RM. The manufacturing capacity of the left-handed RM currently exceeds the right-handed capacity, and as a result Intel recommends that customers design their systems to insure they can use the left-handed version of the AGP RM. The right-handed AGP RM is identical to the left-handed AGP RM, except for the position of the actuation handle. This handle is located on the same end as the primary design, but extends from the opposite side (mirrored about the center axis running parallel to the length of the part). Figure 67 contains keep out information for the left hand AGP retention mechanism. Use this information to make sure that your motherboard design leaves adequate space to install the retention mechanism.

The AGP interconnect design requires that the AGP card must be retained to the extent that the card not back out more than 0.99 mm (0.039 in) within the AGP connector. To accomplish this it is recommended that new cards implement an additional notch feature in the mechanical keying tab to allow an anchor point on the AGP card for interfacing with an AGP RM. The retention mechanism's round peg engages with the AGP or AIMM card's retention tab and prevents the card from disengaging during dynamic loading. The additional notch feature in the mechanical keying tab is required for 1.5-volt AGP cards and is recommended for the new 3.3-volt AGP cards.

Figure 66. AGP Left-Handed Retention Mechanism Drawing

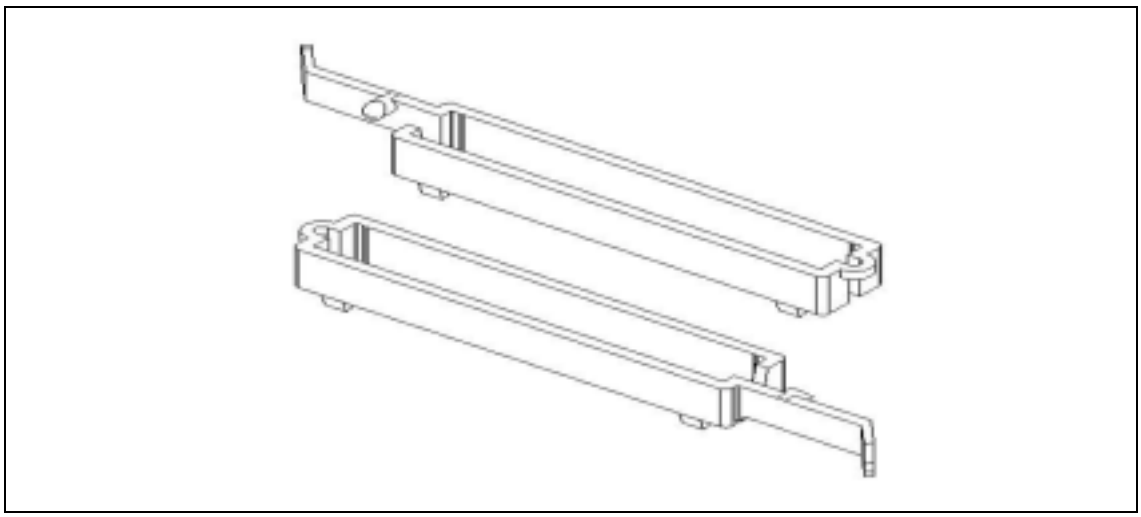
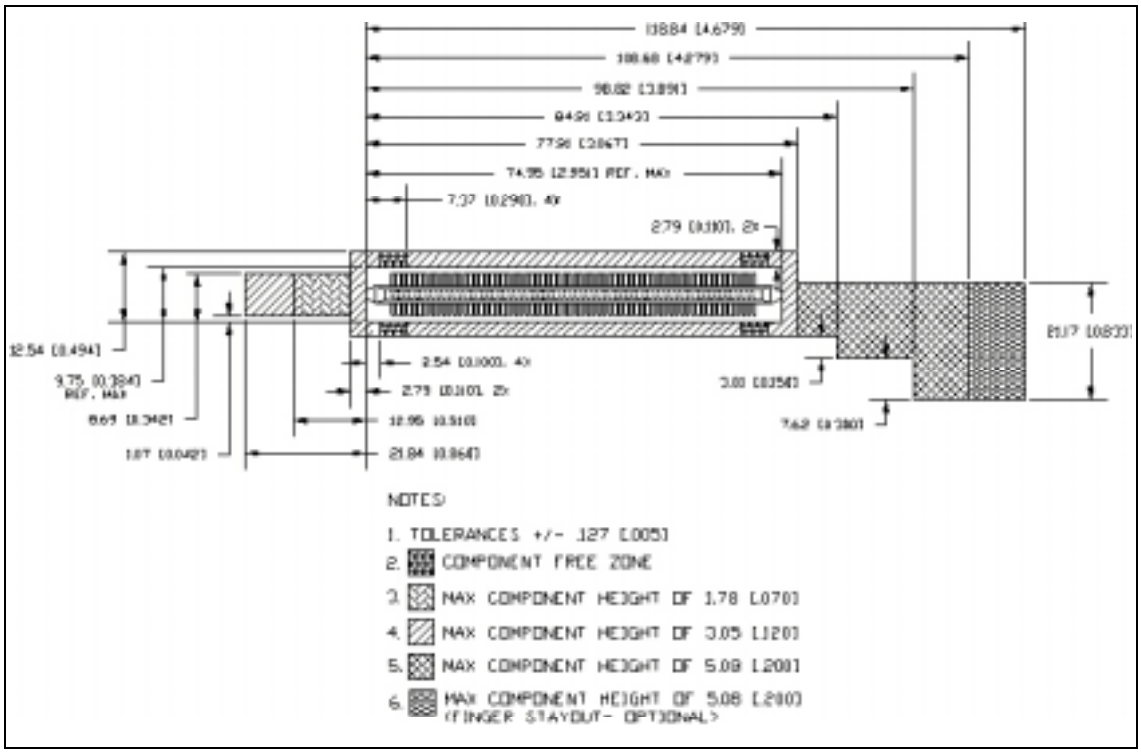


Figure 67. AGP Left-Handed Retention Mechanism Keepout Information



Engineering Change Request number 48 (ECR #48) of the AGP specification details the AGP RM, which is recommended for all AGP cards. These are approved changes to the *Accelerated Graphics Port (AGP) Interface Specification, Revision 2.0*. Intel intends to incorporate the AGP RM changes into later revisions of the AGP Interface Specification. In addition, Intel has defined a reference design of a mechanical device to utilize the features defined in ECR #48.

ECR #48 can be viewed off the Intel Web site at: http://developer.intel.com/technology/agp/ecr.htm

More information regarding this component (AGP RM) is available from the following vendors.

Table 28. List of Vendors for Retention Mechanism

Resin Color	Supplier Part Number	"Left-Handed" Orientation (Preferred)	"Right-Handed" Orientation (Alternate)
Black	AMP P/N	136427-1	136427-2
	Foxconn P/N	006-0002-939	006-0001-939
Green	Foxconn P/N	009-0004-008	009-0003-008

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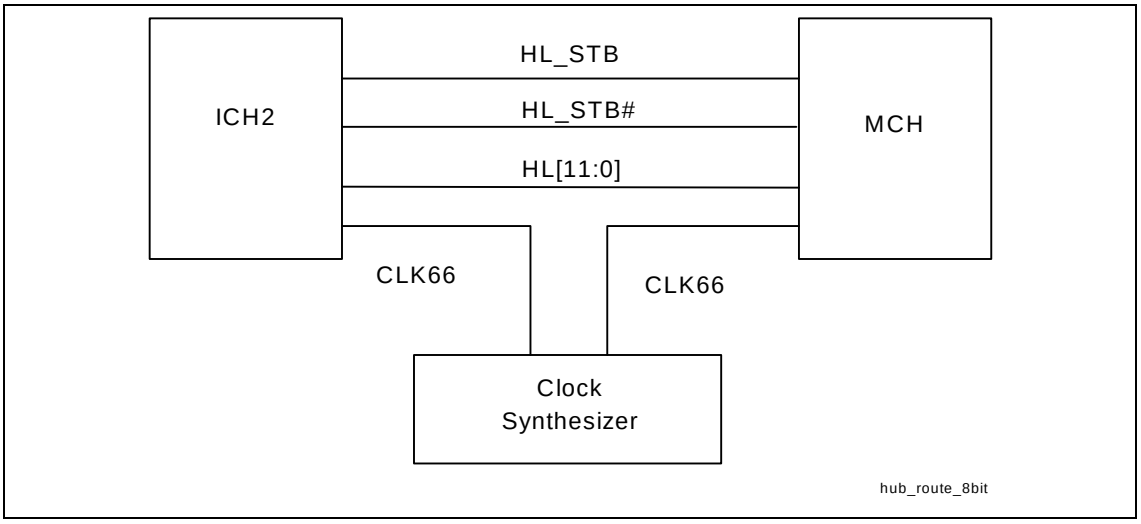
8. Hub Interface Routing

The MCH and ICH2 ballout assignments have been optimized to simplify the hub interface routing between these devices. It is recommended that the hub interface signals be routed directly from the MCH to ICH2 with all signals referenced to V_{SS}. Layer transition should be keep to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signal on the same layer.

The hub interface signals are broken into two groups: data signals (HL) and strobe signals (HL_STB). For the 8-bit hub interface, HL[0:7] are associated with HL_STB and HL_STB#.

Figure 68. 8-Bit Hub Interface Routing Example



8.1. 8-Bit Hub Interface Routing Guidelines

This section documents the routing guidelines for the 8-bit hub interface. This hub interface connects the ICH2 to the MCH. This interface supports normal buffer mode.

When the buffers are configured for normal mode, the trace impedance must equal 60 Ω ± 15%.

Table 29. 8-Bit Hub Interface Buffer Configuration Setting

Component	Hub Interface Buffer Mode	Trace Impedance	Strap
ICH2	Normal	60 Ω	HLCOMP pulled to V_{CC1_8} (1)
MCH	Normal	60 Ω	Default

Note: Reference Section 8.1.4 for the specific resistor value.

8.1.1. 8-Bit Hub Interface Data Signals

The 8-bit hub interface data signal traces should be routed 5 mils wide with 20 mils trace spacing (5 on 20). These signals can be routed 5 on 15 for navigation around components or mounting holes. In order to break out of the MCH and ICH2 package, the hub interface data signals can be routed 5 on 5. The signal must be separated to 5 on 20 within 300 mils of the package. The maximum hub interface data signal trace length in normal buffer mode is 6 inches. Each data signal must be matched within ±0.1 inches of the HL_STB differential pair. There is no explicit matching requirement between the individual data signals.

8.1.2. 8-Bit Hub Interface Strobe Signals

The hub interface strobe signals should be routed 5 mils wide with 20 mils trace spacing (5 on 20). This strobe pair should have a minimum of 20 mils spacing from any adjacent signals. The maximum length for the strobe signal in normal mode is 6 inches. Each strobe signal must be the same length, and each data signal must be matched within ±0.1 inches of the strobe signals.

8.1.3. 8-Bit Hub Interface HIREF Generation/Distribution

HIREF is the hub interface reference voltage. The HIREF voltage requirement must be set appropriately for proper operation. See the table below for the HIREF voltage specifications for normal buffer mode and the associated resistor recommendations for the voltage divider circuit.

Table 30. 8-Bit Hub Interface HUBREF Generation Circuit Specifications

Buffer Mode	HIREF Voltage Specification (V)	Recommend Resistor Values for the HIREF Divider Circuit (Ω)
Normal	1/2 V_{CC1_8} ± 2%	R1 = R2 = 150 ± 1%

The single HIREF divider should not be located more than 3.5 inches away from either MCH or ICH2. If the single HIREF divider is located more than 3.5 inches away, then the locally generated hub interface reference dividers should be used instead.

The reference voltage generated by a single HIREF divider should be bypassed to ground at each component with a 0.01 µF capacitor located close to the component HUBREF pin. If the reference voltage is generated locally, the bypass capacitor needs to be close to the component HUBREF pin.

Example HIREF divider circuits are shown below.

Figure 69. 8-Bit Hub Interface with a Shared Reference Divider Circuit (Normal Mode)

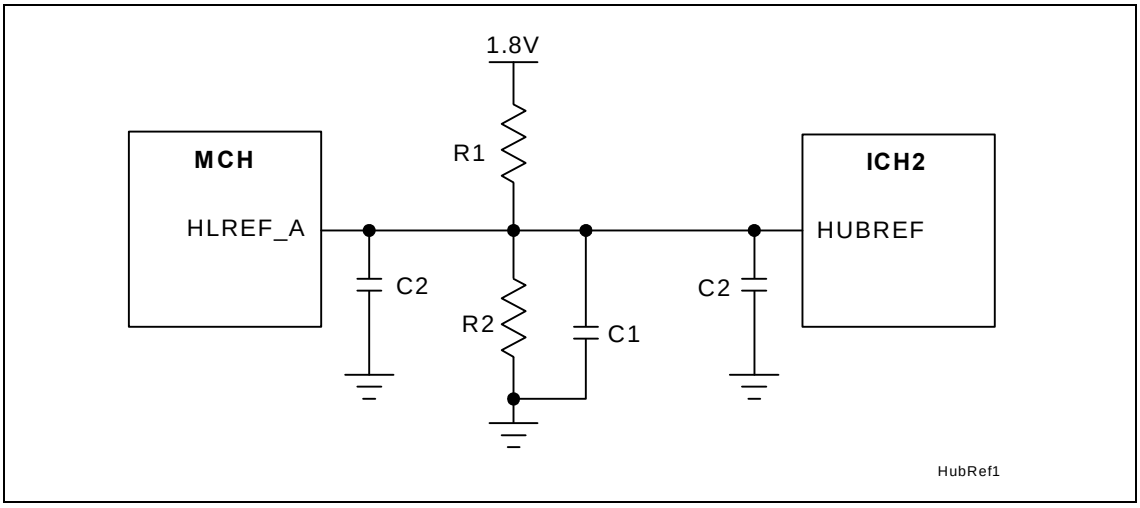
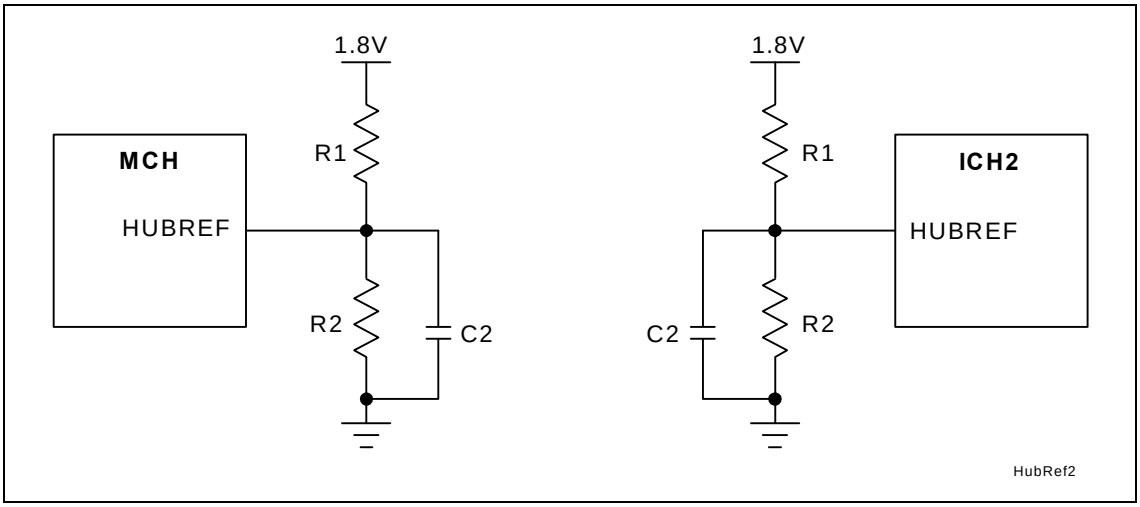


Figure 70. 8-Bit Hub Interface with Locally Generated Reference Divider Circuits



The resistor values, R1 and R2, must be rated at 1% tolerance. The selected resistor values ensure that the reference voltage tolerance is maintained over the input leakage specification. A 0.1 µF capacitor (C1 in the above circuits) should be placed close to R1 and R2. Also, a 0.01 µF bypass capacitor (C2 in the above circuits) should be placed within 0.25 inches of each HUBREF pin. The trace length from the divider circuit to the HLREF pin must be no longer than 3.5 inches.

8.1.4. 8-Bit Hub Interface Compensation

The hub interface uses a compensation signal to adjust buffer characteristics to the specific board characteristic. The hub interface requires Resistive Compensation (RCOMP).

Table 31. 8-Bit Hub Interface RCOMP Resistor Values

Component	Hub Interface Buffer Mode	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied to
ICH2	Normal	60 Ω ± 15%	40 Ω ± 2% or 39 Ω ± 1%	V_{CC1_8}
MCH	Normal	60 Ω ± 15%	40 Ω ± 2% or 39 Ω ± 1%	V_{SS}

8.1.5. 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per each component (i.e., the ICH2 and MCH). These capacitors should be placed within 150 mils from each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the V_{SS} side of the board should connect the V_{CC1_8} side of the capacitors to the V_{CC1_8} power pins. Similarly, if layout allows, metal fingers running on the V_{CC1_8} side of the board should connect the ground side of the capacitors to the V_{SS} power pins.

9. I/O Controller Hub 2 (ICH2)

9.1. IDE Interface

This section contains guidelines for connecting and routing the ICH2 IDE interface. The ICH2 has two independent IDE channels. This section provides guidelines for IDE connector cabling and system-board design, including component and resistor placement, and signal termination for both IDE channels. The ICH2 has integrated series resistors that have been typically required on the IDE data signals (PDD [15:0] and SDD [15:0]) running to the two ATA connectors. We do not anticipate requiring additional series termination, but OEMs should verify system-board signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the system board. The additional resistor layout increases flexibility by offering stuffing options at a later date.

The IDE interface can be routed with 5 mil traces on 7 mil spaces, and with a maximum trace length of 8 inches long (from ICH2 to IDE connector). Additionally, the shortest IDE signal (on a given IDE channel) must be less than 0.5 inches shorter than the longest IDE signal (on that channel).

9.1.1. IDE Cable

The IDE cabling specifications and requirements are listed below:

- **Length of cable:** Each IDE cable must be equal to or less than 18 inches.
- **Capacitance:** Less than 30 pF.
- **Placement:** A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable it should be placed at the end of the cable. If a second drive is placed on the same cable it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).
- **Grounding:** Provide a direct low impedance chassis path between the systemboard ground and hard disk drives.
- **ICH2 Placement:** The maximum trace length from the ICH2 to the ATA connector(s) is 8 inches.
- **PC ’99 requirement:** Support Cable Select for master-slave configuration is a system design requirement for Microsoft PC99. The CSEL signal of each ATA connector must be grounded at the host side.

9.1.2. Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH2 IDE Controller supports PIO, Multi-word (8237 style) DMA, and Ultra DMA modes 0 through 5. The ICH2 needs to determine the type of cable that is present, in order to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra ATA/66 and Ultra ATA/100. This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms

to the *Small Form Factor Specification SFF-8049*. This specification can be obtained from the Small Form Factor Committee.

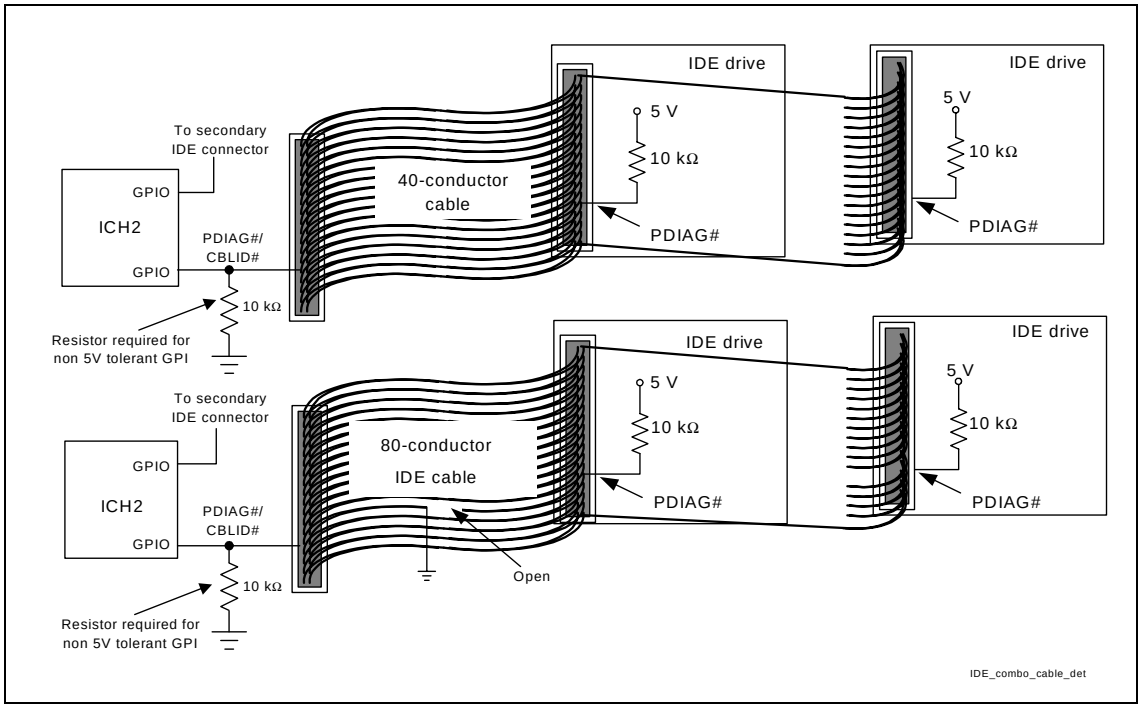
To determine if ATA/66 or ATA/100 mode can be enabled, the ICH2 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be done using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system, since this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

9.1.2.1. Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the ATA/ATAPI-4 Standard, Section 5.2.11) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in the following figure. All IDE devices have a 10K pull-up resistor to 5 V on this signal. Not all of the GPI and GPIO pins on the ICH2 are 5 V tolerant. If non 5 V tolerant inputs are used, a resistor divider is required to prevent 5 volts on the ICH2 or FWH pins. The proper value of the divider resistor is 10 kΩ.

Figure 71. Combination Host-Side/Device-Side IDE Cable Detection



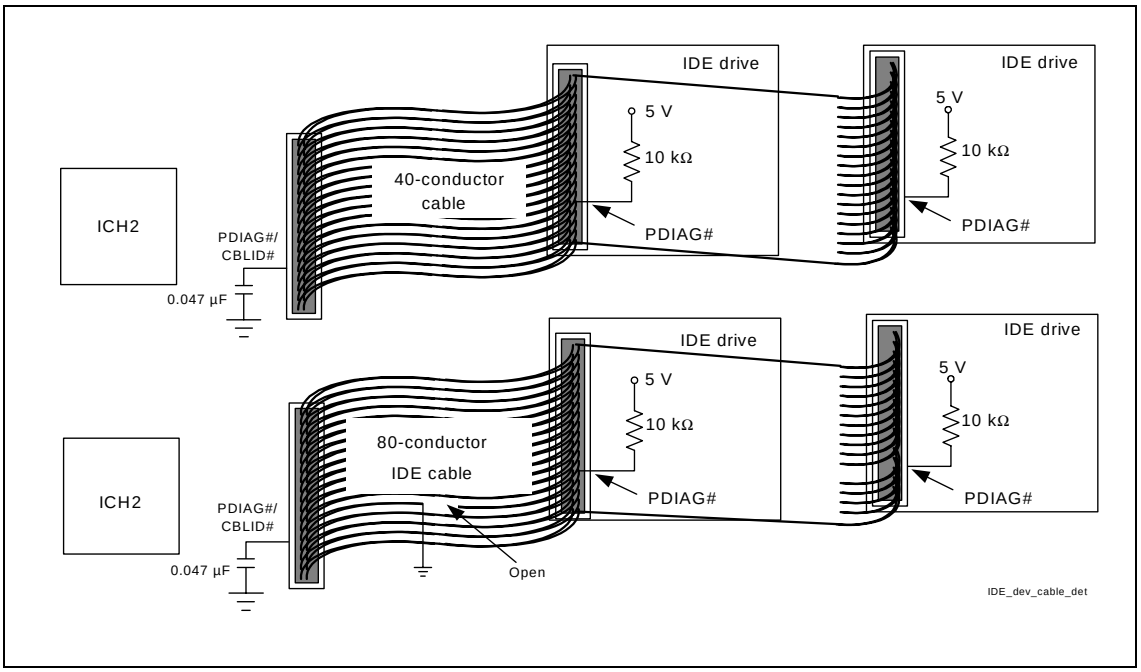
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high then there is 40-conductor cable in the system and ATA modes 3, 4 and 5 must not be enabled.

If PDIAG#/CBLID# is detected low, then there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-4 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93, bit 13 is a "1" then an 80-conductor cable is present. If this bit is "0" then a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present, and notify the user of the problem.

9.1.2.2. Device-Side Cable Detection

For platforms that must implement Device-Side detection *only* (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in the following figure. This capacitor *should not be populated* when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described above.

Figure 72. Device-Side IDE Cable Detection

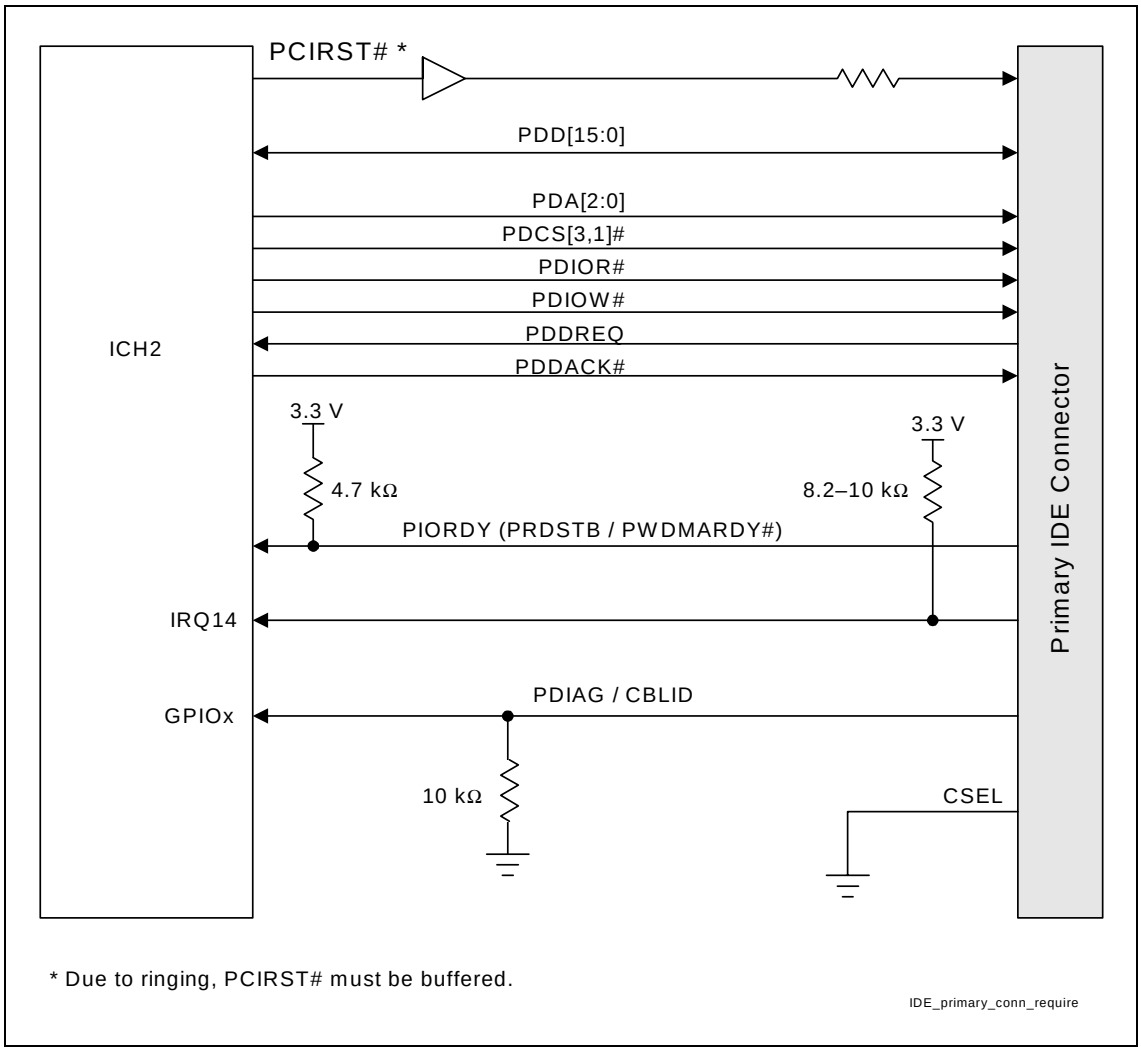


This mechanism creates a resistor-capacitor (RC) time constant. The ATA mode 3, 4, or 5 drive will drive PDIAG#/CBLID# low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host and therefore the capacitor has no effect. In a 40-conductor cable, the signal is connected to the host. Therefore the signal will rise more slowly, as the capacitor charges. The drive can detect the difference in rise times and it will report the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/66 specification.

9.1.3. Primary IDE Connector Requirements

The 10 kΩ resistor to ground on the PDIAG/CBLID signal is now required on both the Primary and Secondary Connectors. This change is to prevent the GPI pin from floating if a device is not present on either IDE interface.

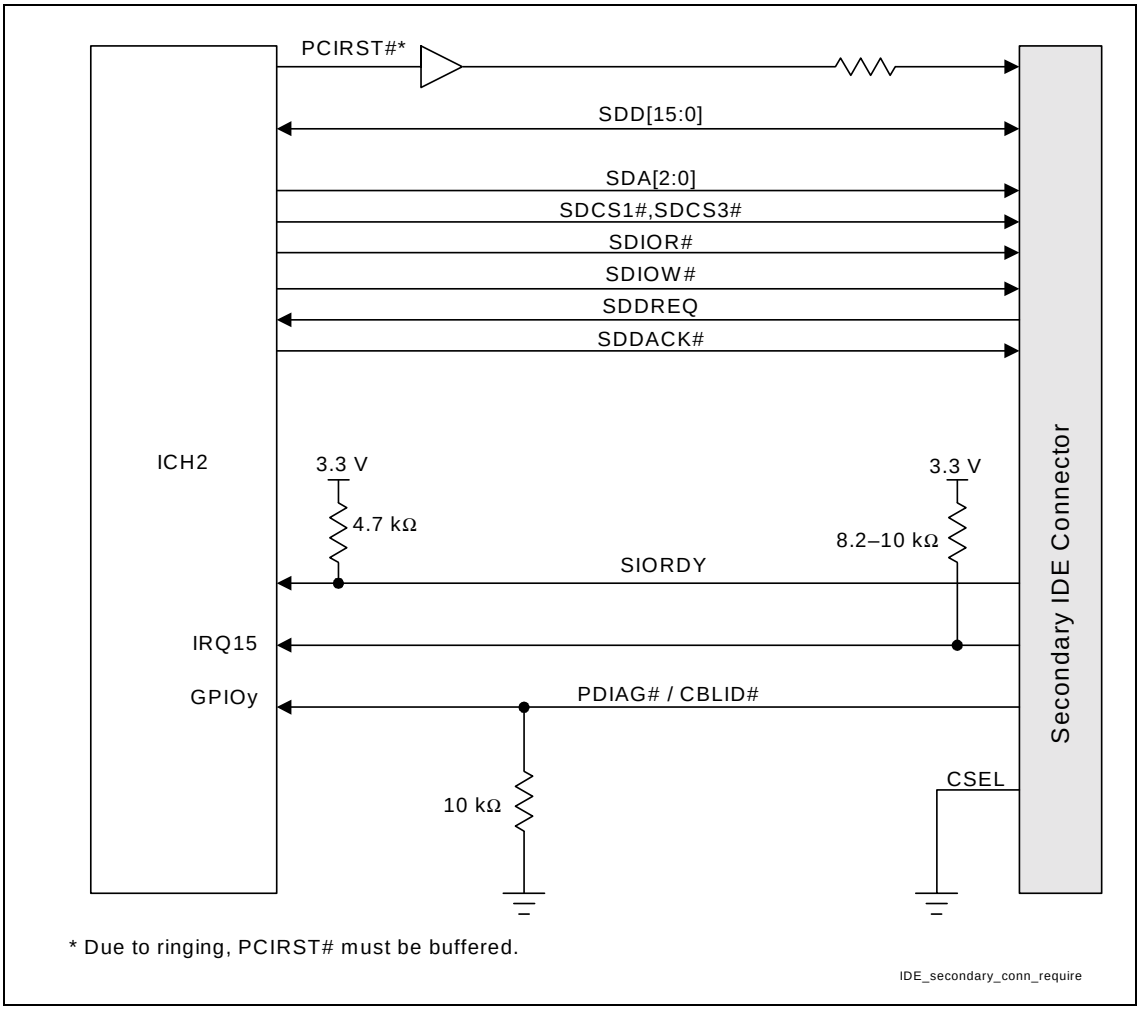
Figure 73. Connection Requirements for Primary IDE Connector



- 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to V_{CC3_3}.
- A 4.7 kΩ pull-up resistor to V_{CC3_3} is required on PIORDY and SIORDY.
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are place as close to the connector as possible. Values are determined for each unique motherboard design.

9.1.4. Secondary IDE Connector Requirements

Figure 74. Connection Requirements for Secondary IDE Connector



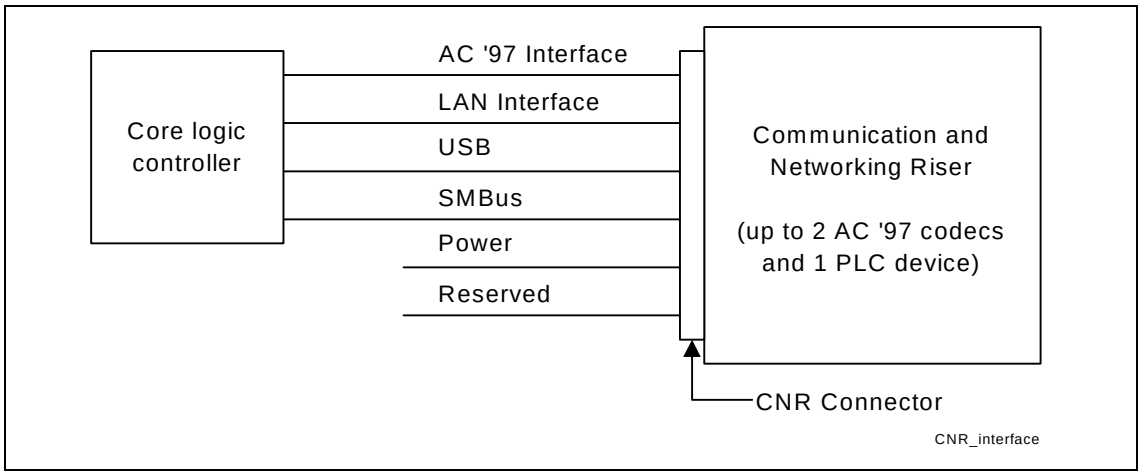
- 22 Ω – 47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design, based on signal quality.
- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and IRQ15 to V_{CC3_3}.
- A 4.7 kΩ pull-up resistor to V_{CC3_3} is required on PIORDY and SIORDY
- Series resistors can be placed on the control and data line to improve signal quality. The resistors are place as close to the connector as possible. Values are determined for each unique motherboard design.

9.2. Communication and Networking Riser (CNR)

The *Communication and Networking Riser (CNR) Specification* defines a hardware scalable Original Equipment Manufacturer (OEM) system board riser and interface. This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, and 10/100 Ethernet based networking. The CNR specification defines the interface, which should be configured prior to shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium.

The following figure indicates the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN* Connection (PLC) can either be an 82562EH or 82562ET component. It is required that the CNR A0-A2 pins be set to a unique address, so that the CNR EEPROM can be accessed. Refer to the CNR specification for additional information.

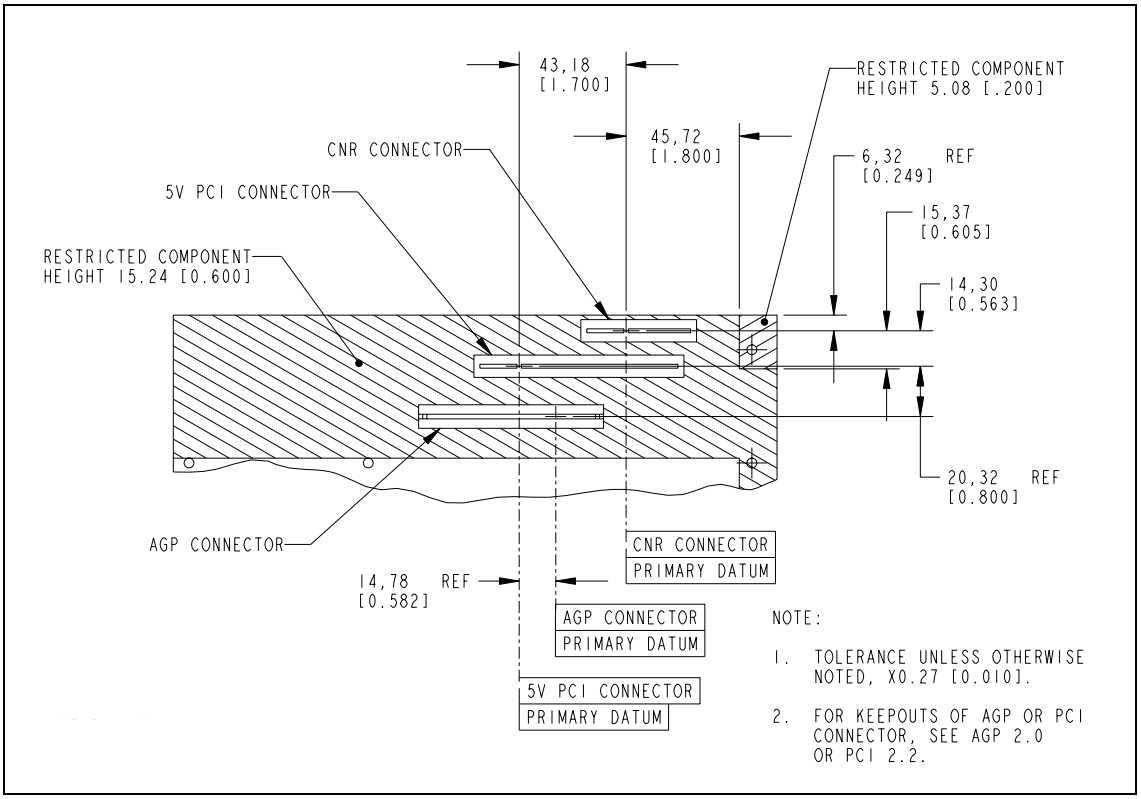
Figure 75. CNR Interface



9.2.1. CNR Placement

The following figure shows the placement of a CNR connector. Note that the following figure also shows the motherboard component height restrictions. Failure to meet the specified height restrictions may prevent a CNR board from properly seating in the CNR connector. In addition, the CNR connector mechanical location is shown relative to the PCI card edge connector. This implies that the absolute placement (relative to board edges and mounting holes) of the CNR connector must be determined from the motherboard specification for the appropriate form factor. If a PCI connector is not placed on the motherboard, the CNR connector placement must be determined relative to a phantom, or assumed PCI connector.

Figure 76. CNR Connector Location

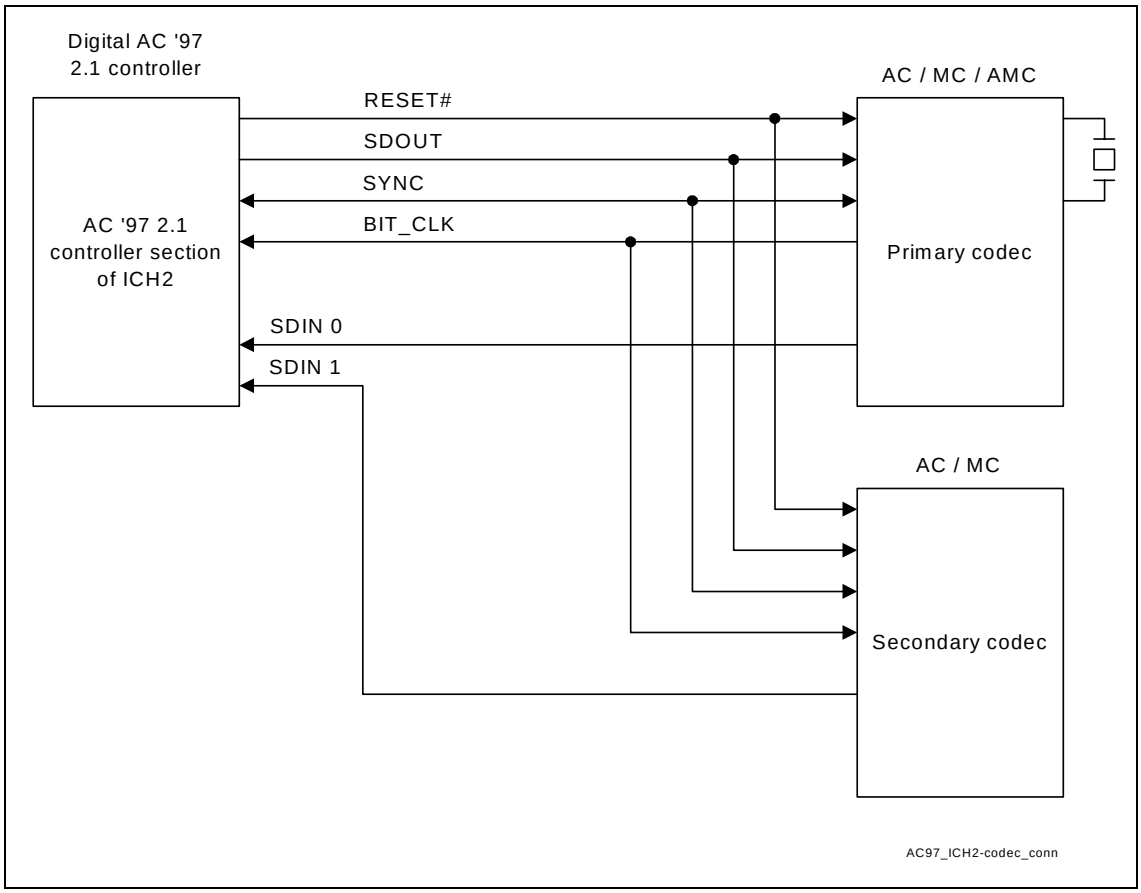


9.3. AC ’97

The ICH2 implements an *AC ’97 Component Specification, Revision 2.1* compliant digital controller. Any codec attached to the ICH2 AC-link must *AC ’97 Component Specification, Revision 2.1* as well. Contact your codec IHV for information *AC ’97 Component Specification, Revision 2.1* compliant products. The *AC ’97 Component Specification, Revision 2.1* is available on the Intel website: http://developer.intel.com/pc-supp/platform/ac97/index.htm

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams, as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH2 AC-link allows a maximum of two codecs to be connected. The following figure shows a two-codec topology of the AC-link for the ICH2.

Figure 77. Intel® ICH2 AC ’97 (Codec Connection)



In a lightly loaded system (e.g., single codec down), AC ’97 signal integrity should be evaluated to confirm that the signal quality on the link is acceptable to the codec used in the design. A series resistor at the driver and a capacitor at the codec can be implemented to compensate for any signal integrity issues. The values used will be design dependent and should be verified for correct timings. The ICH2 AC-link output buffers are designed to meet *AC ’97 Component Specification, Revision 2.1* with the specified load of 50 pF

The ICH2 supports the combinations of codecs shown in the following figures:

Figure 78. Audio Codec

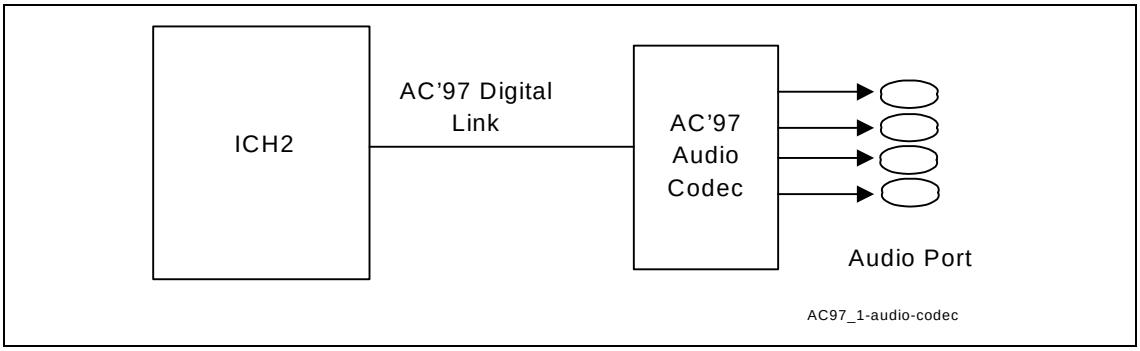


Figure 79. Modem Codec

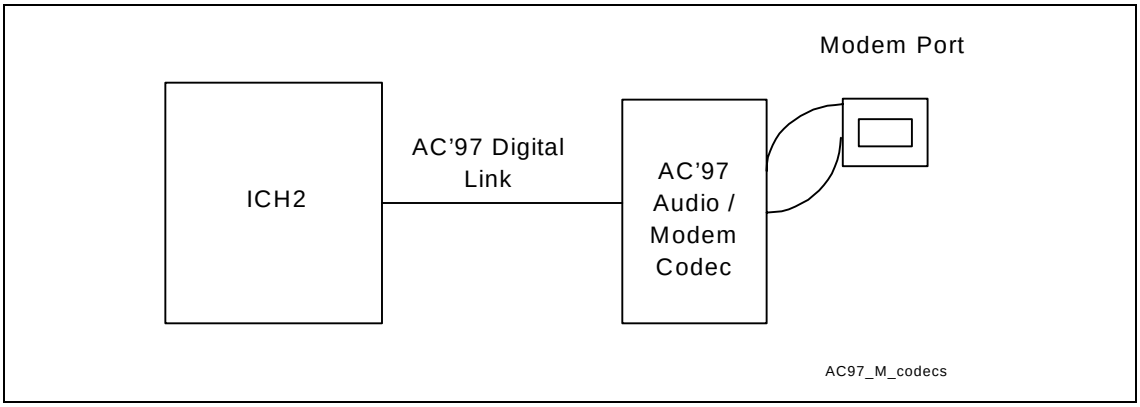


Figure 80. Audio/Modem Codec

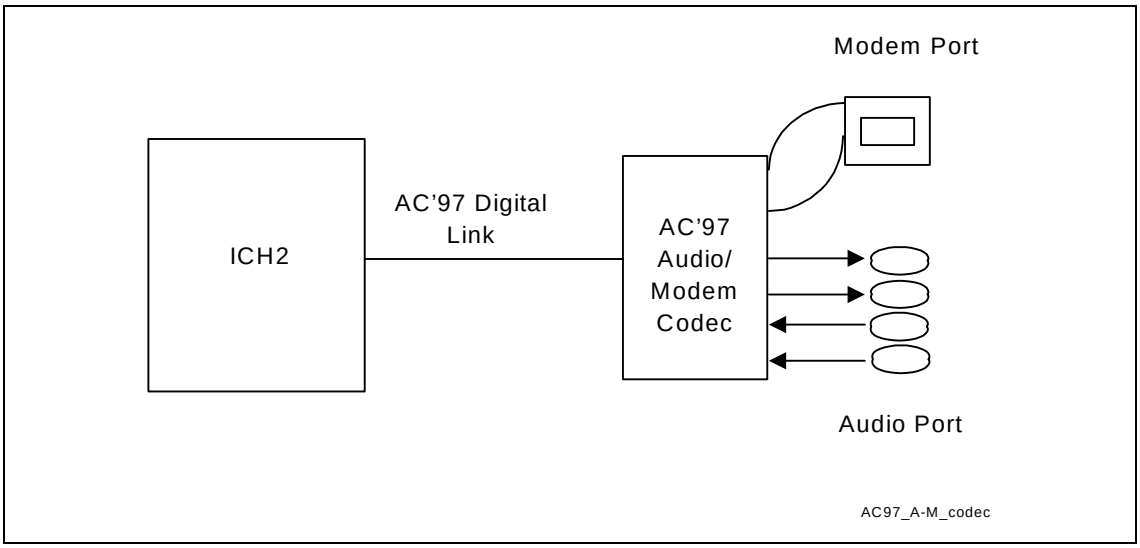


Figure 81. Modem Codecs

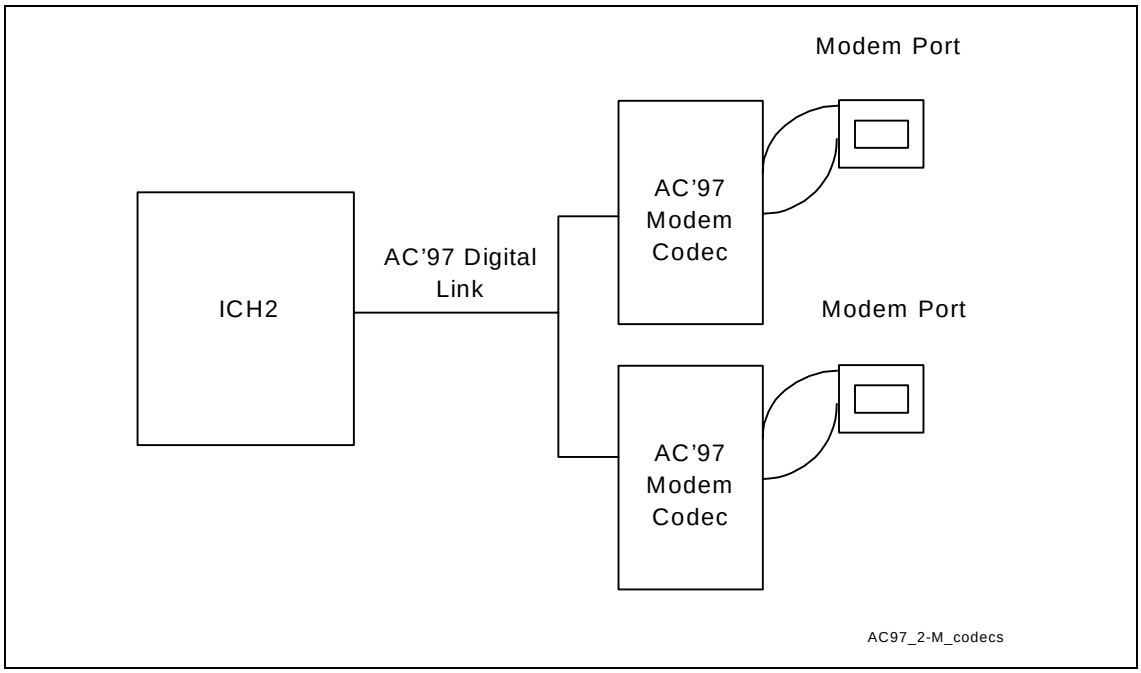


Figure 82. Audio and Modem Codecs

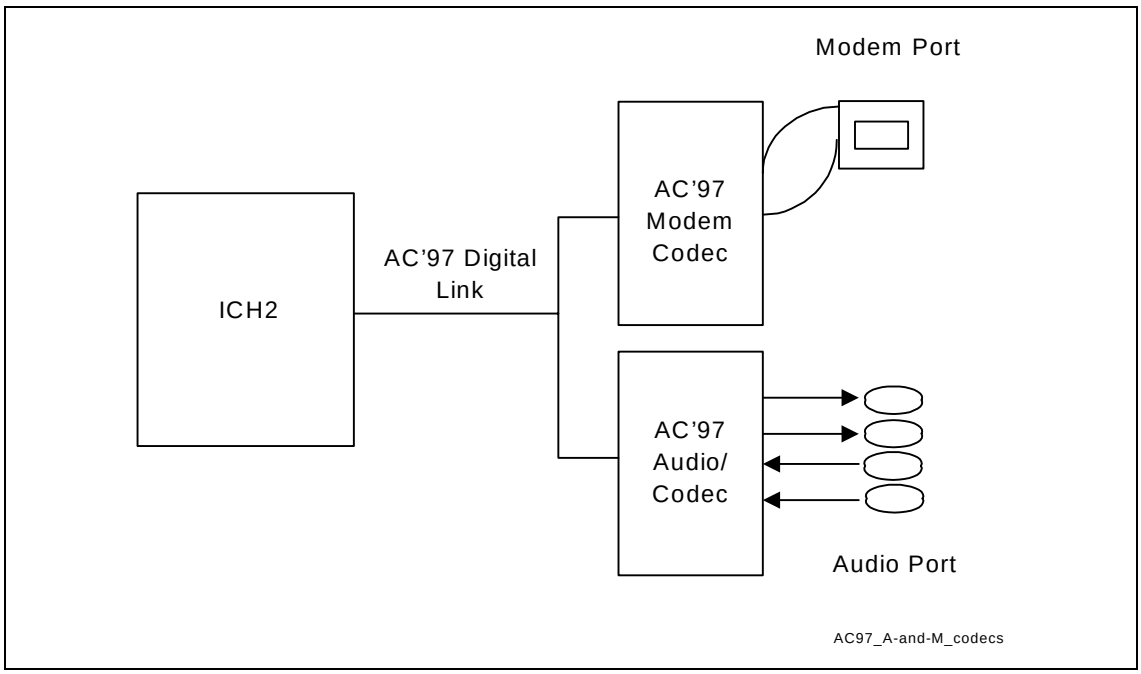


Figure 83. Audio Codecs

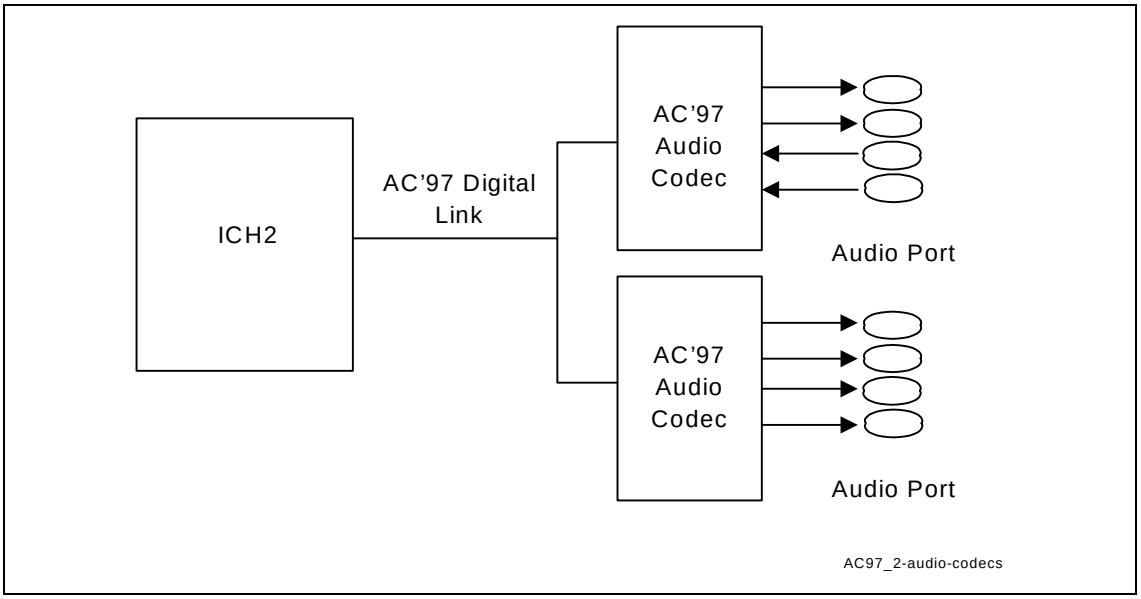
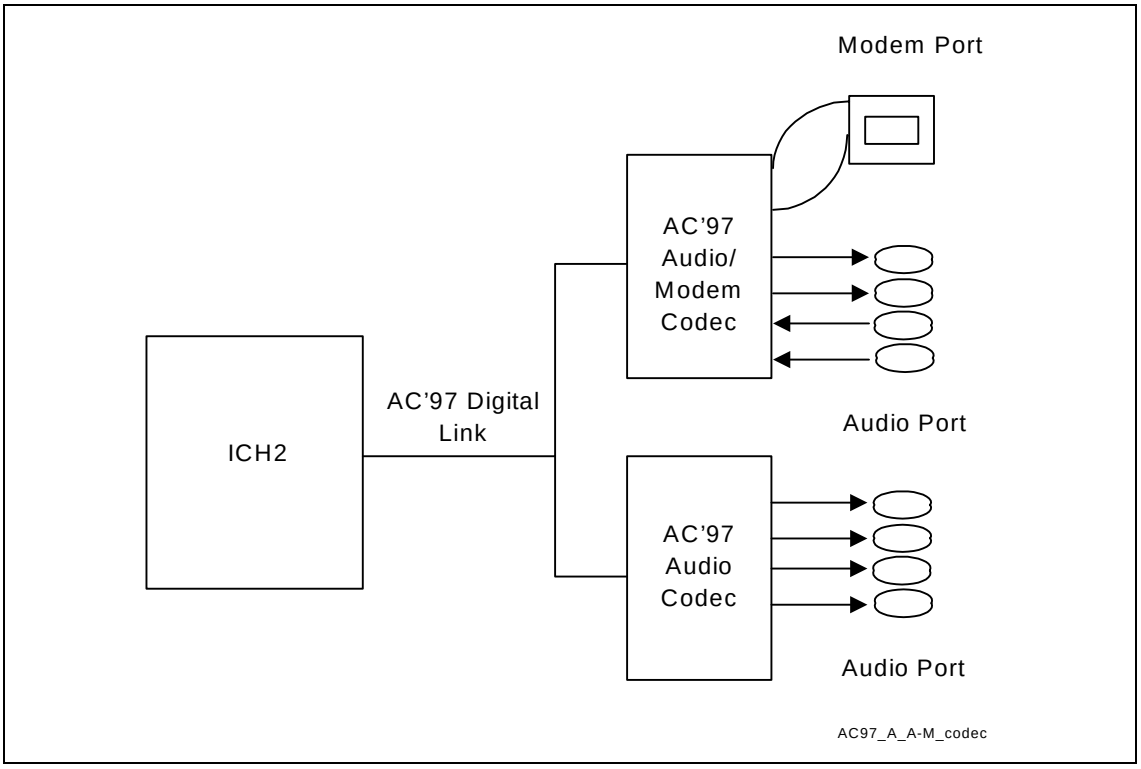


Figure 84. Audio and Audio/Modem Codecs



The AC ’97 interface can be routed using 5 mil traces with 5-mil space between the traces. Maximum length between ICH2 to CODEC/CNR is 14 inches in a tee topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4 inches for the AC’LINK. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$

Intel has developed an advanced common connector for both AC ’97 as well as networking options. This is known as the Communication Network Riser (CNR).

Clocking is provided from the primary codec on the link via BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. BITCLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH2), and any other codec present. That clock is used as the timebase for latching and driving data.

The ICH2 supports wake on ring from S1–S5 via the AC-link. The codec asserts SDATAIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH2 has weak pull-downs/pull-ups that are only enabled when the AC-Link Shut Off bit in the ICH2 is set. This will keep the link from floating when the AC-link is off, or there are no codecs present.

If the Shut-off bit is not set, it implies that there is a codec on the link. Therefore, the codec and ICH2 will drive BITCLK and AC_SDOUT, respectively. However, AC_SDIN0 and AC_SDIN1 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec. If there is one or no CODEC on board, then the unused AC_SDINx pin(s) should have a weak (10 kΩ) pull-down to keep it from floating.

Table 32. AC ’97 SDIN Pull-Down Resistors

System Solution	Pull-up Requirements
On-board Codec Only	Pull-down the SDIN pin that is NOT connected to the codec
AMR Only	Pull-down BOTH SDIN pins
BOTH AMR and On-board Codec	Pull-down any SDIN pin that could be NC(1)

NOTES:
1. If the on-board codec can be disabled, both SDIN pins must have pull-downs. If the on-board codec cannot be disabled, only the SDIN not connected to the on-board codec requires a pull-down.

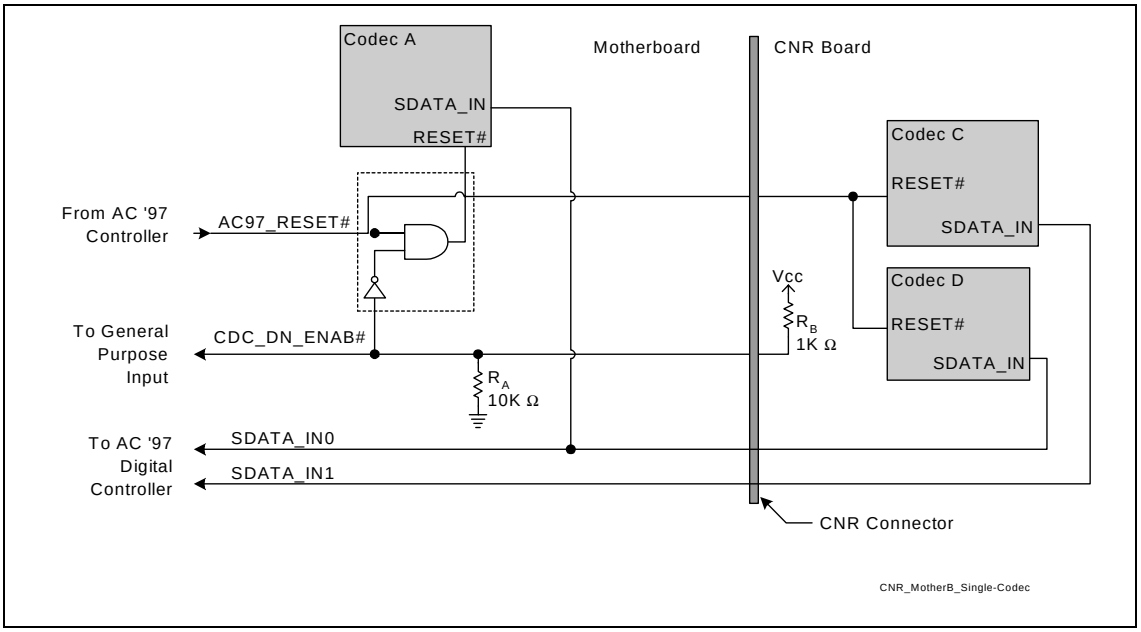
9.3.1. AC ’97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Refer to Intel’s White Paper *Recommendations for ICHx/AC ’97 Audio (Motherboard and Communication and Network Riser)* for Intel’s recommended codec configurations.

To support more than two channels of audio output, the ICH2 allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC ’97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

The following circuits (Figure 85 through Figure 88) show the adaptability of a system with the modification of R_A and R_B combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration and allows the configuration of the link to be determined by the BIOS so that the correct PnP IDs can be loaded.

Figure 85. CDC_DN_ENAB# Support Circuitry for a Single Codec Motherboard



As shown in Figure 85 when a single codec is located on the motherboard, the resistor R_A and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented, on the motherboard. This circuitry is required in order to disable the motherboard codec when a CNR is installed which contains two AC ’97 codecs (or a single AC ’97 codec which must be the primary codec on the AC-Link).

By installing resistor R_B (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset) and the codec(s) on the CNR take control of the AC-Link. One possible example of using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

The architecture shown in Figure 86 has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor R_B on the CNR to 100 kΩ). An example of one such upgrade is increasing from two-channel to four or six-channel audio.

Both Figure 86 and Figure 87 show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_INn line as to not conflict with the motherboard codec(s).

Figure 86. CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade

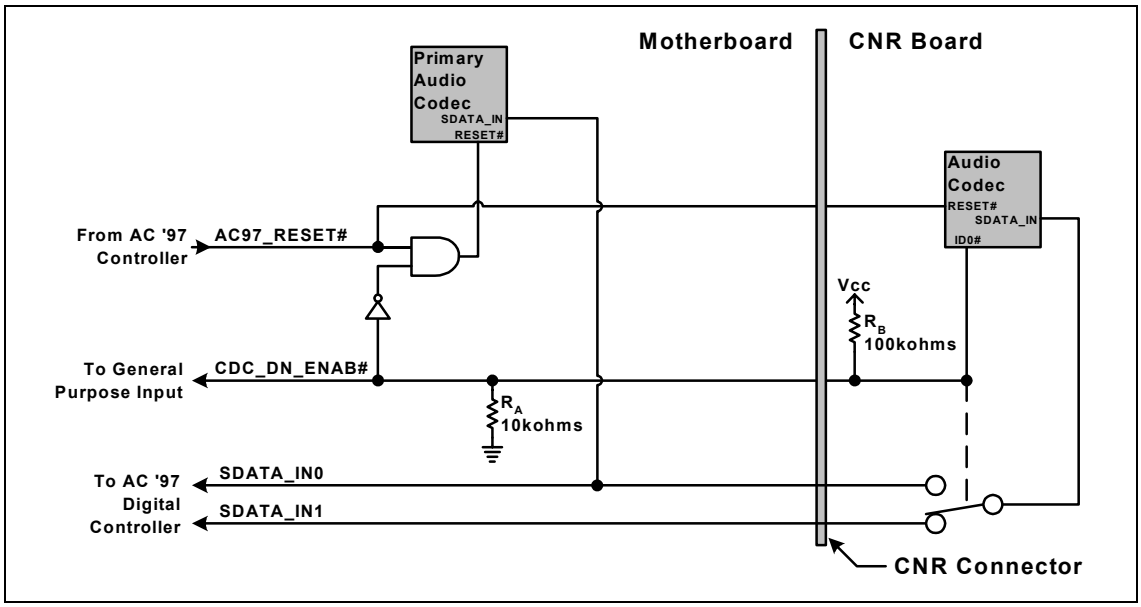
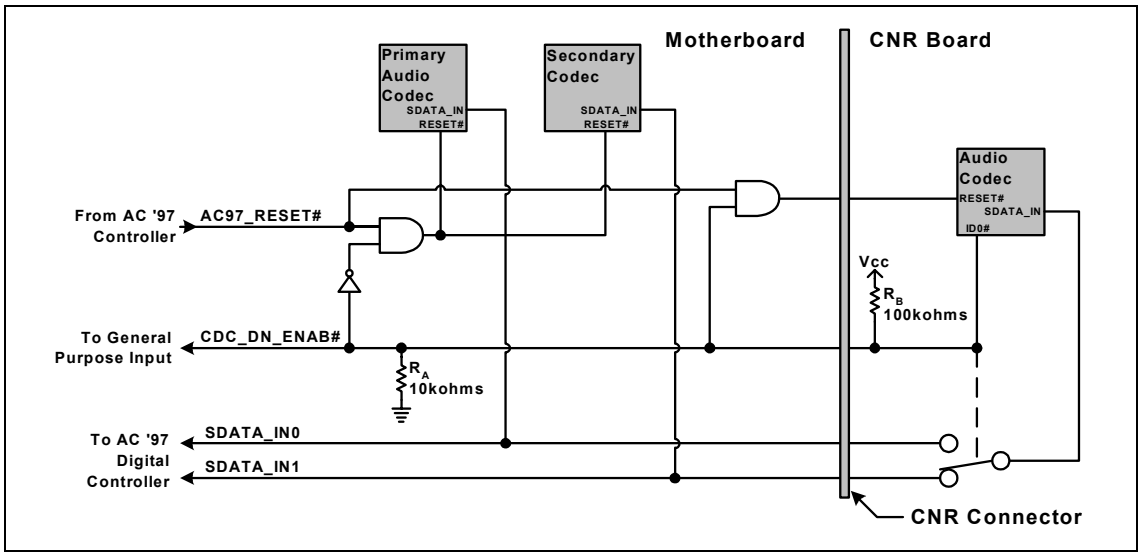


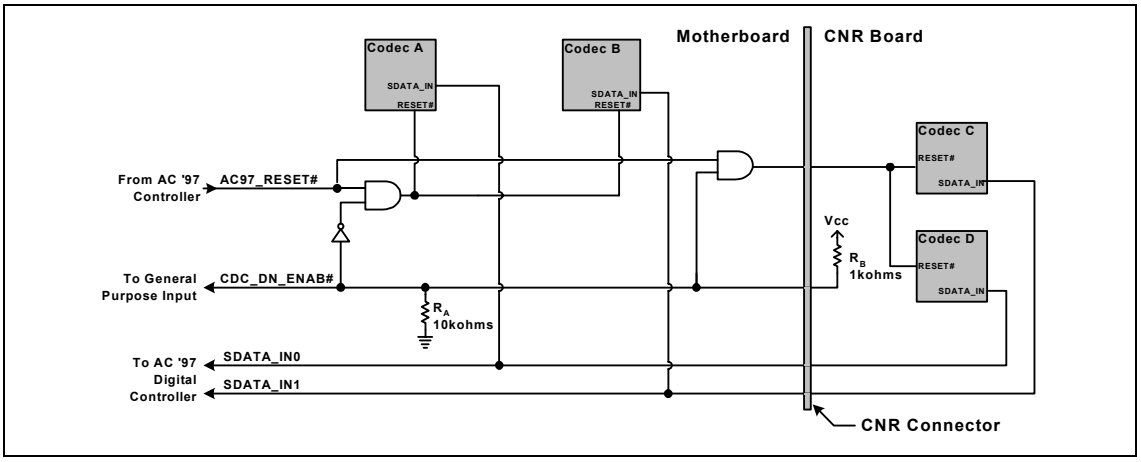
Figure 87 shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration the resistor, R_B, has been changed to 100 kΩ.

Figure 87. CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / One-Codec on CNR



The following figure shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by R_A being 10 kΩ and R_B being 1 kΩ.

Figure 88. CDC_DN_ENAB# Support for Two-Codecs on Motherboard / Two-Codecs on CNR



Circuit Notes

- All CNR designs include resistor R_B. The value of R_B is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
- Any CNR with two codecs must implement R_B with value 1 kΩ. If there is one Codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff R_B. If implemented, R_B must be connected to the same power well as the codec so that it is valid whenever the codec has power.
- A motherboard with one or more codecs down must implement R_A with a value of 10 kΩ.
- The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is *required* to be connected to a GPI; a connection to a GPIO is *strongly recommended* for testing purposes.

Table 33. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC '97 Interface.
AC97_RESET#	Reset signal from the AC '97 Digital Controller (ICH2).
SDATA_Inn	AC '97 serial data from an AC '97-compliant codec to an AC '97-compliant controller (i.e., the ICH2).

9.3.2. Valid Codec Configurations

Table 34. Codec Configurations

Valid Codec Configurations
AC(Primary)
MC(Primary)
AMC(Primary)
AC(Primary) + MC(Secondary)
AC(Primary) + AC(Secondary)
AC(Primary) + AMC(Secondary)

Invalid Codec Configurations
MC(Primary) + X(any other type of codec)
AMC(Primary) + AMC(Secondary)
AMC(Primary) + MC(Secondary)

9.4. USB Guidelines

The following are general guidelines for the USB interface:

- Unused USB ports should be terminated with 15 kΩ pull-down resistors on both P+/P- data lines.
- 15 Ω series resistors should be placed as close as possible to the ICH2 (<1 inch). These series resistors are required for source termination of the reflected signal.
- An optional 47 pF caps must be placed as close to the ICH2 as possible and on the ICH2 side of the series resistors on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). These caps are there for signal quality (rise/fall time) and to help minimize EMI radiation.
- 15 kΩ ±5% pull-down resistors should be placed on the USB side of the series resistors on the USB data lines (P0+/- … P3+/-), and are REQUIRED for signal termination by USB specification. The length of the stub should be as short as possible.
- The trace impedance for the P0+/-… P3+/- signals should be 45 Ω (to ground) for each USB signal P+ or P-. The impedance is 90 Ω between the differential signal pairs P+ and P- to match the 90 Ω USB twisted pair cable impedance. Note that twisted pair characteristic impedance of 90 Ω is the series impedance of both wires, resulting in an individual wire presenting 45-Ω impedance. The trace impedance can be controlled by carefully selecting the line width, trace distance from power or ground planes, and physical proximity of nearby traces.
- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. Lastly, do not route over plane splits.

The following figure illustrates the recommended USB schematic.

Figure 89. USB Data Signals

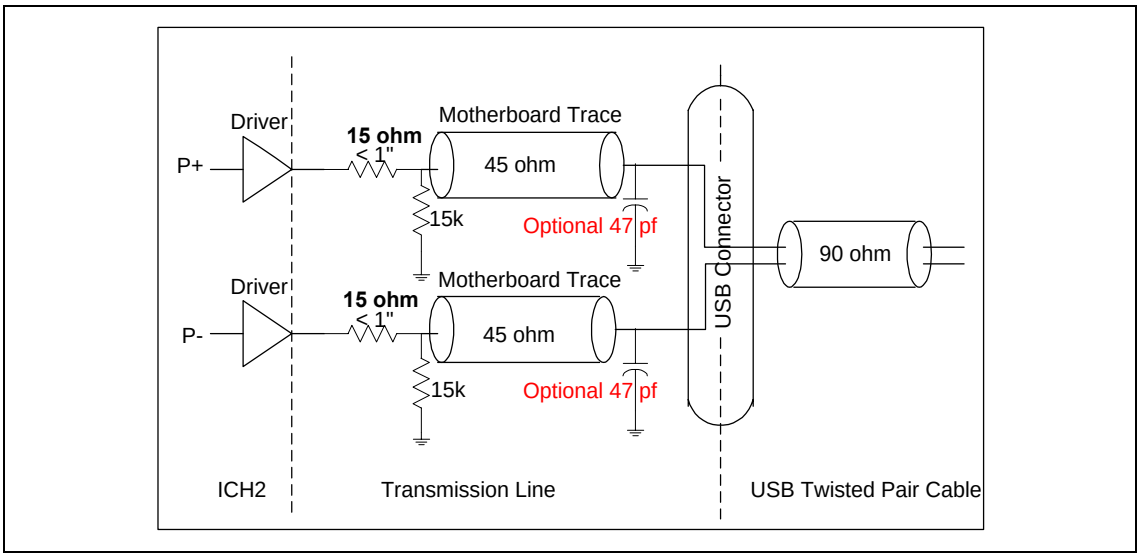


Table 35. Recommended USB Trace Characteristics

Impedance 'Z0' = 45.4 Ω
Line Delay = 160.2 ps
Capacitance = 3.5 pF
Inductance = 7.3 nH
Res @ 20 °C = 53.9 mΩ

9.5. IOAPIC Design Recommendations

The IOAPIC bus is not required in Pentium 4 processor-based designs.

Intel® Pentium® 4 Processor

- The Pentium 4 processor does not have these pins defined. It receives interrupts for servicing via the System Bus interrupt delivery mechanism. Refer to the *ICH2* datasheet for more details.

On the ICH2

- Tie PICCLK directly to ground
- Tie PICD0, PICD1 to ground via 1 kΩ to 10 kΩ resistor

9.6. SMBus/SMlink Interface

The SMBus interface on the ICH2 is the same as that on the ICH. It uses two signals SMBCLK and SMBDATA to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH2. If the SMBus is used only for the RAMBUS* SPD EEPROMs (one on each RIMM connector), both signals should be pulled up with a 4.7 kΩ resistor to 3.3 V.

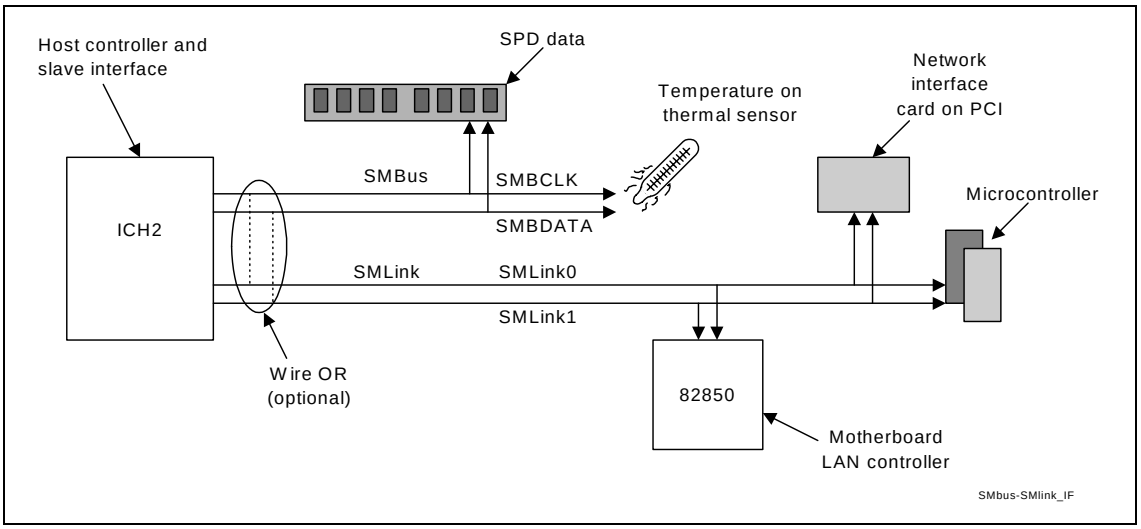
The ICH2 incorporates a new SMLink interface supporting AOL*, AOL2* and a slave functionality. It uses two signals SMLINK[1:0]. SMLINK[0] corresponds to an SMBus clock signal and SMLINK[1] corresponds to an SMBus data signal. Internally the SMLINK signals are connected to the following:

- ICH2 Slave Interface
- ICH2 TCO Host Controller
- ICH2 Integrated LAN* Slave Interface

For Alert on LAN* (AOL*) functionality, TCO Host Controller transmits heartbeat and event messages over the interface. When using the 82562EM LAN* Connect Component, the ICH2's integrated LAN* Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, AOL2-enabled LAN* controller (i.e., Intel PRO/100 S) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH2 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the TCO Host Controller obey the SMBus protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (e.g., Intel PRO/100 S) to access targets on the SMBus as well as the ICH2 Slave interface. This is accomplished by connecting SMLink[0] to SMBCLK and SMLink[1] to SMBDATA (see the following figure).

Figure 90. SMBUS/SMLink Interface



Note: Intel does not support external access of the ICH2's Integrated LAN* controller via the SMLink interface. Also, Intel does not support access of the ICH2's SMBus Slave Interface by the ICH2's SMBUS host controller.

Refer to the ICH2 datasheet for full functionality descriptions of the SMLink and SMBus interface.

9.6.1. SMBus Architecture and Design Considerations

SMBus Design Considerations

There are several possibilities for designing an SMBus using the ICH2. Designs can be grouped into three major categories based on the power supply source for the SMBus microcontrollers. This includes two unified designs, where all devices are powered by either V_{CC_Core} or $V_{CC\_Suspend}$, and a mixed design where some devices are powered by each of the two supplies.

Primary Considerations in Choosing a Design are Based on

- Are there devices that must run in STR?
- Amount of $V_{CC\_Suspend}$ current available, i.e. minimizing load of $V_{CC\_Suspend}$

General Design Issues / Notes

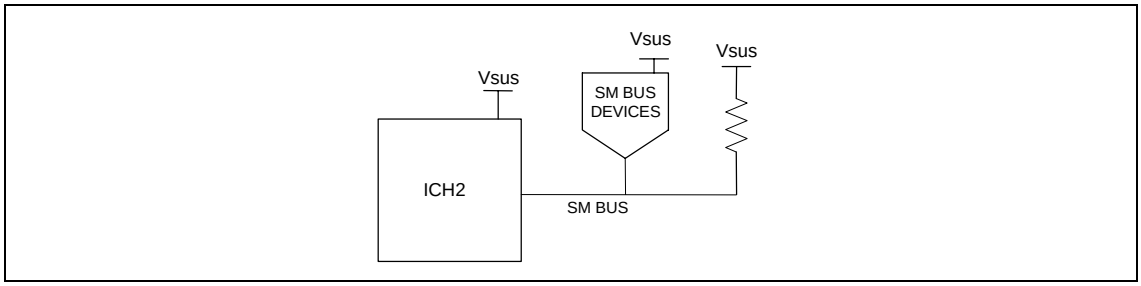
Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the number of devices present on the bus. A typical value is 8.2 kΩ. This should prevent the SMBus signals from floating, which could cause leakage in the ICH2 and other devices.
- SDRAM DIMMs have their SPD device powered by the same power plane as that used for the DRAM array. Thus, in a system where STR is supported, the SPD device must be powered by $V_{CC\_Suspend}$. In a system not supporting STR, this DIMM can be powered by the core supply.
- RIMM modules have a separate power source from the RDRAM array for the SPD device. If this SPD device needs to operate in STR, it should be connected to the $V_{CC\_Suspend}$ supply.
- The ICH2 does not run SMBus cycles while in STR.
- SMBus devices that can operate in STR must be powered by the $V_{CC\_Suspend}$ supply.

The Unified $V_{CC\_Suspend}$ Architecture

In this design all SMBus devices are powered by the $V_{CC\_Suspend}$ supply. Consideration must be made to provide enough $V_{CC\_Suspend}$ current while in STR.

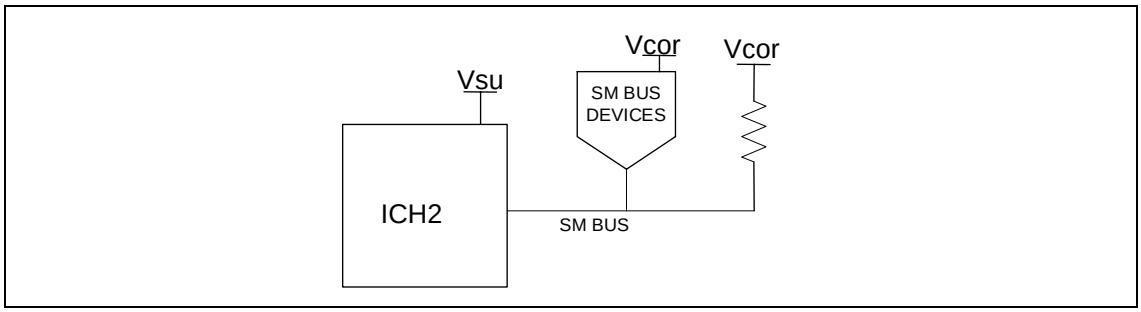
Figure 91. Unified $V_{CC\_Suspend}$ Architecture



The Unified V_{CC_Core} Architecture

In this design, all SMBUS devices are powered by the V_{CC_Core} supply. This architecture allows none of the devices to operate in STR, but minimizes the load on $V_{CC\_Suspend}$ (see the following figure).

Figure 92. Unified V_{CC_Core} Architecture



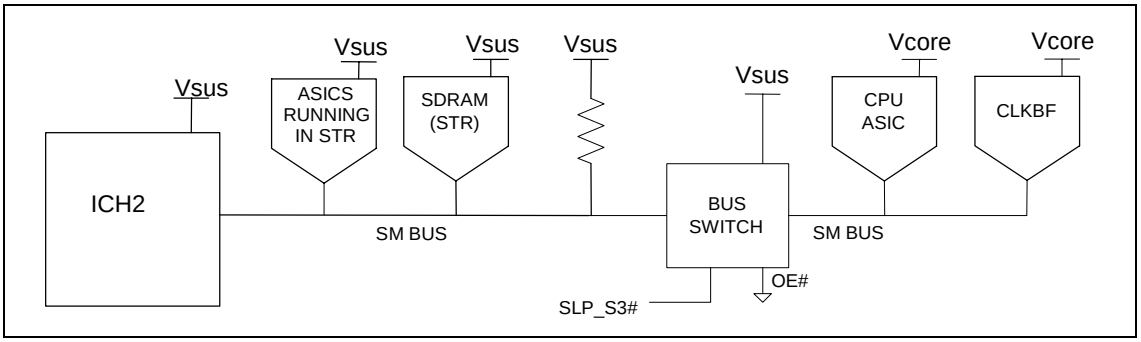
NOTES:

1. The SMBus device needs to be back-drive safe while its supply (Vcore) is off and $V_{CC\_Suspend}$ is still powered.
2. In suspended modes where V_{CC_Core} is OFF and $V_{CC\_Suspend}$ is on, the V_{CC_Core} node will be very near ground. In this case the input leakage of the ICH2 will be approximately 10 µA.

Mixed Architecture:

This design allows for SMBus devices to communicate while in STR, yet minimizes $V_{CC\_Suspend}$ leakage by keeping non-essential devices on the core supply. This is accomplished by the use of a "bus switch" to isolate the devices powered by the core and suspend supplies (see the following figure).

Figure 93. Mixed $V_{CC\_Suspend}$/V_{CC_Core} Architecture



Added Considerations for Mixed Architecture

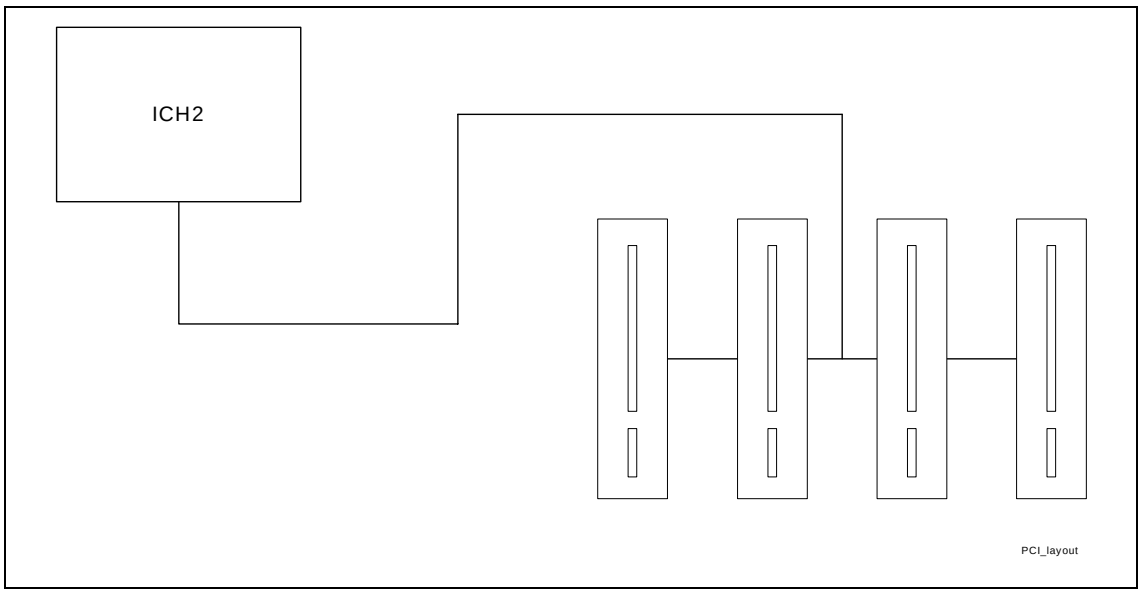
- The bus switch must be powered by $V_{CC\_Suspend}$
- If there are 5 V SMBus devices used, then an added level translator must be used to separate those devices driving 5 V from those driving 3 V signal levels.
- Devices that are powered by the $V_{CC\_Suspend}$ well must not drive into other devices that are powered off. This is accomplished with the "bus switch."

9.7. PCI

The ICH2 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Rev. 2.2*. The implementation is optimized for high-performance data streaming when the ICH2 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification, Rev. 2.2*.

The ICH2 supports six PCI Bus masters (excluding the ICH2), by providing six REQ#/GNT# pairs. In addition, the ICH2 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

Figure 94. PCI Bus Layout Example



9.8. RTC

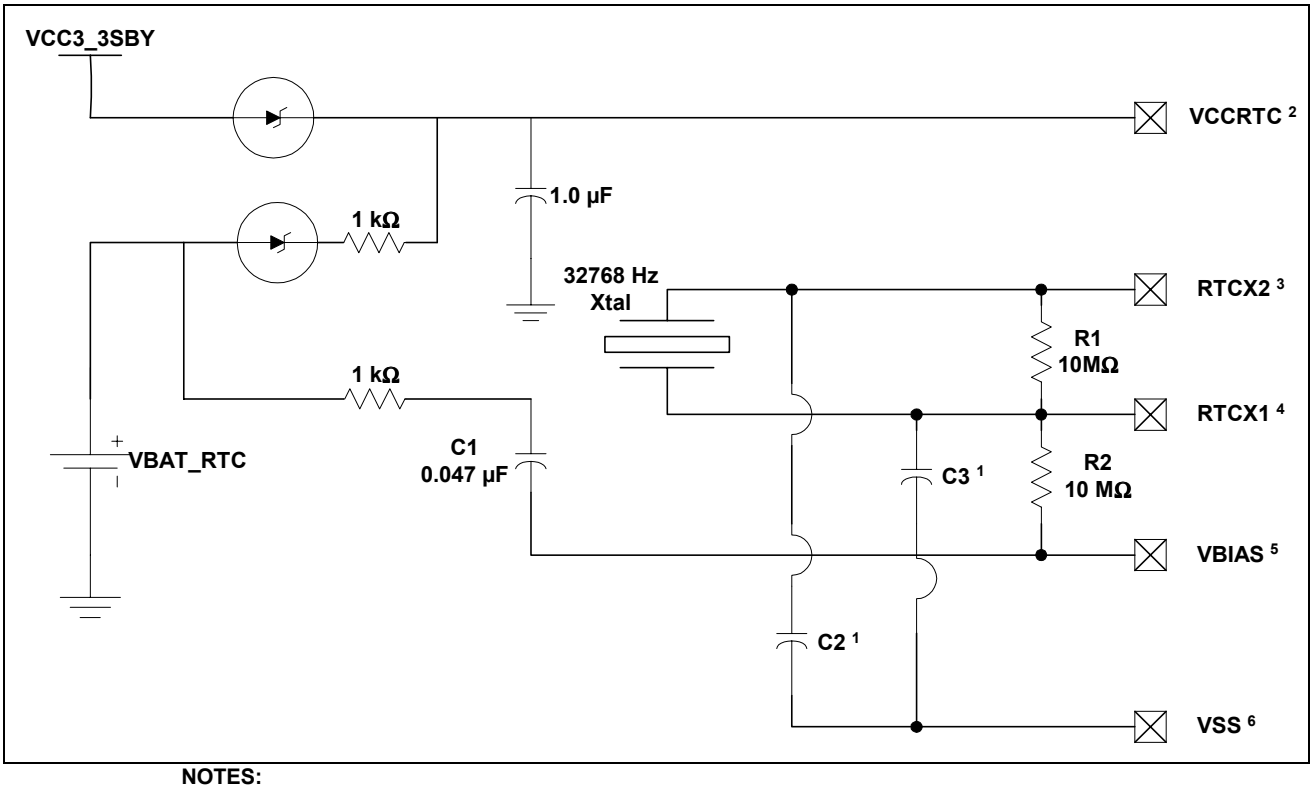
The ICH2 contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

This section will present the recommended hookup for the RTC circuit for the ICH2. **This circuit is not the same as the circuit used for the PIIX4.**

9.8.1. RTC Crystal

The ICH2 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 pins. Figure 95 documents the external circuitry that comprises the oscillator of the ICH2 RTC.

Figure 95. External Circuitry for the Intel® ICH2 RTC



NOTES:

1. The exact capacitor value needs to based on what the crystal maker recommends. (Typical values for C2 and C3 are 18 pF for a crystal with CLOAD=12.5pF).
2. VccRTC: Power for RTC Well
3. RTCX2: Crystal Input 2 – Connected to the 32.768 kHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS Voltage – This pin is used to provide a reference voltage, and this DC voltage sets a current, which is mirrored throughout the oscillator and buffer circuitry.
6. Vss: Ground

9.8.2. External Capacitors

To maintain the RTC accuracy, the external capacitor C1 needs to be 0.047 µF, and the external capacitor values (C2 and C3) should be chosen to provide the manufacturer's specified load capacitance (Cload) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. When the external capacitor values are combined with the capacitance of the trace, socket, and package, the closer the capacitor value can be matched to the actual load capacitance of the crystal used, the more accurate the RTC will be.

Equation 8 can be used to choose the external capacitance values (C2 and C3):

Equation 8. External Capacitance Values

$$C_{LOAD} = (C_2 * C_3)/(C_2+C_3) + C_{PARASITIC}$$

Note: C3 can be chosen such that C3 > C2. Then C2 can be trimmed to obtain the 32.768 kHz.

9.8.3. RTC Layout Considerations

- Keep the RTC lead lengths as short as possible; around ¼ inch is sufficient.
- Minimize the capacitance between X_{IN} and X_{OUT} in the routing.
- Put a ground plane under the XTAL components.
- Do not route switching signals under the external components (unless on the other side of the board).
- The oscillator V_{CC} should be clean; use a filter, such as a RC lowpass, or a ferrite inductor.

9.8.4. RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH2 is not powered by the system.

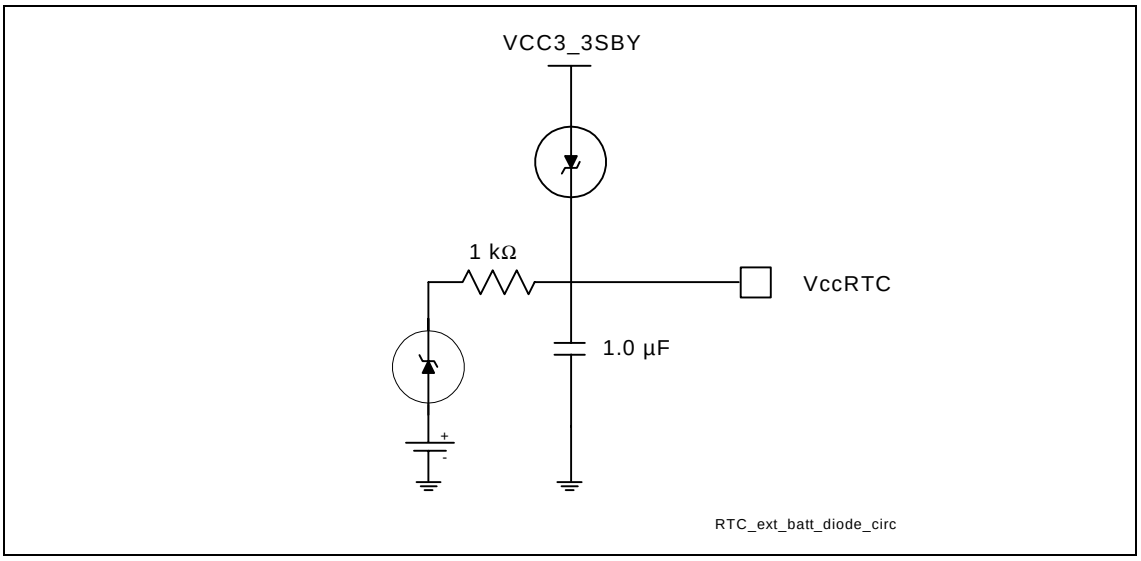
Example batteries are: Duracell* 2032, 2025, or 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 mAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

170,000 uAh / 3 µA = 56,666 h = 6.4 years

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0v to 3.3v.

The battery must be connected to the ICH2 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH2 RTC-well to be powered by the battery when the system power is not available, but by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. The following figure is an example of a diode circuitry that is used.

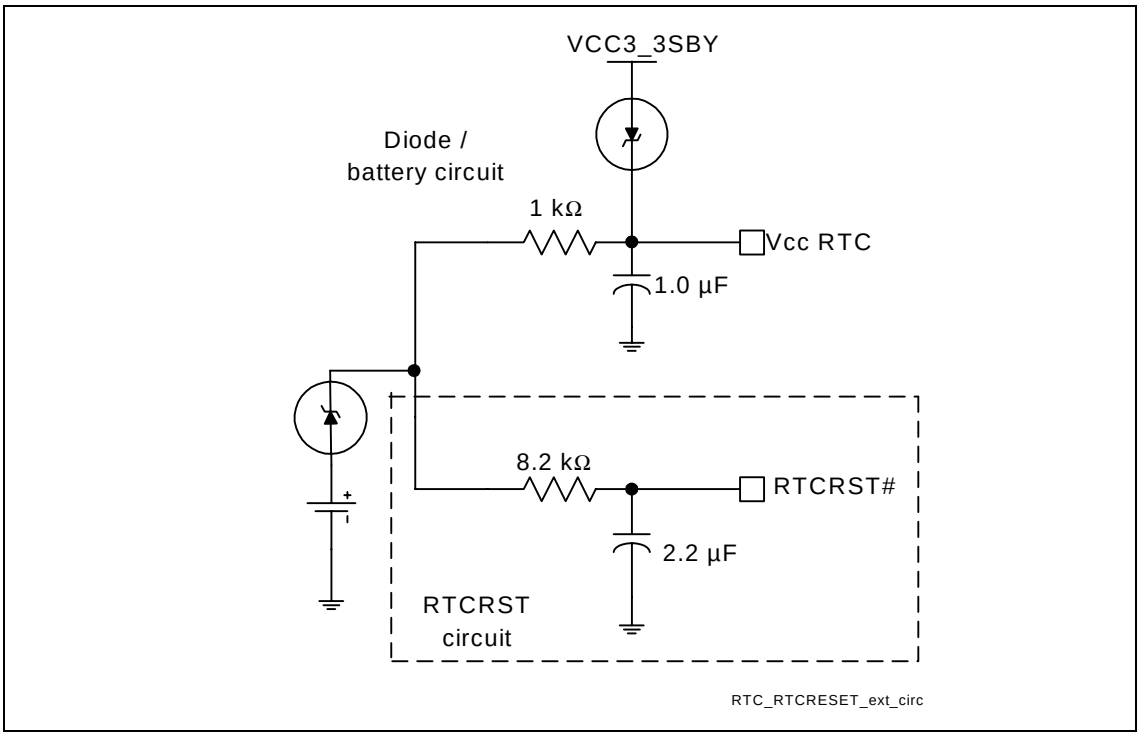
Figure 96. Diode Circuit to Connect RTC External Battery



A standby power supply should be used in a desktop system to provide continuous power to the RTC when available, which will significantly increase the RTC battery life and thereby the RTC accuracy.

9.8.5. RTC External RTCRST Circuit

Figure 97. RTCRST External Circuit for the Intel® ICH2 RTC



The ICH2 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay, such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 10–20 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1, and remains set until software clears it. As a result of this, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (Figure 97) which allows the RTC well to be powered by the battery when the system power is not available. Figure 97 is an example of this circuitry that is used in conjunction with the external diode circuit.

9.8.6. RTC Routing Guidelines

- All RTC OSC signals (RTCX1, RTCX2, VBIAS) should all be routed with trace lengths of less than 1 inch, the shorter the better.
- Minimize the capacitance between RTCX1 and RTCX2 in the routing (optimal would be a ground line between them).
- Put a ground plane under all of the external RTC circuitry.
- Do not route any switching signals under the external components (unless on the other side of the ground plane).

9.8.7. VBIAS DC Voltage and Noise Measurements

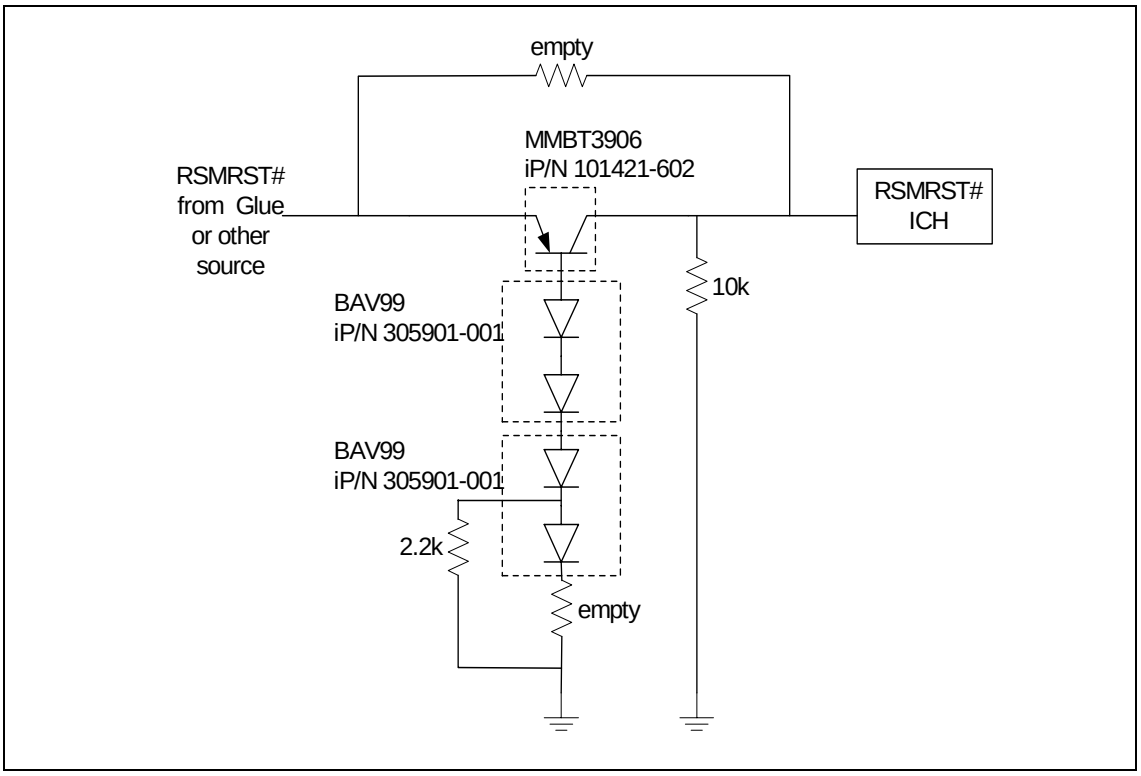
- Steady state VBIAS will be a DC voltage of about 0.38 V ±.06 V
- VBIAS will be “kicked” when the battery is inserted to about 0.7 V–1.0 V, but it will come back to its DC value within a few ms
- Noise on VBIAS must be kept to a minimum, 200 mV or less.
- VBIAS is very sensitive and cannot be directly probed, it can be probed through a 0.01 µF capacitor.
- Excess noise on VBIAS can cause the ICH2 internal oscillator to misbehave or even stop completely.
- To minimize noise of VBIAS It is necessary to implement the routing guidelines described above and the required external RTC circuitry as described in the *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel 82801BAM I/O Controller Hub 2 Mobile (ICH2-M)* datasheet.

9.8.8. Power-Well Isolation Control

The RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 95 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

- The circuit shown in Figure 98 below should be implemented to control well isolation between the 3.3 V resume and RTC power-wells. Failure to implement this circuit may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power).

Figure 98. RTC Power-Well Isolation Control



9.8.9 Power Supply PS_ON Consideration

- If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10-100mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

- The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

- The platform designer must ensure that the power supply used with the platform is not affected by this issue.

9.9. LAN Layout Guidelines

The ICH2 provides several options for integrated LAN capability. The platform supports several components depending on the target market.

Note: These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

Table 36. Integrated LAN Options

LAN* Connect Component	Connection	Features
82562EM	Advanced 10/100 Ethernet	AOL* & Ethernet 10/100 Connection
82562ET	10/100 Ethernet	Ethernet 10/100 Connection
82562EH	1 Mb HomePNA* LAN*	1 Mb HomePNA* connection

Intel developed a dual footprint for 82562ET and 82562EH to minimize the required number of board builds. A single layout with the specified dual footprint will allow the OEM to install the appropriate LAN* connect component to meet the market need. Design guidelines are provided for each required interface and connection. Refer to the following figure and table for the corresponding section of the design guide.

Figure 99. ICH2 / LAN* Connect Section

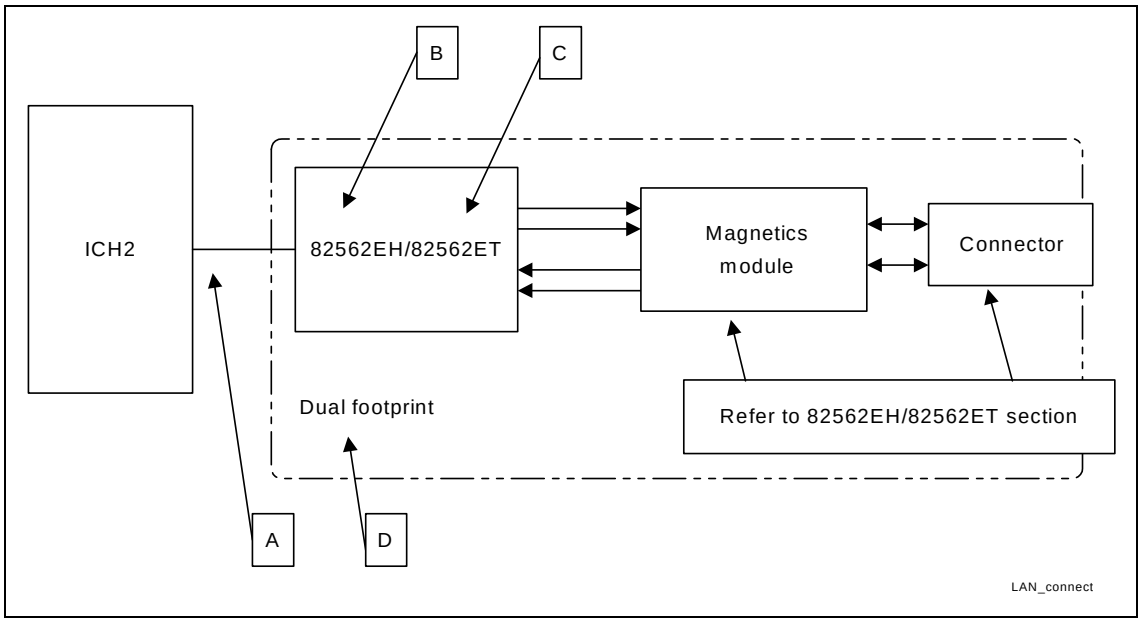


Table 37. LAN Design Guide Section Reference

Layout Section	Layout Section Reference (See Figure 99)	Design Guide Section
ICH2 – LAN* Interconnect	A	Section 9.9.1 ICH2 – LAN* Interconnect Guidelines
General Routing Guidelines	B,C,D	Section 9.9.2 General LAN Routing Guidelines and Considerations
82562EH	B	Section 9.9.3 82562EH Home/PNA* Guidelines

82562ET /82562EM	C	Section 9.9.4 82562ET / 82562EM Guidelines
Dual Layout Footprint	D	Section 9.9.6 82562ET / 82562EH Dual Footprint Guidelines

9.9.1. Intel® ICH2 – LAN Interconnect Guidelines

This section contains guidelines to the design of motherboards and riser cards to comply with LAN* Connect. It should not be treated as a specification and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the **LAN_CLK** traces to those of the other signals, as shown below. The following are guidelines for the ICH2 to LAN* component interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports both 82562EH and 82562ET/82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], and LAN_TXD[0] are shared by both components. Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected when 82562EH is installed Dual footprint guidelines are found in Section 9.9.6.

9.9.1.1. Bus Topologies

The LAN* connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH2 and the LAN* component
- Dual Footprint (See Section 9.9.6)
- LOM/CNR Implementation

9.9.1.2. Point-to-Point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EH, 82562ET, or CNR are installed.

Figure 100. Single Solution Interconnect

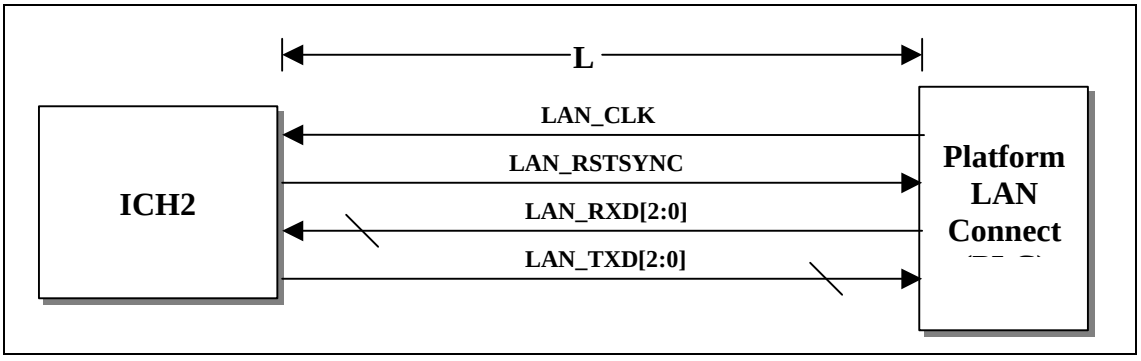


Table 38. Length Requirements for Single Solution Interconnect

Component	Minimum (in.)	Maximum (in.)	Notes
82562EH	L=4.5	L=10	Signal Lines LAN_RXD[2:1] and LAN_TXD[2:1] not connected
82562ET	L=3.5	L=10	
CNR	L=3	L=9	

NOTES: Length of trace from connector to LOM should be 0.5 inches to 3 inches.

9.9.1.3. LOM/CNR Interconnect

The following guidelines allow for an all inclusive motherboard solution. This layout combines LOM, dual footprint, and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN* on motherboard option can be implemented at one time. The recommended trace routing lengths are shown below.

Figure 101. LOM/CNR Interconnect

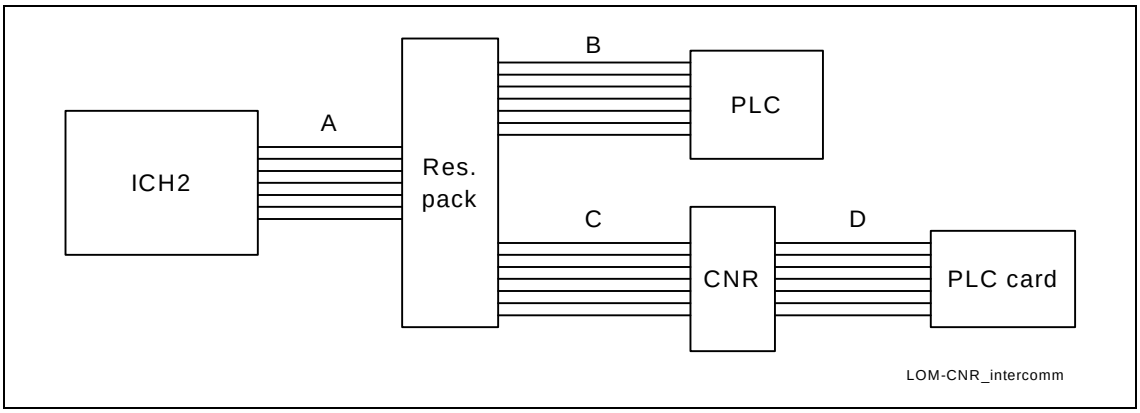


Table 39. Length Requirements for LOM/CNR Interconnect

Configuration	Segment A (in.)	Segment B (in.)	Segment C (in.)	Segment D (in.)
82562EH	0.5 to 6.0	4 to 10 - A	—	—
82562ET	0.5 to 7	3 to 10 - A	—	—
Dual Footprint	0.5 to 6	4 to 10 – A	—	—
82562ET/EH Card(1)	0.5 to 6.5	—	2.5 o 9 – A	0.5 to 3

NOTES:

1. Total trace length should no exceed 13 inches.

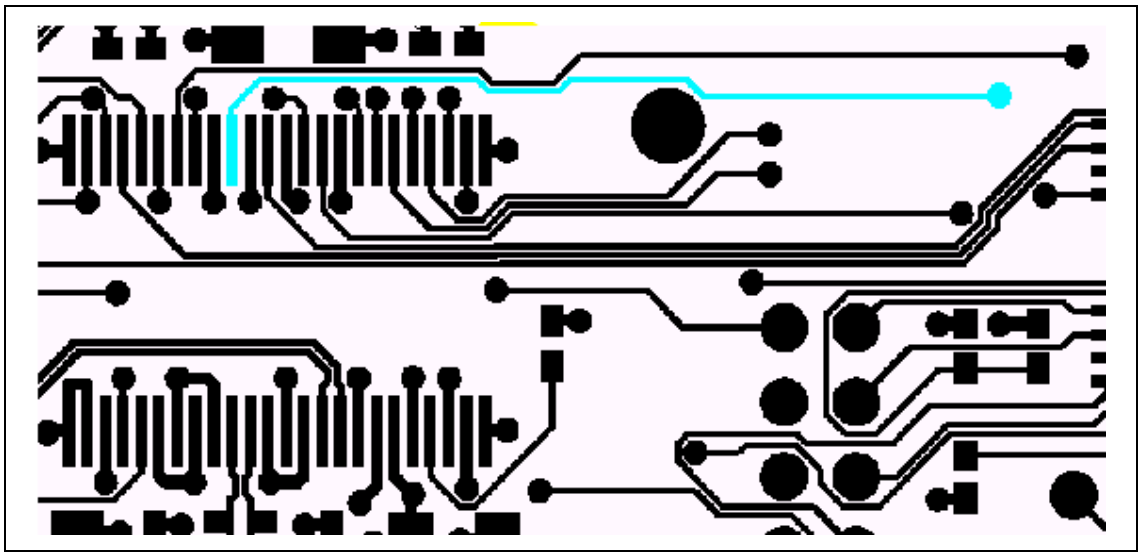
Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 Ω or 22 Ω.
- LAN* on motherboard PLC can be a dual footprint configuration.

9.9.1.4. Signal Routing and Layout

LAN* Connect signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 102. LAN_CLK Routing Example



9.9.1.5. Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the t_{RMATCH} skew parameter.

9.9.1.6. Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ±15% is strongly recommended; otherwise, signal integrity requirements may be violated.

9.9.1.7. Line Termination

Line termination mechanisms are not specified for the LAN* connect interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

9.9.2. General LAN Routing Guidelines and Considerations

9.9.2.1. General Trace Routing Considerations

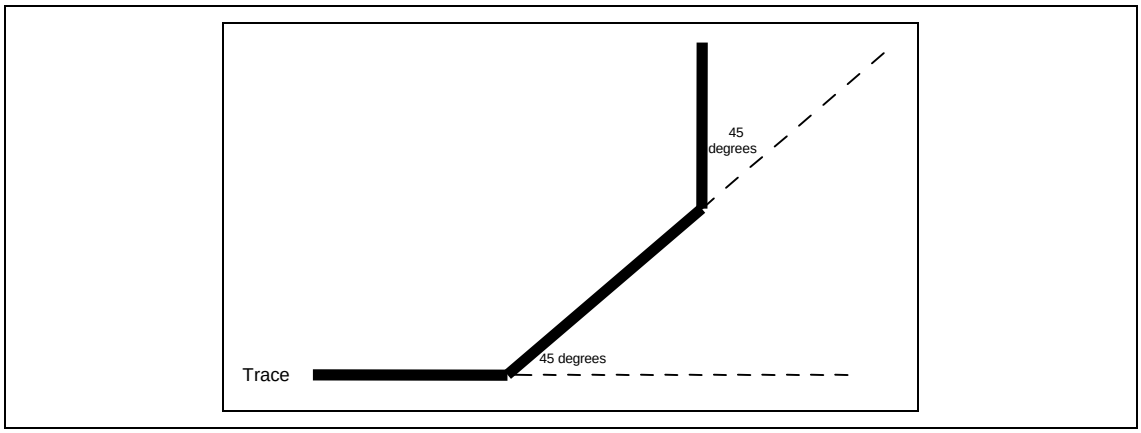
Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes.

Observe the following suggestions to help optimize board performance:

Note: Some suggestions are specific to a 4.5 mil stack-up.

- Maximum mismatch between the length of the clock trace and the length of any data trace is 0.5 inches.
- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other.
- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI, and/or degraded receive BER.]
- Do not route the transmit differential traces closer than 70 mils to the receive differential traces.
- Do not route any other signal traces both parallel to the differential traces, and closer than 70 mils to the differential traces.
- Keep maximum separation between differential pairs to 7 mils.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to the following figure.
- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 103. Trace Routing



9.9.2.1.1. Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by 10 Ω, when the traces within a pair are closer than 0.030 inches (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector / magnetics / edge of the board.

9.9.2.1.2. Signal Isolation

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 70 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together.

  Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.

- Isolate I/O signals from high speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.

- Avoid routing high-speed LAN* or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

9.9.2.2. Power and Ground Connections

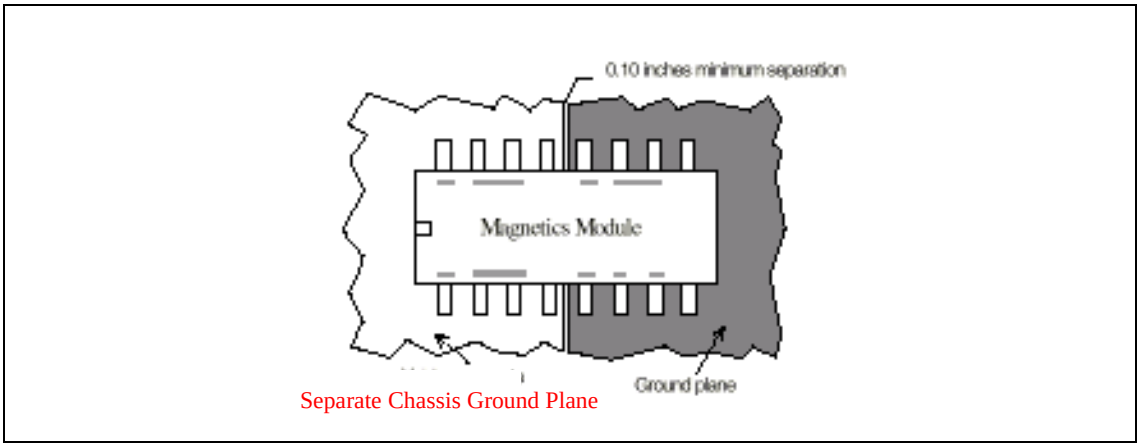
Some rules and guidelines to follow for power and ground connections:

- All V_{CC} pins should be connected to the same power supply.
- All V_{SS} pins should be connected to the same ground plane.
- Use one decoupling capacitor per power pin for optimized performance
- Place decoupling as close as possible to power pins.

9.9.2.2.1. General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 104. Ground Plane Separation



Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

Some rules to follow that will help reduce circuit inductance in both backplanes and motherboards.

- *Route traces over a continuous plane with no interruptions (do not route over a split plane).* If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling.
- Noisy digital grounds may effect sensitive DC subsystems.
- All ground vias should be connected to every ground plane; and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics , which can radiate EMI.
- The ground plane beneath the filter/transformer module should be split. The RJ45 and/or RJ11 connector side of the transformer module should have chassis ground beneath it. By splitting ground

planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

- Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.6 mm (59.0 mil). This is a critical requirement needed to past FCC part 68 testing for phoneline connection. Note: For worldwide certification, a trench of 2.5 mm is required. In North America, the spacing requirements is 1.6mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5 mm spacing.

9.9.2.3. Common Physical Layout Issues

Here is a list of common physical layer design and layout mistakes in LAN* On Motherboard Designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters, the other trace must encounter the same component or a via at the same distance from the PLC.) Asymmetry can create common-mode noise and distort the waveforms.
3. Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (less than or equal to one inch).
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC) and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.
5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45/11, and the PLC.
6. Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)
7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or Application Note.
8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ-45/11 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.
9. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they have designed for 100 Ω.
   (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close† to each other the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. A 10 Ω to 15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specifications. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF (6 pF to 12 pF values have been used on past designs with reasonably good success.) These capacitors are not necessary, unless there is some overshoot in 100 Mbps mode.

Note: It is important to keep the two traces within a differential pair close† to each other. Keeping them close† helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.
†Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.008 inch to 0.012 inch trace-to-trace spacing is recommended.

9.9.3. 82562EH Home/PNA* Guidelines

For correct LAN* performance, designers must follow the general guidelines outlined in Section 9.9.2, *General LAN Routing Guidelines and Considerations*. Additional guidelines for implementing an 82562EH Home/PNA* LAN* connect component are provided below.

9.9.3.1. Power and Ground Connections

Some rules to follow for power and ground connections:

- For best performance place decoupling capacitors on the backside of the PCB directly under the 82562EH with equal distance from both pins of the capacitor to power/ground.

The analog power supply pins for 82562EH (V_{CCA}, V_{SSA}) should be isolated from the digital V_{CC} and V_{SS} through the use of ferrite beads. In addition, adequate filtering and decoupling capacitors should be provided between V_{CC} and V_{SS}, and V_{CCA} and V_{SSA} power supplies.

9.9.3.2. Guidelines for 82562EH Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the HomePNA* LAN* interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the HomePNA* LAN* circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.9.3.3. Crystals and Oscillators

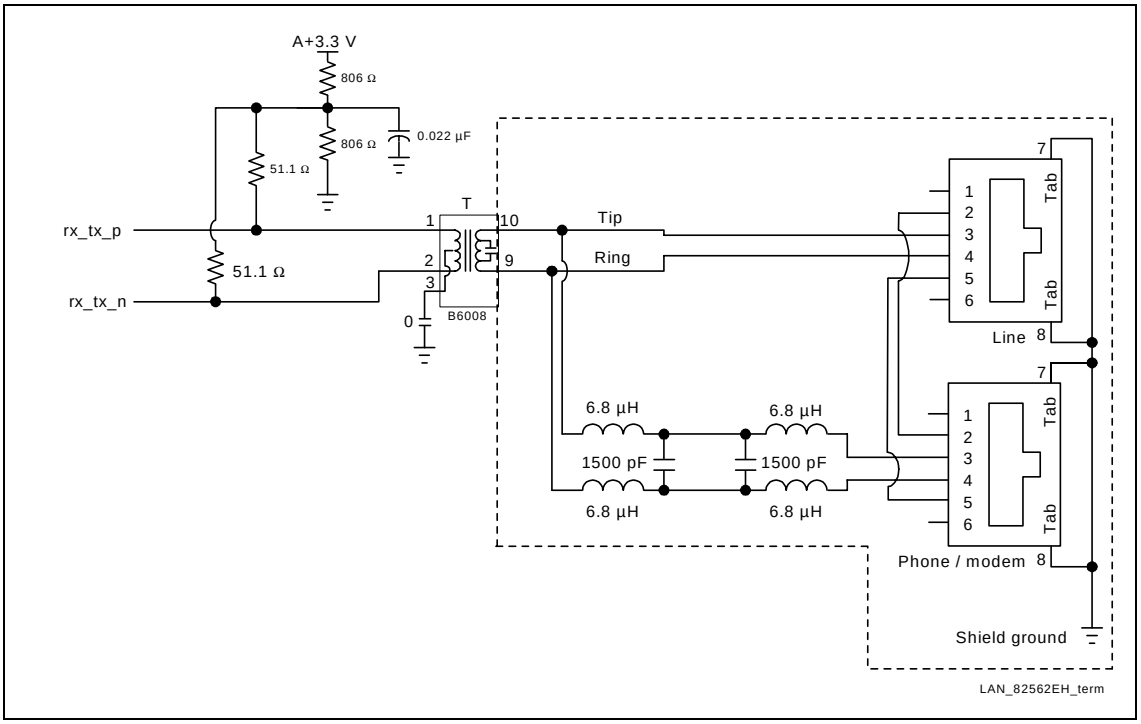
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the *HomePNA* magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise free and stable operation, place the crystal and associated discretes as close as possible to 82562EH, keeping the length as short as possible and do not route any noisy signals in this area.

9.9.3.4. Phoneline HPNA Termination

The transmit/receive differential signal pair is terminated with a pair of 51.1 Ω 1% resistors. This parallel termination should be placed close to the 82562EH. The center, common point between the 51.1 Ω resistors is connected to a pair of 806 Ω resistors and a single 0.022 µF capacitor. The opposite end of one 806 Ω resistor is tied to V_{CCA} (3.3 V), and the opposite end of the other 806 Ω resistor and the capacitor are connected to ground. The termination is shown in the following figure.

Figure 105. 82562EH Termination



The filter and magnetics component T1, integrates the required filter network, high-voltage impulse protection, and transformer to support the HomePNA* LAN* interface.

One RJ-11 jack (labeled “LINE” in allows the node to be connected to the phoneline, and the second jack (labeled “PHONE” in allows other downline devices to be connected at the same time. The second connector is not required by the *HomePNA*. However, typical PCI adapters and PC motherboard implementations are likely to include it for user convenience.

A low-pass filter, setup in-line with the second RJ-11 jack is also recommended by the HomePNA* to minimize interference between the HomeRun connection and a POTs voice or modem connection on the second jack. This places a restriction of the type of devices connected to the second jack as the pass-band of this filter is set approximately at 1.1 MHz. Refer to the HomePNA* website: www.homepna.org for up-to-date information and recommendations regarding the use of this low-pass filter to meet HomePNA* certifications.

9.9.3.5. Critical Dimensions

There are three dimensions to consider during layout. Distance “B” from the line RJ11 connector to the magnetics module, distance “C” from the phone RJ11 to the LPF (if implemented), and distance “A” from 82562EH to the magnetics module (see Figure 106).

Figure 106. Critical Dimensions for Component Placement

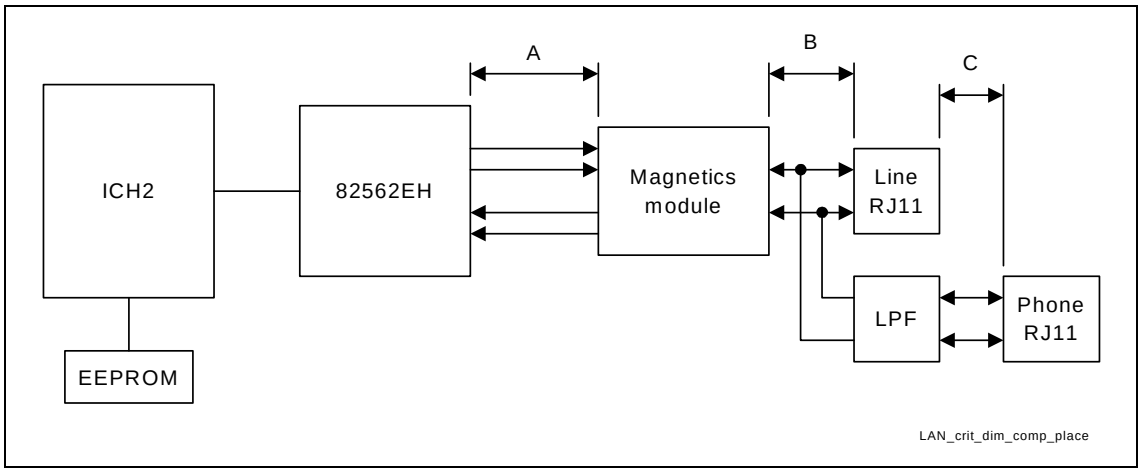


Table 40. Critical Dimension Values

Distance	Priority	Guideline
B	1	< 1 inch
A	2	< 1 inch
C	3	< 1 inch

9.9.3.5.1. Distance from Magnetics Module to Line RJ11

This distance “B” should be given highest priority and should be less then 1 inch. For trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side.

9.9.3.5.2. Distance from 82562EH to Magnetics Module

Due to the high-speed of signals present, distance “A” between the 82562EH and the magnetics should also be less than 1 inch, but should be second priority relative to distance form connects to the magnetics module.

And in general, any section of trace that is intended for use with high-speed signals should observe proper termination practices. Proper signal termination can reduce reflections caused by impedance mismatches between device and traces route. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself.

9.9.3.5.3. Distance from LPF to Phone RJ11

This distance “C” should be less then 1 inch. In regards to trace symmetry, route differential pairs with consistent separation and with exactly the same lengths and physical dimensions.

Asymmetrical and unequal length in the differential pairs contribute to common mode noise and this can degrade the receive circuit performance and contribute to radiated emissions from the transmit side

9.9.4. 82562ET / 82562EM Guidelines

For correct LAN* performance, designers must follow the general guidelines outlined in Section 9.9.2, *General LAN Routing Guidelines and Considerations*. Additional guidelines for implementing a 82562ET or 82562EM LAN* connect component are provided below.

9.9.4.1. Guidelines for 82562ET / 82562EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section will provide guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet FCC and IEEE test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN* interface is important because all other interface will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN* circuits need to be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

9.9.4.2. Crystals and Oscillators

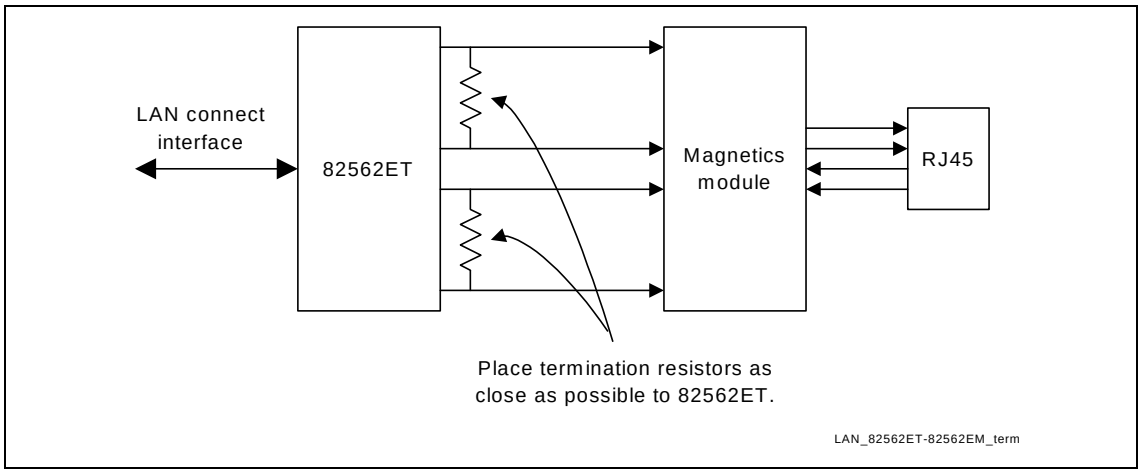
To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise-free and stable operation, place the crystal and associated discretes as close as possible to the 82562ET or 82562EM, keeping the trace length as short as possible and do not route any noisy signals in this area.

9.9.4.3. Intel® 82562ET/EM Termination Resistors

The 100 Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120 Ω (1%) receive differential pairs (RDP/RDN) should be placed as close to the LAN connect component (82562ET or 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer

Figure 107 Intel® 82562ET/EM Termination



9.9.4.4. Critical Dimensions

There are two dimensions to consider during layout. Distance “B” from the line RJ45 connector to the magnetics module and distance “A” from the 82562ET or 82562EM to the magnetics module. (See the following figure).

Figure 108. Critical Dimensions for Component Placement

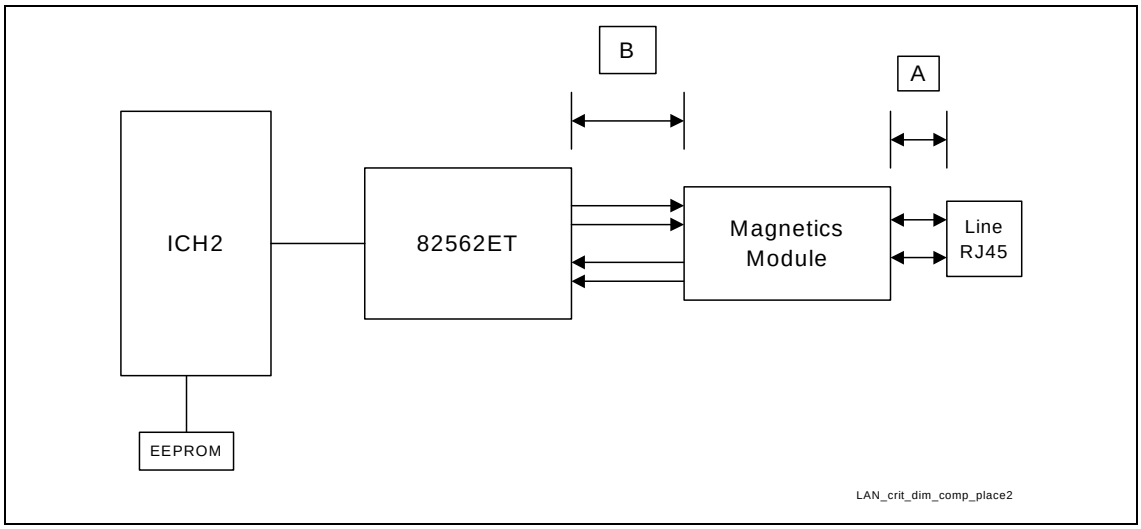


Table 41. Critical Dimension Values

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

9.9.4.4.1. Distance from Magnetics Module to RJ45

The distance "A" in Figure 108 should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation.

The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.
- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562ET must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562ET and RJ-45 will as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω–110 Ω should compensate for second order effects.

9.9.4.4.2. Distance from 82562ET to Magnetics Module

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and equal length within each differential pair.

9.9.4.5. Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because

signals with fast rise and fall times contain many high-frequency harmonics, they can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

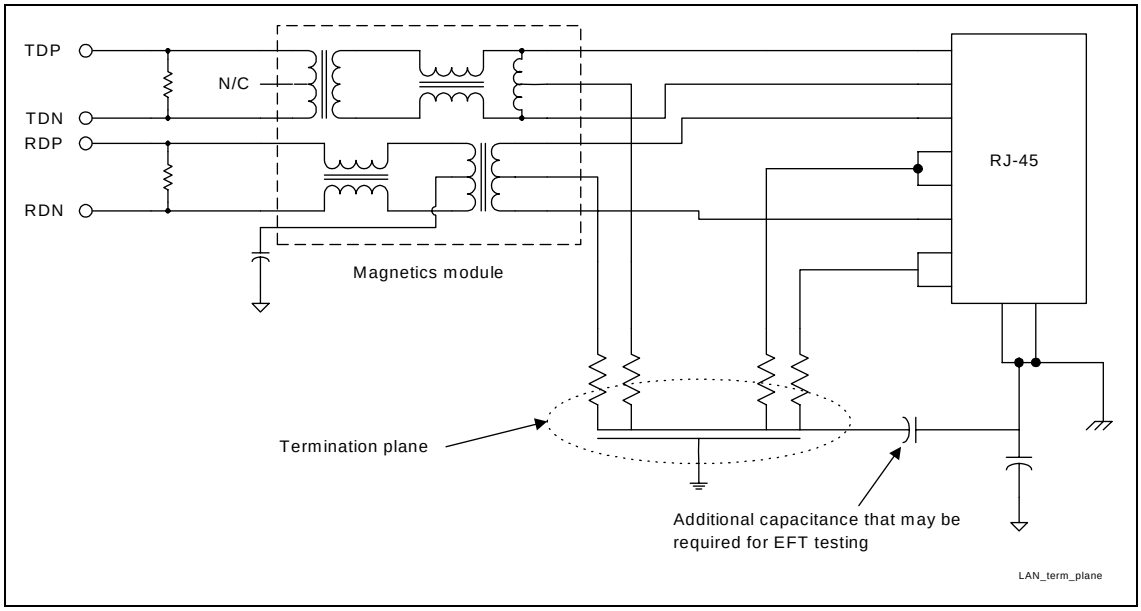
9.9.4.6. Terminating Unused Connections

In Ethernet designs it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the “Bob Smith” Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

9.9.4.6.1. Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, to meet the EFT requirements it should be rated for at least 1000 Vac.

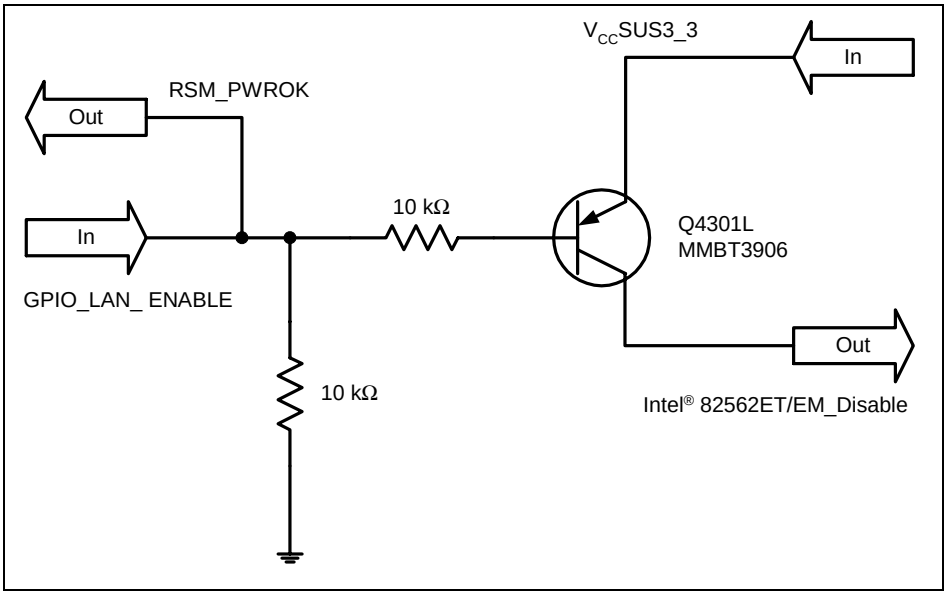
Figure 109. Termination Plane



9.9.5. Intel® 82562 ET/EM Disable Guidelines

To disable the 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. BIOS by controlling the GPIO can disable the LAN microcontroller.

Figure 110: Intel® 82562ET/EM Disable Circuit



There are 4 pins which are used to put the 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

The four control signals shown in the above table should be configured as follows: Test_En should be pulled-down thru a 100 Ω resistor. The remaining 3 control signals should each be connected thru 100 Ω series resistors to the common node “82562ET/EM_Disable” of the disable circuit.

9.9.6. 82562ET / 82562EH Dual Footprint Guidelines

These guidelines characterize the proper layout for a dual footprint solution. This configuration enables the developer to install either the 82562EH or the 82562ET/82562EM components while having only one motherboard design. The following are guidelines for the 82562ET/82562EH Dual Footprint option. The dual footprint for this particular solution uses a SSOP footprint for 82562ET and a TQFP footprint for 82562EH. The combined footprint for this configuration is shown in the following two figures.

Figure 111. Dual Footprint LAN* Connect Interface

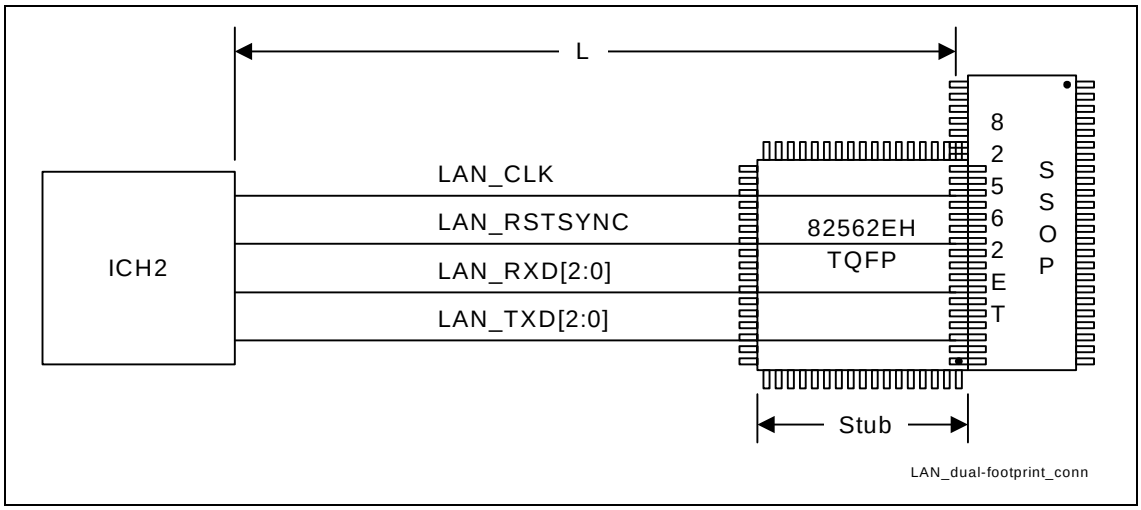
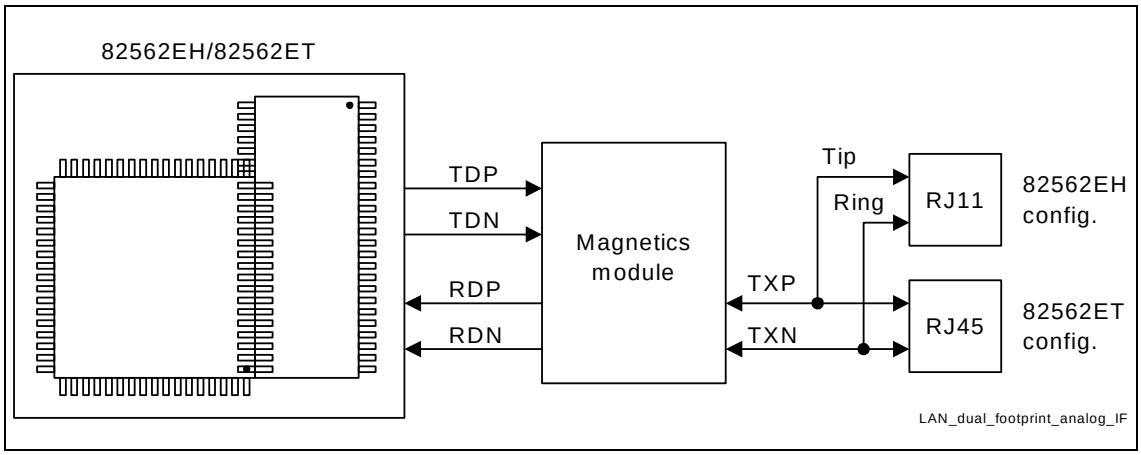


Figure 112. Dual Footprint Analog Interface



The following are additional guidelines for this configuration:

- L = 3.5 inches to 10 inches
- Stub < 0.5 inches
- Either 82562EH or 82562ET/82562EM can be installed. Not both
- 82562ET pins 28,29, and 30 overlap with 82562EH pins 17,18, and 19.
- Overlapping pins are tied to ground.
- No other signal pads should overlap or touch.
- The 82562EH and 82562ET configurations share signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD[0], LAN_TXD[0], RDP, RDN, RXP/Ring, and RXN/Tip.
- No stubs should be present when 82562ET is installed.
- Packages used for the Dual Footprint are TQFP for 82562EH and SSOP for 82562ET.
- A 22 Ω resistor can be placed at the driving side of the signal line to improve signal quality on the LAN connect interface.
- Resistor should be placed as close as possible to the component.
- Use components that can satisfy both the 82562ET and 82562EH configurations (i.e., magnetics module).
- Install components for either the 82562ET or the 82562EH configuration. Only one configuration can be installed at a time.
- Route shared signal lines such that stubs are not present or are kept to a minimum.
- Stubs may occur on shared signal lines(i.e., RDP and RDN). These stubs are due to traces routed to an uninstalled component. In an optimal layout, there should be no stubs.
- Use 0 Ω resistors to connect and disconnect circuitry not shared by both configurations. Place resistor pads along the signal line to reduce stub lengths.
- Traces from magnetics to connector must be shared and not stubbed. An RJ-11 connector that fits into the RJ-45 slot is available. Any amount of stubbing will destroy both HomePNA* and Ethernet performance.

9.10. FWH Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

9.10.1. FWH Decoupling

A 0.1 µF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7uF capacitor should be placed between the Vcc supply pins and the Vss ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the Vcc supply pins.

9.10.2. In Circuit FWH Programming

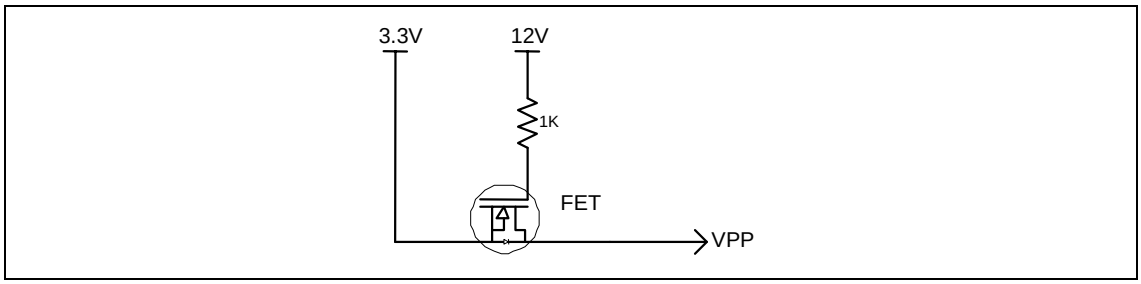
All cycles destined for the FWH will appear on PCI. The ICH2 hub interface to PCI Bridge will put all CPU boot cycles out on PCI (before sending them out on the FWH interface). If the ICH2 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from of a PCI card that positively decodes these memory cycles. In order to boot off a PCI card, it is necessary to keep the ICH2 in subtractive decode mode. If a PCI boot card is inserted and the ICH2 is programmed for positive decode, there will be two devices positively decoding the same cycle. In systems with the 82380AB (ISA bridge), it is also necessary to keep the NOGO signal asserted when booting from a PCI ROM. Note that it is not possible to boot off a ROM behind the 82380AB. Once you have booted from the PCI card, you could potentially program the FWH in circuit and program the ICH2 CMOS.

9.10.3. FWH Vpp Design Guidelines

The Vpp pin on the FWH is used for programming the flash cells. The FWH supports Vpp of 3.3V or 12V. If Vpp is 12V the flash cells will program about 50% faster than at 3.3V. However, the FWH only supports 12V Vpp for 80 hours. The 12V Vpp would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The VPP pin MUST be tied to 3.3V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 113 FWH VPP Isolation Circuitry



9.11. ICH2 Decoupling Recommendations

The ICH2 is capable of generating large current swings when switching between logic high and logic low. This condition could cause the component voltage rails to drop below specified limits. To avoid this type of situation, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in the table below to ensure the component maintains stable supply voltages. Also the capacitors should be placed as close to the package as possible. Maximum distance allowed is 400 mils. It is recommended that the motherboard designer include pads for extra decoupling caps should the recommendation not work on their board.

Table 42. Decoupling Capacitor Recommendation

Power Plane	# Decoupling Capacitors	Capacitor Value
3.3 V Core	6	0.1 µF
3.3 V Stand By	1	0.1 µF
V_{CCP}	1	0.1 µF
1.8 V Core	2	0.1 µF
1.8 V Stand By	1	0.1 µF
5 V Reference	2	0.1 µF and 1 µF
5 V Reference Stand By	1	0.1 µF

9.12. Glue Chip 3 (ICH2 Glue Chip)

To reduce the component count and BOM cost of the 850 chipset based-platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The Glue Chip 3 is designed to integrate some or all of the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Glue Chip 3 Features:

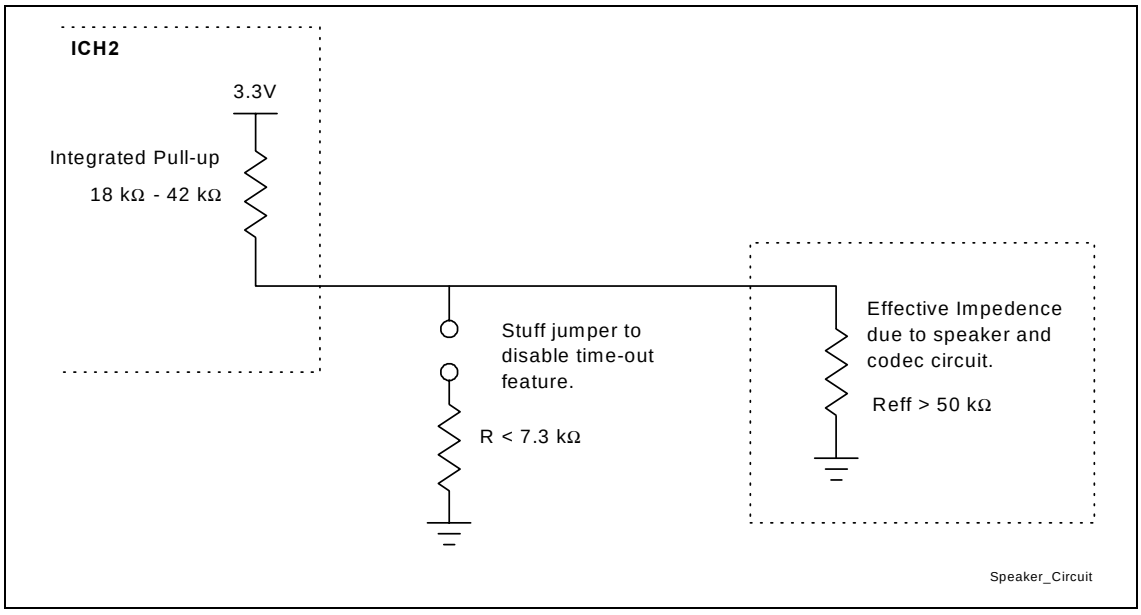
- PWROK signal generation
- Control circuitry for *Suspend To RAM*
- Power Supply power up circuitry
- RSMRST# generation
- Backfeed cutoff circuit for *Suspend to RAM*
- 5 V reference generation
- Flash FLUSH# / INIT# circuit
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- Voltage translation for Audio MIDI signal
- Audio-disable circuit
- Voltage translation for DDC to monitor
- Tri-state buffers for test

More information regarding this component is available from your field representative

9.13. SPKR Pin Consideration

The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 kΩ. Failure to due so will cause the TCO Timer Reboot function to be erroneously disabled. SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of POWEROK. When enabled, the ICH2 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-up resistor (the resistor is only enabled during boot/reset). Therefore, it is default state when the pin is a "no connect" is a logical one or enabled. To disable the feature, a jumper can be populated to pull the signal line low (see following figure). The value of the pull-down must be such that the voltage divider caused by the pull-down and integrated pull-up resistors will be read as logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or lower than the integrated pull-up resistor. It is therefore strongly recommended that the effective impedance be greater than 50 kΩ and the pull-down resistor be less than 7.3 kΩ.

Figure 114. SPKR Circuit



Note that this is not the only solution to this problem. Board designers can also isolate the load from the SPKR pin until POWEROK is in a stable high state. This would allow a weak effective load to be implemented.

9.14. 1.8 V and 3.3 V Power Sequence Requirement

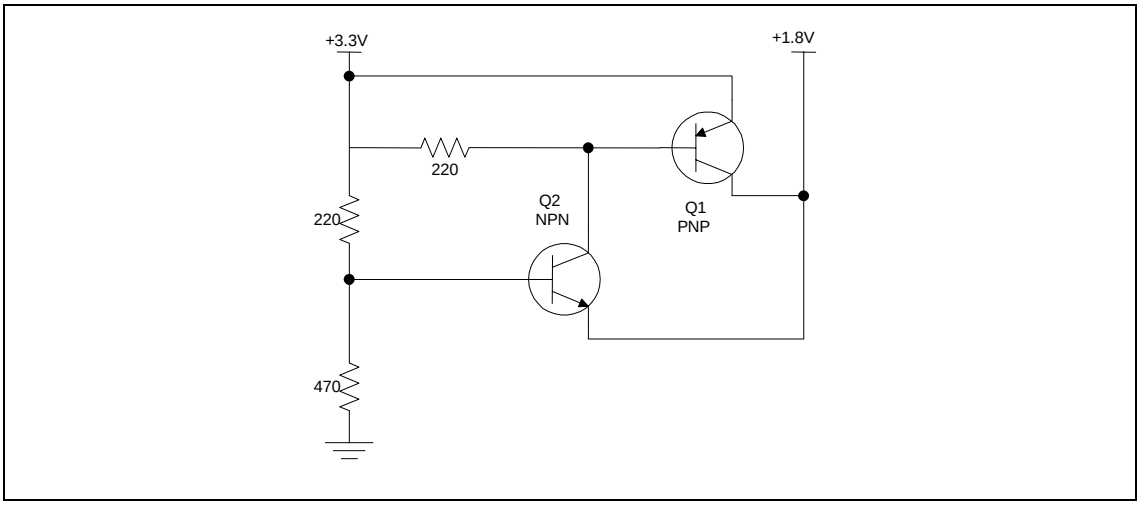
The ICH2 has two pairs of associated 1.8 V and 3.3 V supplies. These supplies are V_{CC1_8}, V_{CC3_3} and V_{CCSUS1_8}, V_{CCSUS3_3}. These pairs are assumed to power up and power down together. The difference between the two associated supplies must never be greater than 2.0 V. The 1.8 V supply may come up before the 3.3 V supply without violating this rule (though this is generally not practical in a desktop environment, since the 1.8 V supply is typically derived from the 3.3 V supply by means of a linear regulator).

One serious consequence of violation of this “2 V Rule” is electrical overstress of oxide layers, possibly resulting in component damage.

The majority of the ICH2 I/O buffers are driven by the 3.3 V supplies, but are controlled by logic that is powered by the 1.8 V supplies. If the 3.3 V supply powers up first, the I/O buffers will be in an undefined state until the 1.8 V logic is powered up. Some signals that are defined as “Input-only” actually have output buffers that are normally disabled, and the ICH2 may unexpectedly drive these signals if the 3.3 V supply is active while the 1.8 V supply is not.

Below is an example power-on sequencing circuit that ensures the 2 V Rule is obeyed. This circuit uses a NPN (Q2) and PNP (Q1) transistor to ensure the 1.8 V supply tracks the 3.3 V supply. The NPN transistor controls the current through PNP from the 3.3 V supply into the 1.8 V power plane by varying the voltage at the base of the PNP transistor. By connecting the emitter of the NPN transistor to the 1.8 V plane, current will not flow from the 3.3 V supply into 1.8 V plane when the 1.8 V plane reaches 1.8 V.

Figure 115. Example Power-On 3.3 V / 1.8 V Sequencing Circuit



When analyzing systems that may be “marginally compliant” to the 2 V Rule, pay close attention to the behavior of the ICH2's RSMRST# and PWROK signals, since these signals control internal isolation logic between the various power planes:

- RSMRST# controls isolation between the RTC well and the Resume wells.
- PWROK controls isolation between the Resume wells and Main wells
- LAN_PWROK controls isolation between the LAN* wells and the Resume wells

If one of these signals goes high while one of its associated power planes is active and the other is inactive, a leakage path will exist between the active and inactive power wells. This could result in high, possibly damaging internal currents.

9.15. PIRQ Routing

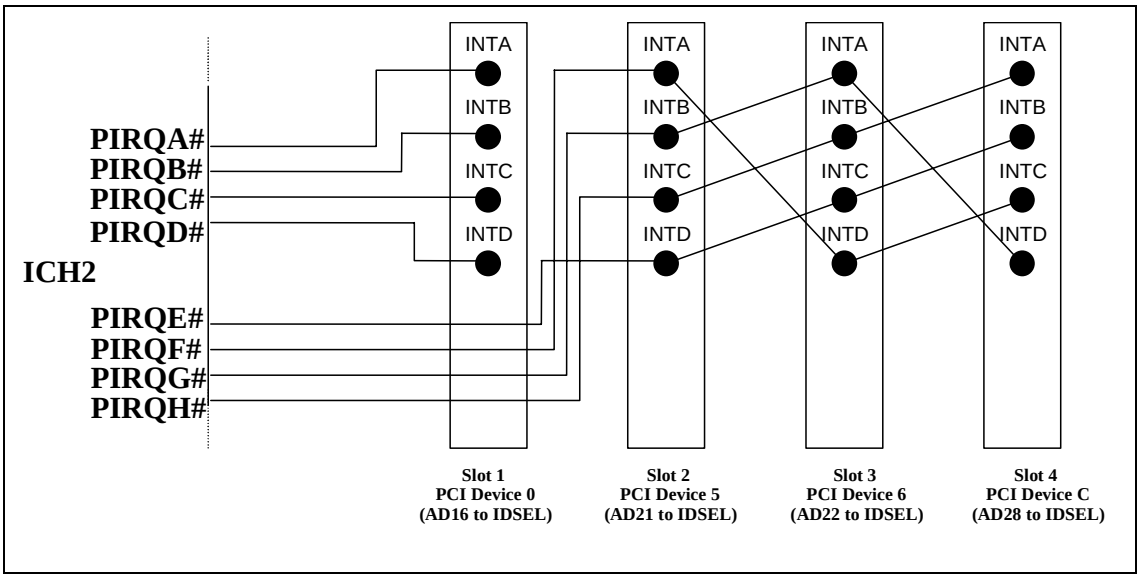
PCI interrupt request signals E-H are new to the ICH2. These signals have been added to lower the latency caused by having multiple devices on one Interrupt line. With these new signals, each PCI slot can have an individual PCI interrupt request line (Assuming that the system has four PCI slots). The following table shows how the ICH2 uses the PCI IRQ when the IOAPIC is active.

Table 43. IOAPIC Interrupt Inputs 16 Through 23 Usage

No	IOAPIC INTIN Pin	Function in ICH2 using the PCI IRQ in IOAPIC
1	IOAPIC INTIN PIN 16 (PIRQA)	
2	IOAPIC INTIN PIN 17 (PIRQB)	AC ’97, Modem and SMBUS
3	IOAPIC INTIN PIN 18 (PIRQC)	
4	IOAPIC INTIN PIN 19 (PIRQD)	USB Controller #1
5	IOAPIC INTIN PIN 20 (PIRQE)	Internal LAN* Device
6	IOAPIC INTIN PIN 21 (PIRQF)	
7	IOAPIC INTIN PIN 22 (PIRQG)	
8	IOAPIC INTIN PIN 23 (PIRQH)	USB Controller #2 (starting from ICH2 B0 silicon)

Interrupts B, D, E, and H service devices internal to the ICH2. Interrupts A, C, F, and G are not used and can be used by PCI slots. The figure below shows an example of IRQ line routing to the PCI slots.

Figure 116. Example PCI IRQ Routing



The PCI IRQ Routing shown in the above figure allows the ICH2 internal functions to have a dedicated IRQ(Assuming add-in cards are single function devices and use INTA). If a P2P bridge card or a multifunction device uses more than one INTn# pin on the ICH2 PCI Bus, the ICH2 internal functions will start sharing IRQs.

The above figure is an example. It is up to the board designer to route these signals in a way that is the most efficient for their particular system. A PCI slot can be routed to share interrupts with any of the ICH2's internal device/functions.

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10. Additional Design Considerations

This chapter describes system design considerations not addressed in previous chapters.

10.1. Retention Mechanism Placement and Keepouts

The retention mechanism requires two keepout zones, one for the EMI ground pads and another for a limited component height area under the retention mechanism as shown in the following figure shows the relationship between the retention mechanism mounting holes and pin one of the socket. In addition it also documents the ground pads and keepouts.

The retention holes should be a non-plated hole.

Figure 117. RM Outline

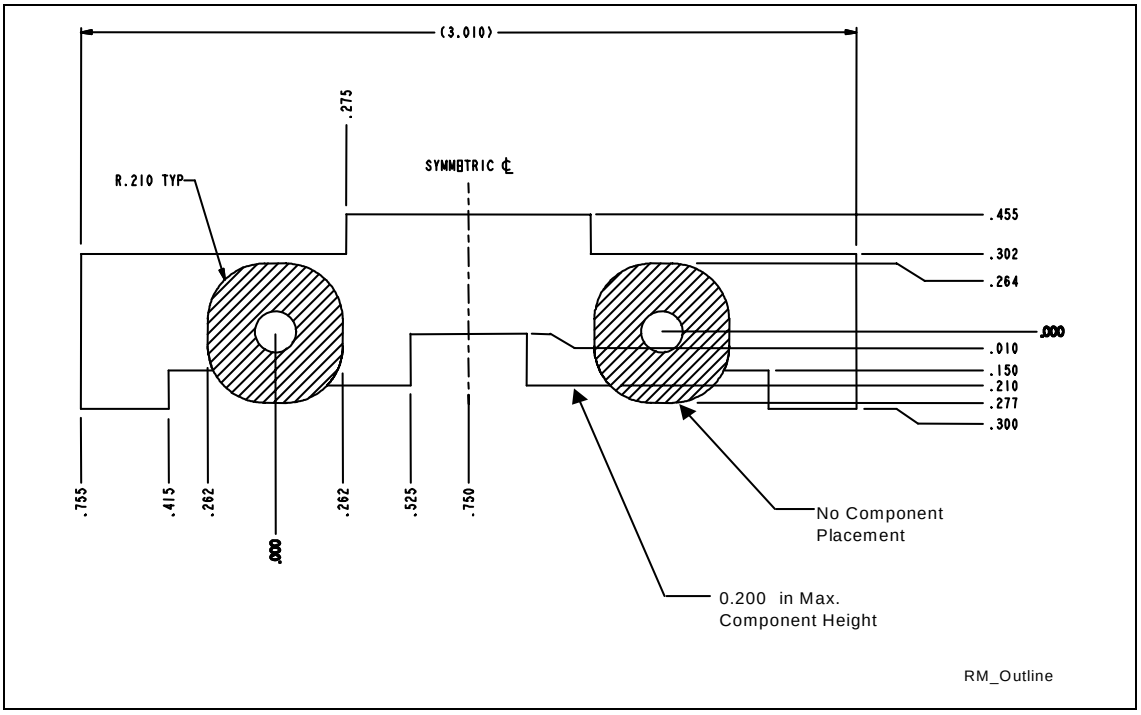
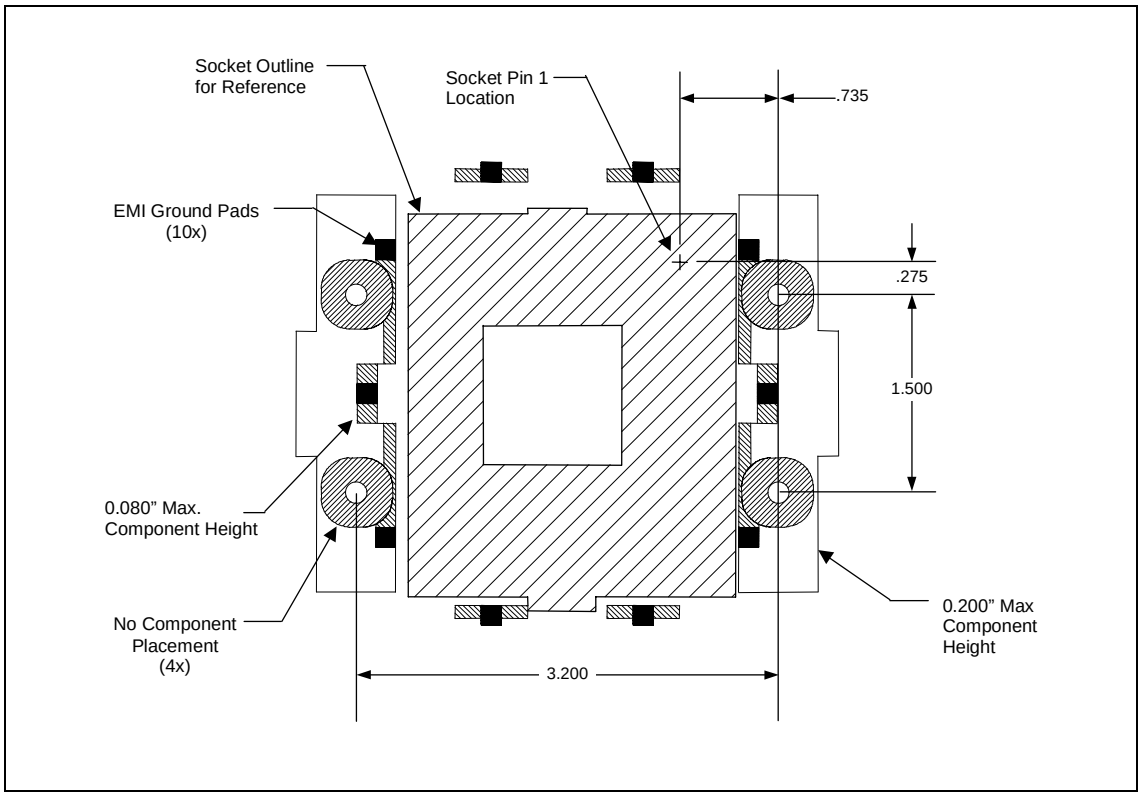


Figure 118. RM Placement Relative to the Socket and Keepout Overview



10.2. Power Header for Active Cooling Solutions

The reference-design heatsink includes an integrated fan. The recommended connector for the active cooling solution will be an AMP* 643815-3 or equivalent.

A tachometer output feature is specified for the fan on the enabled design. This feature allows the system design to detect a failure and take corrective action. The sense line needs to be an open collector (pulled up to 5.0 V with a 10 kΩ resistor). The sensor output is 2 pulses per revolution.

The fan connector pinout is described in the following table.

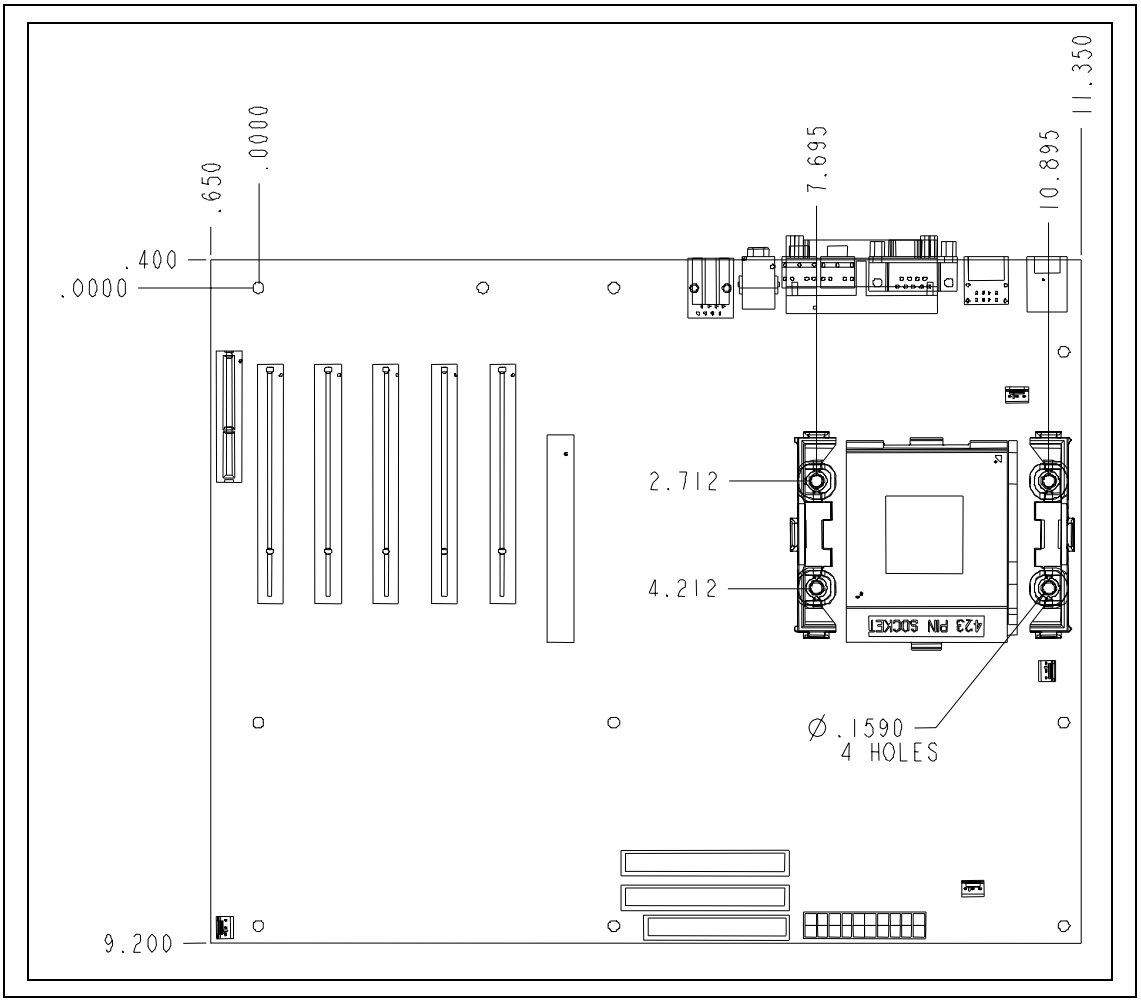
Table 44. Fan Power Header Pinout

Pin Number	Signal
1	Ground
2	+12 V
3	Tachometer Output

10.3. Additional Information for Heatsink Support

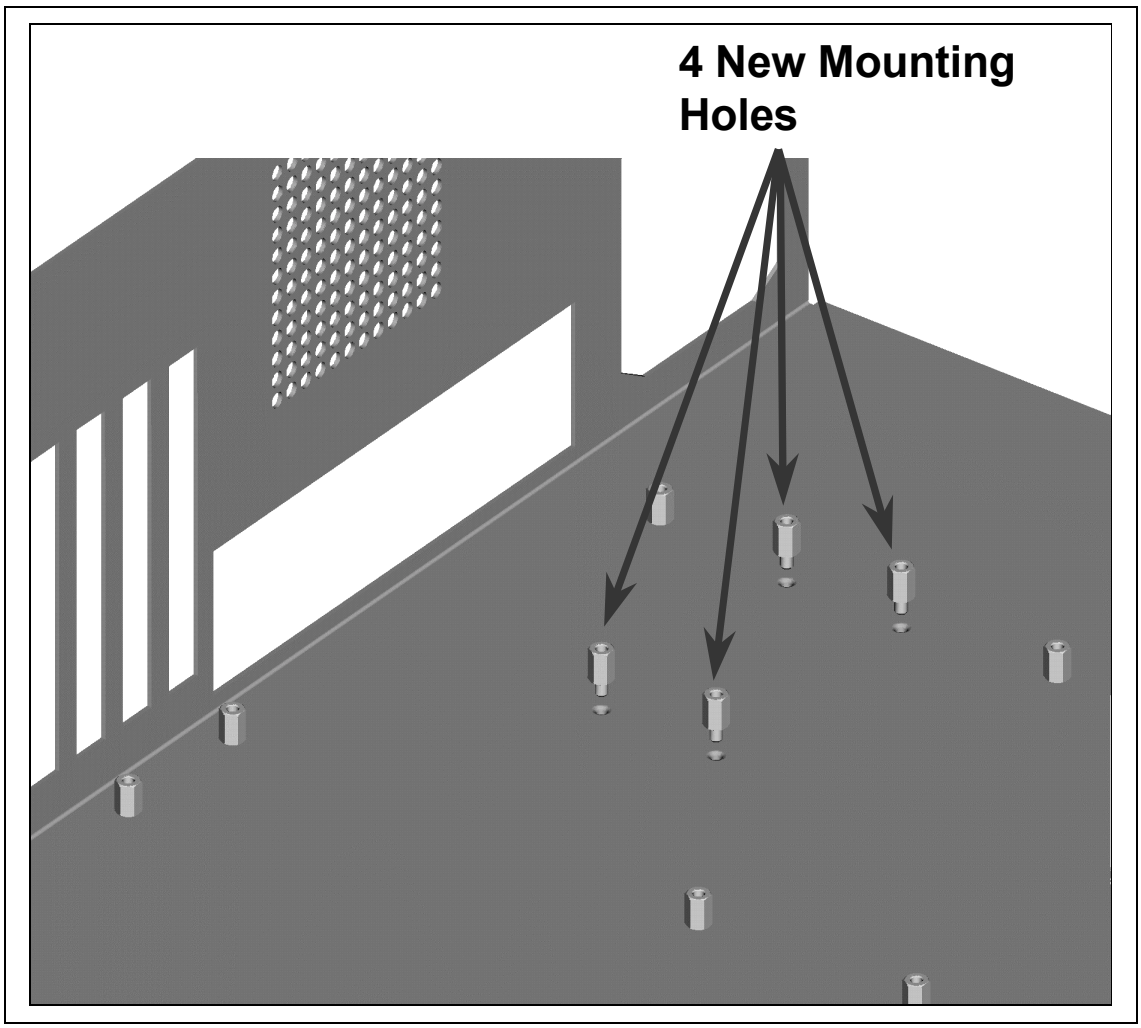
Pentium 4 processor and 850 ATX motherboard designs require additional support for larger mass heatsinks. The solution is to add 4 additional mounting holes to the chassis and mount the motherboard and the processor retention module directly to the chassis. To maintain compatibility with enabled chassis, a common retention module location is required for all motherboards. The following figure illustrates the location of the retention module with respect to the chassis mounting holes.

Figure 119. Fixed Retention Module Location for Direct Chassis Attach



Chassis enabled for this solution have four additional mounting holes as shown in the following figure:

Figure 120. Enabled Chassis Solution

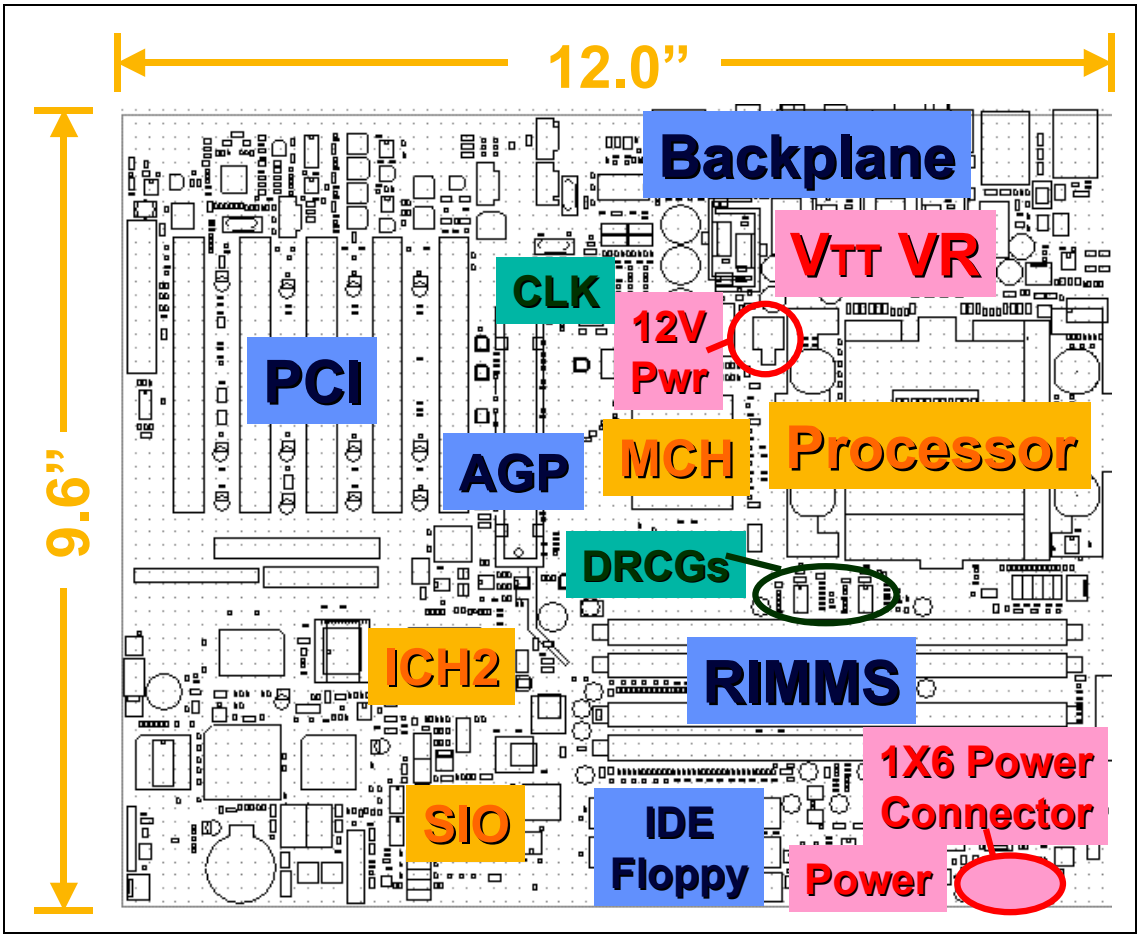


10.4. Typical Power Distribution

DC output power requirements and distributions will vary widely based on specific system options and implementation. Significant dependencies include the quantity and types of processors, memory, add-in card slots, and peripheral bays, as well as support for advanced graphics or other features. **It is ultimately the responsibility of the designer to derive a power budget for a given target product and market.**

Motherboard designs that powers the 2.5 V RDRAM core and 1.8 V 82850 MCH core from the 3.3 V rail may require more than 18 Amps of current from the 3.3 V rail. If the design requires more than 18 Amps from the 3.3 V rail, it is recommended to add ATX/ATX12V 1x6 auxiliary power connector for the additional current on the 3.3 V rail. With the additional 1x6 auxiliary power connector, the current is increased from 18 A to 28 A on the 3.3 V rail. The following figure illustrates the additional 1x6 power connector on the 850 chipset Customer Reference Board.

Figure 121. Intel® 850 Chipset CRB with Additional 1x6 Auxiliary Power Connector



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11. Intel® Pentium® 4 Processor Power Distribution Guidelines

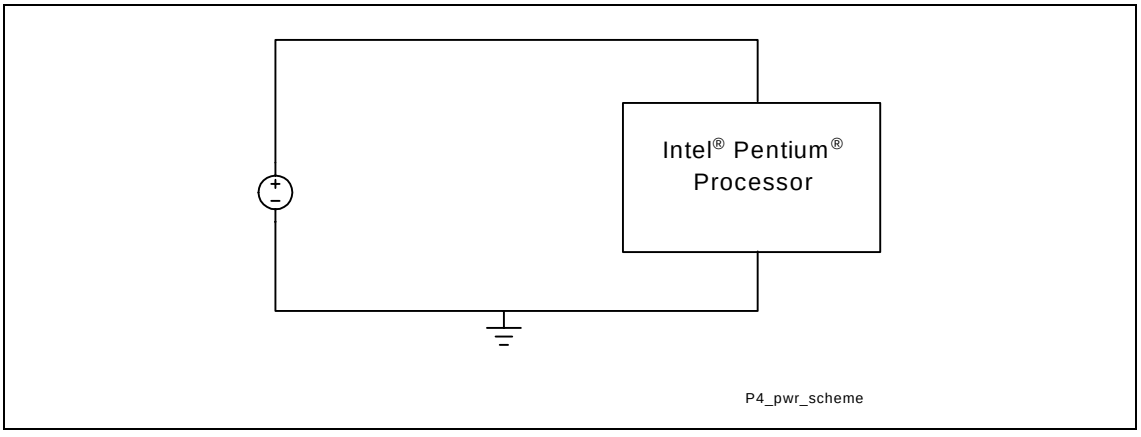
Pentium 4 processors have unique requirements for voltages supplied to them. Unlike previous Intel processors, the Pentium 4 processor's AGTL+ termination and the processor core are being powered from the same voltage supply creating a high demand on the processor core power supply.

The intent of this chapter is to familiarize the reader with the power requirements of the Pentium 4 processor and to show simulation model and power implementation techniques. Only specific power distribution and control issues pertaining to Pentium 4 processors are discussed in this document. It is assumed the reader is familiar with power distribution issues of other Intel processors.

11.1. Typical Power Delivery

Power distribution is generally thought of as *supplying power to the components that require it*. Digital designers want their logic to see power sources approximating an ideal supply. The printed circuit board (PCB) designers attempt to create this ideal supply with two power planes in the PCB or by using large width traces to distribute power. High frequency noise created when logic gates switch is typically controlled with high frequency ceramic capacitors, which are recharged from lower frequency bulk capacitors. Pentium 4 processor-based designs will require major changes in the amount, type, and placement of capacitance, compared with prior processor generations. Figure 122 shows the ideal power model. However, more realistic power distribution schemes appear in Figure 123 and Figure 124.

Figure 122. Ideal Intel® Pentium® 4 Processor Power Supply Scheme



The Pentium 4 processor voltage regulator will supply power to the processor core. Unlike previous Intel processors, AGTL+ termination for most signals is provided on the processor silicon (on-die termination). This termination is pulled to V_{CC} on the processor silicon eliminating the need for a separate voltage regulator for AGTL+ termination. Signals not terminated on die may need to be pulled to V_{CC} on the system board. Refer to the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet for details on on-die termination. Intel chipsets will also provide on-die termination eliminating the need to terminate most bus signals on the system board. The power rail for the chipset on-die termination

voltage may also use the processor's voltage regulator so that a second voltage regulator for the chipset AGTL+ termination voltage is not required.

To completely model the system board system, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 123 and Figure 124.

Figure 123. Detailed Power Distribution Model for System with Voltage Regulator Module

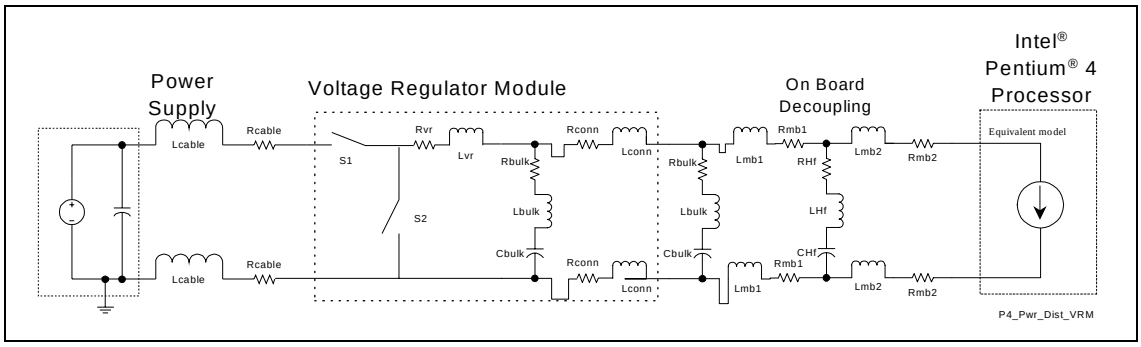
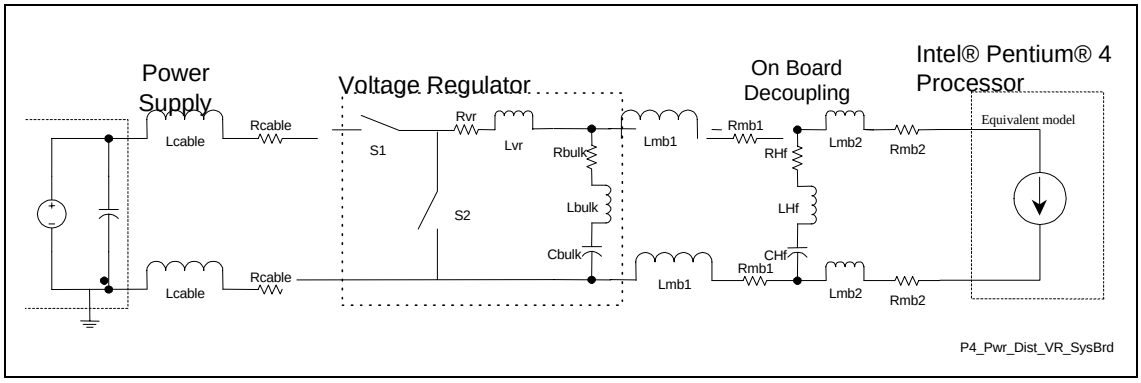


Figure 124. Detailed Power Distribution Model for System with Voltage Regulator on System Board



Section 11.6 includes summary of models for several high frequency and bulk capacitors. The following table lists model parameters for the system board and VRM 9.0 connector shown in Figure 123.

Table 45. Intel® Pentium® 4 Processor Power Delivery Model Parameters

Supply	VRM Connector Inductance	VRM Connector Resistance	System Board Inductance		System Board Resistance	
	L_{conn}	R_{conn}	L_{mb1}	L_{mb2}	R_{mb1}	R_{mb2}
V_{CC}	0.314 nH	0.236 mΩ	21 pH	19 pH	0.094 mΩ	0.086 mΩ

11.2. Intel® Pentium® 4 Processor Power Requirements

This section describes the issues related to supplying power to a Pentium 4 processor. For detailed electrical specifications, refer to the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet. Pentium 4 processors will typically operate at 1.7 V maximum. The processor allows the use of Auto HALT, Stop-Grant, Sleep, and Deep Sleep states to reduce power consumption by stopping the clock to specific internal sections of the processor and the BCLK depending on each particular state. This can create load-change transients with rates as high as 385 A/µS on V_{CC}. Note that Pentium 4 processors can also cause load changes of this magnitude while executing regular code. In this document, a load-change transient is a change from one current requirement (averaged over many clocks) to another. Future Pentium 4 processors may require higher currents and different voltages.

11.2.1. Voltage Tolerance

Refer to the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet for voltage tolerance specifications. Failure to meet the specifications on the low-end tolerance results in transistors slowing down and not meeting timing specifications. Not meeting the specifications on the high-end tolerance can cause damage or reduce the life of the processor.

Unlike previous Intel processors, the Pentium 4 processor specifications for V_{CC} and I_{CC} are not independent. The processor should not be subjected to any static V_{CC} and I_{CC} combination wherein V_{CC} exceeds $V_{CC\_MID} + 0.2 * (1- I_{CC}/I_{CC\_MAX})$, where V_{CC_MID} is defined as $(V_{CC\_MAX}+V_{CC\_MIN})/2$.

11.2.2. Processor Voltages

The VRM 9.0, which provides V_{cc} supply to the Pentium 4 processor, has the capability of supplying voltages from +1.10 V to +1.85 V. Typical Pentium 4 processor V_{CC_MAX} is 1.7 V. V_{CC} supplies power to the processor core and on-die termination voltage used for the AGTL+ bus. The VRM 9.0 can provide adequate power to support the FMB2 of Pentium 4 processors. Refer to *VRM 9.0 DC-DC Converter Design Guidelines* document for details.

$V_{CCIOPLL,}$ V_{CCA} and V_{SSA} are the power supplies to the internal PLL. $V_{CCIOPLL,}$ V_{CCA} and V_{SSA} must be connected to V_{CC} through a discrete RLC filter as described in Section 11.4. Refer to the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet for the location of these pins.

11.3. Meeting Intel® Pentium® 4 Processor Power Requirements

Intel recommends using a VRM 9.0-compliant regulator for Pentium 4 processor system board designs. A VRM 9.0-compliant regulator may be integrated as part of the system board or on a module. The system board designer should properly place high frequency and bulk-decoupling capacitors as needed between the VRM and Pentium 4 processor to ensure voltage fluctuations remain within the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet specifications. See Section 11.4 for recommendations on the amount of decoupling needed.

Pentium 4 processor power supply design requires tradeoffs between power supply, distribution, and decoupling technologies. This section discusses how to do a step-by-step design of a system using the more accurate power distribution model shown in Figure 123.

11.3.1. Voltage Budgeting

Before beginning the design of a power distribution system, one must have an idea of how to budget the tolerance specifications at different points in the system. This provides a target for component and board layout and helps reduce iterations to reach a solution. The following table shows estimations of the factors that system designers need to consider when calculating AC voltage tolerance budgets. The following table also lists the tolerable voltage fluctuations at VR/VRM output and at processor socket pins.

Table 46. Voltage Budget Factors

Frequency (GHz)	Processor Current (A)	ΔV@ VR(M) Output (mV)	Max di/dt @ VR(M) Output (A/µs)	ΔV @ Processor SENSE pins (mV)	ΔV @ Socket pin (mV)	Max di/dt @ Socket pin (A/µs)
1.30	38.1	-101/+0	16	-135/+0	-113/+0	260
1.40	40.6	-104/+0	23	-140/+0	-116/+0	275
1.50	43.0	-107/+0	30	-145/+0	-120/+0	295
Flexible Motherboard (FMB) 2	52.7	-124/+0	50	-170/+0	-139/+0	385

NOTES:
1. FMB2 is for use by systems intending to support the Pentium 4 processor into the first part of the year 2001.
2. The values in this table are provided as reference. In the event that this information conflicts with the *Intel® Pentium® 4 Processor in the 423 Package* datasheet, the values in the datasheet should be considered the official specifications.

Note that as the processor frequency increases the processor current increases and the processor voltage minimum reduces. Relaxing the voltage tolerance helps the system designer to achieve a flexible motherboard design solution for all different frequencies of the Pentium 4 processor. Failure to use the voltage budgets from the Flexible Motherboard row of Table 46 when modeling the system power delivery may result in a system that is not upgradeable.

The shape of the transient current through the processor socket and VRM connectors usually does not have a constant di/dt slope due to the high frequency filtering by the package decoupling. The historical method of specifying the max di/dt value for the processor does not give adequate information in describing the transient current profile. Specifying one value exaggerates the speed of the current transient and can lead to over-design. Intel now provides piecewise-linear (PWL) approximations to specify the transient current allowing the system board and VRM designer to optimize their decoupling solutions.

Figure 123 shows the transient response at the socket pins for the Pentium 4 processor. Table 47 contains the PWL at the socket pins. Figure 126 shows the transient response at the VRM 9.0 connector. Table 48 contains the PWL at the VRM 9.0 connector.

Table 47. Piecewise-Linear (PWL) Approximations at the Intel® Pentium® 4 Processor Socket Pins

1.30 GHz		1.40 GHz		1.50 GHz		FMB2	
Time [ns]	Current	Time [ns]	Current	Time [ns]	Current	Time [ns]	Current
0	5.4	0	5.4	0	5.4	0	5.3
33	11.3	34	11.7	35	12.1	38	13.8
123	37.3	126	39.8	129	42.1	142	51.6
163	44.3	167	47.3	171	50.1	188	61.7
193	46.5	198	49.6	203	52.7	223	64.9
238	45.2	244	48.2	250	51.1	275	62.9
363	33.9	372	36.1	382	38.2	419	46.6
413	31.3	424	33.2	434	35.1	477	42.8
463	32.1	475	34.2	487	36.1	534	44.1
613	38.1	629	40.6	644	43.0	707	52.7
1000	38.1	1000	40.6	1000	43	1000	52.7

Table 48. Piecewise-linear (PWL) Approximations at the VRM 9.0 Connector

Time [us]	Current
0	5.3
1	51
1.31	58.9
1.59	61.1
1.87	58.9
2.71	47.7
3.15	46.7
4.75	52.7
10	52.7

Figure 125. Socket di/dt

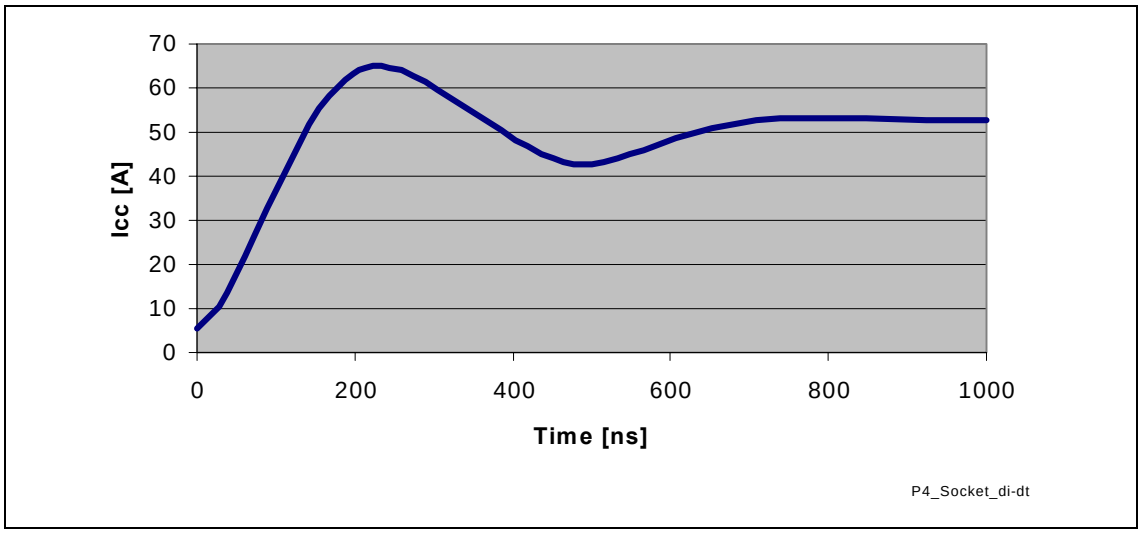
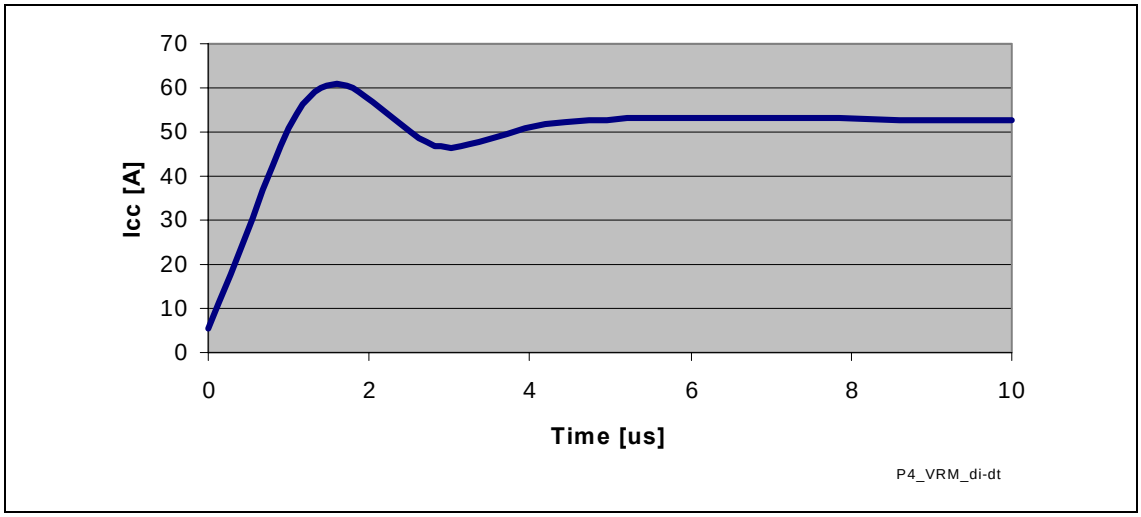


Figure 126. VRM 9.0 di/dt



11.3.2. Supplying Power

The Pentium 4 processor **requires** local regulation due to its higher current requirements, and to maintain power supply tolerance. For example, a local DC-to-DC converter converts a higher DC voltage to a lower level using either a linear or a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R). More importantly however, a discrete regulator regulates the voltage locally, which minimizes DC line losses by eliminating R_{CABLE} and reducing R_{BOARD} on the processor voltage.

11.3.3. Decoupling Technology and Transient Response

The inductance of the system due to cables and power planes slows the power supply's ability to respond quickly to a current transient. Decoupling a power plane can be broken into several independent parts. The closer to the load the capacitor is placed, the more inductance is bypassed. By bypassing the inductance of leads, power planes, etc., less capacitance is required. However, areas closer to the load have less room for capacitance. Therefore, tradeoffs must be made.

The Pentium 4 processor causes very large switching transients. These sharp surges of current occur at the transition between low power states and the normal state. It is the responsibility of the system designer to provide adequate high frequency decoupling to manage the highest frequency components of the current transients. Larger bulk storage (C_{BULK}), e.g., electrolytic capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition.

All of this power bypassing is required due to the relatively slow speed at which a DC-to-DC converter can react. A typical voltage converter has a reaction time on the order of 1 to 100 µs while the processor's current steps are on the order of 30 to 40 ns. Bulk capacitance supplies energy from the time the high frequency decoupling capacitors are drained until the power supply can react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate at which it can respond, while the high-frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate that they can supply.

A load-change transient occurs when coming out of or entering a low power mode. For Pentium 4 processors, this load-change transient can be on the order of 40 amps. These are not only quick changes in current demand, but also long lasting average current requirements. This occurs when the STPCLK# pin is asserted or de-asserted, during AutoHALT, and thermal throttling. AutoHALT is a low power state that the processor enters when the HALT op-code is executed. Note that even during normal operation (not STPCLK# or AutoHALT), the processor current requirements can change by as much as 70% ±10% of the maximum current very quickly.

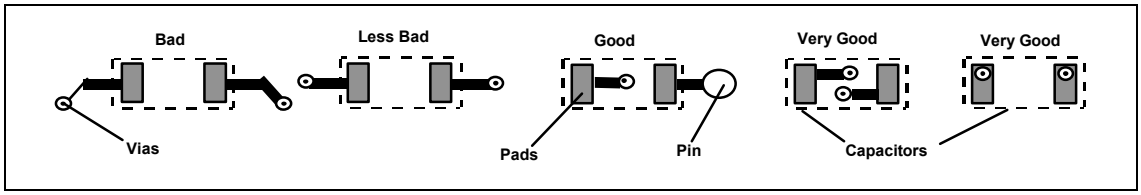
Maintaining voltage tolerance during these changes in current requires high-density bulk capacitors with low Effective Series Resistance (ESR) and low Effective Series Inductance (ESL). Use thorough analysis when choosing these components.

11.3.3.1. Location of High Frequency Decoupling

A system designer for Pentium 4 processors should properly design for high frequency decoupling. High frequency decoupling should be placed as close to the power pins of the processor as physically possible. Use both sides of the board if necessary for placing components in order to achieve the optimum proximity to the power pins. This is vital as the inductance of the board's metal plane layers could cancel the usefulness of these low inductance components.

Another method to lower the inductance is to shorten the path from the capacitor pads to the pins that it is decoupling. If possible, place the vias connecting to the planes within the pad of the capacitor. If this is not possible, keep the traces as short and wide as feasible. Possibly one or both ends of the capacitor can be connected directly to the pin of the processor without the use of a via. Even if simulation results look good, these practical suggestions can be used to create an even better decoupling situation where they can be applied in layout. The following figure illustrates these concepts.

Figure 127. 1206 Capacitor Pad and Via Layouts



11.3.3.2. Location of Bulk Decoupling

The location of bulk capacitance is not as critical as high frequency decoupling since more inductance is already expected for these components. However, knowing their location and the inductance values involved will be useful for simulation. In addition to the bulk capacitors on the VRM9.0, which are electrically *behind* the inductance of the converter pins, several bulk capacitors need to be placed close to the processor socket.

11.3.4. Sheet Inductance/Resistance and EMI Emission Effects of Power Plane

The imperfections of the power planes themselves may introduce unwanted resistance and inductance into the power distribution system. The complex models in Figure 123 and Figure 124 refer to these imperfections as R_{mb1}, R_{mb2}, L_{mb1}, and L_{mb2}.

Assuming layer thickness is smaller than skin depth, the metal layer resistance can be calculated using the following equation.

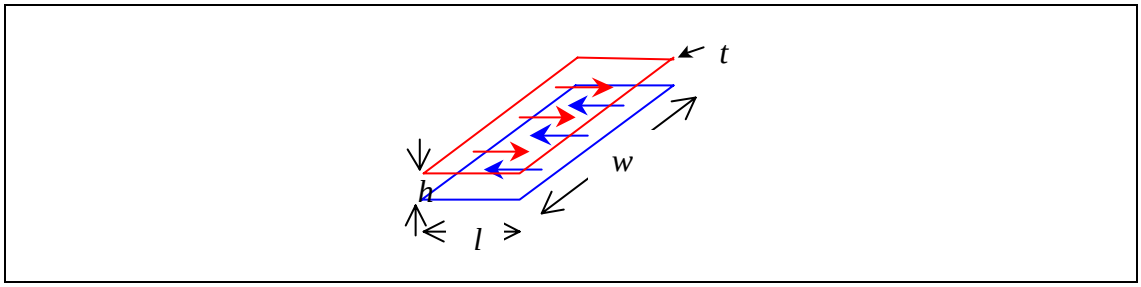
Equation 9. Layer Metal Resistance

$$R = \rho \cdot \frac{l}{w \cdot t},$$

where:

— ρ is the copper resistivity (ρ = 0.667 mΩ·mil),
— l, w, and t are the length, width, and layer thickness, respectively.

Figure 128. Diagram for Calculating Loop Inductance



The loop inductance can be calculated as using the following equation.

Equation 10. Loop Inductance

$$L = 31.9\frac{\text{pH}}{\text{mil}} \cdot \frac{l \cdot h}{w \cdot (N-1)}$$

where:

— N is the number of V_{CC}/V_{SS} planes and *h* is the layer spacing.

To minimize parasitic layer inductance, it is important to reduce the distance from decoupling capacitors to the processor socket (reducing *l*) and to use islands for power distribution (increasing *w*). To reduce *h*, the designer should interleave the V_{CC}/V_{SS} planes in the layer stack up. Since large distances separate the V_{CC} and V_{SS} planes in standard four and six layer stack-ups, it is recommended to reserve the top layer in the voltage regulator area for V_{CC}/V_{SS} routing. As a practical matter it is impossible to get the requisite L_{mb1} and L_{mb2} without locally dedicating at least four planes to carry power from the system board capacitors to the power pins of the processor.

There are impedance consequences for signals that cross over or under the edges of the power island that exists on another layer. There are two reasonable options to consider which can protect a system from these consequences.

Pentium 4 processor power islands can be isolated from signals by one of the solid power plane layers such as the ground layer. This forces a particular stack-up model.

Another option that helps, but does not completely eliminate radiation effects, is to decouple the edges of the processor power islands to ground on regular intervals of about 1 inch using good high frequency decoupling capacitors (1206 packages). This requires more components but does not require any particular board stack-up.

In either event, for controlling emissions and differential-mode noise, all planes and islands should be well decoupled. The amount of decoupling required for controlling emissions will be determined by the exact board layout, and the chassis design. One should plan ahead by allowing additional pads for capacitors to be added in case they are found to be necessary during EMI testing.

11.3.5. Generating and Distributing GTLREF[3:0]

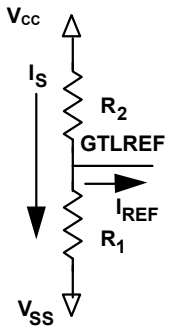
GTLREF[3:0] are low current inputs (less than 15 µA each) to the differential receivers within each of the components on the AGTL+ bus. A simple voltage divider can generate the GTLREF[3:0] inputs. The GTLREF[3:0] inputs need to meet the 2% tolerance specification.

Equation 11 uses $R_1 = 2 \times R_2$ to generate a GTLREF set at a nominal value of 2/3 V_{cc}. Figure 127 illustrates using 1% resistors to generate the GTLREF specification of 2/3 V_{cc} ± 2%.

Equation 11. Creating GTLREF of 2/3 V_{cc}

$$GTLREF = V_{CC} \times \frac{R_1}{R_1 + R_2} = V_{CC} \times \frac{2 \times R_2}{2 \times R_2 + R_2} = \tfrac{2}{3} V_{CC}$$

Figure 129. GTLREF



R_1 = 100 Ω and R_2 = 50 Ω

R_1 and R_2 should be small enough values that the current drawn by the GTLREF inputs (I_{REF}) is negligible versus the current caused by R_2 and R_1.

A complete analysis of this circuit's currents into and out of the center node, as in Equation 12, will provide the final GTLREF of the circuit where *n* is the number of I_{REF} inputs supplied by the divider.

Equation 12. Node Analysis

$$I(R_2) = I(R_1) + n \times I_{REF}$$

Plugging in for the currents and rearranging gives:

Equation 13. Node Analysis in Terms of Voltage

$$\frac{V_{CC} - GTLREF}{R_2} - \frac{GTLREF}{R_1} = n \times I_{REF}$$

Which leads to the following equation:

Equation 14. Solving for GTLREF

$$GTLREF = \frac{V_{CC}/R_2 - n \times I_{REF}}{1/R_2 + 1/R_1}$$

The worst-case GTLREF should be analyzed with I_{REF} at the maximum and minimum values determined for the number of loads being supplied. If the number of loads can change from model to model because of upgrades, this should be taken into account as well. Analyze Equation 14 with R_1 and R_2 at the extremes of their tolerance specifications.

11.4. Recommendations

Intel recommends using simulation to design and verify Pentium 4 processor based systems. With the above estimates, a model of the power source, and the power delivery model of the Pentium 4 processor provided in Section 11.8, system developers can begin analog modeling. This section contains Intel recommended starting points.

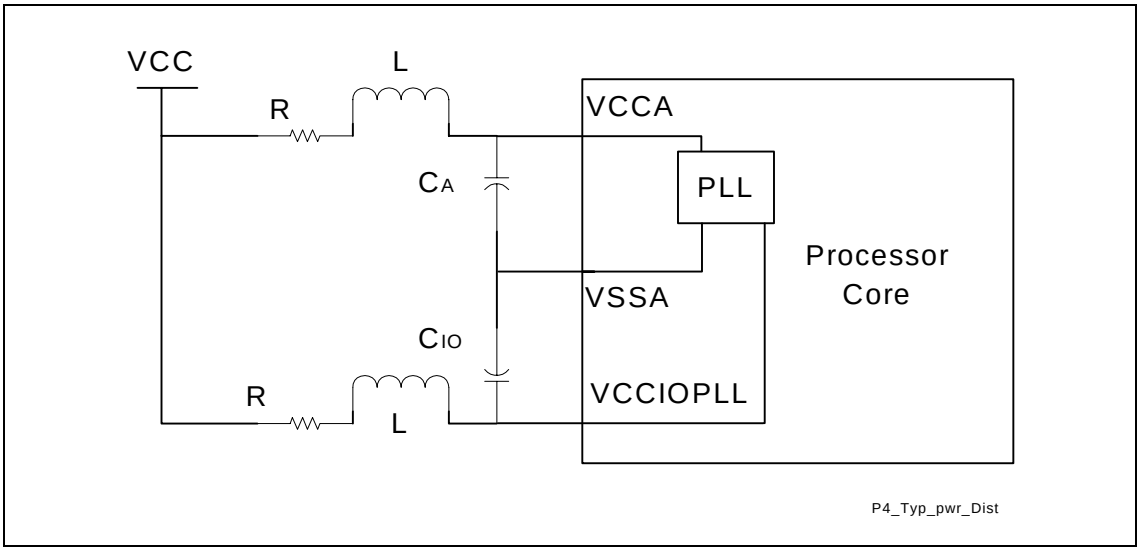
11.4.1. V_{CC_CPU}

Intel recommends using a local Voltage Regulator DC-to-DC converter for V_{cc}. These regulators should be capable of accepting a 5-bit V_{ID} code used to indicate the voltage required by the individual processor unit. Refer to the *VRM 9.0 DC-DC Converter Design Guidelines* and *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet for actual specifications. Note that Intel further recommends proper design of the system board bulk and high frequency decoupling as well as layout to meet the transient tolerance at the processor socket pins.

11.4.2. Filter Specifications for V_{CCA}, $V_{CCIOPLL}$, and V_{SSA}

V_{CCA} and $V_{CCIOPLL}$ are power sources required by the PLL clock generators on the Pentium 4 processor silicon. Since these PLLs are analog in nature they require quiet power supplies for minimum jitter. Jitter is detrimental to the system: it degrades external I/O timings as well as internal core timings (i.e., maximum frequency). To prevent this degradation these supplies must be low pass filtered from $V_{CC.}$ The general desired filter topology is shown in the following figure. Not shown in the core are parasitic routing and local decoupling capacitors. Excluded from the external circuitry are parasitics associated with each component.

Figure 130. Typical, V_{CCA}, $V_{CCIOPLL}$, and V_{SSA} Power Distribution



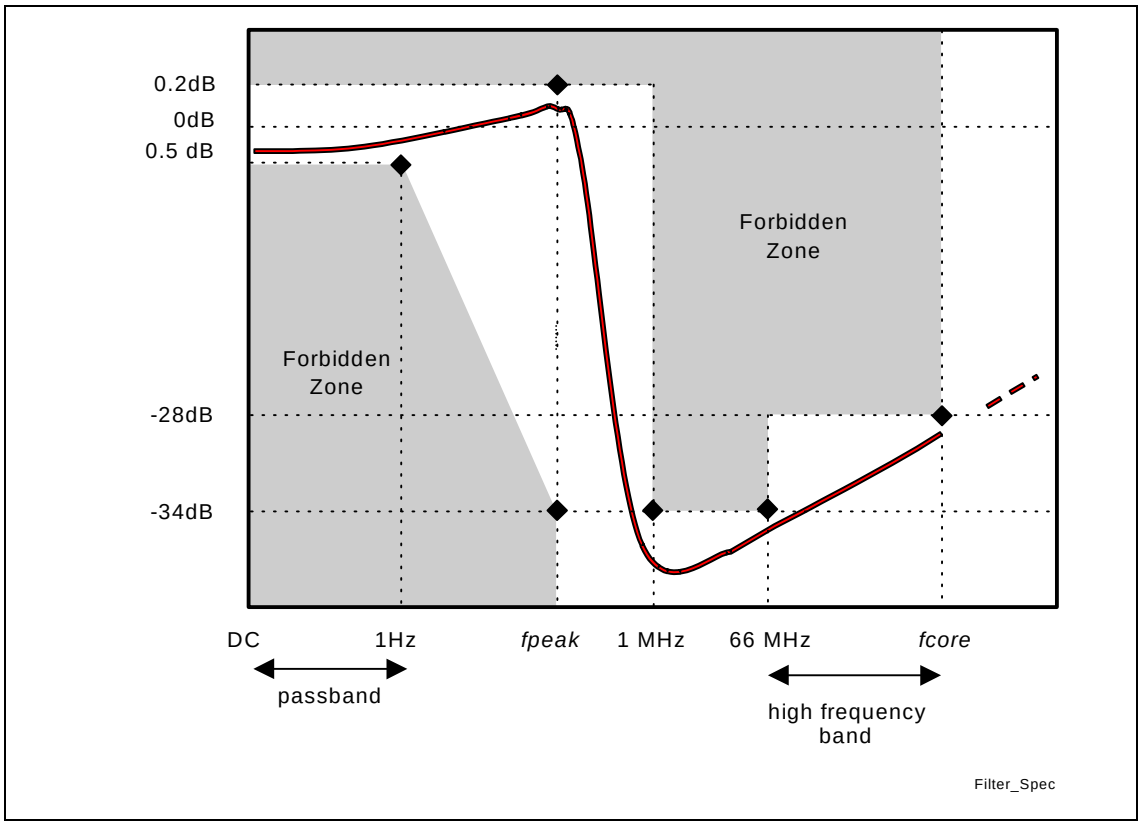
The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity, this document will address the recommendation for the V_{CCA} filter design. The same characteristics and design approach is applicable for the $V_{CCIOPLL}$ filter design.

The AC low-pass recommendation, with input at V_{CC} and output measured across the capacitor (C_A or C_{IO} in Figure 130), is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter recommendation (AC) is graphically shown in the following figure.

Figure 131. Filter Recommendation



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond *fcore* (core frequency).
3. *fpeak*, if existent, should be less than 0.05 MHz.

Other Recommendations

- Use shielded type inductors to minimize magnetic pickup

- Filter should support DC current > 30 mA
- DC voltage drop from V_{CC} to V_{CCA} should be < 60 mV, which in practice implies series R < 2 Ω and means pass band (from DC to 1Hz) attenuation < 0.5 dB for V_{CC} = 1.1 V, and < 0.35 dB for V_{CC} = 1.6 V.

The following three tables list some recommended components for the filter.

Table 49. Recommended Inductor Components

Ref Designator	Value	Tol	SRF	Rated I	DCR
L1	4.7 uH	10%	35 MHz	30 mA	0.56 Ω (1 Ω max)
L2	4.7 uH	10%	47 MHz	30 mA	0.7 Ω (±50%)
L3	4.7 uH	30%	35 MHz	30 mA	0.3 Ω max

Table 50. Recommended Capacitor Components

Value	Tolerance	ESL	ESR
33 µF	20%	2.5 nH	0.225 Ω
33 µF	20%	2.5 nH	0.2 Ω

Table 51. Recommended Resistor Components

Value	Tolerance	Power	Note
1 Ω	10%	1/16 W	Resistor may be implemented with trace resistance such that a discrete R is not needed.

To satisfy damping requirements, total series resistance in the filter (from V_{CC} to the top plate of the capacitor) must be at least 0.35 Ω. This resistor can be in the form of a discrete component, routing, or both. For example, if the selected inductor has minimum DC resistance (DCR) of 0.25 Ω, then a routing resistance of at least 0.10 Ω is required. Be careful not to exceed the maximum resistance (2 Ω). That is, if using discrete R1 (1 Ω ± 10%), the maximum DCR of the inductor should be less than 2.0 - 1.1 = 0.9 Ω, which precludes using some inductors and will set a maximum trace length.

Other routing requirements:

- C should be close to V_{CCA} and V_{SSA} pins, < 0.1 Ω per route
- V_{CCA} route should be parallel and next to V_{SSA} route (minimize loop area)
- L should be close to C; any routing resistance should be inserted between V_{CC} and L
- Any discrete R should be inserted between V_{CC} and L.

Figure 132. Implementation 1: Using Discrete R

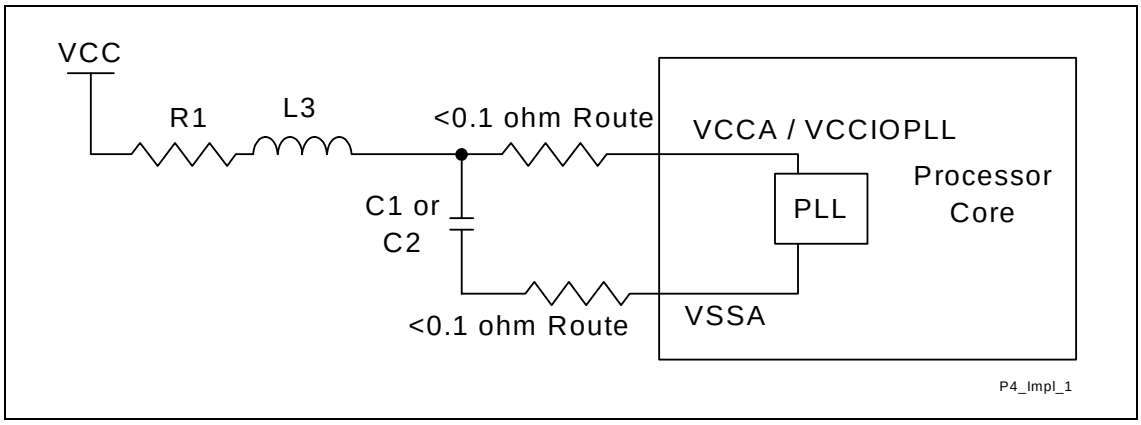
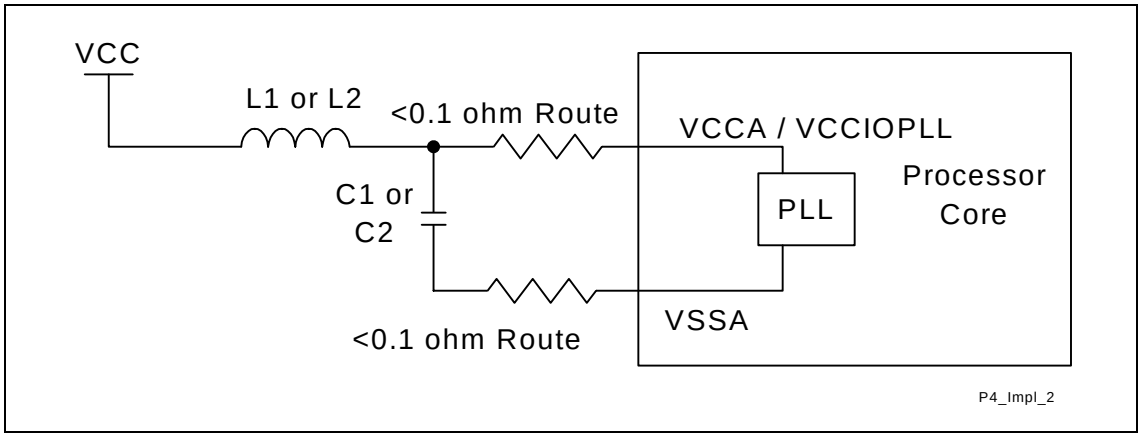
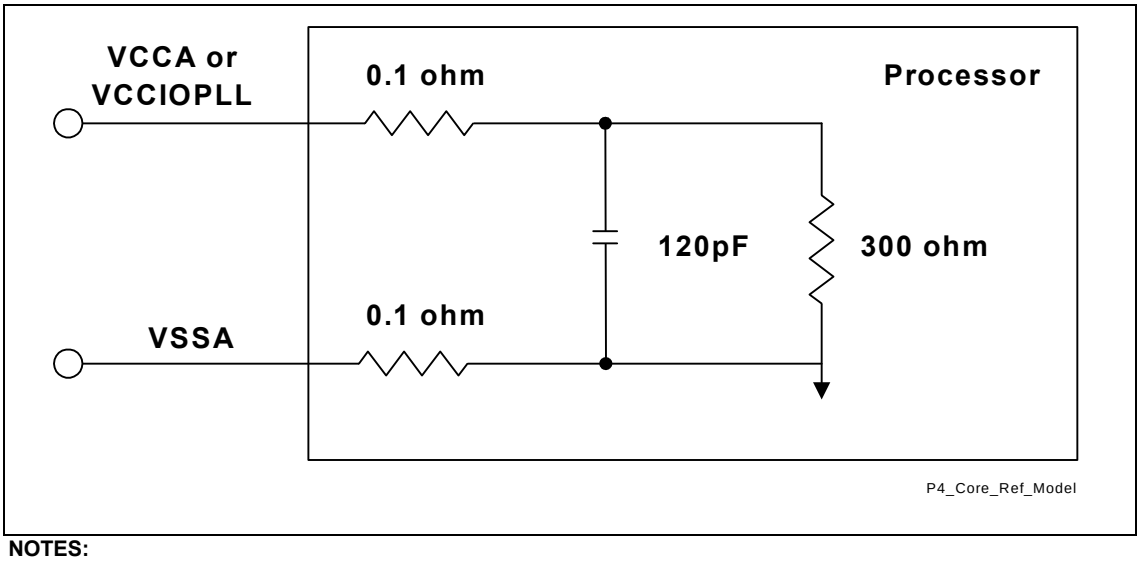


Figure 133. Implementation 2: No Discrete R



As long as filter performance and other requirements outlined in this section are satisfied; alternative solutions are acceptable. Custom solutions should be simulated against a standard reference core model, which is shown the following figure.

Figure 134. Core Reference Model



NOTES:
1. 0.1 Ω resistors represent package routing.
2. 120 pF capacitor represents internal decoupling capacitor.
3. 1 kΩ resistor represents small signal PLL resistance.
4. Be sure to include all component and routing parasitic.
5. Sweep across component/parasitic tolerances.
6. To observe IR drop, use DC current of 30 mA and minimum V_{CC} level.

11.4.3. Recommended System Design For VRM 9.0

Intel has defined VRM 9.0 for supplying V_{CC} power to the Pentium 4 processor. The VRM 9.0 definition includes Remote-Sense, Current Share and Output Enable features. VRM suppliers must provide these features as well as meet voltage and current requirements set forth in the VRM 9.0 DC-DC Converter Design Guidelines.

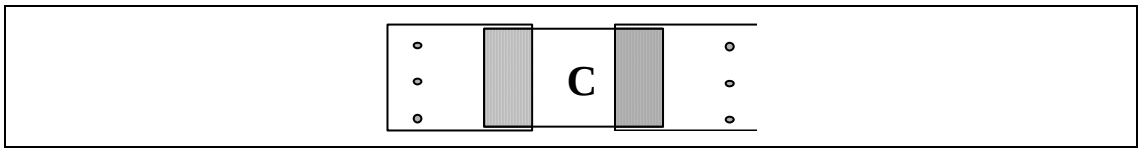
The VRM 9.0 output slew rate is specified at 50 A/µs. The system designer needs to provide adequate bulk and high frequency decoupling on the system board to meet the Pentium 4 processor required slew rate.

The main power source for the VRM 9.0 is 12 V +5%, -8%. This voltage is supplied by a conventional computer power supply through a cable to the system board. The system board needs to supply local bulk bypassing on the 12 V rail. When the VRM 9.0 is providing an output current step to a Pentium 4 processor from $Iout_{MIN}$ to $Iout_{MAX}$ or $Iout_{MAX}$ to $Iout_{MIN}$ at the slew rate of 50 A/µs, the slew rate of the input current to the VRM 9.0 should not exceed 1 A/µsec. Many power supplies currently in use today do not have a sufficient 12 V power supply for Pentium 4 processor systems. Refer to the *ATX / ATX12V Power Supply Design Guide*.

System boards can include a SENSE input for each VRM 9.0. The trace resistance should not be greater than 1.0 Ω. Route from the Pentium 4 processor $V_{CCSENSE}$ and $V_{SSSENSE}$ pins to VO+Sense and VO-Sense of the VRM respectively. VO+Sense and VO-Sense are the remote sense lines for VRM. Care must be taken to prevent shorting of the remote sense lines to the output planes at the VRM connector or vias. The current drawn from $V_{CCSENSE}$ / $V_{SSSENSE}$ shall not exceed 50 µA.

To meet the transient response of a Pentium 4 processor, it is necessary to properly place bulk and high frequency capacitors close to the Pentium 4 processor power and ground pins. Refer to Section 11.4.5 for guidelines on placement of the decoupling capacitors. If polymer capacitors are being used, avoid the loss of the low ESL characteristic by connecting via patterns as wide as the capacitor with multiple via holes per connection, as shown in the following figure.

Figure 135. Connections to Via Patterns



The OUTEN pin on VRM 9.0 can be used to disable the output of the VRM. The system designer should disable the output of the VRM 9.0 in a system when no processor is installed.

11.4.4. Options For Meeting V_{CC} Tolerances

Figure 7 shows suggested stack up configurations for Pentium 4 processor system board designs, in which the internal power and ground planes are used as signal reference planes. Other stack-up configurations are possible but should be used only after a thorough analysis.

Example

Given power bussing area from the regulator to the socket approximated as a rectangle, with the following dimensions for the power and ground plane:

l = 0.279 “; w = 2.09 “; t = 1.24 mils (1 oz. copper):

Equation 15. Sample Calculation

$$R = 0.677\ \text{m}\Omega \cdot \text{mil} \cdot \frac{0.279''}{2.09'' \cdot 1.24\ \text{mil}} = 0.073\ \text{m}\Omega$$

The total resistance of the round trip is:

$$R = 2 \cdot 0.073\ \text{m}\Omega = 0.15\ \text{m}\Omega$$

With the V_{CC}/V_{SS} separated by 4.5 mils, the loop inductance is:

$$L = 31.9\frac{\text{pH}}{\text{mil}} \cdot \frac{0.279\ \text{mil} \cdot 4.5\ \text{mil}}{2.09\ \text{mil} \cdot (2-1)} = 19.2\ \text{pH}$$

Power must be distributed as a plane. This plane can be constructed as an *island* on a layer used for other signals, on a supply plane with other power islands, or as a dedicated layer of the PCB. Processor power should never be distributed by traces alone. Intel recommends that a minimum of four planes be dedicated to power delivery in the power delivery area for Pentium 4 processor system boards.

Due to the fact that Pentium 4 processor voltage is unique to most system designs, a voltage island will probably be the most cost-effective means of distributing power to the processor. This island from the source of power to the load should not have any breaks, so as to minimize inductance in the plane. It should also completely surround all of the pins of the source and all of the pins in the power pin area of the Pentium 4 processor.

The maximum distance between the Pentium 4 processor and its VRM 9.0 should not be greater than 1.5 inches. The bulk capacitors and the high frequency capacitors should be placed close to the Pentium 4 processor.

The Pentium 4 processor socket has 423 pins with 100-mil interstitial pitch. The routing of the signals, power and ground pins will require creation of many vias. These vias cause a “Swiss cheese” effect in the power and ground planes beneath the processor resulting in increased inductance of these planes. It is recommended to place as many high frequency caps as possible close to the processor.

11.4.5. Bulk and High Frequency Decoupling

11.4.5.1. Bulk Decoupling

Designs should place the bulk decoupling on the system board as close to the processor socket as possible (no more than 1.0 inch maximum).

The following table lists the recommended bulk capacitance devices for use with Pentium 4 processor system boards based on simulation.

Table 52. Intel® Pentium® 4 Processor Bulk Capacitance Recommendations

Bulk Capacitance	ESR	ESL	Ripple Current Rating
10 OS-CON(4SP560M), 560 µF	14 mΩ, max	4 nH, max	4.080 Arms

11.4.5.2. High Frequency Decoupling

Pentium 4 processor system boards should include high frequency decoupling capacitors as close to the socket power and ground pins as possible. The following table lists the recommended high frequency capacitance devices for use with Pentium 4 processor system boards based on simulation.

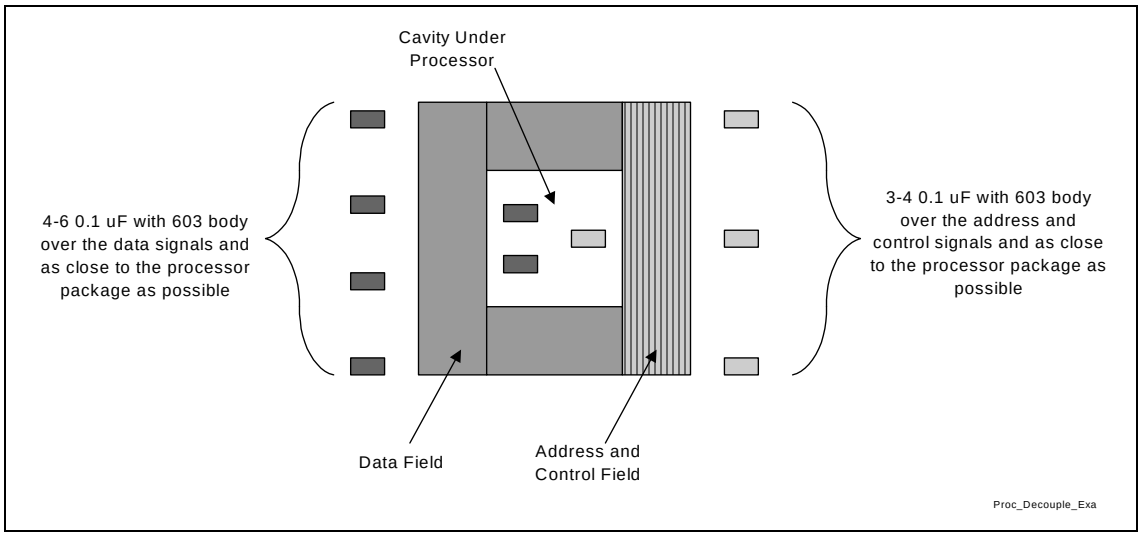
Table 53. Intel® Pentium® 4 Processor High Frequency Capacitance Recommendations

High Frequency Capacitance	ESR	ESL
24 1206 package, 10 µF	3.97 mΩ, typ.	880 pH, typ.

In addition to high frequency decoupling needed to meet voltage transients, high frequency decoupling may be required for signal integrity. System boards designed using striplines with V_{CC} and V_{SS} references should not require high frequency decoupling beyond that recommended above. For systems using microstrip configurations a return path discontinuity will exist between the processor and the system board due to the system board traces having only one reference plane. These systems should distribute decoupling capacitors as shown in the following figure and described as follows:

- 4 minimum, 6 preferred 0.1 µF capacitors with 0603 packages distributed evenly over the data lines.
- 3 minimum, 4 preferred 0.1 µF capacitors with 0603 packages distributed evenly over the address and control lines.
- All capacitors placed as close to the processor package as the keepout zone allows.

Figure 136. Example of Decoupling for a Microstrip System board Design



11.5. GTLREF[3:0]

Intel recommends one voltage divider at each component. Assume a maximum of 15 µA of leakage current per load. Note that these leakage currents can be positive or negative.

The following discussion illustrates using a single voltage divider to support two GTLREF loads assuming a V_{CC} of 1.7 V. Using 1% resistors for the voltage divider in Figure 127, make R_1 a 100 Ω resistor, and use 49.9 Ω for R_2. This creates a static usage of 10.7 mA (1.7 V/149.9 Ω) per voltage divider. After looking at all combinations of R_1 and R_2 (above and below tolerance) and I_{REF} (±30 µA), the worst-case solution for Equation 16 can be found with I_{REF} at 30 µA, R_1 at the low end of its tolerance specification (99 Ω), and R_2 at the high end of its tolerance specification (50.4 Ω). This yields:

Equation 16. Resistor Tolerance Analysis

$$GTLREF = \frac{1.7/50.4 - .000030}{1/50.4 + 1/99} = 1.1256\ V$$

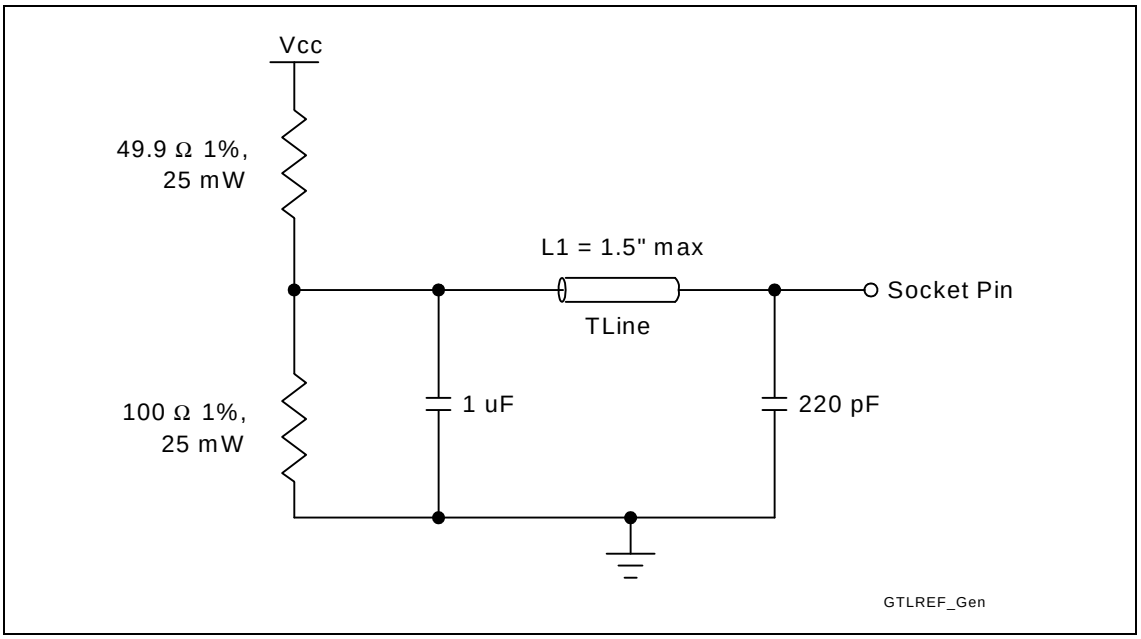
Since the target of 2/3 of V_{cc} is 1.133 V, this setting is within 0.7% of the 2/3 point and satisfies the 2% specification. A spreadsheet program allows the reader to easily verify the other corners. Varying over its tolerance range has minimal effect.

These values chosen for R_1 and R_2 have additional benefits: the parallel combination terminates the GTLREF line to 33 Ω and these generally available resistance values reduce resistor cost.

Decouple GTLREF[3:0] at each pin with a 220 pF capacitor to V_{ss}. Decouple GTLREF to V_{ss} at the voltage dividers with a 1 µF capacitor.

When routing GTLREF to the pins, use a 30–50 mil trace (the wider the better) and keep it as short as possible (less than 1.5 inches). Also, keep all other signals at least 20 mils away from the GTLREF trace. This provides a low impedance line without the cost of an additional plane or island. Due to the placement of the GTLREF pins on the Pentium 4 processor, it may not be possible or convenient to route all four pins from one voltage divider. It is acceptable to use more than one voltage divider with decoupling at each voltage divider and each pin.

Figure 137. Suggested GTLREF Generation



11.6. Capacitor Component Models

Intel recommends that designers acquire component models from their respective manufacturers. Intel cannot guarantee the specifications of another manufacturer's components. This section contains some of the models developed by Intel for internal simulations.

Table 54. Various Capacitor Component Models Used at Intel (Not Vendor Specifications)

Component of Simulation	Typical ESR (Ω)	Typical ESL (nH)
0.1 µF Ceramic 0603 package	0.006	0.63
1 µF Ceramic 0805 package	0.080	0.702
10 µF Ceramic 1206 package	0.004	0.880
22.0 µF Ceramic 1210 package	0.010	0.880
560 µF OS-CON	0.014	4.0

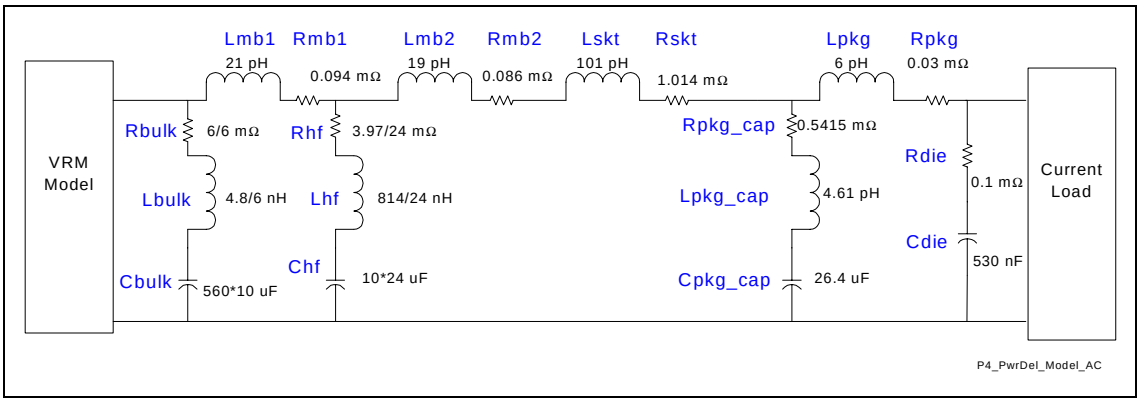
11.7. Measuring Transients

Intel recommends the following guidelines when measuring the transients on the processor V_{cc}: The measurement should be done across the $V_{CCSENSE}$ and $V_{SSSENSE}$ pins on the Pentium 4 processor socket. Use an oscilloscope with 100 MHz bandwidth, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled in the scope probe.

11.8. Intel® Pentium® 4 Processor Power Distribution Network Modeling

Intel provides the AC electrical models, shown in the following figure, for use in the simulation of the AC transient response of Pentium 4 processor power delivery systems. These models are examples only and are based on the Intel customer reference board. Designers who plan to deviate from Intel's design recommendations should simulate using the full power delivery model provided in the following figure and validate their actual design to ensure all *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet specifications are met. Due to tool capability limitations, these models have been simplified and are provided as a rough illustration of Pentium 4 processor power delivery systems. This model assumes 10 OS-CON 560 µF capacitors for bulk decoupling and 24 ceramic 10 µF 1206 package capacitor for high frequency decoupling. The Lmb2, and Rmb2 refer to the inductance and resistance of the power plane below the processor socket area (i.e., "Swiss cheese" area). The inductance and resistance of the power plane between VRM 9.0 and processor is shown as Lmb1 and Rmb1 respectively. A current step stimulus of 5.3 A to 52.7 A is applied with rise time of 150 ns.

Figure 138. V_{CC} Power Delivery Model For AC Transient Response for Intel® Pentium® 4 Processor



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12. Intel® 850 Chipset Power Distribution Guidelines

12.1. Definitions

Suspend-To-RAM (STR): In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to *wake* the system remain powered.

Full-power operation: During *full-power* operation, all components on the motherboard remain powered. Note that *full-power* operation includes both the *full-on* operating state and the S1 (PROCESSOR stop-grant state) state.

Suspend operation: During *suspend* operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3) and Soft-off (S5).

Core power rail: A power rail that is only on during *full-power* operation. These power rails are on when the PSON signal is asserted to the ATX power supply.

Standby power rail: A power rail that in on during *suspend* operation (these rails are also on during *full-power* operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed *directly* from the ATX power supply is: $5V_{SB}$ (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.

Derived power rail: A *derived* power rail is any power rail that is generated from another power rail using an on-board voltage regulator. For example, $3.3V_{SB}$ is usually derived (on the motherboard) from $5V_{SB}$ using a voltage regulator.

Dual power rail: A *dual* power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a *standby supply* during *suspend* operation and derived from a *core supply* during *full-power* operation. Note that the voltage on a *dual* power rail may be misleading.

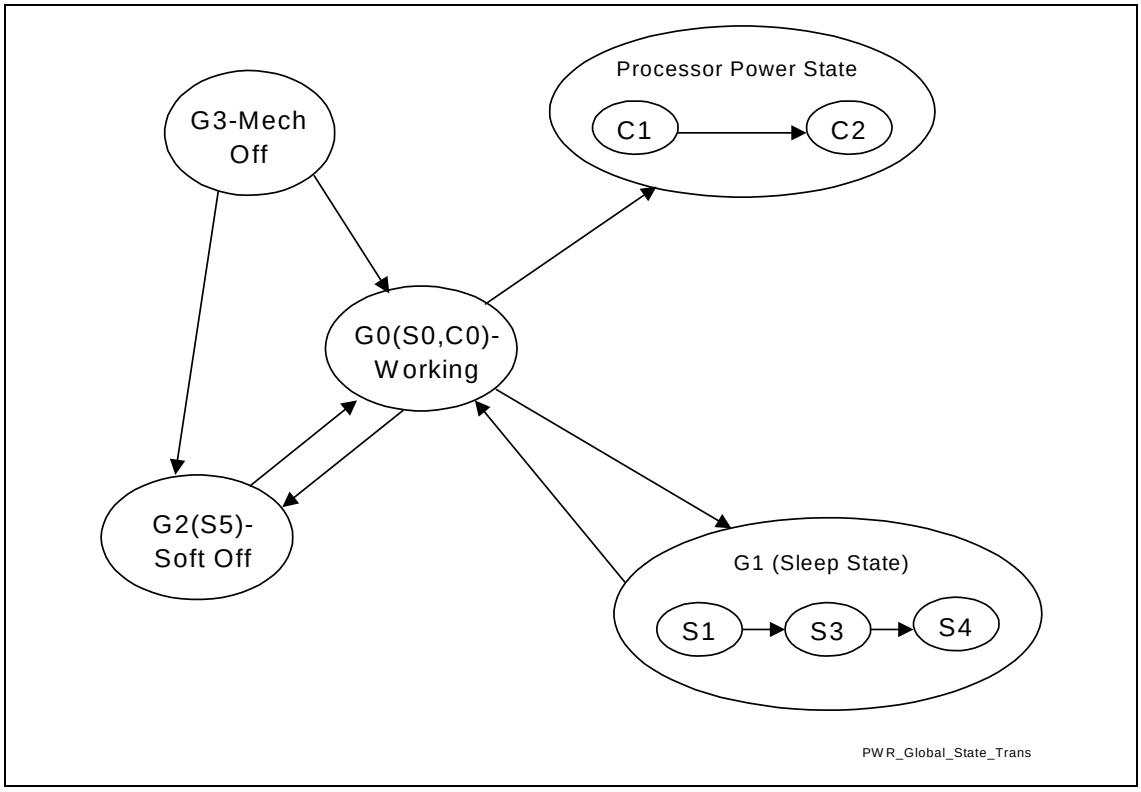
12.2. Power Management

The 850 chipset-based platform implements the ACPI mechanisms software and hardware that enables the system to minimize system power consumption, manage system thermal limits, and maximize the battery life. This implementation involves tradeoffs among system speed and noise.

12.2.1. ACPI Hardware Model

The 850 chipset-based desktop supports both legacy and ACPI operations, which involves sequencing the platform between the various global system states (G0–G3). The following figure depicts global states and the transitions. For complete detail of the mechanisms involved in transition from any of the global states refer to the *ACPI Interface specification, Rev 1.0a* in Section 4.5.

Figure 139. Global System Power States and Transition



12.2.2. Thermal Design Power

The thermal design power numbers are estimation of the maximum expected power generated by a component in a realistic application. It is based on extrapolations in both hardware and software technology over the product life. It does not represent the expected power generated by a power virus. The ICC maximum sustained (WCRA) numbers are estimations of the maximum expected current generated within a die section in a realistic application (e.g., an application that executes extensive memory reads/writes).

Refer to the *Intel® 850 Chipset: Thermal Considerations Application Note (AP-720)* and the *Intel® 850 Chipset: 82850 Memory Controller Hub (MCH) datasheet* for additional thermal package characteristics.

Table 55. Intel® 850 Chipset Thermal Design Power

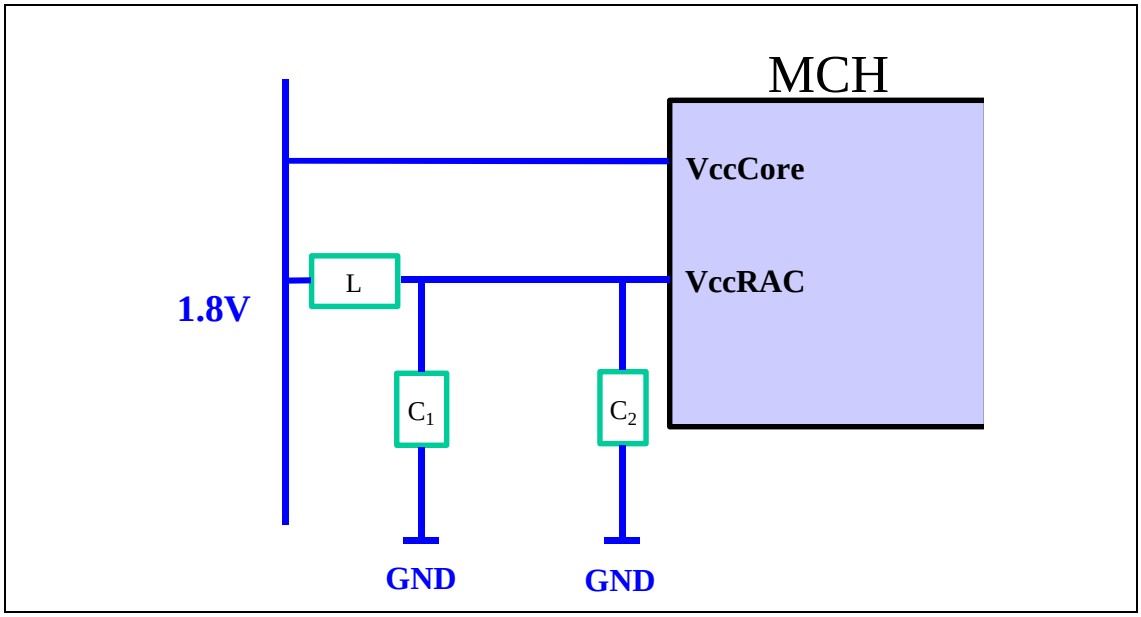
Parameter	Icc Max Sustained Current (A)
MCH • MCH (UP) Typical Thermal Design Power = 5.8W • MCH (UP) Maximum Thermal Design Power = 8.0W	
1.8 V Core	3.2
1.5 V V_{DDQ} AGP I/O	0.37
1.6 V V_{TT}	2.2
ICH2 • ICH2 Max Thermal Design Power = 1.6 W ±15%	
1.8 V Main Logic	0.30
1.8 V (Stand By) Resume Logic + 1.8 V LAN*	0.040
3.3 V Main I/O	0.41
3.3 V (Stand By) Resume Logic	0.062
Processor I/F (1.3 ~ 2.5)	200 µA

NOTES:
1. Remember that values stated for the maximum sustainable current (I_{CC}) of ICH2 are maximum preliminary measurements, and are subject to change.

12.2.3. 1.8V RAC Isolation Solution

Intel® 850 MCH requires a low-pass filter on the VccRAC pins to meet clock jitter specifications. The two possible filter solutions may be configured as either an inductor-capacitor (LC) or ferrite bead-capacitor filters. For more details, please see Figure 140 and Figure 141. The inductor or ferrite bead must have a minimum current capacity of 500 mA and a maximum DC resistance of 100 mOhm. DC drop is a concern due to the series element between the RAC and 1.8V supply. The VccRAC pins for the Intel® 850 MCH are given in Table 56.

Figure 140. Inductor-Capacitor Filter Circuit

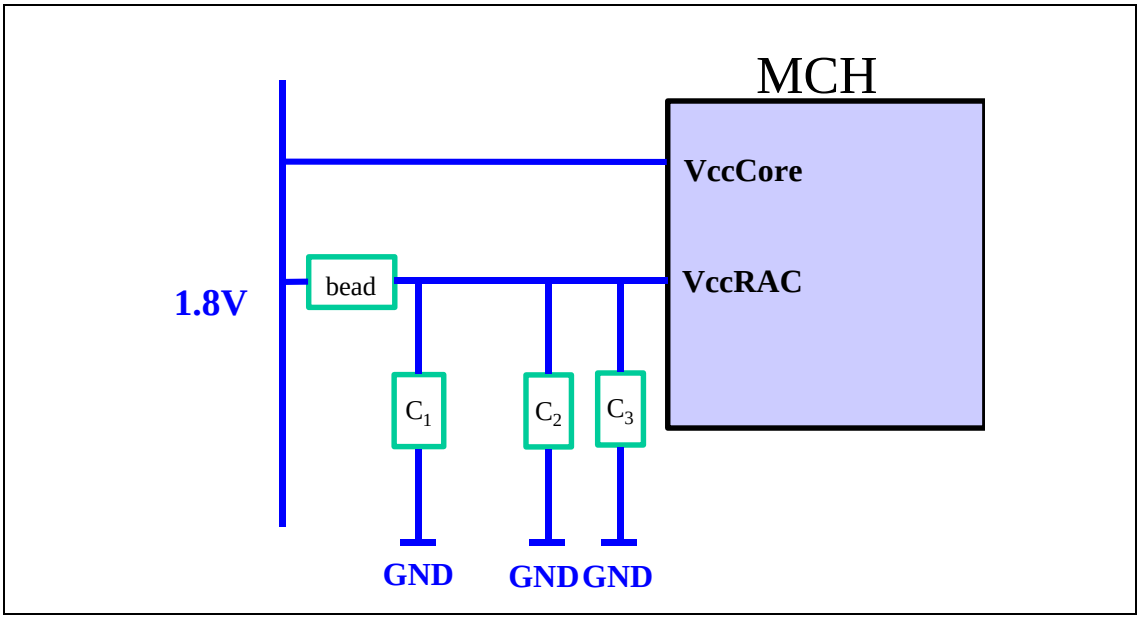


Simulations and validations indicate that L = 3.3 nH and C_1 = 3.3 uF forms an adequate inductor-capacitor filter. The filter must be located within 2-inches the device and the layout of VccRAC connections should follow high-speed design practices.

In addition to the low-pass filter, the RAC requires local decoupling capacitors. These decoupling capacitors should be located close to the RAC pins to control self-induced RAC noise. For the inductor-capacitor filter, two to three 0.1 uF capacitors (C_2) for both RACs should provide adequate decoupling between VccRAC and Vss.

The inductor-capacitor filter and its associated decoupling capacitors can be implemented using 0805 size components.

Figure 141. Ferrite Bead Filter Circuit



As an alternate solution, a 10 ohm (@ 100 MHz) and 10 uF forms an adequate ferrite bead-capacitor filter. The filter must be located within 2-inches the device and the layout of VccRAC connections should follow high-speed design practices.

In addition to the ferrite bead filter, the RAC requires local decoupling capacitors. These decoupling capacitors should be located close to the RAC pins to control self-induced RAC noise. For the ferrite bead filter, use a minimum number of two 0.1 uF capacitors (C_2) per RAC, and a minimum of one 1.0 uF capacitor (C_3) for both RACs should be sufficient. The layout of the capacitor connections should follow high-speed design practices.

The ferrite bead filter and its associated decoupling capacitors can also be implemented using 0805 components except for the 10 uF capacitor, which is a 1206 size component.

Table 56. Intel® 850 MCH 1.8V RAC pinout

Intel® 850 MCH 1.8V RAC pinout location	Channel A	Channel B
Ball	T22	C16
	N22	F15
	J22	F14
	J20	C13
	R19	E9
	P19	C9

Figure 142. Customer Reference Board Layout Example

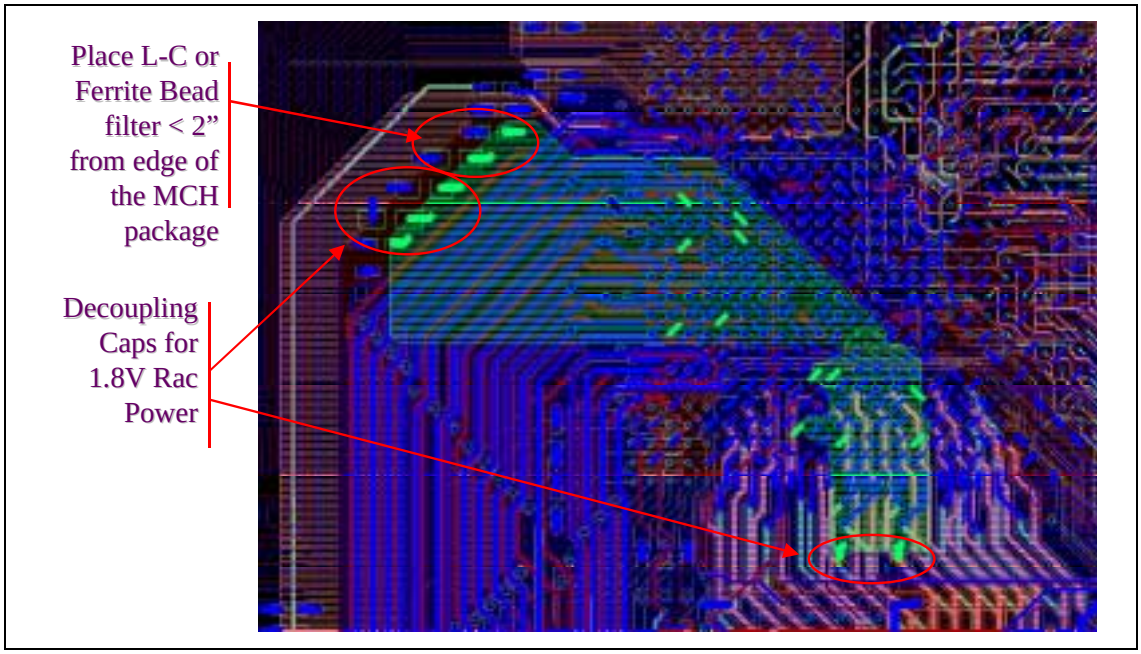


Figure 143. CRB (con't.) Bottom – layer 6

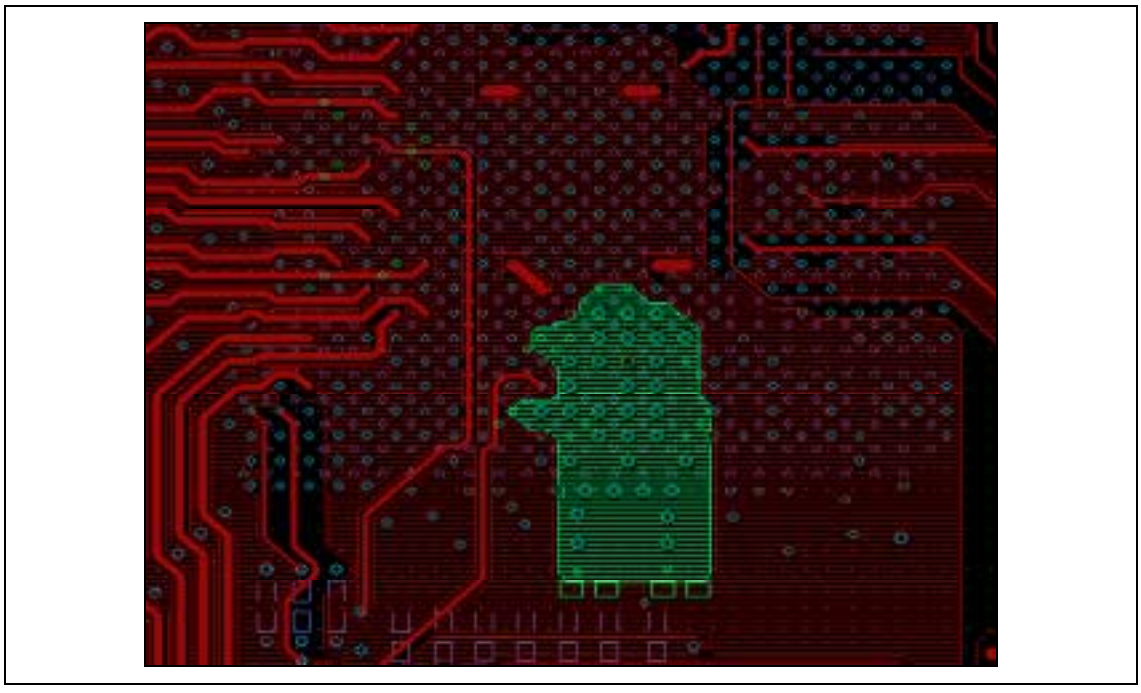
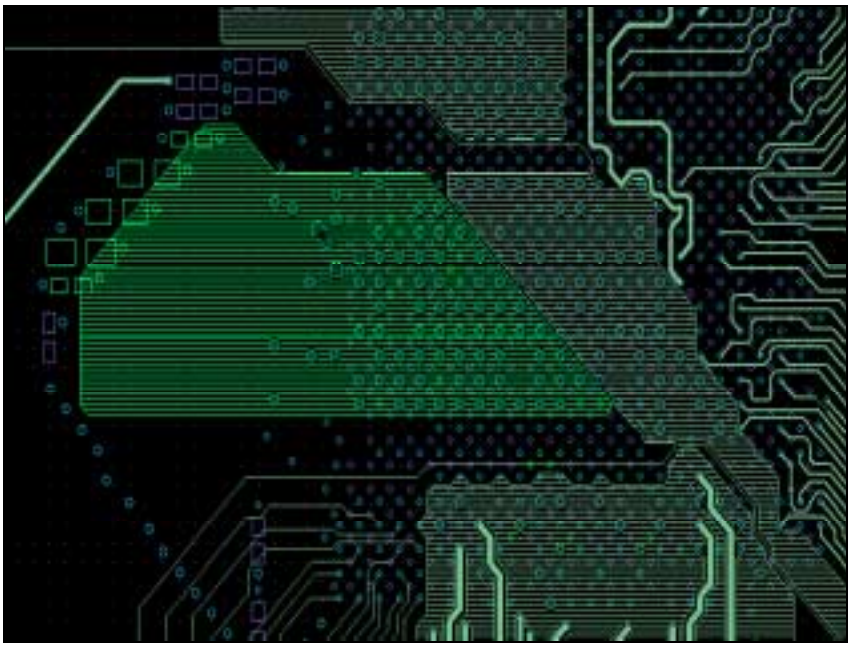


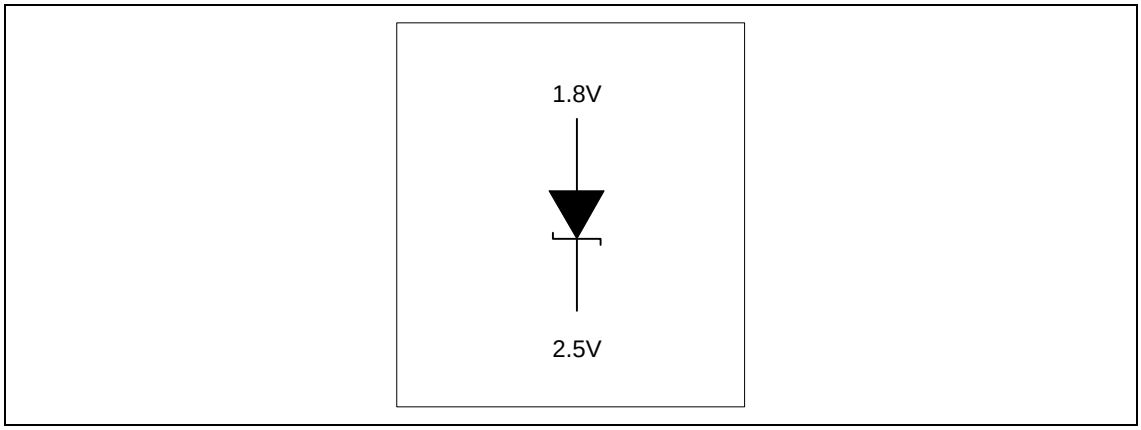
Figure 144. CRB (con't.) Signal 2 – layer 4



12.2.4. V_{TERM}/V_{DD} Power Sequencing Requirement

Power to the RDRAM termination resistors (V_{TERM}) must follow the power to the RDRAM Core. A schottky diode can be placed between the 1.8 V and 2.5 V to ensure this power-up sequence.

Figure 145. 1.8 V and 2.5 V Power Sequence (Schottky Diode)



12.3. Intel® 850 Chipset Power Sequencing Requirements

The 850 chipset needs the following power supplies for operation – V_{CC1_8}, V_{DDQ} and V_{TT}.

To avoid forward-biasing the ESD protection-diodes from the I/O to Core power supplies, it is necessary that the V_{CC1_8} power supply ramp up ahead (See Figure 146) of the V_{DDQ} and V_{TT} power supplies. For the same reason, it is necessary to have the V_{CC1_8} power supply ramp down later than the V_{DDQ} and V_{TT} power supplies. If this cannot be guaranteed, it is important that the V_{CC1_8} power supply lag (see Figure 147) the IO supplies by no greater than 1.0 V. There are no dependencies between V_{DDQ} and V_{TT} supplies.

Figure 146. Desire Mode of Power Sequencing

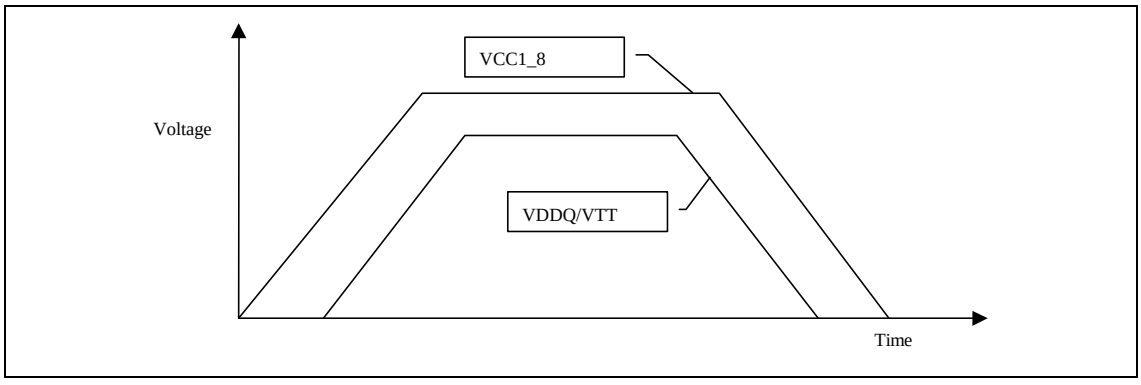
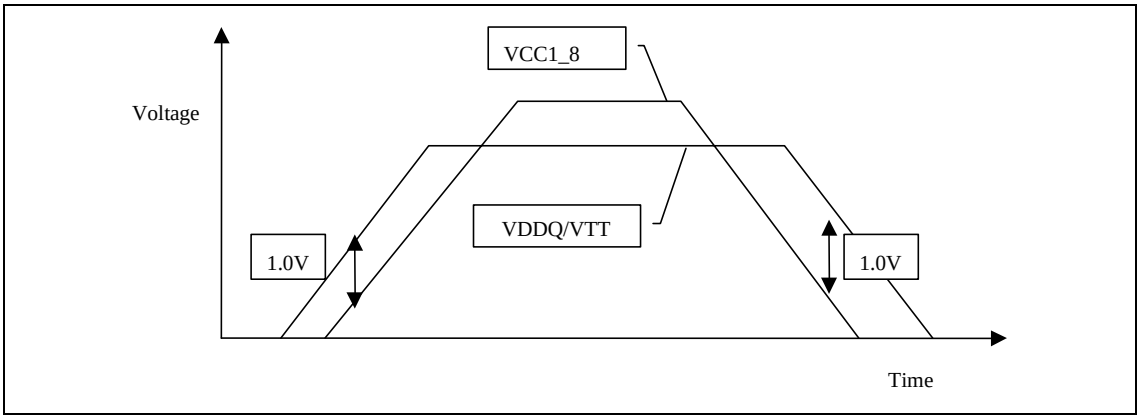


Figure 147. Optional Mode of Power Sequencing



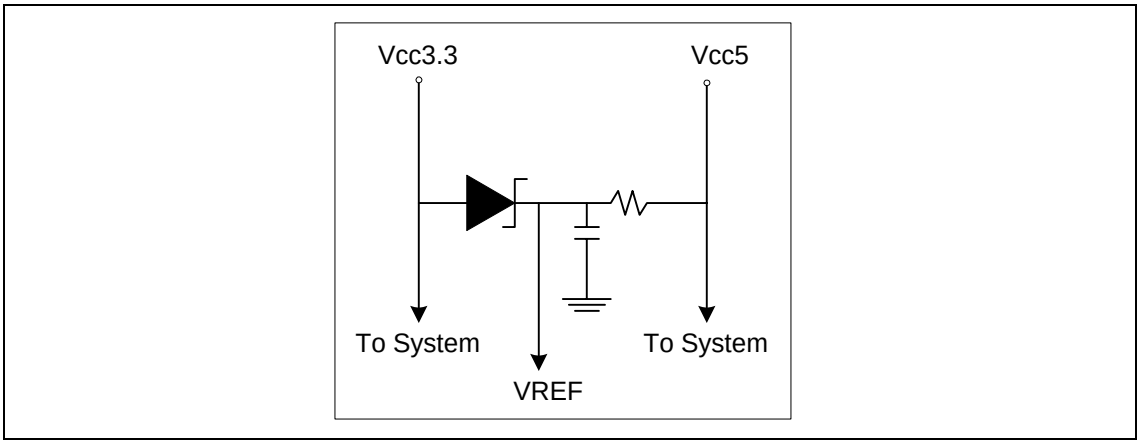
12.4. ICH2 V5REF and VCC3_3 Sequencing Requirement

V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within .7V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within .7V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 148 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend, the only signals that are 5V tolerant capable are USB OC:[3:0]#. If these signals are not needed during suspend, V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX. If OC:[3:0]# is needed during suspend and 5V tolerance is required then V5REF_SUS should be connected to 5V_Always/5V_AUX, but if 5V tolerance is not needed in suspend, then V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX rails.

Figure 148. Example 3.3V/V5REF Sequencing Circuit



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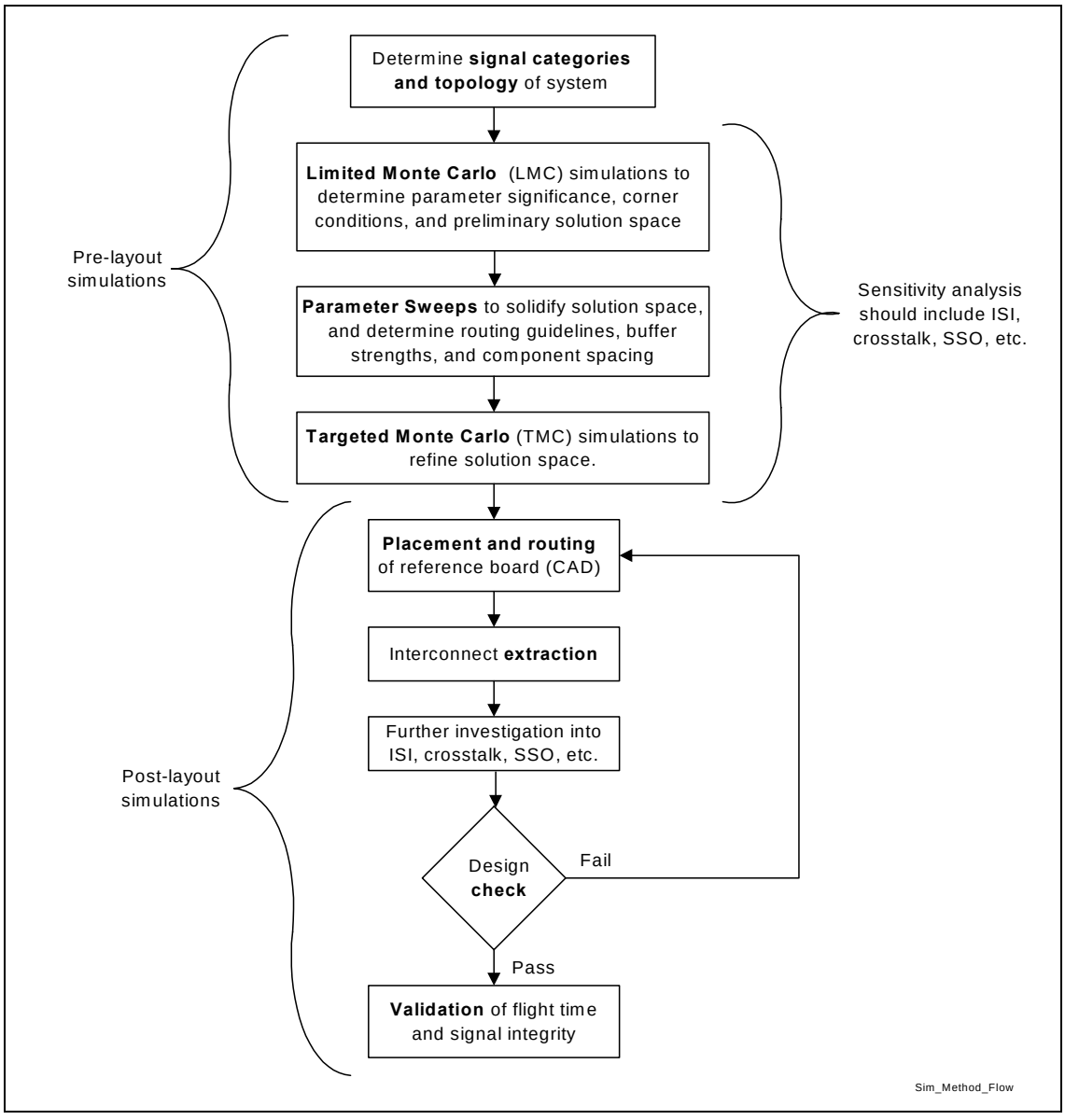
13. Methodology for Determining Topology and Routing Guidelines

This chapter describes the simulation methodology that was used to derive the topology and routing guidelines presented in this design guide. The following figure is a flowchart outlining the process.

Figure 149. Simulation Methodology Flowchart



The design process should begin with an initial timing analysis and topology definition. Pre-layout analog simulations should be performed. These pre-layout simulations will help define routing rules prior to placement and routing. After routing, the interconnect database can be extracted and post-layout simulations can be performed to refine the timing and signal integrity analysis. The analog simulations should be validated when actual systems become available.

Pre-layout simulations provide a detailed picture of the working solution space that meets flight time and signal quality requirements. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulation can be reduced.

Intel recommends running simulations at the device pads for signal quality and for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

Pre-layout analysis includes a sensitivity analysis using parametric sweeps. Parametric sweep analysis involves varying one or two system parameters while all others such as driver strength, package Z_0, and S_0 are held constant. This way, the sensitivity of the proposed bus topology to varying parameters can be analyzed systematically. Sensitivity of the bus to flight time and signal quality should be covered. Suggested sweep parameters include trace lengths, termination resistor values, and any other factors that may affect flight time, signal quality, and feasibility of layout. Minimum flight time and worst signal quality are typically analyzed using fast I/O buffers and interconnect. Maximum flight time is typically analyzed using slow I/O buffers and slow interconnects. However, fast I/O buffers and various system board and package combinations have been found to violate signal quality specifications. It is advisable to perform some level of Monte Carlo analysis that includes varying all possible parameters.

Outputs from each sweep should be analyzed to determine which regions meet timing and signal quality specifications. To establish the working solution space, find the common space across all the sweeps that result in passing timing and signal quality. The solution space should allow enough design flexibility for a cost-effective, manufacturable layout.

The effects of ISI and return path irregularities are difficult and tedious to simulate with 100% accuracy. Intel has found through experimentation and targeted simulations that the effects can have a significant impact on the primary signal. As a result of these studies, it is now possible to more accurately predict the effects. Given the complexity of a quad-pumped source synchronous bus architecture, it was necessary to tighten the component timings and bus requirements to provide a viable routing solution space. Because of this, it is strongly recommended that designs adhere to the design guideline requirements and component specifications.

13.1. Timing Methodology

The timing equations used for both source synchronous and common clock parameters are derived in the following sections.

13.1.1. Source Synchronous

In a source synchronous bus the clock (or strobe) is driven from the same source as the signal it will sample. The strobe and the signal both propagate to the receiver via the PCB. The receiver then uses the strobe to sample the signal. This eliminates the need to account for worst-case flight times and, in theory, will significantly increase the maximum bus speed.

13.1.1.1. Setup Time

Figure 150 shows the setup-timing diagram for a source synchronous bus design. Equation 17 gives the total loop equation derived from the timing diagram.

Equation 17. Source Synchronous Setup Time

$$T_{co}(strobe) + T_{flight}(strobe) - T_{setup} - T_{margin\_setup} - T_{co}(data) - T_{flight}(data) = 0$$

where:

- T_{co}(strobe)[(data)] is the driver delay of the strobe [data]
- T_{flight}(strobe)[(data)] is the flight time of the strobe [data] interconnect
- T_{setup} is the receiver's setup requirement
- T_{margin} is the available timing margin for the setup time

The loop equation can be simplified and solved for T_{margin_setup}. The equation can be broken into two parts, valid before and interconnect skew. Then, the setup margin can be determined.

Equation 18. Source Synchronous, Valid Before

$$T_{vb} = T_{co}(data)_{max} - T_{co}(strobe)_{min}$$

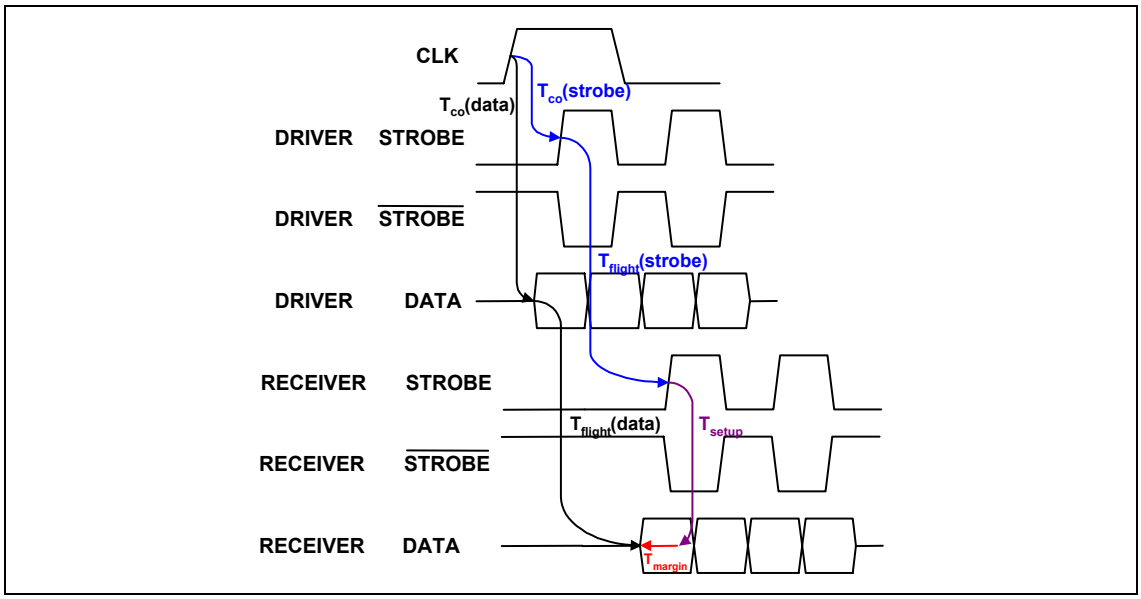
Equation 19. Source Synchronous, Interconnect Skew

$$T_{skew,max} = T_{flight}(data)_{max} - T_{flight}(strobe)_{min}$$

Equation 20. Source Synchronous Setup Margin

$$T_{margin\_setup} = -T_{vb,min} - T_{skew,max} - T_{setup}$$

Figure 150. Source Synchronous Timing Diagram for Setup Time



13.1.1.2. Hold Time

The hold timing diagram for a source synchronous bus design is shown in Figure 151. The total loop equation is derived from the hold timing diagram.

Equation 21. Source Synchronous Loop Equation for Hold Timing Diagram

$$T_{co}(data) + T_{flight}(data) - T_{margin\_hold} - T_{hold} - T_{flight}(strobe) - T_{co}(strobe) = 0$$

where:

- T_{co}(strobe)[(data)] is the driver delay of the strobe [data]
- T_{flight}(strobe)[(data)] is the flight time of the strobe [data] interconnect
- T_{hold} is the receiver's setup requirement
- T_{margin} is the available timing margin for the setup time

The loop equation can be simplified and solved for T_{margin_hold}. The equation can be broken into two parts, valid before and interconnect skew. Then, the hold margin can be determined.

Equation 22. Source Synchronous, Valid After

$$T_{va} = T_{co}(data)_{\min} - T_{co}(strobe)_{\max}$$

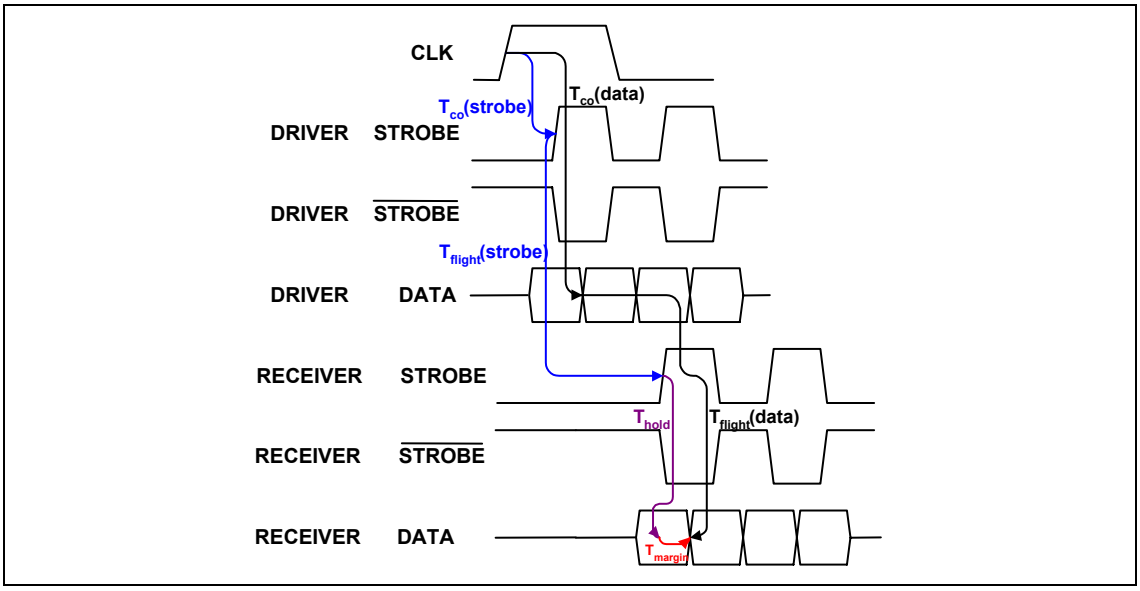
Equation 23. Source Synchronous, Interconnect Skew

$$T_{skew,\min} = T_{flight}(data)_{\min} - T_{flight}(strobe)_{\max}$$

Equation 24. Source Synchronous, Hold Margin

$$T_{margin\_hold} = T_{va,\min} + T_{skew,\min} - T_{hold}$$

Figure 151. Source Synchronous Timing Diagram for Hold Time



13.1.2. Common Clock

A block diagram of a circuit that was used to develop the basic timing equations is shown in Figure 152.

13.1.2.1. Setup Margin

Figure 153 shows the setup timing diagram that was used to develop the final timing equations for the setup margin.

Equation 25. Common Clock Loop Equation

$$T_{cyvle} + T_{drv\_clk}(B) + T_{prop\_clk}(B) - T_{jitter} - T_{setup} - T_{m\,arg\,in} - T_{prop} - T_{drv} - T_{prop\_clk}(A) - T_{drv\_clk}(A) = 0$$

where:

- T_{cycle} is the cycle time
- T_{drv_clk}(A)[(B)] is the delay of the clock buffer circuit connected to device A [B]
- T_{prop_clk}(A)[(B)] is the delay of the interconnect between the clock buffer and device A [B]
- T_{drv} is the delay of the output buffer for the data signal on device A (T_{CO})
- T_{prop} is the interconnect delay between device A and B
- T_{setup} is the setup time required by the buffer
- T_{jitter} is the clock cycle-to-cycle jitter

Figure 152. Circuit Used to Develop the Common Clock Timing Equations

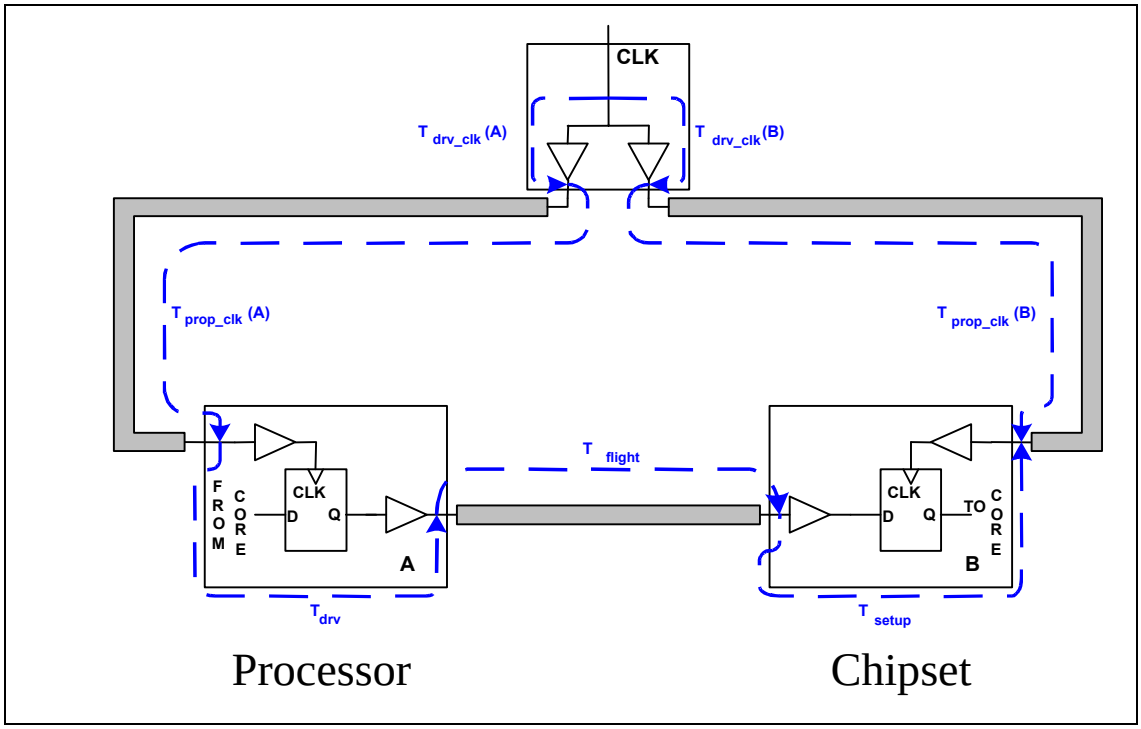
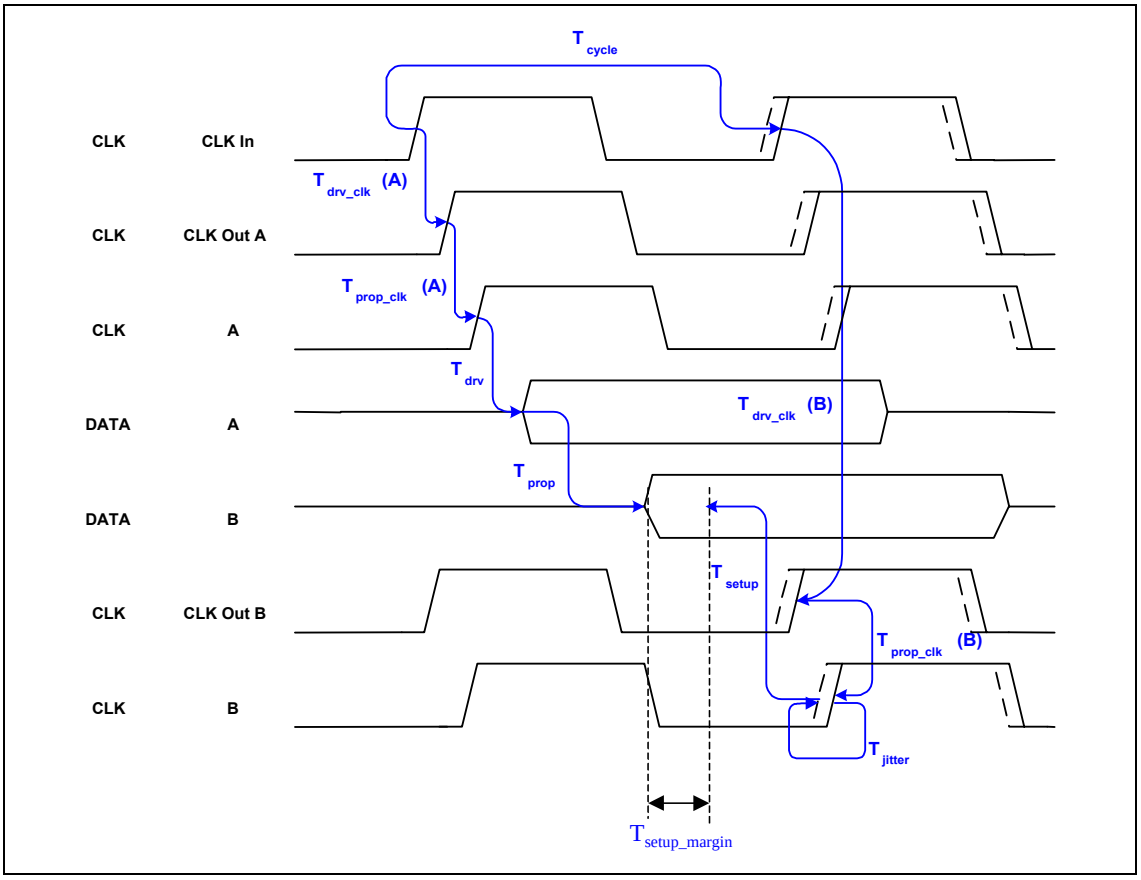


Figure 153. Timing Diagram Used to Determine the Common Clock Setup Timing Equations



13.1.2.2. Hold Margin

Figure 153 also illustrates the timing diagram that was used to develop the final timing equations.

Equation 26. Common Clock Hold Margin

$$T_{margin\_hold} = T_{drv} + T_{prop} - T_{hold} - T_{skew\_hold}$$

13.1.3. Timing Spreadsheet

A timing spreadsheet should be created to keep track of each signal's timing margins.

To effectively manage the timing spreadsheet the following recommendations should be adhered to.

- All assumptions should be stated in the spreadsheet file
- Simulated and measured timings should be tracked separately
- Each timing component has an owner and revision date
- Rising and falling edges should be tracked separately

13.2. Simulation Methodology

This sections outlines the simulation methodology used to determine the topology and routing guidelines.

13.2.1. Design Optimization

The layout for a high-speed bus design can be complex. High frequency phenomena that previously had second or third order effects on system level performance are becoming first order as bus speeds continue to increase. It should be noted that for a high-speed bus, fixing a problem in one area of the board might create another problem in a different area.

The design recommendations of this design guide have been written to provide enough detail to allow a platform designer to go right into layout designs and only perform post-route simulations. If any of the recommendations are not followed, then it is advisable to follow the complete simulation process described below in order to accurately quantify your solution space.

13.2.2. Signal Categories and Topology Options

The first section of the bus design process is to determine all the signal categories contained within the design. All signals should be defined to be in one of the following categories:

- Source synchronous
- Common clock
- CMOS

Once signals have been categorized, all possible interconnect topologies for each signal group must be determined. This requires significant collaboration with the layout engineer and will be the direct result of a layout study. The optimum part placement and all possible interconnect solutions should be determined. The layout study should produce a solution space that lists all possible interconnect topology options including line lengths, widths and spacing. Extensive simulations during the sensitivity analysis will be used to limit the solution space determined from the layout study. This limited solution space becomes a final design solution that meets all timing and signal quality specifications.

13.2.3. Sensitivity Analysis

A sensitivity analysis is used to determine the solution space for all aspects of the design. Every parameter in the System Bus should be varied in simulations. The performance metrics (e.g., flight time, flight skew, and signal integrity) are observed while each one of the variables is swept. The performance as a function of each variable is compared to the timing and signal quality specifications. As a result, limits are placed on each of the components. This produces a solution space that places strict limits on the system variables (e.g., trace lengths, spacing, impedance, etc.). The solution space will lead to design guidelines for the PCB and routing. The following table lists the primary system variables that should be considered in the System Bus sensitivity analysis. The following table indicates the relative effect of each variable on system performance.

Table 57. System Variables to Consider for Sensitivity Analysis

System Variable	Impact on Timings and/or Signal Integrity
Trace/stub lengths	High
Driver Behavior (Edge Rate and Device Strength)	High
Trace impedance variations	High
Er variations	Low to moderate(variation is usually small)
Pattern dependency	Low to High (high for long lines)
Ground return path discontinuities	Presumed High
Trace to trace spacing	High
AC losses	Moderate
Termination resistor variations	Low (if high tolerance resistors are used)
Layer to layer Zo and Er variations	Moderate
Serpentine spacing	Moderate
Simultaneous Switching Outputs (SSO)	Moderate
Inter-Symbol Interference (ISI)	Moderate

13.2.4. Signal Quality Metrics

This section documents signal quality metrics used to derive topology and routing guidelines. Signal quality must be addressed with all System Bus signals. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swing can adversely affect system timings. Excessive ringback, and signal non-monotonicity cannot by tolerated, since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Additionally, over/undershoot can cause timing degradation due to the build up of inter-symbol interference (ISI) effects. These issues hold true for both AGTL+ and Source Synchronous signals. For these reasons, it is important that the designer work to achieve a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

13.2.4.1. Noise Margin

The receiver buffers are designed to switch at the threshold voltage. Due to several variables (e.g., processor variations and system noise), the threshold voltage may change. This variation in the threshold voltage is known as the noise margin. For the processor, the noise margin is assumed to be 100 mV above and 100 mV below the reference voltage, V_{REF}.

Signal quality is measured by observing the linearity of the signal as it transitions between the upper and lower levels of the noise region and by observing any signal ringing into the noise margin region. The upper and lower noise margin levels are referred to as V_{IH} and V_{IL} respectively.

An edge is defined to be linear if it exhibits a linear shape between V_{IH} and $V_{IL.}$ For non-clock and non-strobe signals, the signal seen at the receiver should be linear between V_{IH} and V_{IL}. On a case-by-case basis where it can be shown that the timing can be met with no potential data corruption, it may not be necessary for the signal to be linear between V_{IH} and V_{IL}.

13.2.4.2. Ringback

Ringback is defined as the amount of voltage that 'rings' back towards the threshold voltage and is measured at the receiver. Figure 157 illustrates an example of ringback.

For non-clock and non-strobe signals, the signal at the receiver should not ringback into the noise margin region unless it can be shown that the timing can be met with no potential data corruption.

13.2.5. Timing Metrics

The timing metrics consist of flight time and flight time skew. Flight time is defined as the amount of time between the point where the signal on the unloaded driver (or loaded with a test load) crosses a certain threshold and the time where the signal crosses the threshold at the receiver. Flight time skew is the difference in flight times between two nets. Figure 154 illustrates the definition of flight time (assuming a linear edge from V_{IL} through V_{IH}). The flight time should be evaluated at V_{IL}, $V_{threshold}$, and V_{IH}. The methodology is to measure flight time at these three points and record the worst case. This is valid as long as the edge rate seen at the receiver is equal to the edge rate at which it was characterized. If the device was characterized at a different edge rate than the system edge rate, then the following procedures for setup and hold time calculations should be used.

13.2.5.1. Setup Flight Time

If the edge rate seen at the receiver is faster than the specified edge rate, then the traditional method should be used. If the edge rate seen at the receiver is slower than the specified edge rate, then the flight time must be extrapolated from V_{IL} or V_{IH} to $V_{threshold}$ at the specified edge rate. See Figure 156 and Figure 157 for more details.

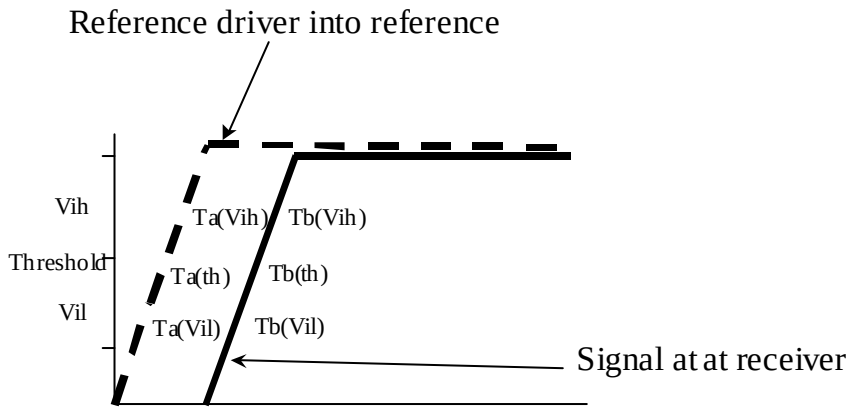
13.2.5.2. Hold Flight Time

If the edge rate seen at the receiver is slower than the specified edge rate, then the traditional method should be used. If the edge rate seen at the receiver is faster than the specified edge rate, then the flight time must be extrapolated from V_{IL} or V_{IH} to $V_{threshold}$ at the specified maximum edge rate. See Figure 156 for more details.

13.2.5.3. Calculating Flight Time for Signals with Corrupt Signal Quality

If nonlinearity or ringback occurs between V_{IL} and V_{IH}, then the last crossing should be extrapolated back at the specification edge rate to $V_{threshold}$. See Figure 156 and Figure 157.

Figure 154. Calculating Rising Edge to Rising Edge Flight Time (Traditional Method)

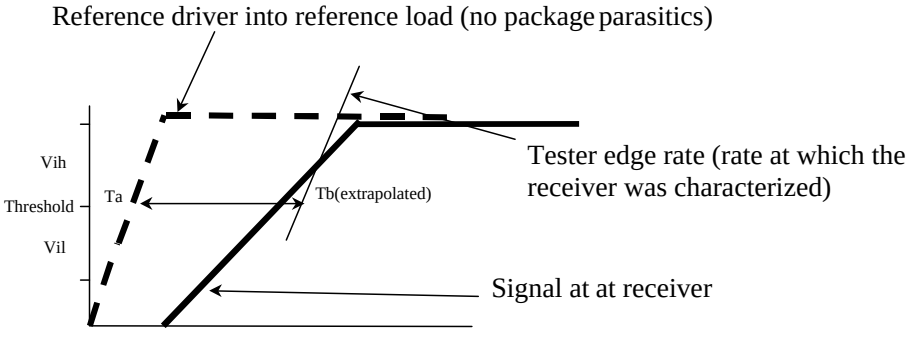


$$\text{Flight Time} = \text{Worst} \begin{cases} Tb(Vih) - Ta(Vih) \\ Tb(th) - Ta(th) \\ Tb(Vil) - Ta(Vil) \end{cases}$$ (Assuming a linear edge Vil and Vih)

Notes:
1. Flight time skew is the difference in flight time between two nets.
2. Assuming a Linear Edge from V_{IL} Through V_{IH} at the Receiver

The following figure shows a method of calculating setup flight time when the edge rate seen at the receiver is slower than the specified edge rate.

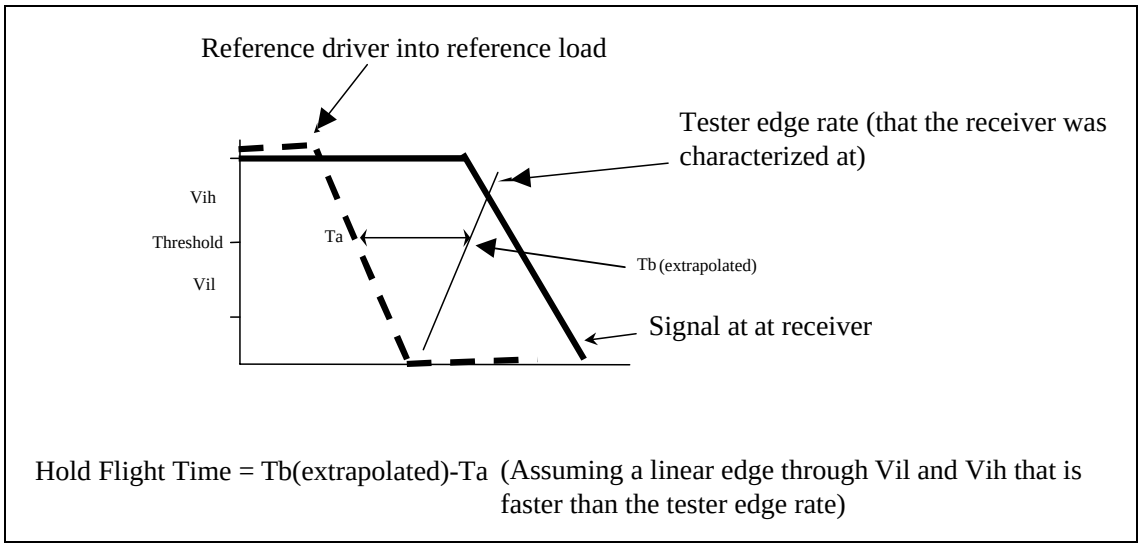
Figure 155. Calculating Setup Flight Time (Receiver Edge Rate is Slower than Specified Edge Rate)



Flight Time = Tb(extrapolated)-Ta (Assuming a linear edge through Vil and Vih that is slower than the tester edge rate)

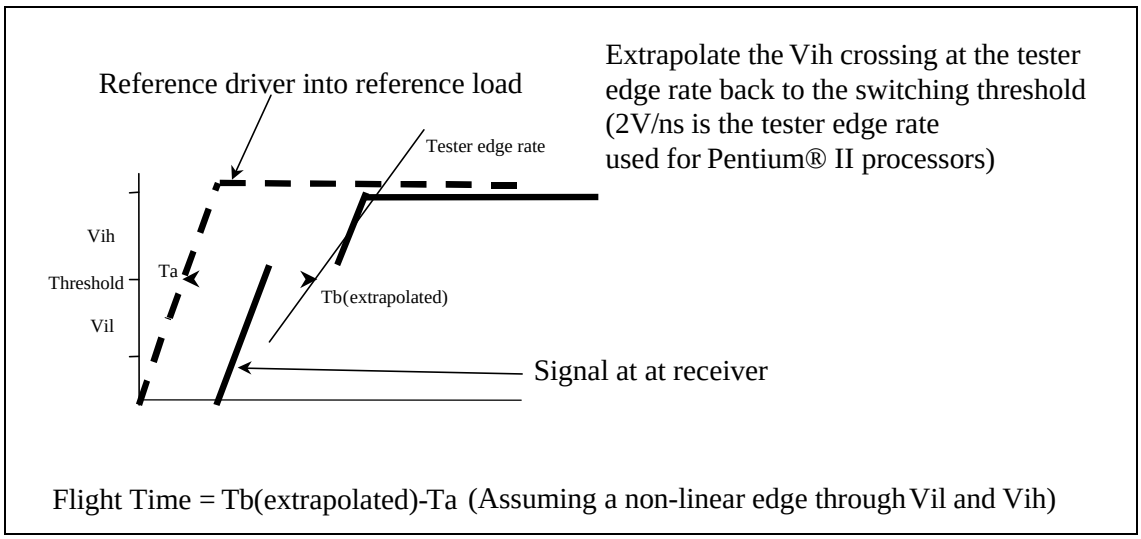
The following figure shows a method of calculating hold flight time when the edge rate seen at the receiver is faster than the specified edge rate.

Figure 156. Calculating Hold Flight Time (Receiver Edge Rate is Faster than Specified Edge Rate)



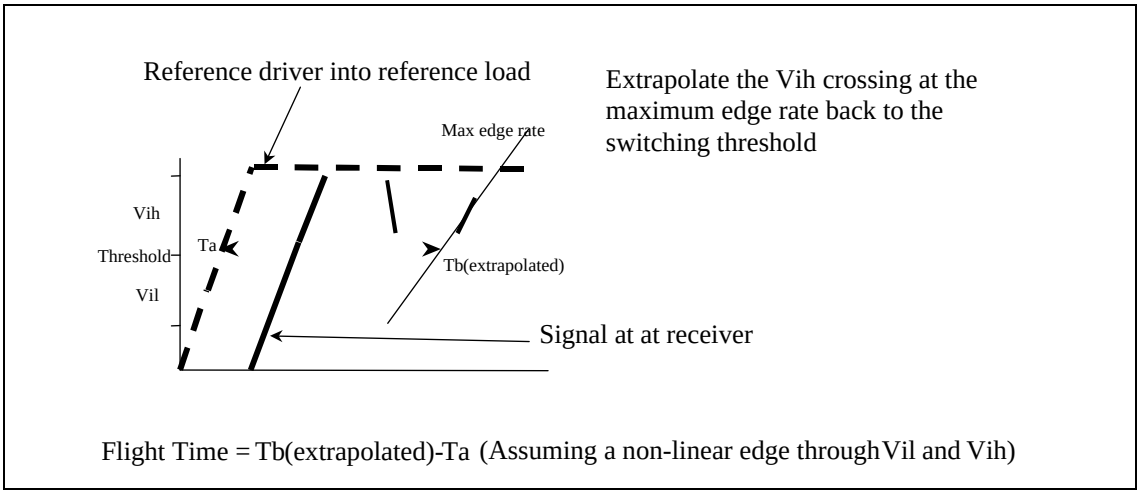
The following figure shows a traditional method of calculating flight time assuming a nonlinear edge from V_{IL} through V_{IH} at the receiver.

Figure 157. Calculating Flight Time (Nonlinear Edge from V_{IL} through V_{IH} at the Receiver)



The following figure shows a traditional method of calculating flight time assuming a ringback violation from V_{IL} through V_{IH} at the receiver.

Figure 158. Calculating Flight Time (Ringback Violation from V_{IL} through V_{IH} at the Receiver)



13.2.5.4. Incorporating Package Effects into the Flight Time

Flight time should be simulated beginning and ending at the pad of the silicon, not at the package pin. This allows the skew due to the package trace length differences to be accounted for. Additionally, the traces on the system board should be line length matched pad-to-pad. Future revisions of the package models for the Pentium 4 processor will include the needed data to make this possible.

13.2.6. Parameter Sweeps and Monte Carlo Analysis

This part of the sensitivity analysis constitutes the bulk of the pre-route design. In this section of the design phase, all system variables shown in Table 56 are varied, and the solution space for the design is determined.

13.2.6.1. Parameter Sweeps

The bulk of the sensitivity analysis consists of parameter sweeps. During a parameter sweep all parameters are held constant except for one or two. The system performance is then observed as the specific variables are being swept. Surface plots can be generated from the results of the parameter sweep. Then the timing and signal quality specifications can be superimposed onto the surface and design limits such as line length, buffer strength, line impedance, etc., can be determined. Figure 152 shows an example of surface plots based on simulated flight times and undershoot. The upper and lower left surface plots show flight time as a function of line lengths L2 and L3. Additional planes are incorporated into the plots that represent the upper and lower flight time specifications. The upper right plot depicts a signal quality metric as a function of L2 and L3 line length. The surfaces of all three of these plots are intersected with the specifications and the resultant solution space for these variables under the conditions of the simulation is shown in the lower right hand side of Figure 152.

Note that the sweeps should be performed using different switching speeds to capture the majority of ISI noise. If *N* is the fastest switching speed for a given bus, then simulations should be performed at a

frequency of *N*, *½N*, and *¼N*. The difference between the timings at the different switching frequencies is a good approximation of the ISI noise. Final checks on fully coupled models with long worst-case bit patterns should be performed in order to find any ISI effects not captured in this analysis. This sweeping technique can be used extensively to get initial bounds on all variables in the system. The resultant solution space will be known as the "Phase 1 solution space."

The drawback of this method is that the sweeps are only good for evaluating two variables at a time. While the two parameters of interest are being varied, the other parameters in the system are held constant at a value that may not yield worst-case performance. For example, if the line lengths are being swept all line and buffer impedances, package parasitics, receiver capacitance, etc., are held at fixed values. Every effort should be made to set these parameters so that the performance will approach worst case. Use Intel's recommendations as a baseline, and work from there to refine corner conditions specific to your environment. To ensure that the worst-case performance is captured, all system variables must be varied simultaneously. This can be accomplished using a targeted Monte Carlo analysis.

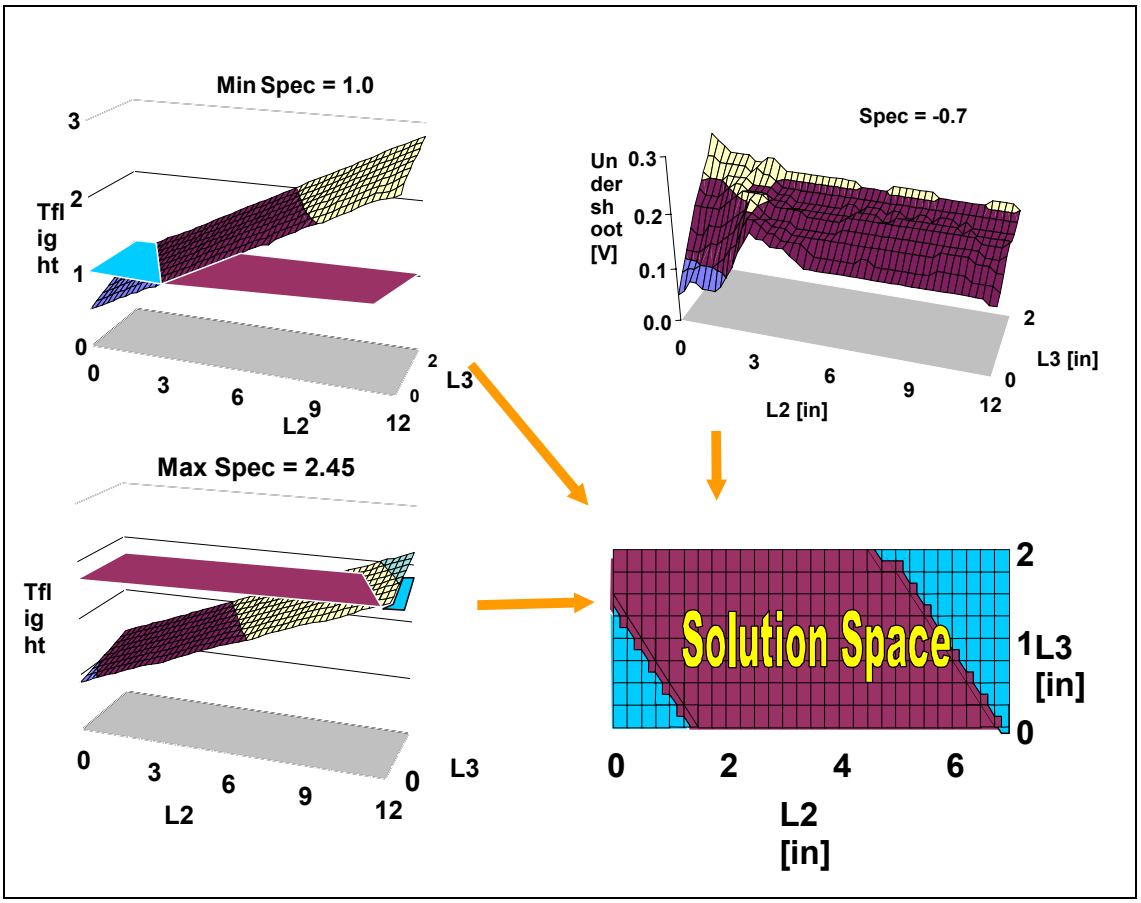
13.2.6.1.1. Targeted Monte Carlo Analysis

Targeted Monte Carlo (TMC) analysis can be used to further refine the Phase 1 solution space and ensure that the worst-case performance has been captured. Performing a full Monte Carlo analysis over all system variables is inefficient because a large number of simulations must be performed to statistically guarantee that all worst-case conditions are captured. If a TMC analysis is performed on the boundaries of the Phase 1 solution space determined by the parametric sweeps, the number of simulations required will decrease dramatically and the solution space can be refined by changing the variables that were held constant during the sweep.

Figure 152 illustrates the area where the TMC analysis was performed to refine the Phase 1 solution space.

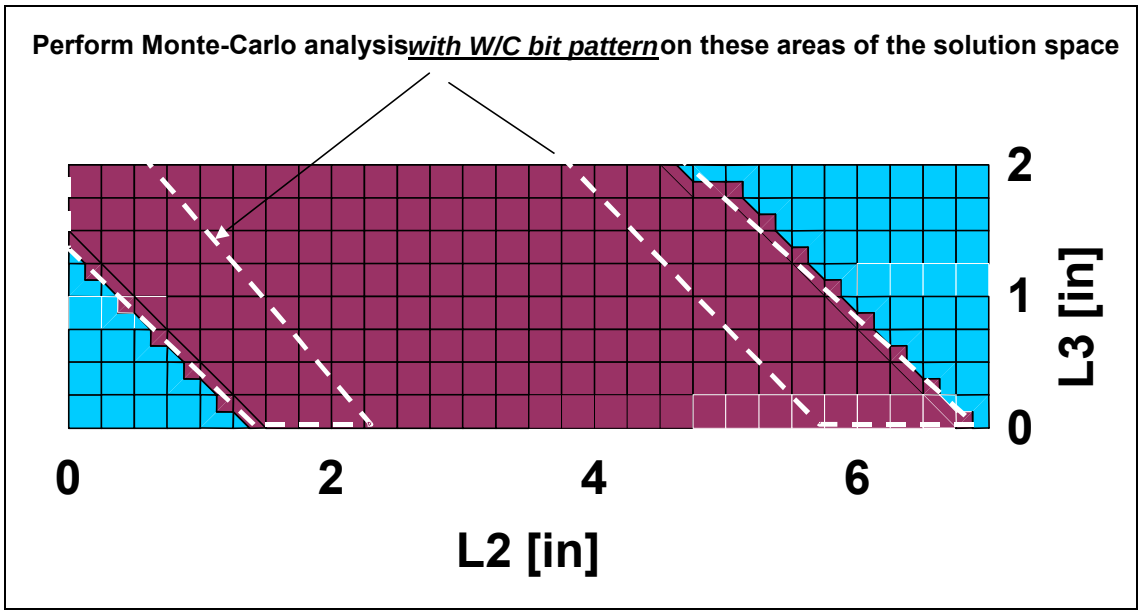
Figure 153 shows the results of the TMC analysis and shows the final solution space. This final solution space will be referred to as the "Phase 2 solution space." Note that the worst-case bit pattern should be included in the TMC analysis.

Figure 159. Example of Sweeps Used to Evaluate the Length Limits of Trace L2 and L3



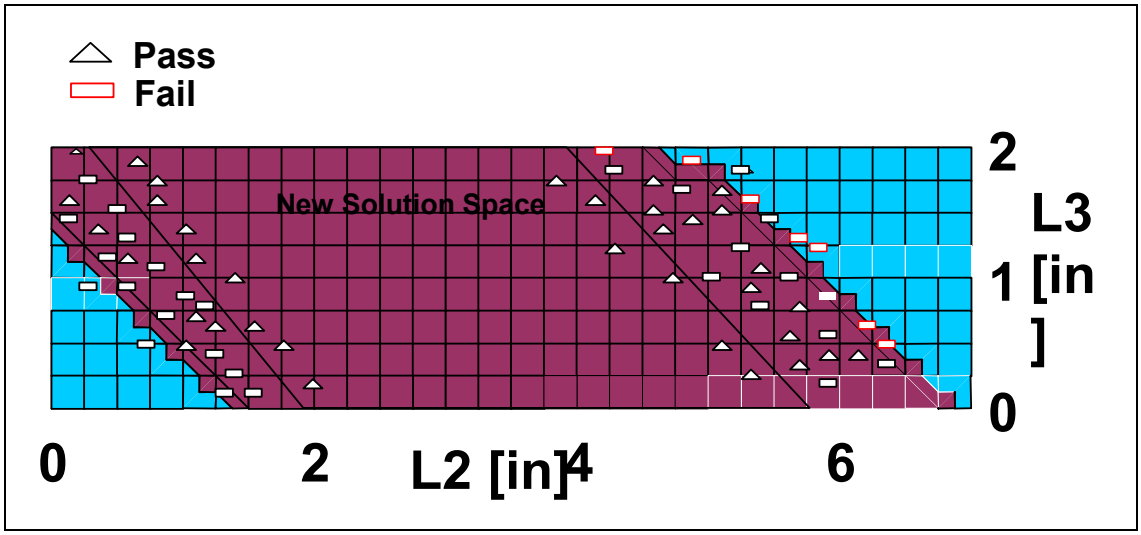
Monte Carlo Analysis should be performed on these areas of the Phase 1 solution space shown in the following figure.

Figure 160. Monte Carlo Analysis (Perform on These Areas of the Phase 1 Solution Space)



The following figure shows the results of targeted Monte Carlo (TMC) analysis and the resultant Phase 2 solution space for variables L2 and L3

Figure 161. Targeted Monte Carlo (TMC) Analysis (Phase 2 Solution Space for Variables L2 and L3)



13.2.6.2. Final Solution Space

The final solution space will be referred to as the “Phase 3 solution space.” This phase incorporates effects that are too computationally demanding to easily include in the Phase 1 or Phase 2 solution spaces. A final check on the worst-case nets under fast and slow conditions should be performed. The sweeps and the Monte Carlo analysis already performed should allow the worst-case conditions to easily be chosen. These simulations should be performed using a fully coupled crosstalk model. The results of the final check should be used to further narrow the solution space.

The routing guidelines should incorporate the entire solution space determined during the sensitivity analysis in order to provide the maximum amount of flexibility. When some portions of the routing guidelines cannot be met due to physical real estate limitations or manufacturing concerns, new solutions need to be determined.

14. System Theory

This chapter provides in-depth information about signal technology and system signal interference.

14.1. AGTL+

AGTL+ is the electrical system bus technology. It is an incident wave switching, open-drain bus with integrated pull-up resistors (p-channel FETs) that provide both the high logic level and the termination.

14.2. Inter-Symbol Interference

Inter-symbol interference (ISI) is the effect of a previous signal (or transition) on the interconnect delay. When a signal is transmitted down a transmission line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI can impact both the timing and the signal integrity. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. Thus, ISI is a major concern in any high-speed design where the period is smaller than the delay of the transmission line. The following figure shows an example of how ISI can affect timing. In this example the starting voltage of the driver is different from the idle state starting voltage. This figure illustrates the ISI effect on both timing and signal integrity.

One method of capturing most of the timing impact due to ISI is to perform parameter sweeps at the fastest bus period, and then at 2x and 3x multiples of the fastest bus period. For example, if the fastest frequency at which the bus will operate is 400 MT, then the pulse duration of a single bit is 2.5 ns (5 ns period). The data pattern should be repeated with pulse durations of 5 ns and 7.5 ns (10 ns and 15 ns periods). This represents the following data patterns transitioning at the highest bus rate.

01010101010101

00110011001100

00011100011100

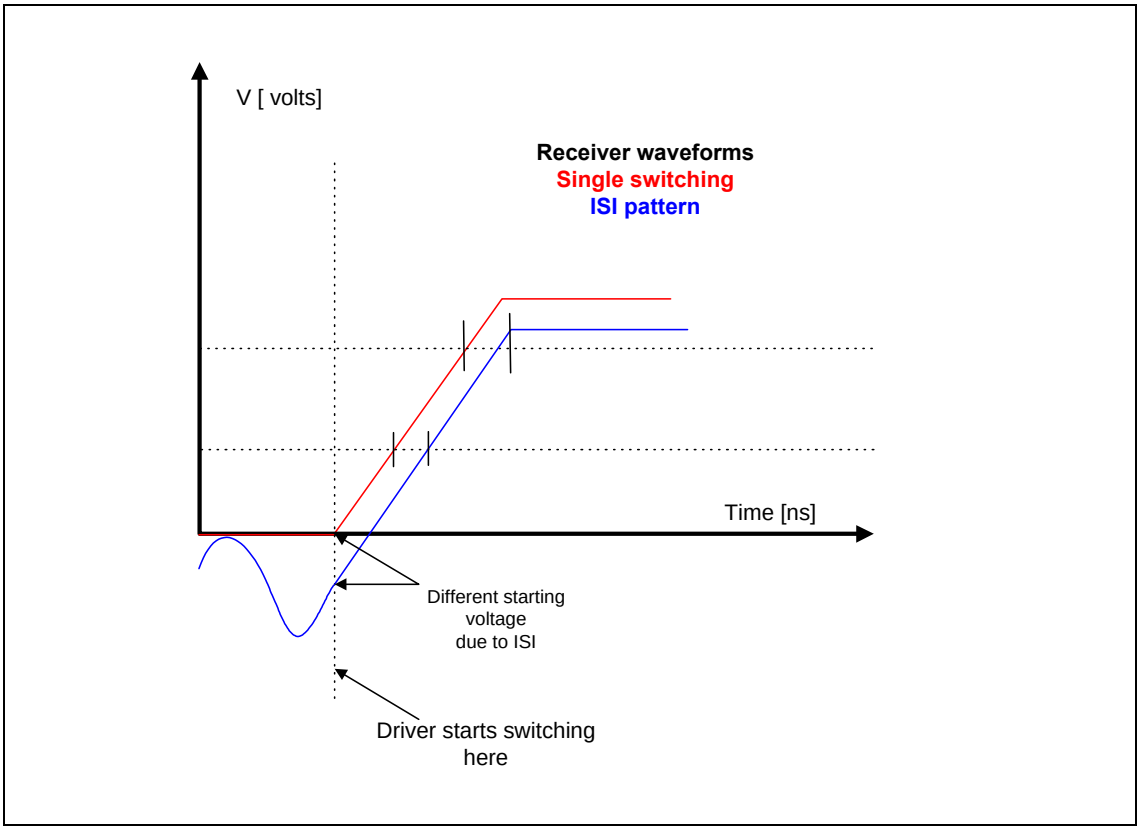
The worst-case results of these patterns can be used to produce the Phase 1 solution space. The maximum difference in flight time between these patterns produces a first order approximation of the ISI impact.

The final solution space must account for the full ISI variations. This can be done by performing targeted simulations at the edges of the Phase 2 solution space using a long pseudo-random pulse train. If the timing impact due to ISI does not violate any timing or signal integrity specifications, then the Phase 2 solution space is acceptable. If timing violations do occur, then steps should be taken to minimize reflections on the bus, and in turn, reduce the ISI. Typically, the best way to limit reflections is to reduce impedance variations and minimize discontinuities (e.g., by shortening stubs and connectors, matching impedance, etc.)

The worst-case ISI can be evaluated using the following procedure:

- Simulate the longest net on the bus using a long pseudo-random bit pattern for both the fast and slow cases.
- Take the first transition of the ISI simulation as the baseline.
- Determine the rising and falling delays for each bus transition.
- Subtract the minimum and maximum delays from the baseline delays and find the worst-case difference.
- Take the smallest negative and the greatest positive difference. This should be the worst-case ISI impact on timing.

Figure 162. Example of ISI Impact on Timing and Signal Integrity



14.3. Crosstalk

Crosstalk is caused through capacitive and inductive coupling between networks. Crosstalk can be backward or forward. Backward crosstalk creates an induced signal on a victim network that travels in a direction opposite that of the aggressor's signal. Forward crosstalk creates a signal that travels in the same direction as the aggressor's signal. On an AGTL+ bus a driver on the aggressor network is not necessarily at the end of the network. Therefore, it sends signals in both directions on the aggressor's network. The signal propagating in each direction causes crosstalk on the victim network. This effect is illustrated in Figure 163, which shows a driver on the aggressor network and a receiver on the victim network. Figure 163 shows two aggressors on each side of the victim. Additional aggressors are possible in the z-direction if adjacent signal layers are not routed in mutually perpendicular directions. Because coupling coefficients decrease rapidly with increasing separation, it is rarely necessary to consider aggressors that are at least five line widths separated from the victim. Additionally, there is crosstalk internal to the IC packages, which can also affect the signal quality.

Figure 163. Propagation on Aggressor Network

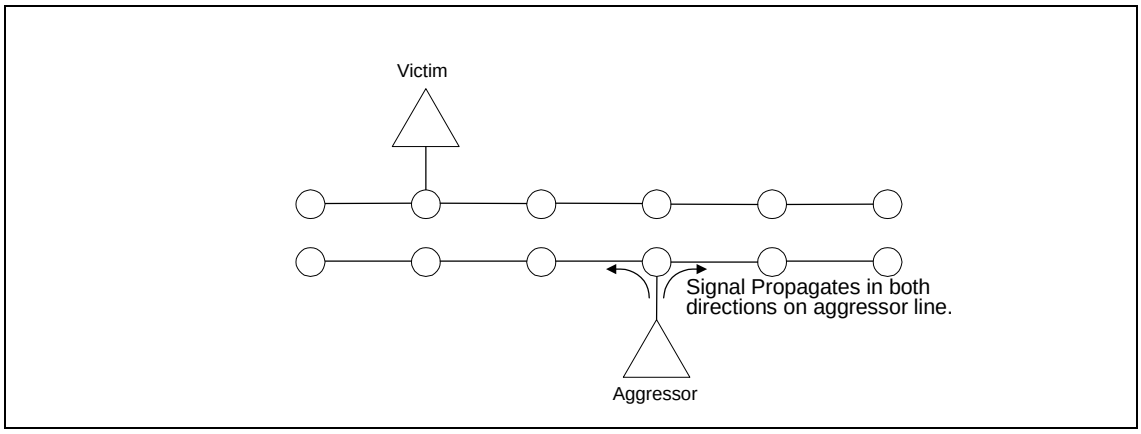


Figure 164. Aggressor and Victim Networks

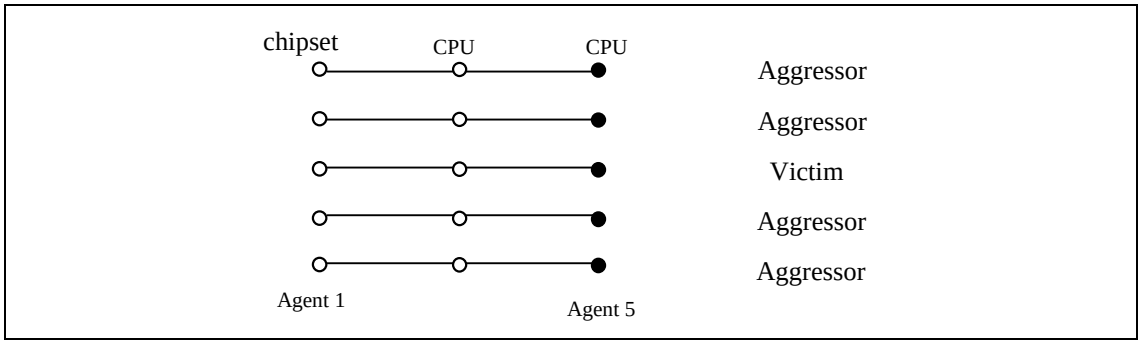
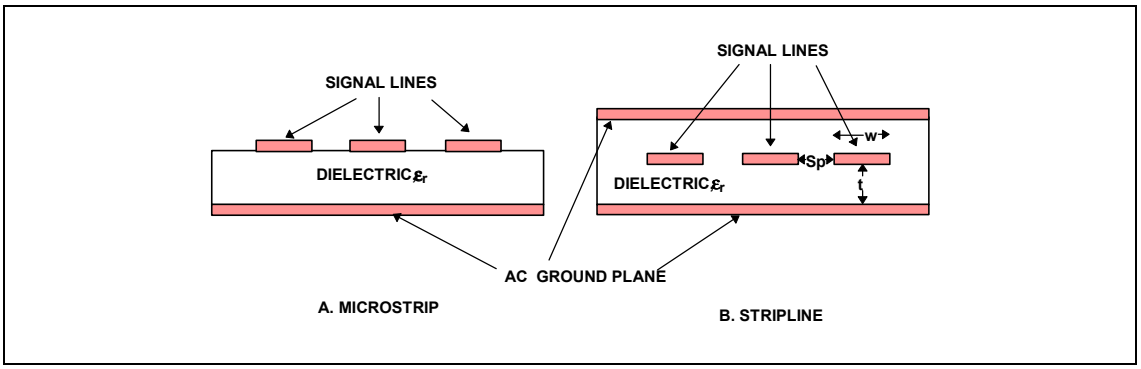


Figure 165. Transmission Line Geometry of Microstrip and Stripline



Backward crosstalk is present in both stripline and microstrip geometry. The backward-coupled amplitude is proportional to the backward crosstalk coefficient, the aggressor's signal amplitude, and the coupled length of the network. Backward crosstalk reaches a maximum (and remains constant) when the propagation time on the coupled network length exceeds one half of the rise time of the aggressor's signal. Assuming the ideal ramp on the aggressor from 0% to 100% voltage swing and the rise time on an unloaded-coupled network, then the following equation applies.

Equation 27. Length for Maximum Backward Crosstalk

$$Length\ for\ Max\ Backward\ Crosstalk = \frac{½ \times Rise\ Time}{Board\ Delay\ Per\ Unit\ Length}$$

An example calculation if fast corner fall time is 1.5 V/ns and board delay is 175 ps/inch (2.1 ns/foot) follows:

Fall time = 1.5 V/1.5 V/ns = 1 ns

Length of maximum backward crosstalk = ½ * 1 ns * 1000 ps/ns /175 ps/in = 2.86 inches

Agents on the AGTL+ bus drive signals in each direction on the network. This will cause backward crosstalk from segments on two sides of a driver. The pulses from the backward crosstalk travel toward each other and will meet and *add* at certain moments and positions on the bus. This can cause the voltage (noise) from crosstalk to double. The following table provides example coupling factors for various stripline space to width to dielectric thickness ratios (see Figure 163) with dielectric constant $\varepsilon_r = 4.5$, $V_{OH\_MAX} = 1.5$ V, and $Z_0 = 65\ \Omega$. Note that the fast edge rates of falling edges place limits on the maximum-coupled length allowable. Also, note that multiple parallel-coupled lines will increase the impact on the noise budget.

Forward crosstalk is absent in stripline topologies, but present in microstrip. This is for the ideal case with a *uniform* dielectric constant. In actual boards, forward crosstalk is *nearly* absent in stripline topologies, but *abundant* in microstrip. The forward-coupled amplitude is proportional to the forward crosstalk coefficient, the aggressor's signal edge rate (*dv/dt*), and the coupled network's electrical length. The forward crosstalk coefficient is also a function of the geometry. Unlike backward crosstalk, forward crosstalk can grow with coupled section length, and may transition in a direction similar to or opposite to that of the aggressor's edge. Unlike backward crosstalk, forward crosstalk on the victim signal will continue to grow as it passes through more coupled length before the aggressor's wave front is absorbed by the termination resistance.

To Minimize Crosstalk

- Route adjacent trace layers in different directions (orthogonally preferred) to minimize the forward and backward crosstalk that can occur from parallel traces on adjacent layers.
- Maximize the spacing between traces. Where traces have to be close and parallel to each other, minimize the length that they are close together, and maximize the distance between sections that have close spacing. Routing close together could occur where multiple signals have to route between a pair of pins. When this happens, the signals should be spread apart where possible. Also, note that routing multiple layers in the same direction between reference planes can result in parallel traces that are close enough to each other to have significant crosstalk.
- Minimize the variation in board impedance (Z0). For the example topologies covered in this guideline, either 50 Ω ± 15% was assumed.
- Minimize the nominal board impedance within the AGTL+ specification while maintaining the same line width/spacing ratio. For a given dielectric constant, this reduces the line width/trace height ratio, which reduces the backward and forward crosstalk coefficients. Having reduced crosstalk coefficients reduces the magnitude of the crosstalk.
- Minimize the dielectric constant used in the PCB fabrication. As above, all else being equal, this puts the traces closer to their reference planes and reduces the magnitude of the crosstalk.
- Watch out for voltage doubling at a receiving agent, caused by the adding of the backward crosstalk on either side of a driver. Minimize the total network length of signals that have coupled sections. If there has to be closely spaced/coupled lines, place them near the center of the net. This causes the point in time that voltage doubling occurs to be before the setup window.
- Route synchronous signals that could be driven by different components in separate groups to minimize crosstalk between these groups. The Pentium 4 processor uses a split transaction bus with six independent sub buses (arbitration, request, error, snoop, response, and data). This implies that in a given clock cycle, each sub bus could be driven by a different agent. If these two agents are at the opposite process corner (one fast and one slow), then separating the bus types will reduce the impact of crosstalk.

Table 58. Example Backward Crosstalk Coupling Factors

Space: Width:Thickness	Coupling Factor	Maximum Crosstalk
24:4:8	0.65%	9.8 mV
20:4:8	1.3%	19. 5 mV
16:4:8	1.75%	26.2 mV
14:4:8	2.5%	37.5 mV
12:4:8	3.4%	51.0 mV
8:4:8	6.55%	98.2 mV
4:4:8	13.5%	202.5 mV

NOTES:

1. $\varepsilon r = 4.5$, $V_{OH\_MAX} = 1.5$ V, and $Z_0 = 65\ \Omega$

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15. Debug Port Routing Guidelines

In the Pentium 4 processor based system, debug port can be implemented either as an **on board debug port** or as a **debug port interposer.**

15.1. On Board Debug Port

15.1.1. Signal Layout Guidelines

The Debug Port, Test Access Port (TAP), is expected to be treated as a part of the Processor Cluster (processors and chipset members). It will need to be part of the Processor Cluster JTAG scan chain and connected to the bus clock and system bus signals. This implies that the designer will place the Debug Port within 2-6 inches of the nearest Processor Cluster member and will not cross board boundaries.

There are three signal groups within the debug port. Each group has a different set of layout requirements. The system signals are treated as analog signals by the ITP. These are special ITP-specific signals and are both inputs and outputs. These resources may be shared with local JTAG tools and are also both inputs and outputs. The execution signals are AGTL+ level and are the most critical in terms of routing considerations.

15.1.1.1. System Signal Layout Guidelines

BCLK has very specific routing constraints with respect to BPM[5:0]#, RESET#, and FBO. BCLK must be routed to recover the BPM[5:0]# and RESET# system bus signals. FBO must have the same phase relationship with BCLK at the Debug Port as TCK has with BCLK at the closest Processor.

Table 59. System Signal Layout Guidelines

Signal	Description
PWR (without local JTAG)	Route with normal trace less than 5 inches to the debug port connector. Add a 1.5 kΩ resistor in series to V_{CC}
PWR (with local JTAG)	Route with normal trace less than 5 inches to the debug port connector. Add open drain control gate with 1.5 kΩ pull-up resistor to V_{CC}
BCK[1:0]	This is a critical system signal requiring timing and signal integrity considerations. The ITP load model consists of: • 0.25 inch 50 Ω connector pin with 180ps/inch flight time • 1 inch 50 Ω trace on FR4 (stripline) • QS3384 gate element voltage limited analog switch • 5 pF gate loading on clock driver • Terminator on target matches all other BCLK load models BCLK must be delayed to the Debug Port by the propagation delay of the BPM[5:0]# and RESET# signals from the closest processor. This will insure that these critical signals will have the same phase relationship at the Debug Port as seen by the closest processor. The propagation delay fixed by BPM[5:0]# and RESET# and added to BCLK[1:0] must also be the total propagation delay of FBO (TCK) from the processor back to the Debug Port.
FBO	FBO is used to monitor the phase relationship of TCK to BCLK and recover TDO; therefore, it must have special attention during routing. FBO contains a 75 Ω end termination. The FBO recovery requires a clean rising edge with a minimum signal swing of 0.8 V peak through its 1 V transition region, and a V_{IH} (max) of 2.5 V. FBO connects to a buffered copy of TCK and is routed to the Debug Port. It is important that the phase of FBO-to- BCLK at the Debug Port is the same as the TCK to BCLK phase at the closest processor.
FBI	FBI is a fast edge copy of TCK that may be used as an input to the TCK buffer. It has a 25 Ω series resistor and should not be heavily loaded.
DBR# DBA#	This is a non-critical route. Target circuit is a 150 Ω to 240 Ω pull-up into the master reset generator. The ITP driver is a FET switch closure to ground. DBR# is asserted on a BCLK boundary and released on a BCLK boundary, as an artifact of the ITP and not to satisfy any known constraints. Pull-up voltage can be up to 10 V without causing any problem for the ITP. Pull-up voltage can be up to 3.3 V.

15.1.1.2. JTAG Signal Layout Guidelines

TCK is very sensitive. Reflections that cause mid-threshold ringing will render the primary system debug tool inoperative. Simulate the behavioral model, and verify signal integrity using the system bus signal analysis tools. The following table provides the JTAG signal layout guidelines. It is highly recommended that TCK be simulated to ensure proper signal quality is maintained.

Table 60. JTAG Signals Layout Guidelines

Signal	Description
TCK	Critical JTAG signals that requires timing and signal integrity considerations. This is a clock signal and should be simulated.
TMS, TDI, TDO, TRST#	Critical JTAG signals that require timing and signal integrity considerations. TMS must be routed with TCK. On target resistors should be used to force TRST# assertion (low). Be sure to observe setup and hold time requirements.

15.1.1.3. Execution Signal Layout Guidelines

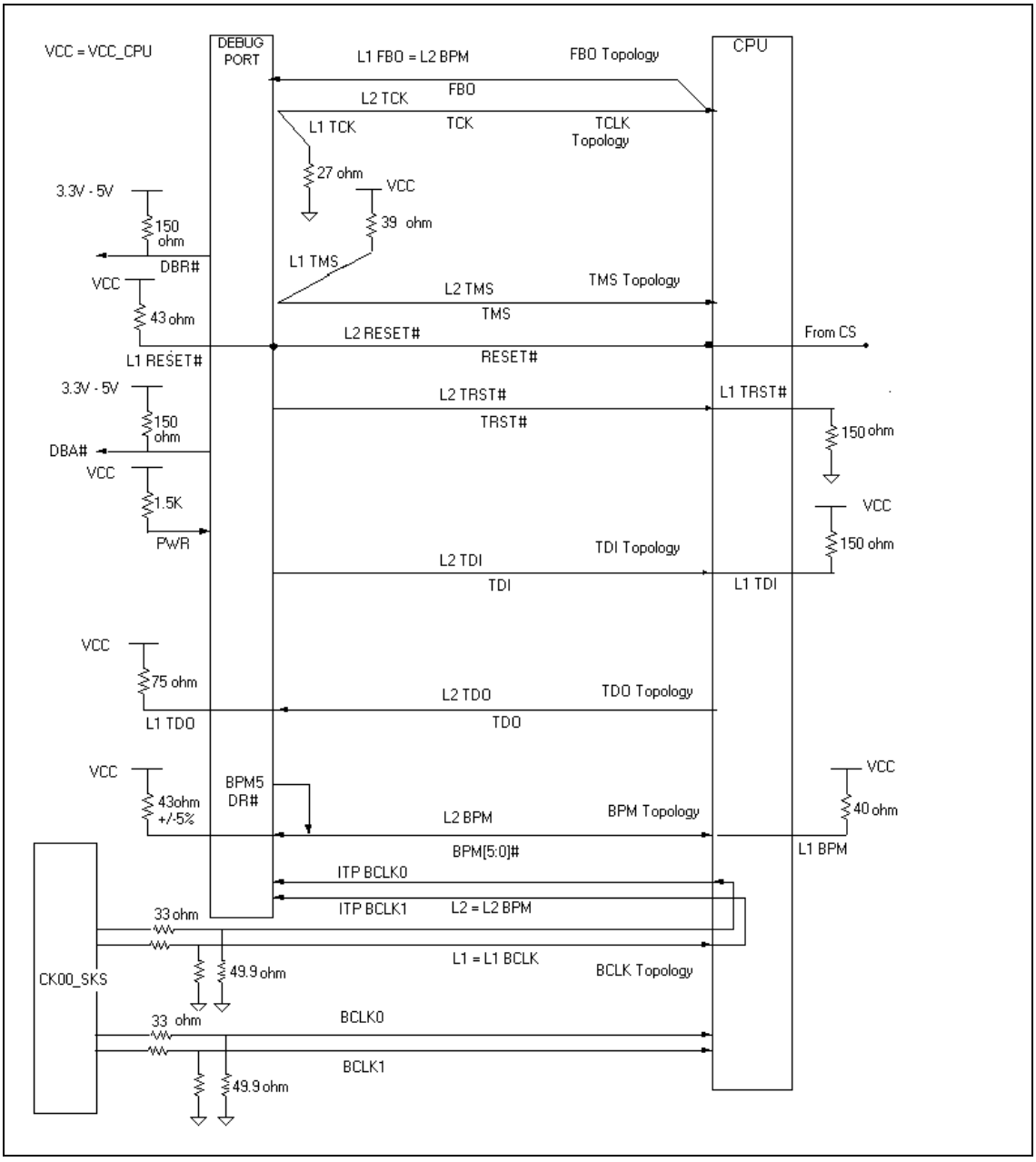
The flight time of the BPM[5:0]# and RESET# signal from the processor must be added to the arrival time of BCLK at the Debug Port. It must also match the flight time of FBO from the processor to the Debug Port. The following table provides the execution signal layout guidelines.

Table 61. Execution Signals Layout Guidelines

Signal	Description
BPM[5:0]# RESET#	These are system bus AGTL+ level signals that are routing critical. The Debug Port load is a 0.65 inch stub, approximately 75 Ω trace impedance with 25 Ω series resistance, and 50 kΩ to ground. Capacitance is approximately 4 pF at signal end. BCLK for these signals should be routed with the same timing considerations as the processor load, with the caveat that additional flight time which matches the routing of the execution signals is permitted. These signals on the Debug Port have a setup time of 1.4 ns and a hold time of 800 ps relative to BCLK at the port pins.
BPM5DR#	BPM5DR# should be connected to the BPM5# pin at the debug port connector to enable the ITP or run-time control tool to drive BPM5# at reset.

15.1.2. Routing Topology

Figure 166. On Board Debug Port Routing Topology



15.1.3. Routing Guidelines

Table 62. On-Board Debug Port Routing Guidelines

Parameter	Trace Impedance	Trace Spacing	Description
TCK	50 Ω	10 mil	
L1 TCK			1 inch max from Debug Port (DP) to RTT
L2 TCK			12 inches max from DP to processor
RTT TCK			27 Ω
FBO	50 Ω	10 mil	
L1 FBO			L1 FBO = L2 BPM
TMS	50 Ω	10 mil	
L1 TMS			1 inch max from DP to RTT
L2 TMS			12 inches max from DP to processor
RTT TMS			39 Ω ±5%
TRST#	50 Ω	10 mil	
L1 TRST#			1 inch max from processor to RTT
L2 TRST#			20 inches max from DP to processor
RTT TRST#			150 Ω ±5%
RESET#	50 Ω	10 mil	
L1 RESET#			1 inch max from DP to RTT
L2 RESET#			L2 RESET# = L2 BPM max
RTT RESET#			43 Ω ±5%
TDI	50 Ω	10 mil	
L1 TDI			1 inch max from processor to RTT
L2 TDI			20 inches max from DP to processor
RTT TDI			150 Ω ±5%
TDO	50 Ω	10 mil	
L1 TDO			1 inch max from DP to RTT
L2 TDO			20 inches max from DP processor
RTT TDO			75 Ω ±5%

Parameter	Trace Impedance	Trace Spacing	Description
BPM	50 Ω	10 mil	
L1 BPM			1 inch max stub length from processor or DP to RTT. Length should be symmetric at each end of the bus
L2 BPM			1 inch – 8 inches from DP to processor. Limited by max BCLK length (1 inch - 8 inches) from DP to processor. Limited by max BCLK length. Length compensation within the BPM signal group is not required.
BPM5DR#			Connect to BPM5#
RTT BPM			43 Ω ±5% , 39 Ω will work
ITP BCLK	50 Ω	10 mil	
L1 ITP BCLK			L1 BCLK0 + L2 BPM
L2 ITP BCLK			L2 BCLK1 + L2 BPM
Total length L1 +L2			Total routed length of BCLK0 and BCLK1. Not to exceed maximum clock routing length. Route from the clock chip directly to DP. Figure 166 shows L1 routed from clock chip to processor for illustration of length compensation only.
L1 BCLK0			Equal to the BCLK0 length from CK00 to processor
L2 BCKL1			Equal to the BCLK1 length from CK00 to processor
RS			33 Ω ±5%
RT			49.9 Ω ±1%

NOTES:

1. On production boards DP can be depopulated. Although, termination on the TAP signals that are inputs to the processor (TCK, TDI, TMS, TRST#) and those that are I/O (BPM) should be maintained.

16. Schematic Review Checklist

16.1. Intel® Pentium® 4 Processor Checklist (All Signals)

All signals of the Pentium 4 processor are provided in this section.

Checklist Items	Recommendations	Reason/Impact/Documentation
A[35:3]#	• Connect A[31:3]# to MCH. Leave A[35:32]# as No Connect.	• Chipset does not support extended addressing over 4GB, leave A[35:32]# unconnected. • AGTL+ source synch I/O signal • Refer to the schematics.
A20M#	• Connect to ICH2. No pull-up required.	• Asynch GTL+ Input Signal • Refer to Section 5.4.1.2.
ADS#	• Connect to MCH	• AGTL+ common clock I/O signal • Refer to the schematics.
ADSTB[1:0]	• Connect to MCH	• AGTL+ source synch I/O signal • Refer to the schematics.
AP[1:0]#	• Leave as No Connect	• Chipset does not support parity protection on the address bus. • AGTL+ common clock I/O signal • Refer to the schematics.
BCLK[1:0]	• Connect to SKx_SKS clock. Refer to clock routing guidelines in the latest rev of the design guide. • Connect 20 – 33 Ω series resistor on each clock signal. • Connect a “shunt source termination (Rt)” resistor to GND for each signal on processor side of the series resistor. The Rt value should be 49.9 Ω ±1% for 50 Ω MB impedance.	• Rt resistors should be selected to match the characteristic impedance of the board. • System bus clock signal • Refer to Section 4.1 of this document.
BINIT#	• Leave as No Connect.	• Chipset does not support this signal. • AGTL+ common clock I/O signal • Refer to the schematics.
BNR#	• Connect to MCH	• AGTL+ common clock I/O signal • Refer to the schematics.
BPRI#	• Connect to MCH	• AGTL+ common clock input signal • Refer to the schematics.

Checklist Items	Recommendations	Reason/Impact/Documentation
BR0#	• Terminate to V_{CC} with a 36 Ω to 46 Ω resistor. Connect to the MCH.	• The Intel® 850 chipset contains on-die termination for the BR0# signal. The Intel® Pentium® 4 processor does not contain on-die termination for this particular AGTL+ signal; thus, external termination is required only on the processor end. BR0# termination should equal the resistance value of on die AGTL+ termination resistance (Rtt) value. • AGTL+ common clock I/O signal • Refer to Section 5.4.1.6
COMP[1:0]	• Terminate to GND with a 43.2 Ω ±1% resistor as close as possible to the pin.	• Each COMP pin requires a separate resistor for each pin. • Refer to Section 5.4.1.7.
D[63:0]#	• Connect to MCH	• AGTL+ source synch I/O signal • Refer to the schematics.
DBI[3:0]	• Connect to MCH	• AGTL+ source synch I/O signal • Refer to the schematics.
DBSY#	• Connect to MCH	• AGTL+ common clock I/O signal • Refer to the schematics.
DEFER#	• Connect to MCH	• AGTL+ common clock input signal • Refer to the schematics.
DP[3:0]#	• Leave as No Connect	• Chipset does not support Enhanced Data Bus Parity. • AGTL+ common clock I/O signal • Refer to the schematics.
DRDY#	• Connect to MCH	• AGTL+ common clock I/O signal • Refer to the schematics.
DSTBN[3:0]	• Connect to MCH	• AGTL+ source synch I/O signal • Refer to the schematics.
DSTBP[3:0]	• Connect to MCH	• AGTL+ source synch I/O signal • Refer to the schematics.
FERR#	• Terminate to V_{CC} with a 56 Ω ±5% resistor. • Connect to ICH2.	• This output signal is not terminated on the processor. Termination is required on the system board. • Asynch GTL+ output signal • Refer to Section 5.4.1.1.
GTLREF[3:0]	• Should be set to 2/3 of V_{CC}. Processor should have at least 2 dedicated voltage dividers for GTLREF signals. Requires a 49.9 Ω ±1% termination resistor to V_{CC} and a 100 Ω ±1% pull-down resistor to GND as well as additional decoupling capacitors depending on topology.	• Correct settings are critical. This signal controls the signal reference of the AGTL+ input pins. • Refer to Section 11.3.5.

Checklist Items	Recommendations	Reason/Impact/Documentation
HIT#	• Connect to MCH	• AGTL+ Common Clock I/O Signal • Refer to the schematics.
HITM#	• Connect to MCH	• AGTL+ Common Clock I/O Signal • Refer to the schematics.
IERR#	• Leave as a No Connect	• Chipset does not support this signal. • Asynch GTL+ output signal. • Refer to the schematics.
IGNNE#	• Connect to ICH2. • No pull-up required.	• Termination not required. • Asynch GTL+ input signal. • Refer to Section 5.4.1.2.
INIT#	• Connect to ICH2 and Firmware Hub (FWH). • No pull-up required.	• Termination not required. • Asynch GTL+ input signal. • Refer to the schematics. • Refer to Section 5.4.1.2.
LINT[1:0]	• Connect to ICH2. LINT[1] connects to ICH2 NMI and LINT[0] connects to ICH2 INTR. • No pull-up required.	• Asynch GTL+ Input Signal. • Refer to Section 5.4.1.2.
LOCK#	• Connect to MCH	• AGTL+ Common Clock I/O Signal • Refer to the schematics.
MCERR#	• Leave as No Connect	• Chipset does not support this signal. • AGTL+ common clock I/O signal • Refer to the schematics.
PROCHOT#	• Terminate to V_{CC} with a 56 Ω ±5% resistor. • Connect to ICH2.	• Asynch GTL+ output signal • Refer to Section 5.4.1.1.
PWRGOOD	• Terminate to V_{CC} with a 300 Ω ±5% resistor. • Connect to ICH2.	• Asynch GTL+ input signal • Refer to Section 5.4.1.3.
REQ[4:0]#	• Connect to MCH	• AGTL+ source synch I/O signals • Refer to the schematics.
Reserved	• Reserved signals must remain as a No Connect.	•
RESET#	• Terminate to V_{CC} with a 43 Ω ±5% resistor. • Connect to the MCH.	• AGTL+ common clock input signal • Refer to the schematics.
RS[2:0]#	• Connect to MCH	• AGTL+ common clock input signal • Refer to the schematics.

Checklist Items	Recommendations	Reason/Impact/Documentation
RSP#	• Leave as No Connect.	• Chipset does not support this signal. • AGTL+ common clock input signal • Refer to the schematics.
SKTOCC#	• Connect to glue logic if pin is used.	• Processor pulls this signal to GND. System board designers may use this pin to determine if the processor is present in the socket. • Refer to the schematics.
SLP#	• Connect to ICH2. • No pull-up required.	• Asynch GTL+ input signal • Refer to Section 5.4.1.2.
SMI#	• Connect to ICH2. • No pull-up required.	• Asynch GTL+ input signal • Refer to Section 5.4.1.2.
STPCLK#	• Connect to ICH2. • No pull-up required.	• Asynch GTL+ input signal • Refer to Section 5.4.1.2.
TESTHI	• Option 1: Terminate individually to V_{CC} with 1 kΩ–10 kΩ resistor. • Option 2: TESTHI[1:0] may be tied together and terminated to V_{CC} via 1 kΩ–4.7 kΩ resistor. — TESTHI[7:2] may be tied together and terminated to V_{CC} via 1 kΩ–4.7 kΩ resistor. — TESTHI[10:8] may be tied together and terminated to V_{CC} via 1 kΩ–4.7 kΩ resistor	• Tying any of the TESTHI pins together will prevent the ability to perform boundary scan testing. • Refer to *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet
THERMTRIP#	• Terminate to V_{CC} via 56 Ω ±5% resistor.	• Asynch GTL+ output signal • Refer to Section 5.4.1.4.
TRDY#	• Connect to MCH	• AGTL+ common clock input signal • Refer to the schematics.
V_{CCA}	• Connect with isolated power circuitry to V_{CC}.	• Isolated power for internal processor system bus PLLs. • Refer to Section 5.4.1.5 and Section 11.4.2.
$V_{CCIOPLL}$	• Connect with isolated power circuitry to V_{CC}.	• Isolated power for internal processor system bus PLLs • Refer to Section 5.4.1.5 and Section 11.4.2.
$V_{CCSENSE}$	• Connect to additional glue logic if used. This signal is an output signal.	• Isolated low impedance connection to processor core power (V_{CC}) • Refer to *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet • Refer to the schematics.
V_{ID}[4:0]	• Connect to VR or VRM.	• Refer to the schematics. • Refer to the *VRM9.0 DC-DC Converter Design Guidelines*

Checklist Items	Recommendations	Reason/Impact/Documentation
V_{SSA}	• Connect with isolated power circuitry to V_{CC}.	• Isolated GND for internal PLLs • Refer to Section 5.4.1.5 and Section 11.4.2.
$V_{SSSENSE}$	• Connect to additional glue logic if used. This signal is an output signal.	• Isolated low impedance connection to core V_{SS}. • Refer to *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet • Refer to the schematics.

16.2. CK_SKS Clock Generator Checklist

Checklist Items	Recommendations	Reason/Impact/Documentation
Ref/MultSel[0:1]	• Use 33 Ω series termination resistor for each signal. • Connect to ICH2 and SIO.	• Refer to the schematics.
PCICLK [0:9]	• Use 33 Ω series termination resistor for each signal. • Connect to PCI slots 0 through 4 • Connect to ICH2, FWH, SIO, Glue Chip and Audio Logic Device.	• Refer to Section 4.3.3.
3V66 [0:3]	• Use 33 Ω series termination resistor for each signal. • Connect to AGP Connector, MCH, and ICH2.	• Refer to Section 4.3.2.
3VMRef 3VMRef_b	• Use 33 Ω series termination resistor for each signal. • Connect 3VMRef to DRCG1. • Connect 3VMRef_b to DRCG2	• 3VMRef_b is 180° out of phase with 3VMRef. • Refer to the schematics.
SEL100/133	• Connect this signal to GND with a 470 Ω ±5% resistor.	• This signal needs to be connected to GND for 100 MHz operation. • Refer to the schematics.
48 MHz /SelA 48 MHz /SelB	• Terminate to GND with 1 kΩ ±5% resistors	• Terminating to GND sets CK_SKS for 100 MHz host clock operation • Refer to the schematics.
SPREAD#	• Terminate to GND with a 470 Ω ±5% resistor.	• Terminating to GND enables this function • Refer to the schematics.
PWRDWN#	• Terminate to V_{CC} with 4.7 kΩ resistor. • Connect to DRCG1 and DRCG2 clock generators.	• Refer to the schematics.

Checklist Items	Recommendations	Reason/Impact/Documentation
CPUCLK/ CPUCLK_B[0:3]	• Connect a 33 Ω ±5% series resistor on each clock signal. Series resistor should be placed on the clock driver side of the shunt source resistor. • Simulations indicate that 20–33 Ω resistor to be effective. • Connect a “shunt source termination (Rt)” resistor to GND for each signal after series termination resistor. • Connect differential clock pair to processor, MCH, ITP connector.	• These are differential clocks. • Rt resistors should be selected to match the characteristic impedance of the board. • Refer to Section 4.1 • Refer to the schematics.
3.3 V(V_{CC})	• Connect to 3.3 V power plane	• Refer to the schematics.
GND	• Connect to GND plane.	• Refer to the schematics.
XTAL_in XTAL_out	• Connect a 10 pf capacitor from each signal to GND. • Connect to 14.318 MHz crystal oscillator.	• Capacitor values may vary slightly from manufacturer to manufacturer. • Refer to the schematics.

16.3. RDRAM* Clock Generator (DRCG1 and DRCG2) Checklist

Checklist Items	Recommendations	Reason/Impact
VddIR	• Connect to 3.3 V	• Provides the voltage reference for the Refclk clock output from CK_SKS clock generator • Refer to the schematics. • Refer to Section 4.2.1.
Refclk	• Connect Refclk pin of DRCG1 and DRCG2 to 3VMRef and 3VMRef_b outputs from the CK_SKS clock generator.	• Refer to the schematics.
ddP, VddC, VddO,	• These are all 3.3 V voltage pins. Tie directly to V_{CC3_3} supply. • Place a 0.1µF cap between each pin and the V_{SS} plane for decoupling purposes.	• Refer to the schematics.
GndP, GndI, GndC, GndO	• Connect to GND.	• These are all ground pins. • Refer to the schematics.
PclkM	• Connect to HCLKOUT on MCH.	• This is a host clock feedback input. • Refer to the schematics. • Refer to Section 4.2.2.
SynclkN	• Connect to RCLKOUT on MCH.	• This is a RAMBUS* clock feedback input. • Refer to the schematics. • Refer to Section 4.2.2.
VddIPD	• Connect to 1.8 V power plane.	• This is a voltage reference for PclkM and SynclkN signals. • Refer to the schematics.
STOPB#	• Terminate to 1.8 V power plane with a 4.7 kΩ resistor.	• This function is not used for Intel® 850 chipset-based platform. • Refer to the schematics.
PWRDN#	• Terminate to 3.3 V through a 4.7 kΩ resistor. • Connect to CK_SKS PWRDN# signal.	• Refer to the schematics.
S1, S0	• Connect 1 kΩ ±5% series resistors to S0 and S1 and connect signals together. Connect joined signals through a 4.7 kΩ ±5% pull-down resistor to GND and connect a series resistor to a GPIO	• A low voltage (logic “0”) on S1 and S0 places the DRCG in normal operation mode. The GPIO connection allows software adjustable mode control over CLK and CLKB • Refer to the schematics.

Checklist Items	Recommendations	Reason/Impact
Mult[1:0]	• Connect to GPIO.	• These pins determine the internal PLL divider ratio in the DRCG. Connection to GPIO allows software adjustable PLLCLK and REFCLK multipliers. • The Intel® 850 chipset platform supports 400 MHz (PC800) and 300 MHz (PC600) RAMBUS* operation only. • Refer to the schematics.
ClkB/Clk	• Connect a 39 Ω ±5% series resistor near the pins. Connect 51 Ω ±5% parallel resistors after the series resistors through a 0.1 µF capacitor to ground. Connect to RIMM connector. • These signals should be terminated with 28 Ω ±2% or 27Ω ±1% resistors to ground through a 0.1 µF capacitor.	• This is the main clock (CTM/CTM#) for the Direct RAMBUS* channel. • Refer to Section 4.2.4. • Refer to Section 4.2.3.3. • Refer to the schematics.
Global decoupling	• It is recommended that a ferrite filter with 2 capacitors (10 µF and 0.1 µF) be placed near the part for both the 3.3 V planes. Capacitors should be placed on the device side of the Ferrite Bead. Ferrite bead should be 50 Ω at 100 MHz. • Discrete caps are recommended for all the aforementioned decoupling. • Cpacks are not recommended.	• This recommendation is to reduce jitter and voltage supply noise for the part. • Cpacks will increase the parasitic inductance of the capacitors, and may require more capacitors than specified above. • Refer to section 4.2.4. • Refer to the schematics.

16.4. Intel® 850 Chipset Checklist

Checklist Items	Recommendations	Reason/Impact
HL_STB HL_STB#	• Connect to ICH2	• The length of both hub interface strobe signals must be matched within ±0.1 inches of the HL_STB differential pair. • Refer to Section 8.1.1.
HDVREF[3:0] HAVREF[3:0] CCVREF	• Connect voltage divider to pins. 50 Ω ±1% pull-up to V_{CC} and 100 Ω ±1% pull-down resistor to GND. • Decouple the voltage divider with a 1µf capacitor. • Keep the voltage divider within 1.5 inches of the MCH V_{REF} ball.	• A single reference divider circuit for all signals is considered sufficient. • Refer to Section 5.5.
HUBREF	• Use a voltage divider circuit with R1=R2=150Ω ±1% • The reference voltage generated by a single HUBREF divider should be bypassed to ground at each component with a 0.01 µF capacitor located close to the component (MCH and ICH2) HUBREF pin. Decouple the voltage divider circuit with a 0.1 µF capacitor placed near the voltage divider circuit.	• Refer to Section 8.1.3.
GRCOMP	• Must be tied to a 40 Ω ±2% or 39 Ω ±1% pull-down resistor to ground.	• Connect within 0.5 inches of the ball. • Refer to Section 7.1.8.
HLR_COMP	• RCOMP Resistor tied to V_{SS}: • Normal: 40 Ω ±2% or 39 Ω ±1% with a trace impedance of 60 Ω ±15%.	• Refer to Section 8.1.4.
HR_COMP	• Use 20.75 Ω ±1% pull-down to V_{SS}	• Refer Section 5.5.
HSWNG [1:0]	• Connect voltage divider to pins. 150 Ω pull-down to GND and a 301 Ω pull-up resistor to V_{TT}. • Decouple the voltage divider with a 1 µf capacitor. • Keep the voltage divider within 1.5 inches of the MCH V_{REF} ball.	• Refer to Section 5.5.

Checklist Items	Recommendations	Reason/Impact
I/O Decoupling requirements	• 4 minimum, 5 preferred 0.1 µf capacitors with 603 packages distributed evenly over the System Bus data lines. • 2 minimum, 3 preferred 0.1 µf capacitors with 603 packages distributed evenly over the system bus address and control lines. • All capacitors placed as close as possible to the MCH package (within 150 mils)	• This is to provide clean power delivery to the system bus I/O ring. • Refer to Section 5.5.1.
1.8 V RAC Power Isolation	• **Option 1 — Low pass filter with inductor:** Place 3.3 nH inductor between V_{CC}RAC and the 1.8 V power plane. Place a 3.3 µf capacitor on MCH side of the inductor. Place 2–3 0.1 µF capacitors near the V_{CC}RAC pins for adequate decoupling between V_{CC}RAC and V_{SS}. Use 0805 size components. • **Option 1 — Low pass filter with Ferrite Bead:** Place 10 Ω (at 100 MHz) between V_{CC}RAC and the 1.8 V power plane. Place a 10 µF capacitor on MCH side of the inductor. Use a minimum of 2 .1 µF capacitors per RAC and a minimum of one 1.0 µF capacitor for both RACs located near the V_{CC}RAC pins. Use 0805 size components except for the 10 µF capacitor, which can be 1206.	• The Intel® 850 chipset requires a low-pass filter on the V_{CC}RAC pins to meet clock jitter specifications. The low-pass filter isolates V_{CC}RAC from the 1.8 voltage plane that powers the MCH core. • Refer to Section 6.2.
SCK/CMD Circuitry	• This implementation is applicable for RIMM modules down solution only. Also, this implementation is not necessary if Suspend-to-RAM is not supported in the system. • Transistor needs to be connected to SCK and should be gated with PWROK circuitry. A dummy transistor needs to be connected to the CMD signal to minimize impedance discontinuities. • The transistor should have a Cobo of 4 pF or less.	• This circuitry is needed to avoid the MCH inadvertently taking the RDRAMs out of power-down due to the CMOS interface being driven during power ramp, the SCK signal should be shunted to ground when the MCH is entering and exiting Suspend-to-RAM. • Refer to Section 6.1.7.

16.5. AGP Checklist

Checklist Items	Recommendations	Reason/Impact
G_FRAME# G_IRDY# G_TRDY# G_DEVSEL# G_STOP# G_SERR# G_PERR# G_RBF# G_PIPE# G_REQ# G_GNT# G_PAR AD_STB[0:1] SB_STB WBF#	• These signals require pull-up resistors to V_{DDQ}. • Acceptable values are between 4 kΩ and 16 kΩ. The recommended value is 8.2 kΩ.	• V_{DDQ} = 1.5 V for 1X, 2X and 4X mode • Pull-up to V_{DDQ} ensures that stable values are maintained when agents are not actively driving the bus. • Refer to Section 7.1.9.
AD_STB#[0:1] SB_STB#	• These signals require pull-down resistors. • Acceptable values are between 4 kΩ and 16 kΩ. The recommended value is 8.2 kΩ.	• Pull-down to GND ensures that stable values are maintained when agents are not actively driving the bus. • Refer to Section 7.1.9.
INTA# INTB#	• 8.2 kΩ pull-up resistors to 3.3 V • Range is 4 kΩ– 16 kΩ	• These signals should be pulled up only once (for both PCI and AGP). They should be pulled to 3.3 V and MUST NOT be pulled to 5 V. • INTB# is for a two function device and may not be seen with AGP down • Refer to Section 7.1.9 this document.
VREFCG[B66] VREFGC[A66] G_REF[1:0]	• VREFCG should be tied to a resistor divider near the AGP device. • VREFGC should be a no connect. • A 220 Ω – 330 Ω series resistor should be connected from the voltage divider network to the G_REF[1:0] pins on the MCH.	• The V_{REF} divider network should be placed near the AGP interface to achieve the common mode power supply effect. A 0.1 µF decoupling capacitor should be placed near the G_REF[1:0 • Refer to Section 7.1.7.
TYPEDET# [A2]	• Intel® 850 chipset only supports 1.5 V add-in card. Therefore, TYPEDET# detection on the motherboard is not required.	• Refer to Section 7.1.6.
PME#	• Connect to PCI PME#	• This is an open drain signal from the AGP connector and does not require pull-up resistor to V_{CC3_3} if connected to ICH2. • Refer to the schematics.
3.3Vaux (B24)	• Connect to $3.3V_{SB}$	• May not be seen with AGP down • Refer to the schematics.

Checklist Items	Recommendations	Reason/Impact
Decoupling Capacitors	• Use a 0.01µF capacitor for each power pin and a bulk 10 µF tantalum capacitor on V_{DDQ} and a 20 µF tantalum capacitor on V_{CC3_3} plane near the connector.	• This is to ensure that the AGP connector is well decoupled. • Refer to Section 7.1.11
SBA[7:0]	• No extra pull-up resistors. Connect to AGP connector.	• In the MCH, weak pull-ups are integrated for SBA[7:0] signals. These signals implement internal pull-ups of a nominal value of 8 kΩ. • Refer to the schematics.

16.6. Rambus* RIMM* Module Checklist

Note:

- S3 (Suspend To RAM):
  — RDRAM Support → 2.5 V (ON), 1.8 V (ON), 3.3 V (N/A)
- S5 – 2.5 V (OFF), 1.8 V (OFF), 3.3 V (OFF)

Checklist Items	Recommendations	Reason/Impact
LCTM, LCTM# RCTM, RCTM# LCFM, LCFM# RCFM, RCFM# LROW[2:0] RROW[2:0] LCOL[4:0] RCOL[4:0] RDQA[8:0] LDQA[8:0] RDQB[8:0] LDQB[8:0] CMD SCK	• 0.8 pF – 1.35 pF compensating capacitance is required on each of these RSL connector pins.	• The RIMM connector pin inductance has been shown to cause an impedance discontinuity on the RAMBUS* channel. This may reduce voltage and timing margin. • Above are examples of calculated numbers. Actual calculated values may vary with board variations. Use CTAB calculations for specific values. • Refer to Section 6.1.2.5.
RSL Signal Termination	• All RSL signals must be terminated to 1.8 V (V_{TERM}) using 27 Ω 1% or 28 Ω 2% tolerance resistors at the end of the channel opposite the MCH.	• Rpacks are OK. • Refer to Section 6.1.3.
RC Termination	• Due to the buffer strengths in the MCH, the high-speed CMOS signals require DC termination. • Terminate with 91 Ω ±2% pull-up and a 39 Ω ±2% pull-down resistor to ensure proper resuming from S3.	• The MCH tri-states SCK during STR entry causing a glitch on SCK. • Refer to Section 6.1.5.
SVDD (A56 and B56)	• Should be tied to 3.3 V for EEPROM (SPD) on RIMM modules • If the SMBus is tied to $3.3V_{SB}$, then either: — provide proper isolation on SCL /SDA and pull SVDD to 3.3 V OR — tie SVDD to $3.3V_{SB}$.	• Ensure proper isolation if some SMBUS devices are powered by $3.3V_{SB}$. • Refer to the RAMBUS* datasheets at http://www.rambus.com

Checklist Items	Recommendations	Reason/Impact
SA Pins	• Should be connected to V_{CC3_3} or GND to set the SMBus address for that RIMM module's EEPROM. • If the SMBus is tied to $3.3V_{SB}$, then either: — provide proper isolation on SCL /SDA and pull the HIGH SA pins to 3.3 V OR — tie the HIGH SA pins to $3.3V_{SB}$.	• This sets the SMBus address. Each device on the SMBus must have an address to distinguish it from another device of the same type. That is, each RIMM module EEPROM must be strapped to a different address or they will all respond on an access. • Refer to the RAMBUS* datasheets at http://www.rambus.com
SIN & SOUT	Should be daisy-chained between RIMM modules: • MCH SIO pin connects to 1st RIMM connector SIN (B36) • SOUT (A36) on 1st RIMM connector connects to 2nd RIMM connector SIN (B36) • A 2.2 kΩ–10 kΩ terminating resistor, tied to GND, is required on the last RIMM connector's SOUT pin.	• Refer to Section 6.1.6. • Refer to the RAMBUS* datasheets at http://www.rambus.com
SWE (A57)	• If an OEM needs to write to the SPD devices, it is recommended that this signal be tied to a GPO pin from either the ICH2 or the SIO. • If an OEM does not need to write to the SPD devices, it is recommended that this signal be tied to 3.3 V via a weak pull-up resistor (4.7 kΩ).	• If SWE = 1, write protected. • If SWE = 0, not write protected. • These signals must be driven; do not leave floating. • Refer to the RAMBUS* datasheets at http://www.rambus.com
RESET	• For the 168-pin RIMM connector, this is a reserved pin.	• The connector pad is reserved for future use for the 168-pin RIMM connector. • Refer to the RAMBUS* datasheets at http://www.rambus.com
V_{DD}	• This is connected to 2.5 V (or $2.5V_{SB}$) • It is REQUIRED that the voltage regulator to the RDRAMS* (2.5 V RDRAM* Core) is turned OFF in S5. This can be accomplished by connecting the SLP_S5# signal to the 2.5 V RDRAM* Core voltage regulator.	• It supplies the core voltage for the RDRAM* and interface logic. • Refer to the schematics.
V_{CMOS}	• This is connected to 1.8 V for RDRAM* • V_{CMOS} must be OFF in S5. • V_{CMOS} can be generated with a voltage divider consisting of a 36 Ω pull-up resistor to V_{CC2_5} and 100 Ω resistor to GND.	• S5 is a suspend state and power is removed from some components on the motherboard. Therefore, V_{CMOS} should be off while in suspend state. • Refer to Section 6.1.5.

Checklist Items	Recommendations	Reason/Impact
2.5 V (V_{DD}) decoupling	• Low frequency decoupling: • This needs to be done on the motherboard with bulk capacitors. • Linear regulator design: 8x 100 µF • Switching regulator: 5x 47µF or 6x 20 µF	• These are EXAMPLES. The exact decoupling requirements are dependent on the voltage regulator design. Refer to the RAMBUS* RDRAM* specification for the power delivery requirements.
1.8 V (V_{TERM}) decoupling	• High frequency decoupling: — One 0.1 µF ceramic capacitor per 2 RSL signals. These should be placed near the termination resistor pack. • Low frequency decoupling: — 2 x 100 µF tantalum capacitors.	• RSL termination voltage decoupling is required on the motherboard. Both high and low frequency decoupling needs to be added on the motherboard. • These are EXAMPLES. The exact decoupling requirements are dependent on the voltage regulator design. Refer to the RAMBUS* RDRAM* specification for the power delivery requirements. • Refer to Section 6.1.3.
1.4 V (RAMREF) decoupling	This plane must be decoupled in the following manner: • Each RIMM Connector: Locally – A value of 0.1 µF is required for local decoupling. • RAMREF Generation Circuit: At resistor divider – The RAMREF generation circuitry should be placed near the MCH. A 75 Ω ±2% pull-up resistor and 300 Ω ±2% pull-down resistor is required for proper reference voltage. • MCH: Locally – A value of 0.1 µF is required for local decoupling and a 100 Ω series resistor is required near the MCH, but before the voltage divider circuit.	• Refer to Section 6.1.4.

16.7. I/O Controller Hub 2 (ICH2) Checklist

16.7.1. PCI Interface

Checklist Items	Recommendations	Reason/Impact
FYI	• All inputs to the ICH2 must not be left floating	• Many GPIO signals are fixed inputs that must be pulled up to different sources. See Section 16.7.7 for recommendations
PERR# SERR# PLOCK# STOP# DEVSEL# TRDY# IRDY# FRAME# REQ#[0:4] GPIO[0:1] THRM#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to V_{CC3_3} or a 2.7 kΩ pull-up resistor to V_{CC5}.	• See PCI 2.2 Component Specification Pull-up recommendations for V_{CC3_3} and V_{CC5}.
PCIRST#	• The PCIRST# signal should be buffered to form the IDERST# signal • 33 Ω series resistor to IDE connectors.	• Improves signal integrity
PCIGNT#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented, they must be pulled up to V_{CC3_3}.	• These signals are actively driven by the ICH2
PME#	• No extra pull-up resistors	• This signals has an integrated pull-up of 24kΩ
SERIRQ	• External weak (8.2 kΩ) pull-up resistor to V_{CC3_3} is recommended.	• Open drain signal
GNT[A]# /GPIO[16], GNT[B]/ GNT[5]#/ GPIO[17]	• No extra pull-up needed	• These signals have integrated pull-ups of 24 kΩ. • GNT[A] has an added strap function of “top block swap”. The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function.

16.7.2. Hub Interface

Checklist Items	Recommendations	Reason/Impact
HL[11]	• No pull-up resistor required	• Use a no-stuff or a test point to put the ICH2 into NAND chain mode testing
HL_COMP	• Tie the COMP pin to a 40 Ω 1% or 2% (or 39 Ω 1%) pull-up resistor (to V_{CC1_8}) via a 10-mil wide, very short (~0.5 inch) trace.	• ZCOMP No longer supported.

16.7.3. LAN* Interface

Checklist Items	Recommendations	Reason/Impact
LAN_CLK	• Connect to LAN_CLK on platform LAN connect device.	•
LAN_RXD[2:0]	• Connect to LAN_RXD on platform LAN connect device.	• ICH2 contains integrated 9 kΩ pull-up resistors on interface
LAN_TXD[2:0] LAN_RSTSYNC	• Connect to LAN_TXD on platform LAN connect device.	•
	• LAN connect interface can be left NC if not used.	• Input buffers internally terminated
	• In the event of EMI problems during emissions testing (FCC Classifications) you may need to place a decoupling cap (~470 pF) on each of the 4 LED pins.	• Reduces emissions attributed to LAN subsystem.

16.7.4. EEPROM Interface

Checklist Items	Recommendations	Reason/Impact
EE_DOUT	• Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM or CNR Connector.	• Connected to EEPROM data input signal • (Input from EEPROM perspective and output from ICH2 perspective)
EE_DIN	• No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector.	• ICH2 contains integrated pull-up resistor for this signal. • Connected to EEPROM data output signal • (Output from EEPROM perspective and input from ICH2 perspective)

16.7.5. FWH/LPC Interface

Checklist Items	Recommendations	Reason/Impact
FWH[3:0]/ LAD[3:0] LDRQ[1:0]	• No extra pull-ups required. Connect straight to FWH/LPC.	• ICH2 integrates 24 kΩ pull-up resistors on these signal lines.

16.7.6. Interrupt Interface

Checklist Items	Recommendations	Reason/Impact
PIRQ#[D:A]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to V_{CC5} or 8.2 kΩ to V_{CC3_3}.	• In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section of this document. Each PIRQx# line has a separate Route Control Register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: - PIRQ[A]# is connected to IRQ16, - PIRQ[B]# to IRQ17, - PIRQ[C]# to IRQ18, - PIRQ[D]# to IRQ19. This frees the ISA interrupts.
PIRQ#[G:F]/ GPIO[4:3]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to V_{CC5} or 8.2 kΩ to V_{CC3_3}.	• In Non-APIC Mode the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15 as described in the Interrupt Steering section of this document. Each PIRQx# line has a separate Route Control Register. • In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: - PIRQ[E]# is connected to IRQ20, - PIRQ[F]# to IRQ21, - PIRQ[G]# to IRQ22, - PIRQ[H]# to IRQ23. This frees the ISA interrupts.
PIRQ#[H] PIRQ#[E]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to V_{CC5} or 8.2 kΩ to V_{CC3_3}.	• Since PIRQ[H]# and PIRQ[E]# are used internally for LAN and USB controllers, they cannot be used as GPIO(s) pin.

Checklist Items	Recommendations	Reason/Impact
APIC	**Pentium® 4 processor based systems:** • These processors do not have APIC pins so all platforms using this processor should both tie APICCLK to ground and tie APICD:[1:0] to ground via a 1K-10K pull-down resistor. **Non-Pentium® 4 processor based systems:** **If the APIC is used:** • 150Ω pull-up resistors on APICD[1:0] • Connect APICCLK to CK133 with a 20-33Ω series termination resistor. **If the APIC is not used on UP systems:** • The APICCLK can either be tied to GND or connected to CK133, but not left floating. Pull APICD[1:0] to GND through 10kΩ pull-down resistors.	**If the APIC is not used on UP systems:** • Use pull downs for each APIC signal. Do not share resistor to pull signals up.

16.7.7. GPIO

Checklist Items	Recommendations	Reason/Impact
GPIO Pins	**GPIO[0:7]:** • These pins are in the Main Power Well. Pull-ups must use the V_{CC3_3} plane. • Unused **core** well inputs must either be pulled up to V_{CC3_3} or be pulled down. • GPIO[1:0] can be used as REQ[A:B]#. • GPIO[1] can also used as PCI REQ[5]#. • These signals are 5 V tolerant **GPIO[8, 11:13]:** • These pins are in the resume power well. Pull-ups must use the V_{CCSUS3_3} plane. • Unused **resume** well inputs must be pulled up to V_{CCSUS3_3}. • These are the only GPIs that can be used as ACPI compliant wake events. • These signals are not 5 V tolerant **GPIO[16:23]:** • Fixed as output only. Can be left NC. • In main power well. • GPIO22 is open drain. **GPIO[24,25,27,28]:** • I/O pins. Can be left as No Connect. • From resume power well.	• Ensure ALL unconnected signals are OUTPUTS ONLY! • The GPIO signals listed in the Recommendations column are the only GPI signals in the resume well with associated status bits in the GPE1_STS register.

16.7.8. USB

Checklist Items	Recommendations	Reason/Impact
USBP[3:0]P USBP[3:0]N	• See Figure 89 for circuitry needed on each differential Pair.	

16.7.9. Power Management

Checklist Items	Recommendations	Reason/Impact
THRM#	• Connect to temperature sensor. • Pull-up if not used.	• Input to ICH2 cannot float. THRM# polarity bit defaults THRM# to active low, so pull-up.
SLP_S3# SLP_S5#	• No pull-up/pull-down resistors needed. Signals driven by ICH2.	• Signal driven by ICH2
PWROK	• This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both V_{CC3_3} and V_{CC1_8} have reached their nominal voltages	• Timing requirement
PWRBTN#	• No extra pull-up resistors	• This signals has an integrated pull-up of 24 kΩ
RI#	• RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to resume well	• If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns, the RI_STS bit will be set and the system will interpret that as a wake event.
RSMRST#	• This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both V_{CCSUS3_3} and V_{CCSUS1_8} have reached their nominal voltages. Requires weak pull-down. Also requires well isolation control as directed in section 6.5.	• Timing requirement • Power well isolation

16.7.10. Processor Signals

Checklist Items	Recommendations	Reason/Impact
A20M#, CPUSLP#, IGNNE#, INIT#, INTR, NMI, SMI#, STPCLK#	• Internal circuitry has been added to the ICH2, external pull-up resistors are not needed.	• Push/pull buffers now drive the output signals.
FERR#	• Requires weak external pull-up resistor.	• Refer to processor documentation for specific values.
RCIN# A20GATE	• Pull-up signals to V_{CC3_3} through a 10 kΩ resistor.	• Typically, driven by Open Drain external microcontroller
CPUPWRGD	• Connect to the processor's CPUPWRGD input. Requires weak external pull-up resistor.	• Refer to processor documentation of the processor that platform utilizes for specific values.

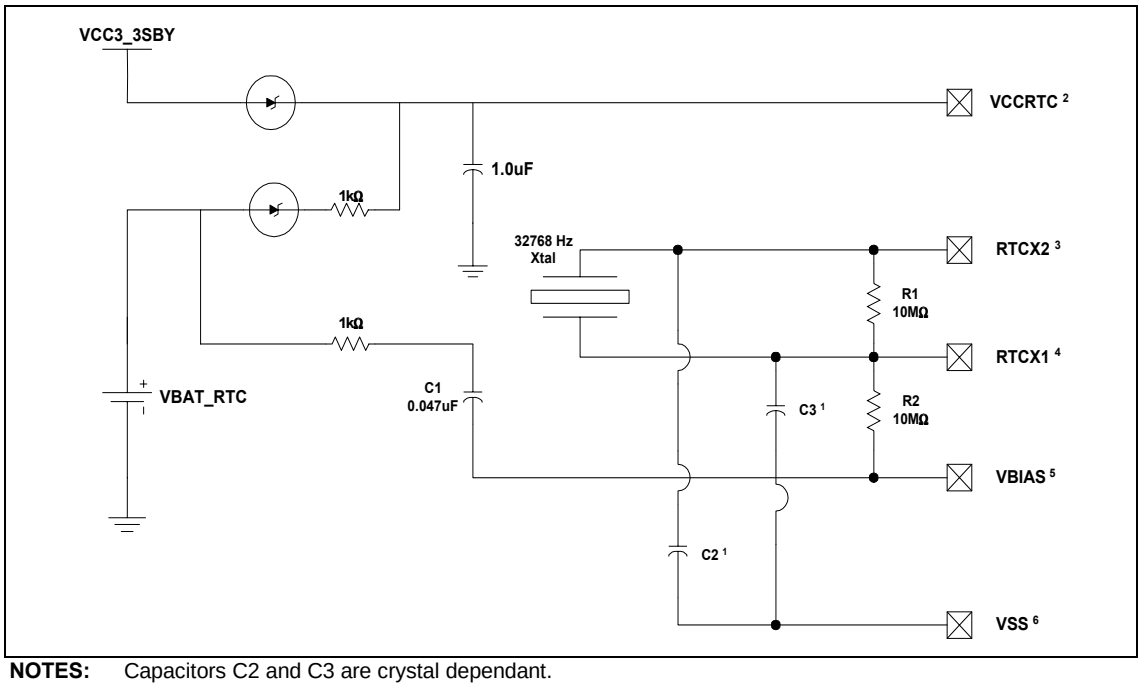
16.7.11. System Management

Checklist Items	Recommendations	Reason/Impact
SMBDATA SMBCLK	• Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)	• Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ.
SMBALERT#/ GPIO[11]	• See GPIO section if SMBALERT# not implemented	
SMLINK[1:0]	• Requires external pull-up resistors. See SMBus Architecture and Design Consideration section to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination.)	• Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ.
INTRUDER#	• Pull signal to V_{CC}RTC (V_{BAT}) if not needed	• Signal in V_{CC}RTC (V_{BAT}) well

16.7.12. RTC

Checklist Items	Recommendations	Reason/Impact
VBIAS	The VBIAS pin of the ICH2 is connected to a 0.047 µF cap. See Figure 162.	For noise immunity on VBIAS signal
RTCX1 RTCX2	Connect a 32.768 kHz crystal oscillator across these pins with a 10 mΩ resistor and use 18 pF decoupling caps (assuming crystal with C_{LOAD} = 12.5 pF) at each signal. Refer to Section 4.16 for more details. RTCX1 may optionally be driven by an external oscillator, instead of a crystal. These signals are 1.8 V only, and must not be driven by a 3.3 V source.	The ICH2 implements new internal oscillator circuit as compared with the PIIX4 to reduce power consumption. The external circuitry shown in Figure 167, below, will be required to maintain the accuracy of the RTC. The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in V_{CC}RTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.
VBIAS	The VBIAS pin of the ICH2 is connected to a 0.047 µF cap. See Figure 167.	For noise immunity on VBIAS signal
SUSCLK	Route to Test Point if SUSCLK is unused	To assist in RTC circuit debug

Figure 167. Intel® ICH2 Oscillator Circuitry



NOTES: Capacitors C2 and C3 are crystal dependant.

16.7.13. AC '97

Checklist Items	Recommendations	Reason/Impact
AC_SDOUT	• Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation.	• This pin has a weak internal pull-down. To properly detect a safe_mode condition a strong pull-up will be required to over-ride this internal pull-down.
AC_SDIN[1], AC_SDIN[0]	• Requires pads for weak 10 kΩ pull-downs. Stuff resistor for unused AC_SDIN signal or AC_SDIN signal going to the CNR connector. • If there is no codec on the system board, then both AC_SDIN[1:0] should be pulled down externally with resisters to ground.	• AC_SDIN[1:0] are inputs to an internal OR gate. If a pin is left floating, the output of the OR gate will be erroneous.
AC_BITCLK,	• No extra pull-down resistors required.	• When nothing is connected to the link, BIOS must set a shut-off bit for the internal keeper resistors to be enabled. At that point, you do not need pull-ups/pull-downs on any of the link signals.
AC_SYNC	• No extra pull-down resistors required.	• Some implementations add termination for signal integrity. Platform specific.

16.7.14. Miscellaneous Signals

Checklist Items	Recommendations	Reason/Impact
SPKR	• No extra pull-up resistors • Effective Impedance due speaker and codec circuitry must be greater than 50 kΩ or a means to isolate the resistive load from the signal while PWROK is low be found.	• Has integrated pull-up of between 18 kΩ and 42 kΩ. The integrated pull-up is only enabled at boot/reset for strapping functions; at all other times, the pull-up is disabled. • A low effective impedance may cause the TCO Timer Reboot function to be erroneously disabled.
TP[0]	• Requires external pull-up resistor to V_{CCSUS3_3}	• This signal is used for BATLOW in Mobile. • Not required for desktop.
FS[0]	• Rout to a test point.	• ICH2 contains an integrated pull-up for this signal. Test point used for manufacturing appears in XOR tree.

16.7.15. Power

Checklist Items	Recommendations	Reason/Impact
V_CPU_IO[1:0]	• The power pins should be connected to the proper power plane for the processor's CMOS compatibility signals. Use one 0.1 µF decoupling capacitor.	• Used to pull-up all processor interface signals.
VccRTC	• No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safemode strapping for Clear CMOS	
Vcc3_3	• Requires six 0.1µF decoupling capacitors.	
VccSus3_3	• Requires one 0.1µF decoupling capacitor.	
Vcc1_8	• Requires two 0.1µF decoupling capacitors.	
VccSus1_8	• Requires one 0.1µF decoupling capacitor.	
V5REF SUS	• Requires one 0.1uF decoupling cap • V5REF_SUS only affects 5 V tolerance for USB OC[3:0]# pins and can be connected to VccSUS3.3 or 5V_Always/5V_AUX if 5 V tolerance on OC[3:0]# is not required. If 5V tolerance on OC[3:0]# is needed then V5REF_SUS USB must be connected to 5V_Always/5V_AUX which remains powered during S5.	
V5REF	• V5REF is the reference voltage for 5 V tolerant inputs in the ICH2. Tie to pins VREF[2:1]. 5VREF must power up before or simultaneous to V_{CC3_3}. It must power down after or simultaneous to V_{CC3_3}.	• Refer to Section 12 for an example circuit schematic that may be used to ensure the proper V5REF sequencing.

16.7.16. IDE Interface

Checklist Items	Recommendations	Reason/Impact
PDD[15:0], SDD[15:0]	• No extra series termination resistors or other pull-ups/pull-downs are required. • PDD7/SDD7 does not require a 10 kΩ pull-down resistor. • Refer to ATA ATAPI-4 specification.	• These signals have integrated series resistors. • Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31Ω to 43 Ω.
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	• No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	• These signals have integrated series resistors. • Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.
PDREQ SDREQ	• No extra series termination resistors. • No pull-down resistors needed.	• These signals have integrated series resistors in the ICH2. • These signals have integrated pull-down resistors in the ICH2.
PIORDY SIORDY	• No extra series termination resistors. • Pull-up to V_{CC3_3} via a 4.7 kΩ resistor.	• These signals have integrated series resistors in the ICH2.
IRQ14, IRQ15	• Recommend 8.2 kΩ–10 kΩ pull-up resistors to V_{CC3_3}. • No extra series termination resistors.	• Open drain outputs from drive.
IDERST#	• The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.	
Cable Detect:	• **Host Side/Device Side Detection** — Connect IDE pin PDIAG/CBLID to an ICH2 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. • **Device Side Detection** — Connect a 0.047 µF capacitor from IDE pin PDIAG/CBLID to GND. No ICH2 connection.	• The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. • **NOTE:** All ATA66/ATA100 drives will have the capability to detect cables

17. Layout Review Checklist

17.1. Introduction

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements an 850 chipset. The items contained within this checklist attempt to address important connections to these devices and any critical supporting circuitry. This is not a complete list and does not guarantee that a design will function properly. Beyond the items contained in the following text, refer to the most recent version of the design guide for more detailed instructions on designing a motherboard.

17.2. Processor and System Bus

17.2.1. AGTL+ Signals

This section covers the address, Data, DSTBn/p#, ADSTBn/p# and common clock signals. Refer to the *Intel® Pentium® 4 Processor in the 423-pin Package* datasheet for a system bus list, signal types and definitions.

√	Recommendations	Reason/Impact/Documentation
	• Greater than 3:1 edge-to-edge spacing versus trace to reference plane ratio. Trace impedance should be 50 Ω ±15%.	• This recommendation has been simulated and ensures a low cross talk coefficient. A smaller ratio would have an unpredictable impact due to cross talk. If 3:1 ratio is requirement cannot be achieved, the separation should be maximized and the distance of the violation should be minimized. • Refer to Section 5.
	• Trace width recommendation is 7 mils with 13 mil edge-to-edge spacing for all signals. Traces can be approximately 5 mils within pin field, and spacing may be less than 13 mils for short lengths where spacing is constrained.	• Intel has simulated these recommendations for normal conditions. • Refer to Section 5.3 and Section 5.3.1.
	• Data signal (D[63:0], and DBI[3:0]#) length should be 2 inches – 10 inches pin-to-pin. Data signals of the same source synchronous group should be routed to the same pad-to-pad length ±100 mils. Length must be added to the motherboard to compensate for package length differences.	• The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. • Refer to Section 5 and Section 5.3.1

<table>
<tr><th>√</th><th>Recommendations</th><th>Reason/Impact/Documentation</th></tr>
<tr><td></td><td>• DSTBn/p[3:0]# should be routed the same length as corresponding data signals within ±25 mils (pad-to-pad). A strobe and its complement (DSTBP[3:0# and DSTBN[3:0]#) should be routed within ±25 mils of the same pad-to-pad length</td><td>• The impact of this recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. It is recommended to simulate skew in order to determine the length that best centers the strobe for a given system.
• Refer to Section 5 and Section 5.3.1.</td></tr>
<tr><td></td><td>• Address signal (A[35:3]# and REQ[4:0]#) length should be 2 inches – 10 inches pin-to-pin. Address signals of the same source synchronous group should be routed to the same pad-to-pad length ±100 mils. Length must be added to the motherboard to compensate for package length differences.</td><td>• The length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without trace matching and length compensation flight times between the data signals and the strobes will result in inequity between the setup and hold times. Address signals may change layers if reference plane remains the same. V_{CC} and/or V_{SS} vias are placed as close to the signal via as possible to provide the shortest possible path for return current.
• Refer to Section 5 and Section 5.3.1.</td></tr>
<tr><td></td><td>• ADSTB[1:0]# should be routed the same length as their corresponding address signals within ±25 mils (pad-to-pad).</td><td>• The impact of this routing recommendation causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times.
• Refer to Section 5 and Section 5.3.1.</td></tr>
<tr><td></td><td>Source Synchronous AGTL+ signals and its associated strobes (see below) should be routed on the same layer for the entire length of the bus. Address signals may change if same reference plane is maintained.

<table><tr><th>Signals</th><th>Associated Strobes</th></tr><tr><td>REQ[4:0#, A[16:3]#</td><td>ADSTB0#</td></tr><tr><td>A[35:17#</td><td>ADSTB1#</td></tr><tr><td>D[15:0#, DBI0#</td><td>DSTBP0#, DSTBN0#</td></tr><tr><td>D[31:16#, DBI1#</td><td>DSTBP1#, DSTBN1#</td></tr><tr><td>D[47:32#, DBI2#</td><td>DSTBP2#, DSTBN2#</td></tr><tr><td>D[63:48]#, DBI3#</td><td>DSTBP3#, DSTBN3#</td></tr></table></td><td>• These recommendations result in a significant reduction of flight time skew since the dielectric thickness, line width, and velocity of the signals will be uniform across a single layer of the stack-up.
• Refer to Section 5 and Section 5.3.1.</td></tr>
<tr><td></td><td>All common clock AGTL+ signals (See below) routed 6.2 inches – 10 inches (pin-to-pin) on same layer. No length compensation is necessary.

BPRI# DEFER# RESET#
RS[2:0]# RSP# TRDY#
AP[1:0]# ADS# BINIT#
BNR# BPM[5:0]# BR0#
DBSY# DP[3:0]# DRDY#
HIT# HITM# LOCK#
MCERR#</td><td>• Refer to Section 5 and Section 5.3.1.</td></tr>
</table>

√	Recommendations	Reason/Impact/Documentation
	• The serpentine height (height to reference plane) to serpentine width (width between the serpentine bends) ratio should be greater than or equal to 4. Minimize 90° serpentine bends. Utilize 45° serpentine bends as much as possible.	• This recommendation helps to control the serpentine to avoid signal integrity and timing problems that could occur from the coupling of the serpentine net. If coupling between serpentine parallel sections is high, this will cause significant timing skew when attempting to match trace lengths. • Refer to Section 5.
	• All signals impedance's should equal 50 Ω ±15%	• Refer to Section 5.
	• 25 mil spacing should be maintained around all clock and strobe traces	• Refer to Section 5 and, Section 4.1.

17.2.2. Asynchronous GTL+ and Other Signals

√	Recommendations	Reason/Impact/Documentation
	• FERR# and PROCHOT connects with the “T” topology. Processor to T-junction should be 1 inch–12 inches. T junction to the ICH2 should be 1.1 inches max. T- junction to pull-up should be 3 inches max. A 10 mil spacing is required. Trace impedance should be 50 Ω.	• Refer to Section 5.4 and Section 5.4.1.1
	• A20M#, IGNNE#, INIT#, LINT[1:0], SLP#,SMI# and STPCLK# connect in a point-to-point topology. Trace length should be 12 inches max. A 10 mil spacing required. Trace impedance should be 50 Ω.	• Refer to Section 5.4 and Section 5.4.1.2
	• THERMTRIP# connects in a “T” topology. Processor to T-junction should be 1 inch–12 inches max. T junction to ICH2 should be 1.1 inches max. T junction to pull-up resistor should be 3 inches max. Trace impedance should be 50 Ω. Trace spacing should be 10 mils.	• Refer to Section 5.4 and Section 5.4.1.4
	• PWRGOOD connected in a “T” topology. Pull-up resistor to T-junction should be 3 inches max. T-junction to processor should be 1.1 inches max. T-junction to ICH2 should be 1 inch–12. Trace impedance should be 50 Ω. Trace spacing should be 10 mils.	• Refer to Section 5.4 and Section 5.4.1.13
	• THERMDA/THERMDC should connect to remote sensor within 4-8 inches as long as worst-case noise sources (e.g., the clock generator, data and address signals) are avoided. A 10 mil wide trace recommended. Shielded twisted pair recommended for long distance remote sensor.`	• Refer to Section 5.4 and Section 5.4.1.9
	• $V_{CCIOPLL}$, V_{CCA}, V_{SSA} circuitry should be routed away from noisy signals or high free signals. Keep traces as short as possible.	• Refer to Section 5.5.
	• Place 43.2 Ω ±1% resistors as close to COMP[1:0] as possible	• Refer to Section 5.4.1.7

17.2.3. Processor Keepout Zones

√	Recommendations	Reason/Impact/Documentation
	• 4 circular keep-out zones are required for the use of retention mechanism. A pair of keep-out zones is located on the two sides of the socket where the retention mechanism is to be located. The 2 keep-out zones on each side are separated by 1.5 inches. This measurement is from the center of each keep-out zone. Retention mechanism keep-out pads need to be placed at specific locations on the board to align with processor support structure. • Each pair of keep-out zones is separated from the pair of keep-out zones on the opposing side of the socket by 3.2 inches. This measurement is also from center of each keep-out zone.	• Further keep-out zone requirements for the circular retention mechanism holes can be obtain the document reference below. • Circular keep-out zone locations can be found in the below document references. • Refer to Section 10.1.
	• Due to retention mechanism (RM) design, maximum height of components placed under the end edges of the RM is 0.2 inches max. The maximum height of the component placed under the center of RM is 0.08 inches max.	• Refer to Section 10.1.

17.2.4. Processor Decoupling

√	Recommendations	Reason/Impact/Documentation
	• Place 4-6 high frequency 0.1 µF capacitors with 603 package distributed evenly over the scalable bus data lines.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane (microstrip). • Refer to Section 11.4.5.2 and section 5.2.
	• Place 3-4 high frequency 0.1 µF capacitors with 603 package distributed evenly over the scalable bus address and control lines.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane (microstrip). • Refer to Section 11.4.5.2 and section 5.2.
	• Place 24 1206 package 10 µF capacitors as close to processor ground and power pins as possible.	• These high frequency decoupling capacitors are needed to meet voltage transients. • Refer to Section 11.4.5.2 and section 5.2.
	• All capacitors should be placed as close to the processor package as the processor keep-out zone allows.	• Refer to Section 11.4.5.2 and section 5.2.

17.2.5. 82850 MCH Decoupling

√	Recommendations	Reason/Impact/Documentation
	• 4–5 0.1µF capacitors with 603 packages distributed evenly over the scalable bus data lines. Place as close as possible (within 150 mils) to the chipset package.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane (microstrip). • Refer to Section 5.5.1
	• V_{CC}RAC isolation: Low pass filter circuit should be located within 2 inches of the MCH and the layout of V_{CC}RAC connections should follow high-speed design practices. Decoupling capacitors should be placed as close to the RAC pins as possible to control self-induced RAC noise.	• Proper routing of V_{CC}RAC isolation ensures RAMBUS* clock jitter specifications are met. • Refer to section 12.2.4.
	• 2–3 0.1µF capacitors with 603 packages distributed evenly over the system bus address and control lines. Place as close as possible (within 150 mils) to the chipset package.	• This recommendation reduces return path discontinuities that result from system board traces having only one reference plane. These recommendations are only used for designs containing microstrip configurations. • Refer to Section 5.5.1

17.2.6. AGTL+ (Vref. HDVREF [3:0], HAVREF [1:0] and CCVREF)

√	Recommendations	Reason/Impact/Documentation
	• Processor must have at least two dedicated voltage dividers. There are four GTLREF signals on the processor. Keep voltage dividers within 1.5 inches of the first V_{REF} pin.	• Refer to Section 5.3.
	• 82850 MCH requires one dedicated voltage divider. Voltage divider must be within 1.5 inches of MCH V_{REF} ball.	• Refer to Section 5.5.
	• Decouple each voltage divider with a 1 µF capacitor and each V_{REF} pin with a 220 pF capacitor as close to the pin as possible.	• This recommendation provides a low impedance line without the cost of additional plane or island. • Refer to Section 5.3.
	• When routing V_{REF} use a ~30–50 mil line trace width.	• This recommendation provides a low impedance line without the cost of additional plane or island. • Refer to Section 11.5.
	• Keep other signals 20 mils away from V_{REF} signal.	• V_{REF} signal must be a clean as possible from noise. • Refer to Section 5.3.

17.3. CK_SKS Routing Guidelines

17.3.1. CK_SKS Clocking

√	Recommendations	Reason/Impact/Documentation
	• 25 mil spacing required around all 100 MHz differential clocks	• Refer to Section 4.1.
	• Differential clocks should be routed on same layer. If via is required, then dummy vias need to be placed on other differential clock signals.	• This recommendation is to minimize clock skew due to clock pair to clock pair inconsistencies. • Refer to Section 4.1.
	• Route 100 MHz differential clocks to all agents on the same physical layer.	• Constraining all bus clocks to one physical layer minimizes the impact on skew due to variations in Er (dielectric constant) and impedance due to physical tolerances of circuit board material. Routing on internal layers reduces impedance variations and Er. • Refer to Section 4.1.
	• Connect individual differential clock signal from the CK_SKS to the MCH, ITP port, and the processor. • CK_SKS to series resistor should be 0.5 inches max. • Series resistor to termination resistor node should be 0.2 inches max. Termination resistor node to actual termination resistor should be 0.2 inches max. Termination resistor node to processor socket should be 12 inches max for Host_CPU and Host_ITP clocks. • Termination resistor node to MCH should be 12 inches for Host_MCH clocks. Add 0.850 inches ± for length matching to Host_MCH clock to compensate for processor socket and package delay.	• Refer to Section 4.1
	• Traces need to be 50 Ω ±15% single-ended and 100 Ω differential.	• Refer to Section 4.1.
	• Trace width for clocks is 7 mils and spacing between each end of the differential clock should be 28 mils min and 35 mils max. Uniform spacing should be maintained through the entire length of the trace.	• Degradation in noise rejection will occur if spacing is not uniform. • Refer to Section 4.1
	• All host clocks must be ground referenced.	• This ensures that proper current return path is available. • Refer to Section 4.1

√	Recommendations	Reason/Impact/Documentation
	• Connect individual 33 MHz clock signals to ICH2, FWH, and SIO. Trace length from CK_SKS chip to series resistor should be 0 inch –0.5 inches and from series resistor to receiver should be Z + (4 inches – 6 inches). Route singles on a single layer. • Z = 5 inches to 9 inches	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships, located in Section 4.3.1 of this document, between clock signals should be observed. • Refer to Section 4.3 and Section 4.3.3.
	• Connect individual PCI 33 MHz clock signals to PCI slots. Trace length from CK_SKS chip to series resistor should be 0 inch – 0.5 inches and from series resistor to receiver should be Z + (2 inches – 4 inches). Route signals on a single layer. • Z = 5 inches to 9 inches	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships, located in Section 4.3.1 of this document, between clock signals should be observed. • Refer to Section 4.3 and Section 4.3.3.
	• Connect individual 66 MHz clock signals to ICH2 and MCH. • Trace length from CK_SKS to series resistor should be 0 inches – 0.5 inches and from series resistor to receiver should be Z + (4 inches – 5 inches). Route signals on a single layer. • Z = 5 inches to 9 inches.	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships, located in Section 4.3.1 of this document, between clock signals should be observed. • Refer to Section 4.3 and Section 4.3.2.
	• Connect 66 MHz clock signal to AGP connector. • Trace length from the CK_SKS to series resistor should be 0 inches – 0.5 inches and from series resistor to receiver should be equal to Z (5 inches –9 inches). Route signals on a single layer.	• This recommendation insures setup and hold times in relation to the other clock signals are maintained. Clock length routing relationships, located in Section 4.3.1 of this document, between clock signals should be observed. • Refer to Section 4.3 and Section 4.3.2.

17.4. RAMBUS* Routing Guidelines

17.4.1. Rambus* Signaling Level (RSL) Signals

√	Recommendations	Reason/Impact
	• MCH to 1st RIMM connector of Channel A or 1st RIMM connector of Channel B 1 inch–6 inches	• Refer to Section 6.1.1.
	• RIMM connector to RIMM connector of the same channel 0.4 to 1 inch.	• Refer to Section 6.1.1.
	• RIMM connector to termination less than 2 inches. • The trace length between the last RIMM connector and the termination resistors should be less than 2 inches.	• Length matching in this section is not required. • Refer to Section 6.1.3.
	• RSL traces 18 mils trace width, 6-mil space, and 10-mil ground flood, 6-mil space.	• Refer to Section 6.1.1.
	• All signals must be length matched within ±10 mils of the Nominal RSL length as described in this design guide. Ensure that signals with a dummy via are compensated correctly.	• Refer to Section 6.1.1.
	• ALL RSL signals must have 1 via near the MCH BGA pad. Signals routed on the secondary side of the MB will have a “real via” while signals routed on the top layer will have a “dummy via”. Additionally, all signals with a dummy via must have an additional trace length of 25 mils.	• Refer to Section 6.1.2.2 for further explanation and examples.
	• Signals must “alternate” layers.	• Refer to Section 6.1.2.4 of this document.
	• At least 10 mils ground flood isolation required around ALL RSL signals (ground isolation must be exactly 6 mils from RSL signals). Ground flood recommended for isolation. This ground flood should be as close to the MCH (and the 1st RIMM connector) as possible. If possible, connect the flood to the ground balls/pins on the MCH/connector.	• To control cross talk and odd/even mode velocity deltas. • Refer to Section 6.1.1
	• When RSL traces neckdown to exit the MCH BGA, the minimum width is 15 mils and the neckdown is no longer than 25 mils in length.	• To minimize impedance discontinuities
	• Uniform ground isolation flood is exactly 6 mils from the RSL signals at all times.	• Refer to Section 6.1.1.
	• RSL traces Do NOT neckdown when routing into the RIMM connector.	• To minimize impedance discontinuities

√	Recommendations	Reason/Impact
	• If tight serpentining is necessary, 10-mil ground isolation MUST be between serpentine segments	• A RSL signal **cannot** serpentine so tightly that the signal is adjacent to itself with no ground isolation between the serpentines.
	• ALL RSL, CMD/SCK and CTM/CTM#/CFM/CFM# signals have CTABs on each RIMM connector pin.	• Compensation for the inductance of the connector. Voltage and timing margins may be reduced with CTABs. • Refer to Section 6.1.2.5.
	• CTABs must not cross (or be on top of) power plane splits. They must be ENTIRELY referenced to ground.	• Refer to Section 6.1.2.5.
	• All RSL signals are routed adjacent to a ground reference plane.	• This includes all signals from the 2nd RIMM connector to the termination. If signals are routed referenced to ground from the 2nd RIMM connector to the termination, the ground reference plane MUST extend under these signals AND include the groundside of the V_{TERM} decoupling capacitors.
	• The traces for CMD and SCK must have a neck down from 18-mil traces to 5-mil traces for 175-mils on either side of the SCK/CMD attach point.	• To minimize impedance discontinuities. Refer to Section 6.1.7.
	• Voltage divider network go reference voltage generation should be within 1.5 inches of the MCH V_{REF} ball.	• Refer to Section 5.5.
	• RSL traces do not cross power plane splits. RSL signals must also not be routed *next to* a power plane split	• To maintain signal integrity.

17.4.2. Ground Isolation

√	Recommendations	Reason/Impact
	• Via to ground every ½ inches around edge of isolation island, between RIMM connector s and between RSL signals (from MCH to 1St RIMM connector)	In channel Ideal 0.5 inches Acceptable: 1.0 inches At end Ideal 0.25 inches Acceptable : 0.5 inches * If 3/4 inch end of ground plane: shorten ground plane by 1/4 inch to meet ½ inch recommendation.
	• Via between every signal within 100 mils of the MCH edge and the connector edge.	
	• No unconnected ground floods	• To avoid discontinuity in ground planes.
	• Ground isolation fills between serpentines	• To avoid crosstalk.
	• Ground isolation not broken by C-tabs	• To avoid discontinuity in the ground plane. • Refer to Section 6.1.2.5.
	• Ground isolation connects to the ground pins in the middle of the RIMM connector.	
	• Ground isolation vias connect on all layers and should NOT have thermal reliefs.	
	• Ground pins in RIMM connector should connect on all layers.	

17.4.3. V_{TERM} Layout

√	Recommendations	Reason/Impact
	• Solid V_{TERM} island is on top routing layer; do not split this plane	
	• Ground island (for ground side of V_{TERM} capacitors) is on top routing layer	
	• Termination resistors connect directly to the V_{TERM} island on the top routing layer (without vias)	• Resistor packs are acceptable; however, discrete resistors are recommended for increase margin and control. • Refer to Section 6.1.3.
	• Decoupling caps connect to top layer V_{TERM} island and top routing layer ground island directly.	
	• Use at least 2 vias per decoupling capacitor in the top layer ground island.	
	• Use 2x100 µF Tantalum capacitors to decouple V_{TERM}.	• Refer to Section 6.1.3.
	• Hi-frequency decoupling capacitors must be spread-out across the termination island so that all termination resistors are near high frequency capacitors.	• Refer to Section 6.1.3.
	• 100 µF Tantalum capacitor should be at each end of the V_{TERM} island.	• Refer to Section 6.1.3.
	• 100 µF Tantalum capacitors must be connected to the V_{TERM} island directly	• Refer to Section 6.1.3.
	• 100 µF Tantalum capacitors must have at least 2 vias/cap to ground.	
	• V_{TERM} island should be at least 50 mils wide	• Refer to Section 6.1.3

17.4.4. DRCG Clock Routing Recommendation

√	Recommendations	Reason/Impact/Documentation
	• 3VMRef trace routed from CKx-SKS must be 6 mils wide and separated by 6 mil space on both sides. A 6 mil wide ground isolation trace should be placed after 6 mil space. Max trace length is 8 inches.	• This recommendation is for micro strip applications. • Refer to Section 4.2.1.
	• VddiR pin on DRCG can be connected to 3.3 V plane near the DRCG if the plane extends near the DRCG. However, if a 3.3 V trace must be used, it should originate at the clock synthesizer and routed 6 mil wide with 6 mil spacing with 6 mil wide ground trace following.	• Refer to Section 4.2.1.
	• Rclkout and Hclkout from MCH must be routed to Synclkn and Pclkm on the DRCG. Signals must be routed together about 12 mils apart with 6 mil wide traces. A 6 mil wide ground trace located on each side of the pair. A 6 mil spacing between the ground trace and Rclkout and Hclkout signals. Max trace length is 6 inches and must be length matched within 50 mils	• If signals must switch layers then they should switch layers together. • Refer to Section 4.2.2.
	• VddiPD pin on DRCG can be connected to 1.8 V plane near the DRCG if the plane extends near the DRCG. However, if a 1.8 V trace must be used, it should originate at the CK00 clock synthesizer and routed 5 mil wide with 6 mil spacing with 6 mil-wide ground trace.	• Refer to Section 4.2.2.
	• Series resistors (39 Ω) should be mounted very near CTM/CTM# pins. Parallel resistors (51 Ω) should be very near series resistors.	• Refer to Section 4.2.5.
	• CFM pair trace length: — MCH-to-1st RIMM connector 1 inch-6 inches — RIMM connector -to- RIMM connector 0.4 inches –1.0 inches. — 2nd RIMM connector -to-termination 0–2 inches	• Refer to Section 4.2.3.1.
	• CTM pair trace length: — DRCG-to-2nd RIMM connector 0–6 inches — RIMM connector -to- RIMM connector 0.4–1.0 inches — 1st RIMM connector-to-MCH 1 inch–6 inches	• Refer to Section 4.2.3.1.

√	Recommendations	Reason/Impact/Documentation
	• CTM and CFM pairs routed differentially should be routed: — 22 mil ground trace — 6 mil spacing — 14 mil trace width (clock) — 6 mil spacing — 14 mil trace width (clock#) — 6 mil spacing — 22 mil ground trace.	• Refer to Section 4.2.3.1
	• If CTM and CFM pairs routed single-ended, route: — 10 mil ground trace — 6 mil spacing — 18 mil wide clock trace — 6 mil wide spacing — 10 mil ground trace.	• Refer to Section 4.2.3.1.
	• CFM and CTM pairs must be ground referenced at all time.	• This recommendation ensures a proper return current path. • Refer to Section 4.2.3.2.
	• CFM and CTM pairs must have additional 0.021 inches of trace for every 1 inch of RSL trace.	• This added length is to compensate for the clocks faster velocity. • Refer to Section 4.2.3.2
	• Ensure that each clock pair is length matched within ±2 mils of the RSL channel length. Exact matching is preferred.	• Refer to Section 4.2.3.1.
	• Vias are placed in ground isolation traces and ground reference every 1 inch.	• Refer to Section 4.2.3.1.
	• When CTM/CTM# serpentine together, they MUST maintain EXACTLY mils spacing	

17.4.5. DRCG Layout (Clean Power Supply)

√	Recommendations	Reason/Impact
	• 3.3 V DRCG power flood on the top layer. This should connect to each high frequency (0.1 µF) capacitors are near the DRCG power pins. One capacitor next to each power pin.	• Refer to Section 4.2.5.
	• 10 µF bulk *tantalum* capacitor near DRCG connected directly to the 3.3 V DRCG power flood on the top layer	• Refer to Section 4.2.5.
	• Ferrite bead isolating DRCG power flood from 3.3 V main power.	• Refer to Section 4.2.4.

17.4.6. DRCG (CTM/CTM# Output Network Layout)

√	Recommendations	Reason/Impact
	• Series resistors (39 Ω) should be mounted very near CTM/CTM# pins. Parallel resistors (51 Ω) should be very near series resistors.	• Refer to Section 4.2.5.
	• CTM/CTM# should be 18 mils wide from the CTM/CTM# pins to the resistors	• Refer to Section 4.2.3.1.
	• CTM/CTM# should be 14 on 6 routed differential as soon as possible after the resistor network. When not 14 on 6, the clocks should be 18 mils wide	
	• Ensure CTM/CTM# are **ground referenced** and the ground reference is connected to the ground plane every ½ inch to 1 inch with vias.	
	• Ensure CTM/CTM# are **ground isolated** and the ground isolation is connected to the ground plane every ½ inch to 1 inch with vias.	

17.4.7. RAMREF Routing

√	Recommendations	Reason/Impact
	• Ensure 1 x 0.1 µF capacitor on V_{REF} at each RIMM connector	• Refer to Section 6.1.4.
	• Use 10-mil wide trace.	• Refer to Section 6.1.4.
	• Do not route V_{REF} near high-speed signals	
	• V_{REF} minimum trace spacing should be 25 mils.	• To reduce crosstalk and maintain signal integrity.

17.5. AGP Guidelines

17.5.1. All 1X Signals

The 1X signals are: CLK, RBF#, WBF#, ST [2:0], PIPE, REQ#, GNT#, PAR, FRAME#, IRDY#, TRDY, STOP# and DEVSEL#.

√	Recommendations	Reason/Impact
	• Max trace length 7.5 inches	• Refer to Section 7.1.1.
	• 5mil trace width, 5 mil trace separation	• Refer to Section 7.1.1.
	• No trace matching requirements for 1X signals.	• Refer to Section 7.1.1.

17.5.2. 2X/4X Signals

The 2X/4X signals are: AD [31:0], C/BE [3:0]#, ADSTB [1:0]#, SBA [7:0], SB_STB, SB_STB#

17.5.2.1. AGP Less Than 6 Inches

√	Recommendations	Reason/Impact
	• 5 mil trace width 15 mil separation between data to data for 60 Ω ±10%; for 60 Ω ±15%, its 20 mils	• Refer to Section 7.1.2.1.
	• 5 mil trace width 20 mil separation between data (and all other signals) to strobes for 60 Ω ±10% and 60 Ω ±15%	• Refer to Section 7.1.2.1.
	• 5 mil trace width 15 mil separation between strobe-to-strobe for 60 Ω ±10%; for 60 Ω ±%, its 20 mils	• Refer to Section 7.1.2.1.
	• If AGP Interface is <6 inches long, then DATA and C/BE#s need to be length matched within ±.25 inches of strobes.	• Refer to Section 7.1.2.1.
	• Strobe pairs must be length matched ±0.1 inches	• Refer to Section 7.1.2.1.
	• Route AD [15:0], C/BE [1:0]#, AD_STB0, and AD_STB0# together. (Good recommendation, but not in AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline. • Refer to Section 7.1.2.1.
	• Route AD [31:16], C/BE [3:2]#, AD_STB1, and AD_STB1# together. (Good recommendation, but not in AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline. • Refer to Section 7.1.2.1.
	• Route SBA [7:0], SB_STB, SB_STB# together. (Good recommendation, but not in AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline. • Refer to Section 7.1.2.1.
	• Recommended that all strobes be ground referenced as well as TRDY#, IRDY#, GNT#.	• Refer to Section 7.1.5.

√	Recommendations	Reason/Impact
	• Recommended that ½ the AGP signals are ground referenced.	• Refer to Section 7.1.5.
	• For signals that require pull-up or pull-down resistors, keep stub less than 0.5 inches for 1X signals and 0.01 inches for 2X/4X signals.	• This is to minimize signal reflections from the stub. • Refer to Section 7.1.9.
	• Pour a Ground flood under the V_{DDQ} plane	• Optimizes the mutual inductance between two planes. • Refer to Section 7.1.4.

17.5.2.2. AGP Interface Greater Than 6 Inches and Less Than 7.25 Inches

√	Recommendations	Reason/Impact
	• Board impedance must be 60 Ω ±10%	• Refer to Section 7.1.2.2.
	• 5 mil trace width 20 mil separation between data to data	• Refer to Section 7.1.2.2.
	• 5 mil trace width 20 mil separation between data (and all other signals) to strobes	• Refer to Section 7.1.2.2.
	• 5 mil trace width 20 mil separation between strobe to strobe	• Refer to Section 7.1.2.2.
	• DATA and C/BE#s need to be length matched within ±0.125 inches of strobes.	• Refer to Section 7.1.2.2.
	• Strobe pairs must be length matched ±0.1 inches	• Refer to Section 7.1.2.1.
	• Route AD [15:0], C/BE [1:0]#, AD_STB0, and AD_STB0# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline.
	• Route AD [31:16], C/BE [3:2]#, AD_STB1, and AD_STB1# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline.
	• Route SBA [7:0], SB_STB, SB_STB# together. (Good recommendation, but not in the AGP specification)	• Signals to be kept on same layers. Microstrip-to-microstrip and stripline-to-stripline.
	• Recommended that all strobes be ground referenced as well as TRDY#, IRDY#, GNT#.	• Refer to Section 7.1.5.
	• Recommended that ½ the AGP signals are ground referenced.	• Refer to Section 7.1.5.
	• For signals that require pull-up or pull-down resistors, keep stub less than 0.5 inches for 1X signals and less than 0.01 inches for 2X/4X signals.	• This is to minimize signal reflections from the stub. • Refer to Section 7.1.9.
	• Pour a V_{SS} flood under V_{DDQ} plane	• Optimizes the mutual inductance between two planes. • Refer to Section 7.1.9.

17.5.3. MCH AGP Decoupling

√	Recommendations	Reason/Impact
	• Min of 6 0.01 µF capacitors spread evenly around the MCH AGP interface.	• It is recommended that a low ESL ceramic capacitor, such as a 0603 body type, X7R dielectric. • Refer to Section 7.1.4.
	• Must be within 0.15 inches from package	• Refer to Section 7.1.4.
	• Pour a V_{SS} flood under V_{DDQ} plane to decouple AGP.	• To help lower inductive path from the decoupling capacitor. • Refer to Section 7.1.4.

17.5.4. AGP Connector Decoupling

√	Recommendations	Reason/Impact
	• One 0.01 µF capacitor next to each power pin on connector, V_{CC1_5}, V_{DDQ}, +5, +12, 3.3VAUX.	• Refer to Section 7.1.11.
	• For Bulk decoupling, need one 10 µF tantalum capacitor to V_{DDQ} and a 20 µF tantalum capacitor on V_{CC3_3} plane near connector.	• Refer to Section 7.1.11.

17.6. 8 Bit Hub Interface

√	Recommendations	Reason/Impact
	• Board impedance needs to be 60 Ω ±15%	• Refer to Section 8.1.
	• Traces need to be routed 5 mils wide with 20 mils spacing	• Refer to Section 8.1.
	• To breakout of the MCH and ICH2 package the hub interface signals can be routed 5 on 5. Signals need to be separated to 5 on 20 within 300 mils of the package.	• Refer to Section 8.1.
	• Max trace length is 6 inches long.	• Refer to Section 8.1.
	• Data signals must be matched within ±0.1 inches of the HL_STB diff pair.	• Refer to Section 8.1.2.
	• Each strobe signal needs to be the same length.	• Refer to Section 8.1.2.
	• HUBREF divider should be placed no more than 3.5 inches of away from MCH or ICH2. If so then need separate resistor divider placed locally.	• Refer to Section 8.1.3. • Also, refer to Figure 69 and Figure 70 of Section 8.1.3.

17.6.1. Hub Decoupling

√	Recommendations	Reason/Impact
	• Two 0.1 µF capacitors per each component (MCH and ICH2) spread over the Hub Interface.	• Refer to Section 8.1.5.
	• Place within 150 mils of each package.	• Refer to Section 8.1.5.

17.7. IDE Interface

√	Recommendations	Reason/Impact
	• 5 mil wide and 7 mil spaces	• Refer to Section 9.1.
	• Max trace length is 8 inches long	• Refer to Section 9.1.
	• Shortest trace length must be 0.5 inches shorter than the longest trace length.	• Refer to Section 9.1.

17.8. CNR

√	Recommendations	Reason/Impact
	• 4.5 inches min to 8.5 inches max trace length for LAN* Connect signals	• Refer to Section 9.2.
	• 60 Ω ±15%	• Refer to Section 9.2.
	• Maximum mismatch between length of clock trace and length of any data trace is 0.5 inches	• Refer to Section 9.2.

17.9. AC ’97

√	Recommendations	Reason/Impact
	• Z_O AC97 = 60 Ω ± 15%	• Refer to Section 9.3.
	• 5 mil trace width, 5 mil spacing between traces	• Refer to Section 9.3.
	• Max Trace Length ICH2/Codec/CNR = 12 inches	• Refer to Section 9.3.

17.10. USB

√	Recommendations	Reason/Impact
	• Characteristic impedance of individual signal lines P+, P- Zo = 45 Ω (90 Ω Differential)	• Refer to Section 9.4 and Figure 89.
	• Stack-up: 9 mils wide, 25 mil spacing between Differential pairs	• Refer to Section 9.4 and Figure 89.
	• Trace Characteristics: — Line Delay = 160.2 ps — Capacitance = 3.5 pF — Inductance = 7.3 nH — Res @ 20^{o} C = 53.9 mΩ	• Refer to Section 9.4 and Table 35.
	• 15 Ω series resistor to be placed < 1 inch from ICH2	• This is required for source termination of the reflected signal. • Refer to Section 9.4 and Figure 89.
	• 47 pF paralleled caps should be placed as close to the ICH2 as possible	• Refer to Section 9.4 and Figure 89.
	• 15 kΩ ± 5% pull-down resistors should be placed as close to the ICH2 as possible.	• Refer to Section 9.4 and Figure 89.
	• Optional 47 pF capacitor placed close to the USB connector as possible to the USB data lines	• This capacitor can be used for signal quality (rise/fall) times and to help minimize EMI radiation • Refer to Section 9.4 of this document.
	• Stub length due to 15 kΩ pull-downs should be as short as possible.	• Refer to Section 9.4 and Figure 89.

17.11. ICH2 Decoupling

√	Recommendations	Reason/Impact
	• 3.3 V Core—six 0.1 µF capacitors	• Refer to Section 9.11 and Table 42.
	• 3.3 V Stand By –one 0.1 µF capacitor	• Refer to Section 9.11 and Table 42.
	• Processor I/F(V_{CC_Core}) –one 0.1µF capacitor	• Refer to Section 9.11 and Table 42.
	• 1.8 V Core–two 0.1 µF capacitors, already included in Hub decoupling	• Refer to Section 9.11 and Table 42.
	• Place Decoupling capacitors as close to the ICH2 as possible (~ 400 mils)	• Refer to Section 9.11 and Table 42.

17.12. RTC

√	Recommendations	Reason/Impact
	• RTC LEAD length ≤ 0.25 inches Max	• Refer to Section 9.8.3.
	• Minimize capacitance between Xin and Xout	• Refer to Section 9.8.3.
	• Put GND plane underneath crystal components	• Refer to Section 9.8.3.
	• Do not route switching signals under the external components (unless on other side of board)	• Refer to Section 9.8.3.

17.13. LAN Connect Interface

√	Recommendations	Reason/Impact
	• Stack-up: 5 mils wide, 10 mil spacing	
	• Z_O = 60 Ω ±15%	• Signal integrity requirement.
	• LAN Max Trace Length ICH2 to CNR: L = 3 inches to 9 inches (0.5 inches to 3 inches on card)	• To meet timing requirements.
	• Stubs due to R-pak CNR/LOM stuffing option should not be present.	• To minimize inductance.
	• Maximum Trace Lengths: ICH2 to 82562EH/ET/EM : L = 4.5 inches to 8.5 inches	• To meet timing requirements.
	• Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches	• To meet timing and signal quality requirements.
	• Maintain constant symmetry and spacing between the traces within a differential pair.	• To meet timing and signal quality requirements.
	• Keep the total length of each differential pair under 4 inches.	• Issues found with traces longer than 4 inches : IEEE phy conformance failures, excessive EMI and or degraded receive BER.
	• Do not route the transmit differential traces closer than 70 mils to the receive differential traces.	• To minimize cross-talk.
	• Distance between differential traces and any other signal line is 70 mils.	• To minimize cross-talk.
	• Keep Max separation between differential pairs to 7 mils.	• To meet timing and signal quality requirements.
	• Differential trace impedance should be controlled to be ~100 Ω.	• To meet timing and signal quality requirements.
	• For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two 45 degree bends.	• To meet timing and signal quality requirements.

√	Recommendations	Reason/Impact
	• Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	• This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
	• Do not route traces and vias under crystals or oscillators.	• This will prevent coupling to or from the clock.
	• Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	• To control trace EMI radiation.
	• Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	• Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.
	• Vias to decoupling capacitors should be sufficiently large in diameter.	• To decrease series inductance.
	• Avoid routing high-speed LAN* or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.	• To minimize crosstalk.
	• Isolate I/O signals from high-speed signals.	• To minimize crosstalk.
	• Place the 82562ET/EM part more than 1.5 inches away from any board edge.	• This minimizes the potential for EMI radiation problems.
	• Verify proper EEPROM size: — 82562ET – 64 word — 82562EM – 256 word	• The 82562EM requires a larger EEPROM to store the alert envelope and other configuration information.
	• Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the 82562ET/EM.	• Research and development has shown that this is a robust design recommendation.
	• Place decoupling capacitors (0.1 µF) as close to the 82562ET/EM as possible.	
	• RBIAS10 and RBIAS100 resistors should be 1% values	• These are biasing resistors that require 1% accuracy. Note that the values shown on the reference schematic are recommended starting values. Fine tuning (via IEEE conformance testing) is required for every new design.

17.14. Miscellaneous

√	Recommendations	Reason/Impact
	• 1.8 V Stand By: one 0.1 µF capacitor	• Refer to Section 9.11 and Table 42.
	• 5 V Reference: two 0.1 µF capacitors	• Refer to Section 9.11 and Table 42.
	• 5 V Reference Stand By: one 0.1 µF capacitor	• Refer to Section 9.11 and Table 42.

Appendix A: Customer Reference Board Schematics

This appendix provides a set of schematics for the Pentium 4 processor / 850 chipset Platform Customer Reference Board (CRB).

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