Intel® 815E Chipset Platform

Design Guide Update

August 2002

Notice: The Intel® 815E chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 298249-006

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release: Schematic, Layout and Routing Updates 1–2; Documentation Changes 1–5	August 2000
-002	Added General Design Considerations #1 and #2; added Schematic, Layout, and Routing Updates #3–6; added Documentation Changes #6–21.	January 2001
-003	Added Documentation Changes #22 – 41.	July 2001
-004	Added Documentation Changes #42 – 52.	February 2002
-005	Added Documentation Changes #53, 54	April 2002
-006	Added Schematic, Layout and Routing Update #7	August 2002

Preface

This Design Guide Update document is an update to the specifications and information contained in the documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and document changes. This document is intended for hardware system manufacturers and for software developers of applications, operating system, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2000. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This update document contains a complete list of all known information types.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 815E Chipset Platform Design Guide	298234-001

Nomenclature

General Design Considerations includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® 815E chipset.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Shaded:	This item is either new or modified from the previous version of the document.

NO.	GENERAL DESIGN CONSIDERATIONS
1	Future Designs Require Pull-Ups and Pull-Downs on any Unused Input and I/O Pins
2	Designs That Do Not Use the AGP Port

NO.	SCHEMATIC, LAYOUT AND ROUTING UPDATES
1	Changed: Clock Routing Guidelines, Section 11.3; New Layout Guidelines for SDRAM, SCLK, and GMCH HCLK
2	Changed: Schematic Page 4 of 42; VCOREDET Pin
3	Changed: Schematic Page 12 of 42, SA0 and WP Pullup; Note Added
4	Changed: Schematic Page 26 of 42, TV OUT/Flat Panel Combo Chip Pin-Out; Note Added
5	Changed: IDE Interface, Section 10.1; Routing Spacing Changed
6	Changed: Schematic Page 14 of 42, GPIO[7:0] Strapping Requirements; Note Added
7	Changed: Schematic Page 15 of 42, pin TP0, Pull-up voltage

NO.	DOCUMENTATION CHANGES
1	Changed: Third-Party Vendor Information, Chapter 14; Tables Added
2	Changed: System Memory Checklist, Section 13.10; Checklist Item SRCOMP
3	Changed: Clock Synthesizer Checklist, Section 13.8
4	Changed: Digital Video Output Port, Section 13.3.3; Replaced
5	Changed: Miscellaneous Checklist for 370-Pin Socket Processors, Section 13.2.4; Checklist Item VCORE_DET (E21)
6	Added: Clock Skew Assumptions Table, Section 11.5
7	Changed: GPIO[7:0] Strapping Requirements, Section 13.4.7
8	Changed: USB, Section 10.5; General Guidelines Are Changed and Expanded
9	Changed: AC'97, Section 10.3; Guidelines Are Expanded
10	Added: AC'97 Audio Codec Detect Circuit and Configuration Options, Section 10.3.1
11	Added: SPKR Pin Considerations, Section 10.3.2
12	Added: Disabling the Native USB Interface of the ICH2, Section 10.5.1
13	Changed: LAN Layout Guidelines, Section 10.11; Modified
14	Changed: LAN Interface, Section 13.4.3; Checklist Is Expanded
15	Changed: AC'97, Section 13.4.14; Checklist Is Expanded
16	Changed: LPC/FWH, Section 10.12; Guidelines Are Expanded
17	Added: FWH Decoupling, Section 10.12.3
18	Changed: Primary IDE Connector Requirements, Section 10.2.3; Expanded
19	Changed: Secondary IDE Connector Requirements, Section 10.2.4; Expanded
20	Changed: 82562ET / 82562EH Dual Footprint Guidelines, Section 10.11.5; Modified
21	Added: 3.3V/V5REF Sequencing, Section 12.4.3
22	Added: Section 10.10.8, RTC-Well Input Strap Requirements
23	Changed: Section 10.11, LAN Layout Guidelines; Modified
24	Changed: Section 10.11.1.2, Point-To-Point Interconnect; Table 28 Modified
25	Changed: Section 10.11.2.1, General Trace Routing Considerations; Modified

NO.	DOCUMENTATION CHANGES
26	Changed: Section 10.11.4.3, 82562ET / 82562EM Termination Resistors; Modified
27	Changed: Section 10.11.5, 82562ET / 82562EH Dual Footprint Guidelines; Modified
28	Changed: Section 12.4.3, 3.3V/V5REF Sequencing; Modified
29	Changed: Section 10.3.1, AC'97 Audio Codec Detect Circuit and Configuration Options; Table 25a; Modified
30	Changed: Section 13.4.1, PCI Interface, PME# Checklist Item; Modified
31	Changed: Section 13.4.9, Power Management, PWRBTN# Checklist Item; Modified
32	Changed: Title of Section 10.10.8, RTC-Well Input Strap Requirements; Modified
33	Changed: Section 10.10.1., RTC Crystal, Note 1 under Figure 57; Modified
34	Changed: Section 13.4.13, RTC, RTCX1-RTCX2 Checklist Item; Modified
35	Changed: Section 2, General Design Considerations; Modified
36	Changed: Section 10.11.5, 82562ET / 82562EH Dual Footprint Guidelines; Modified
37	Changed: Section 10.12.2, FWH Vpp Design Guidelines; Modified
38	Added: Section 10.11.4.6, Intel® 82562ET/EM Disable Guidelines
39	Changed: Section 13.4.13., RTC; Modified Checklist Item
40	Changed: Section 10.5, USB; Modified
41	Changed: RTC Crystal, Section 10.10.1, Figure 57, ICH2 RTC Crystal Circuit Capacitor C1 Value; Modified
42	Replaced Figure 77, Power Delivery Map
43	Changed Section 13.4.9, Power Management
44	Added Information to Section 1.2.2.1, Intel® 82815 GMCH, Packaging Power
45	Replaced Figure 77, Power Delivery Map
46	Added: Section 9.5 Power_Supply PS_ON Considerations
47	Changed: Section 13.4.13, RTC, Add SUSCLK to the Checklist
48	Changed: Section 13.4.16, Power, Modify Checklist Recommendations for 5V_REF_SUS
49	Changed: Section 12.4.3, 3.3V/V5REF Sequencing
50	Changed: Figure 64, Trace Routing, in Section 10.11.2.1, General Trace Routing Considerations
51	Changed Table 30, Intel® CK-815 (2-DIMM) Clocks, in Section 11.1, 2-DIMM Clocking
52	Changed Table 31, Intel® CK-815 (3-DIMM) Clocks, in Section 11.2, 3-DIMM Clocking
53	Changed: Section 12.4.3, 3.3V/V5REF Sequencing
54	Changed: Figure 77, Power Delivery Map, in Section 12, Power Delivery

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General Design Considerations

1. Future Designs Require Pull-Ups and Pull-Downs on Any Unused Input and I/O Pins

Any new 815E chipset platform design should insure no input or I/O pin is left floating. For example, the TVCLKIN/INT# pin on many current 815E designs is left floating. This pin should be pulled up to 1.8 V by a weak pull-up resistor (8.2 KΩ to 10 KΩ resistor) on any future 815E design.

2. Designs That Do Not Use the AGP Port

82815 designs that do not use the AGP port should terminate the AGP pins of the 82815. Except for the GPAR pin (which requires a 100 kΩ pull-down resistor to ground), the pull-up or pull-down resistor value should be 8.2 kΩ. Any external graphics implementation not using the AGP port should terminate the 82815 AGP control and strobe signals in the following way:

Signal	Pull up / Pull Down
FRAME#	Pull-up to +VDDQ
TRDY#	Pull-up to +VDDQ
IRDY#	Pull-up to +VDDQ
DEVSEL#	Pull-up to +VDDQ
STOP#	Pull-up to +VDDQ
SERR#	Pull-up to +VDDQ
PERR#	Pull-up to +VDDQ
RBF#	Pull-up to +VDDQ
WBF#	Pull-up to +VDDQ
INTA#	Pull-up to +VDDQ
INTB#	Pull-up to +VDDQ
PIPE#	Pull-up to +VDDQ
REQ#	Pull-up to +VDDQ
GNT#	Pull-up to +VDDQ
GPAR	Pull-down to Ground using a 100 kΩ Resistor
AD_STB[1:0]	Pull-up to +VDDQ
SB_STB	Pull-up to +VDDQ
AD_STB[1:0]#	Pull-down to Ground
SB_STB#	Pull-down to Ground
ST[2:0]	Pull-up to +VDDQ

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Schematic, Layout and Routing Updates

1. Changed: Clock Routing Guidelines, Section 11.3; New Layout Guidelines for SDRAM, SCLK, and GMCH HCLK

These new clock guidelines are for future designs to improve PC133 SDRAM Clock Quality. Replace Section 11.3 with the following:

11.3 Clock Routing Guidelines

This section presents the generic clock routing guidelines for both 2-DIMM and 3-DIMM boards. For 3-DIMM boards, additional analysis must be performed by the motherboard designer to ensure that the clocks generated by the external PCI clock buffer meet the PCI specifications for clock skew at the receiver, when compared with the PCI clock at the ICH2.

Figure 75. Clock Routing Topologies

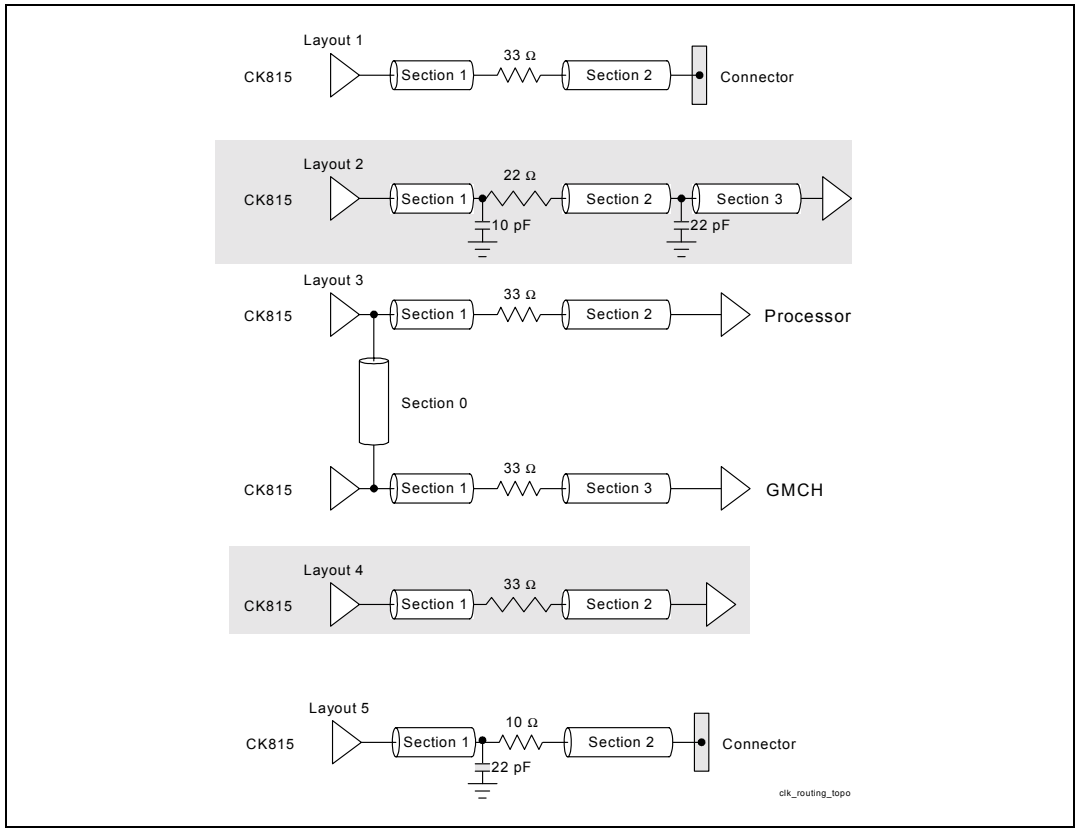


Table 32. Simulated Clock Routing Solution Space

Destination	Topology from Previous Figure	Section 0 Length	Section 1 Length	Section 2 Length	Section 3 Length
SDRAM MCLK	Layout 5	N/A	< 0.5”	A[1]	N/A
GMCH SCLK[3]	Layout 2	N/A	< 0.5”=L1	A + 3.5” – L1	0.5”
Processor BCLK	Layout 3	< 0.1”	< 0.5”	A + 5.2”	A + 8”
GMCH HCLK			<0.5”		
GMCH HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH2 HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH2 PCICLK	Layout 4	N/A	<0.5”	A + 8”	N/A
AGP CLK	Layout 4	N/A	<0.5”	A + 3" to A + 4"	N/A
PCI down[2]	Layout 4	N/A	<0.5”	A + 8.5” to A + 14”	N/A
PCI slot[2]	Layout 1	N/A	<0.5”	A + 5” to A + 11”	

NOTES:
1. Length “A” has been simulated up to 6”.
2. All PCI clocks must be within 6” of the ICH2 PCICLK route length. Routing on PCI add-in cards must be included in this length. In the presented solution space, ICH2 PCICLK was considered to be the shortest in the 6” trace routing range, and other clocks were adjusted from there. The system designer may choose to alter the relationship of PCI device and slot clocks, as long as all PCI clock lengths are within 6”. Note that the ICH2 PCICLK length is fixed to meet the skew requirements of ICH2 PCICLK to ICH2 HUBCLK
3. 22 pF Load cap should be placed 0.5” from GMCH Pin.

General Clock Layout Guidelines

- All clocks should be routed 5 mils wide with 15-mil spacing to any other signals.
- It is recommended to place capacitor sites within 0.5 inch of the receiver of all clocks. They are useful in system debug and AC tuning.
- Series resistor for clock guidelines: 22 Ω for GMCH SCLK and 10 Ω for SDRAM clocks. All other clocks use 33 Ω.
- Each DIMM clock should be matched within ±10 mils.

Clock Decoupling

Several general layout guidelines should be followed when laying out the power planes for the CK815 clock generator, as follows:

- Isolate power planes to the each of the clock groups.
- Place local decoupling as close as possible to power pins, and connect with short, wide traces and copper.
- Connect pins to appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling should be connected to a plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14-mil finished hole with a 24-mil to 26-mil path. An example power via is an 18-mil finished hole with a 33-mil to 38-mil path. For large decoupling or power planes with large current transients, a larger power via is recommended.

2. Changed: Schematic Page 4 of 42; VCOREDET Pin

Page 4 of 42 (370-Pin Socket, Part 2) of the 82815 Customer Reference Board (CRB) Schematics show the VCOREDET pin (lower right corner of the schematic) pulled high to VCC3_3 through a 220 Ω resistor and also connected to VCOREDET page 8 of 42 (GMCH Reset Straps). These connections are not correct.

The VCOREDET pin on the 370-Pin Socket, Part 2, page 4 of 42, should be left as a no-connect.

3. Changed: Schematic Page 12 of 42, SA0 and WP Pull-Up; Note Added

The following ***note*** should be added to schematic page 12 of 42:

Note: Do not depopulate R30 in an attempt to write to SPD. If R30 is removed, SA0 is left floating which adversely affects SMBus operation.

4. Changed: Schematic Page 26 of 42, TV OUT/Flat Panel Combo Chip Pin-Out; Note Added

The following ***note*** should be added to the schematic page 26 of 42:

Note: The pin-out shown for the TV OUT/Flat Panel Combo Chip is for the TI 6422 device. Other third-party vendor's devices may have different pin-outs. See the Third-Party Vendor Information in this Design Guide and in the Design Guide Update for additional vendors of these devices.

5. Changed: IDE Interface, Section 10.1; Routing Spacing Changed

Reference Section 10.1, IDE Interface, page 101. The first sentence in the second paragraph should read:

"The IDE interface can be routed with 5-mil traces on **7**-mil spaces and must be less than 8 inches long (from ICH2 to IDE connector)."

6. Changed: Schematic Page 14 of 42, GPIO[7:0] Strapping Requirements; Note Added

The following ***note*** should be added to schematic page 14 of 42:

Note: Unused GPIO[7:0] **core** well inputs must either be pulled up to VCC3.3 or be pulled down. Inputs must not be allowed to float.

7. Changed: Schematic Page 15 of 42, pin TP0, Pull-up voltage:

The Pull-up voltage for ICH pin TP0 should be changed from VCC3_3 to VCCSUS3_3

Documentation Changes

1. Changed: Third-Party Vendor Information, Chapter 14; Tables Added

The following four new tables are to be added to Chapter 14, “Third-Party Vendor Information”:

TMDS Transmitters

Vendors	Component	Contact	Phone
Silicon Images	SII164	John Nelson	(408) 873- 3111
Texas Instrument	TFP420	Greg Davis [gdavis@ti.com]	(214) 480-3662
Chrontel	CH7301	Chi Tai Hong [cthong@chrontel.com]	(408) 544-2150

TV Encoders

Vendors	Component	Contact	Phone
Chrontel	CH7007 / CH7008	Chi Tai Hong [cthong@chrontel.com]	(408) 544-2150
Chrontel	CH7010 / CH7011	Chi Tai Hong [cthong@chrontel.com]	(408) 544-2150
Conexant	CN870 / CN871	Eileen Carlson [eileen.carlson@conexant.com]	(858) 713-3203
Focus	FS450 / FS451	Bill Schillhammer [billhammer@focusinfo.com]	(978) 661-0146
Philips	SAA7102A	Marcus Rosin [marcus.rosin@philips.com]	None
Texas Instrument	TFP6022 / TFP6024	Greg Davis [gdavis@ti.com]	(214) 480-3662

Combo TMDS Transmitters/TV Encoders

Vendors	Component	Contact	Phone
Chrontel	CH7009 / CH7010	Chi Tai Hong [cthong@chrontel.com]	(408) 544-2150
Texas Instrument	TFP6422 / TFP6424	Greg Davis [gdavis@ti.com]	(214) 480-3662

LVDS Transmitter

Vendors	Component	Contact	Phone
National Semiconductor	387R	Jason Lu [Jason.Lu@nsc.com]	(408) 721-7540

2. Changed: System Memory Checklist, Section 13.10; Checklist Item SRCOMP

In Section 13.10, change the SRCOMP "Recommendations" information as shown below:

SRCOMP	Needs a 40-Ω resistor pulled up to 3.3 V

3. Changed: Clock Synthesizer Checklist, Section 13.8

In Section 13.8, changes from the Layout Updates are reflected in modifications to the last box, as follows:

MEMCLK0/DRAM_0, MEMCLK1/DRAM_1, MEMCLK2/DRAM_2, MEMCLK3/DRAM_3, MEMCLK4/DRAM_4, MEMCLK5/DRAM_5, MEMCLK6/DRAM_6, MEMCLK7/DRAM_7,	Pass through 10 Ω resistor
SCLK	Pass through 22 Ω resistor

4. Changed: Digital Video Output Port, Section 13.3.3; Replaced

Checklist Section 13.3.3, page 161, is replaced with the following:

13.3.3 Digital Video Input Checklist

Checklist Items	Recommendations
DVI Input Reference Circuit	See reference schematics in the documentation of the third party vendor of the device of choice in your design. The Third Party Vendor information is a part of this Design Guide and its associated Design Guide Updates.

5. Changed: Miscellaneous Checklist for 370-Pin Socket Processors, Section 13.2.4; Checklist Item VCORE_DET (E21)

Checklist Section 13.2.4, page 159: Change the VCORE_DET (E21) "Recommendations" information as shown below:

VCORE_DET (E21)	This pin should be left as a no-connect.

6. Added: Clock Skew Assumptions Table, Section 11.5

New Section 11.5, *Clock Skew Assumptions*, has been added:

11.5 Clock Skew Assumptions

The clock skew assumptions in the following table are used in the system clock simulations.

Table 32a. Simulated Clock Skew Assumptions

Skew Relationships	Target	Tolerance (±)	Notes
HCLK @ GMCH to HCLK @ processor	0 ns	150 ps	Assumes ganged clock outputs will allow max. of 50-ps skew
HCLK @ GMCH to SCLK @ GMCH	0 ns	600 ps	500-ps pin-to-pin skew 100-ps board/package skew
SCLK @ GMCH to SCLK @ SDRAM	0 ns	630 ps	250-ps pin-to-pin skew 380-ps board + DIMM variation
HLCLK @ GMCH to SCLK @ GMCH	0 ns	900 ps	500-ps pin-to-pin skew 400-ps board/package skew
HLCLK @ GMCH to HCLK @ GMCH	0 ns	700 ps	500-ps pin-to-pin skew 200-ps board/package skew
HLCLK @ GMCH to HLCLK @ ICH	0 ns	375 ps	175-ps pin-to-pin skew 200-ps board/package skew
HLCLK @ ICH to PCICLK @ ICH	0 ns	900 ps	500-ps pin-to-pin skew 400-ps board/package skew
PCICLK @ ICH to PCICLK @ other PCI devices	0 ns	2.0-ns window	500-ps pin-to-pin skew 1.5-ns board/add-in skew
HLCLK @ GMCH to AGPCLK @ connector			Total electrical length of AGP connector + add-in card is 750 ps (according to AGP2.0 spec and AGP design guide 1.0). Motherboard clock routing must account for this additional electrical length. Therefore, AGPCLK routed to the connector must be shorter than HLCLK to the GMCH, to account for this additional 750 ps.

8. Changed: GPIO[7:0] Strapping Requirements, Section 13.4.7

Reference Section 13.4.7, *GPIO Checklist*, page 163. The schematic checklist for GPIO[7:0] in the Recommendations Section, second sentence, currently says, “Unused core well inputs must be pulled up to VCC3.3”. This sentence is changed to two sentences that read, “Unused core well inputs must either be pulled up to VCC3.3 or be pulled down. Inputs must not be allowed to float.”

9. Changed: USB, Section 10.5; General Guidelines Are Changed and Expanded

The third bullet is changed to read:

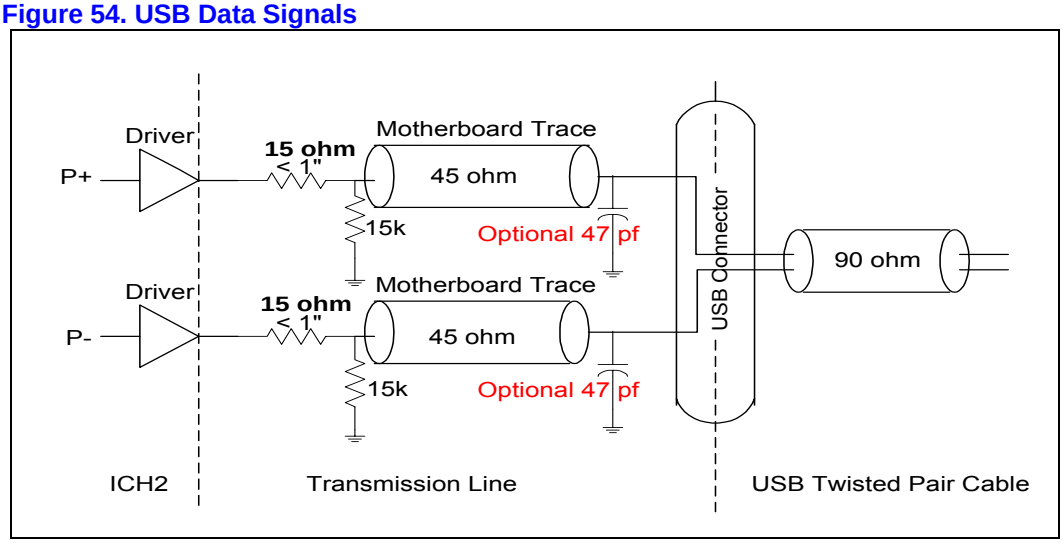
- An optional 47 pF cap may be placed as close to the USB connector as possible on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). This cap can be used for signal quality (rise/fall time) and to help minimize EMI radiation.

The sixth bullet is changed to read:

- USB data lines must be routed as critical signals. The P+/P- signal pair must be routed together, parallel to each other on the same layer, and not parallel with other non-USB signal traces to minimize crosstalk. Doubling the space from the P+/P- signal pair to adjacent signal traces will help to prevent crosstalk. Do not worry about crosstalk between the two P+/P- signal traces. The P+/P- signal traces must also be the same length. This will minimize the effect of common mode current on EMI. Lastly, do not route over plane splits.

Figure 54, USB Data Signals, page 109, is replaced with the following figure:

Figure 54. USB Data Signals



10. Changed: AC'97, Section 10.3; Guidelines Are Expanded

Reference Section 10.3, *AC'97*, page 106. Note the three paragraphs below Figure 52. Add the following new paragraph beneath the paragraph beginning with, "Intel has. . .":

The AC'97 interface can be routed using 5 mil traces with 5 mil space between the traces. Maximum length between ICH2 to CODEC/CNR is 14 inches in a tee topology. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 4 inches for the AC'LINK. Trace impedance should be $Z_0 = 60\ \Omega \pm 15\%$.

11. Added: AC'97 Audio Codec Detect Circuit and Configuration Options, Section 10.3.1

New Section, 10.3.1, *AC'97 Audio Codec Detect Circuit and Configuration Options*, is added:

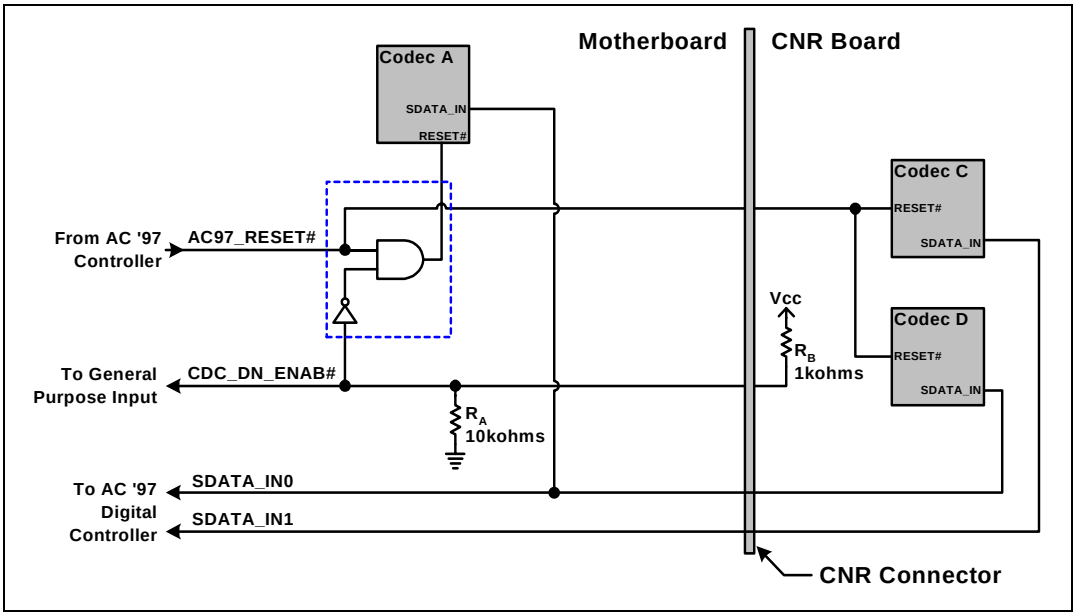
10.3.1 AC'97 Audio Codec Detect Circuit and Configuration Options

The following provides general circuits to implement a number of different codec configurations. Please refer to Intel's White Paper Recommendations for ICHx/AC'97 Audio (Motherboard and Communication and Network Riser) for Intel's recommended codec configurations.

To support more than two channels of audio output, the ICH2 allows for a configuration where two audio codecs work concurrently to provide surround capabilities. To maintain data-on-demand capabilities, the ICH2 AC'97 controller, when configured for 4 or 6 channels, will wait for all the appropriate slot request bits to be set before sending data in the SDATA_OUT slots. This allows for simple FIFO synchronization of the attached codecs. It is assumed that both codecs will be programmed to the same sample rate, and that the codecs have identical (or at least compatible) FIFO depth requirements. It is recommended that the codecs be provided by the same vendor, upon the certification of their interoperability in an audio channel configuration.

The following circuits (Figure 52.a, Figure 52.b, Figure 52.c, and Figure 52.d) show the adaptability of a system with the modification of R_A and R_B combined with some basic glue logic to support multiple codec configurations. This also provides a mechanism to make sure that only two codecs are enabled in a given configuration and allows the configuration of the link to be determined by the BIOS so that the correct PnP IDs can be loaded.

Figure 52.a CDC_DN_ENAB# Support Circuitry for a Single Codec on Motherboard



NOTES:
As shown in Figure 52.a, when a single codec is located on the motherboard, the resistor R_A and the circuitry (AND and NOT gates) shown inside the dashed box must be implemented, on the motherboard. This circuitry is required in order to disable the motherboard codec when a CNR is

installed which contains two AC ’97 codecs (or a single AC ’97 codec which must be the primary codec on the AC-Link).

By installing resistor R_B (1 kΩ) on the CNR, the codec on the motherboard becomes disabled (held in reset) and the codec(s) on the CNR take control of the AC-Link. One possible example of using this architecture is a system integrator installing an audio plus modem CNR in a system already containing an audio codec on the motherboard. The audio codec on the motherboard would then be disabled, allowing all of the codecs on the CNR to be used.

The architecture shown in Figure 52.b has some unique features. These include the possibility of the CNR being used as an upgrade to the existing audio features of the motherboard (by simply changing the value of resistor R_B on the CNR to 10 kΩ). An example of one such upgrade is increasing from two-channel to four or six-channel audio.

Both Figure 52.b and Figure 52.c show a switch on the CNR board. This is necessary to connect the CNR board codec to the proper SDATA_IN*n* line as to not conflict with the motherboard codec(s).

Figure 52.b CDC_DN_ENAB# Support Circuitry for Multi-Channel Audio Upgrade

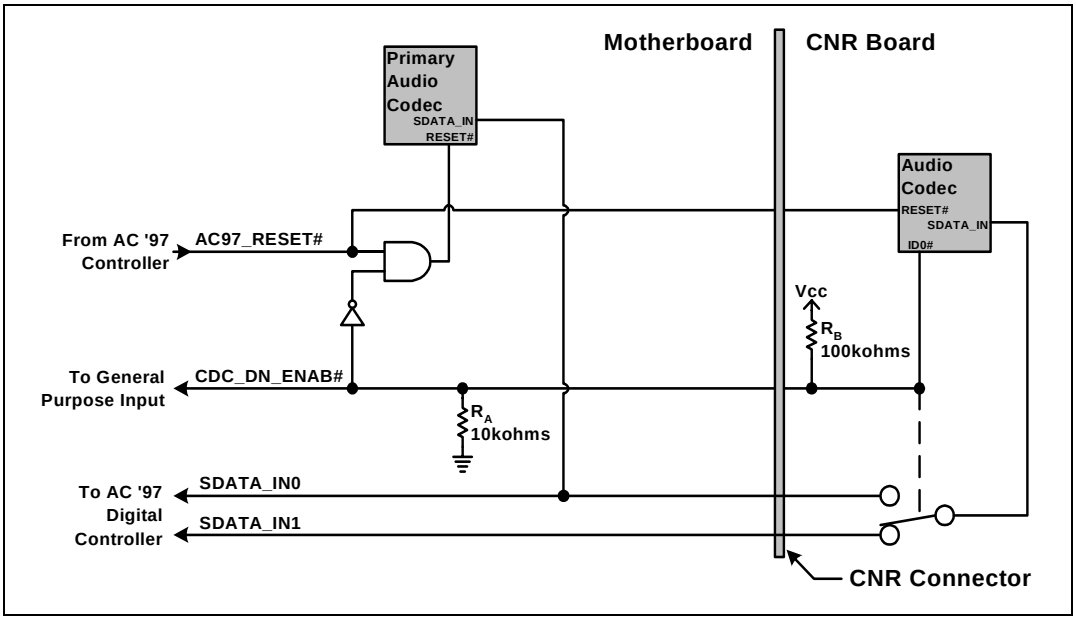


Figure 52.c shows the circuitry required on the motherboard to support a two-codec down configuration. This circuitry disables the codec on a single codec CNR. Notice that in this configuration the resistor, R_B, has been changed to 100 kΩ.

Figure 52.c CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / One-Codec on CNR

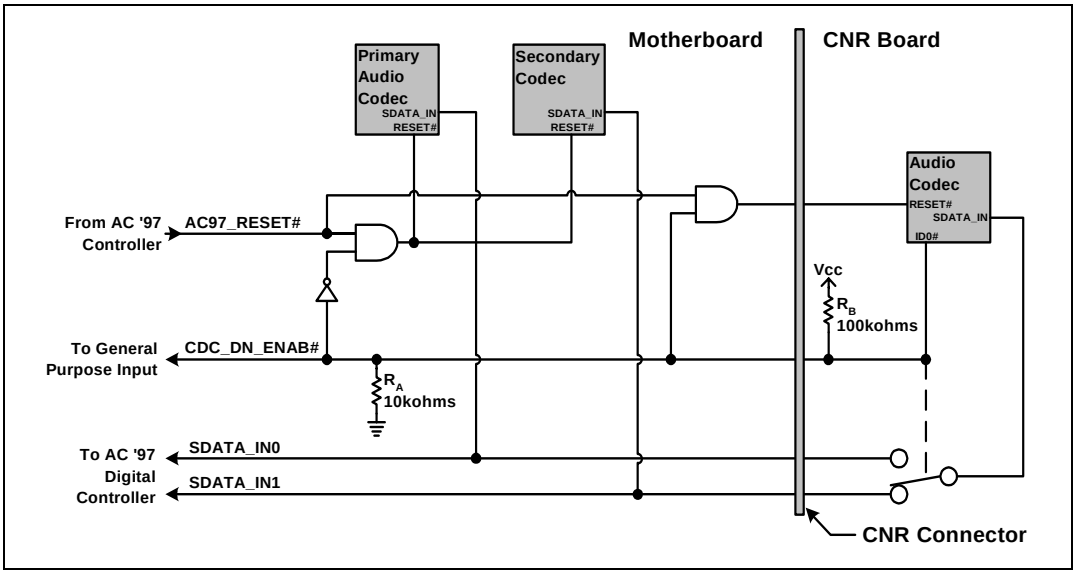
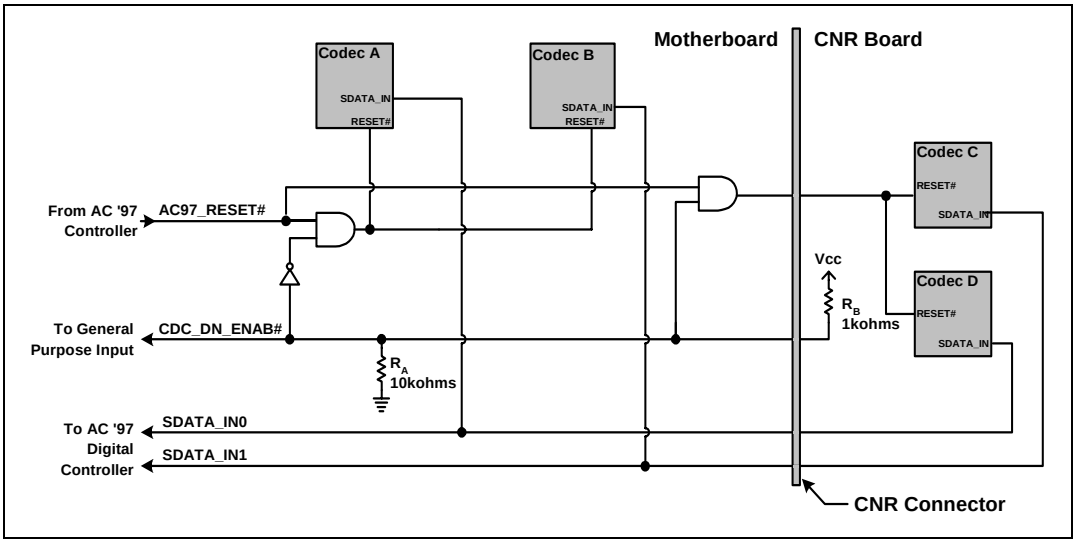


Figure 52.d shows the case of two-codecs down and a dual-codec CNR. In this case, both codecs on the motherboard are disabled (while both on CNR are active) by R_A being 10 kΩ and R_B being 1 kΩ.

Figure 52.d CDC_DN_ENAB# Support Circuitry for Two-Codecs on Motherboard / Two-Codecs on CNR



Circuit Notes:

1. While it is possible to disable down codecs, as shown in Figure 52.a and Figure 52.d, it is recommended against for reasons cited in the ICHx/AC'97 White Paper, including avoidance of shipping redundant and/or non-functional audio jacks.
2. All CNR designs include resistor RB. The value of RB is either 1 kΩ or 100 kΩ, depending on the intended functionality of the CNR (whether or not it intends to be the primary/controlling codec).
3. Any CNR with two codecs must implement RB with value 1 kΩ. If there is one codec, use a 100 kΩ pull-up resistor. A CNR with zero codecs must not stuff RB. If implemented, RB must be connected to the same power well as the codec so that it is valid whenever the codec has power.
4. A motherboard with one or more codecs down must implement RA with a value of 10 kΩ.
5. The CDC_DN_ENAB# signal must be run to a GPI so that the BIOS can sense the state of the signal. CDC_DN_ENAB# is required to be connected to a GPI; a connection to a GPIO is strongly recommended for testing purposes.

Table 25.a. Signal Descriptions

CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC '97 Interface.
AC97_RESET#	Reset signal from the AC '97 Digital Controller (ICH3).
SDATA_INn	AC '97 serial data from an AC '97-compliant codec to an AC '97-compliant controller (i.e., the ICH3).

Valid Codec Configurations

Table 25.b. Codec Configurations

Valid Codec Configurations
AC(Primary)
MC(Primary)
AMC(Primary)
AC(Primary) + MC(Secondary)
AC(Primary) + AC(Secondary)
AC(Primary) + AMC(Secondary)

Invalid Codec Configurations
MC(Primary) + X(any other type of codec)
AMC(Primary) + AMC(Secondary)
AMC(Primary) + MC(Secondary)

12. Added: SPKR Pin Considerations, Section 10.3.2

New Section, 10.3.2, *SPKR Pin Considerations*, is added:

10.3.2 SPKR Pin Considerations

The effective impedance of the speaker and codec circuitry on the SPKR signal line must be greater than 50 KΩ. Failure to due so will cause the TCO Timer Reboot function to be erroneously disabled. SPKR is used as both the output signal to the system speaker and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of POWEROK. When enabled, the ICH2 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull up resistor (the resistor is only enabled during boot/reset). Therefore it's default state when the pin is a "no connect" is a logical one or enabled. To disable the feature, a jumper can be populated to pull the signal line low (see figure). The value of the pull-down must be such that the voltage divider caused by the pull down and integrated pull up resistors will be read as logic low. When the jumper is not populated, a low can still be read on the signal line if the effective impedance due to the speaker and codec circuit is equal to or lower than the integrated pull up resistor. It is therefore strongly recommended that the effective impedance be greater than 50 kΩ and the pull-down resistor be less than 7.3 kΩ.

13. Added: Disabling the Native USB Interface of the Intel® ICH2, Section 10.5.1

New Section, 10.5.1, *Disabling the Native USB Interface of the ICH2*, is added:

10.5.1 Disabling the Native USB Interface of the Intel® ICH2

The ICH2 native USB interface can be disabled. This can be done when an external PCI-based USB controller is being implemented in the platform. To disable the native USB Interface, ensure the differential pairs are pulled down thru 15 kΩ resistors, ensure the OC[3:0]# signals are de-asserted by pulling them up weakly to VCC3SBY, and that both function 2 & 4 are disabled via the D31:F0;FUNC_DIS register. Ensure that the 48MHz USB clock is connected to the ICH2 and is kept running. This clock must be maintained even though the internal USB functions are disabled.

14. Changed: LAN Layout Guidelines, Section 10.11; Modified

Section 10.11, *LAN Layout Guidelines*, is modified as follows:

Section 10.11.1, *ICH2 – LAN Interconnect Guidelines*, add the following sentence to the last paragraph:

"The AC characteristics for this interface are found in the ICH2 datasheet. Dual footprint guidelines are found in Section 4.17.5."

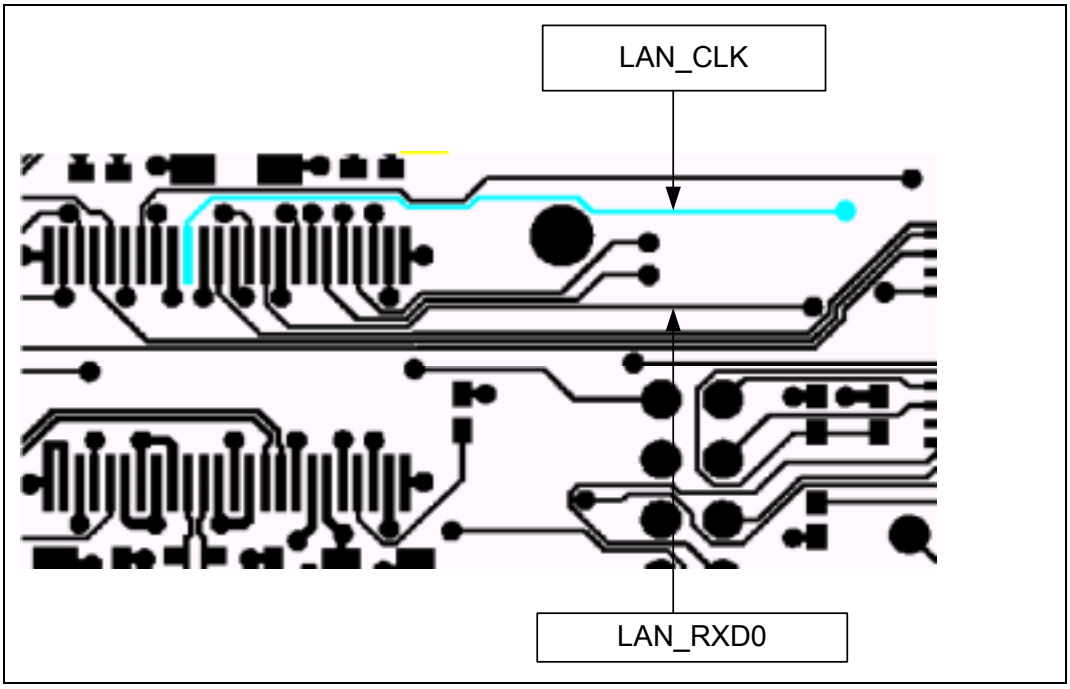
Section 10.11.1.2, *Point-to-Point Interconnect*, Table 28, *Single-Solution Interconnect Length Requirements*, is changed to show:

Configuration	L	Comment
82562EH	4.5" to 10"	Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected.
82562ET	4.5" to 10"	
CNR	3" to 9"	The trace length from the connector to LOM should be 0.5" to 3.0"

Section 10.11.1.3, *LOM/CNR Interconnect*, Table 29, *LOM/CNR Length Requirements*, is changed to show:

Configuration	A	B	C	D
82562EH	0.5" to 6.0"	4.0" to (10.0" – A)		
82562ET	0.5" to 7.0"	3.0" to (10.0" – A)		
Dual Footprint	0.5" to 6.5"	3.5" to (10.0" – A)		
82562ET/EH Card*	0.5" to 6.5"		2.5" to (9" – A)	0.5" to 3.0"

Section 10.11.1.4, *Signal Routing and Layout*, Figure 63, *LAN_CLK Routing Example*, is changed to show:



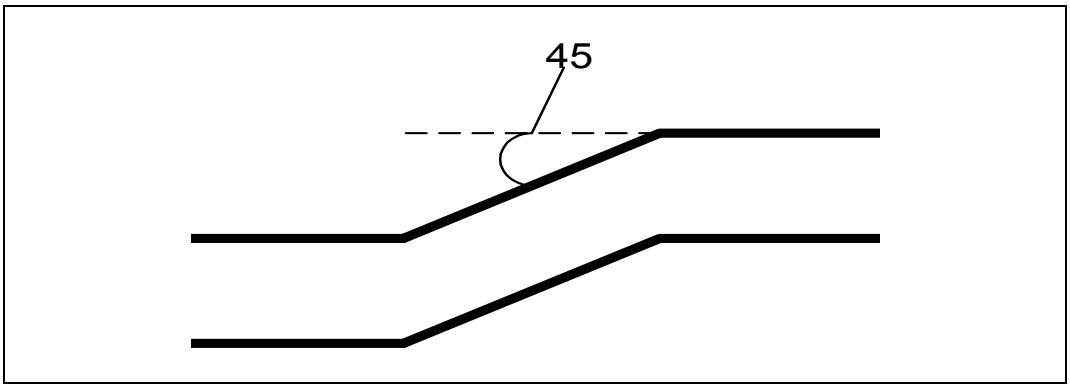
Section 10.11.2.1, *General Trace Routing Consideration*, the sixth bullet is changed to read:

"Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils recommended)."

Section 10.11.2.1, *General Trace Routing Considerations*, the eighth bullet is changed to read:

"For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. Refer to Figure 64."

Section 10.11.2.1, *General Trace Routing Considerations*, Figure 64, *Trace Routing*, is replaced with the following graphic:



Section 10.11.2.1.1, *Trace Geometry and Length*, the following sentence is added to the last paragraph:

"Additionally, the PLC should not be closer than one inch to the connector/magnetics/edge of the board."

Section 10.11.2.1.2, *Signal Isolation*, change the first bullet to read:

"Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Phoneline and Ethernet) and other nets, but group associated differential pairs together."

Section 10.11.2.2.1, *General Power and Ground Plane Considerations*, change the last bullet to read:

"*Create a spark gap between pins 2 through 5 of the Phoneline connector(s) and shield ground of 1.6mm (59.0 mil).* This is a ***critical*** requirement needed to past FCC part 68 testing for Phoneline connection. Note: For worldwide certification a trench of 2.5mm is required. In North America, the spacing requirement is 1.6mm. However, home networking can be used in other parts of the world, including Europe, where some Nordic countries require the 2.5mm spacing."

Section 10.11.2.3, *A 4-Layer Board Design*, change the material under the heading "Ground Plane" to read:

"A layout split (100 mils) of the ground plane under the magnetics module between the primary and secondary side of the module is recommended. It is also recommended to minimize the digital noise injected into the 82562 common ground plane. Suggestions include optimizing decoupling on neighboring noisy digital components, isolating the 82562 digital ground using a ground cutout, etc."

Section 10.11.2.4, *Common Physical Layout Issues*, change item 3 to read:

3. "Excessive distance between the PLC and the magnetics or between the magnetics and the RJ-45/11 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. Also any impedance mismatch in the traces will be aggravated if they are longer (see #9). The magnetics should be as close to the connector as possible (<= 1 inch)."

Section 10.11.2.4, *Common Physical Layout Issues*, change the ***Note*** following the last item (number 10) to read:

Note: "It is important to keep the two traces within a differential pair close to each other. Keeping them close helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e. FCC compliance) from the transmit traces, and better receive BER for the receive traces. Close should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended."

15. Changed: LAN Interface, Section 13.4.3; Checklist Is Expanded

Section 13.4.3, *LAN Interface*, is expanded as follows:

13.4.3 LAN Connect Interface

Checklist Items	Recommendations	Comments
1	Trace Spacing: 5 mils wide, 10 mil spacing	
2	LAN Max Trace Length ICH2 to CNR: L = 3” to 9” (0.5” to 3” on card)	To meet timing requirements.
3	Stubs due to R-pak CNR/LOM stuffing option should not be present.	To minimize inductance.
4	Maximum Trace Lengths: ICH2 to 82562EH: L = 4.5 inches to 10 inches; 82562ET: L = 3.5 inches to 10 inches; 82562EM: L = 4.5 inches to 8.5 inches.	To meet timing requirements.
5	Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches (clock must be longest trace)	To meet timing and signal quality requirements.
6	Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN phy.	To meet timing and signal quality requirements.
7	Keep the total length of each differential pair under 4 inches.	Issues found with traces longer than 4 inches : IEEE phy conformance failures, excessive EMI and or degraded receive BER.
8	Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	To minimize cross-talk.
9	Distance between differential traces and any other signal line is 100 mils. (300 mils recommended)	To minimize cross-talk.
10	Route 5 mils on 7 mils for differential pairs (out of LAN phy)	To meet timing and signal quality requirements.
11	Differential trace impedance should be controlled to be ~100 ohms.	To meet timing and signal quality requirements.
12	For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two 45 deg. bends.	To meet timing and signal quality requirements.
13	Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
14	Do not route traces and vias under crystals or oscillators.	This will prevent coupling to or from the clock.
15	Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	To control trace EMI radiation.
16	Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.

Checklist Items	Recommendations	Comments
17	Vias to decoupling capacitors should be sufficiently large in diameter.	To decrease series inductance.
18	Avoid routing high-speed LAN* or Phoneline traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.	To minimize cross-talk.
19	Isolate I/O signals from high speed signals.	To minimize cross-talk.
20	Place the 82562ET/EM part more than 1.5 inches away from any board edge.	This minimizes the potential for EMI radiation problems.
21	Place at least one bulk capacitor (4.7 µF or greater) on each side of the 82562ET/EM.	Research and development has shown that this is a robust design requirement.
22	Place decoupling caps (0.1 µF) as close to the 82562ET/EM as possible.	
23 LAN_CLK	Connect to LAN_CLK on Platform LAN Connect Device.	
24 LAN_RXD[2:0]	Connect to LAN_RXD on Platform LAN Connect Device. ICH2 contains integrated 9 KΩ pull-up resistors on interface.	
25 LAN_TXD[2:0] LAN_RSTSYNC	Connect to LAN_TXD on Platform LAN Connect Device.	

16. Changed: AC '97, Section 13.4.14; Checklist Is Expanded

Section 13.4.14, *AC '97*, is expanded by adding the following items to the existing checklist:

13.4.14. AC' 97

Checklist Items	Recommendations	Comments
1	Z_O AC97 = 60 Ω ± 15%	
2	5 mil trace width, 5 mil spacing between traces	
3	Max Trace Length ICH2/Codec/CNR = 14"	

17. Changed: LPC/FWH, Section 10.12; Guidelines Are Expanded

Section 10.12, *LPC/FWH* add the following paragraph that explains the contents of the subsections:

10.12. LPC/FWH

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

18. Added: FWH Decoupling, Section 10.12.3

New section 10.12.3, *FWH Decoupling*, is added:

10.12.3 FWH Decoupling

A 0.1 µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pins to decouple high frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the V_{CC} supply pins and the V_{SS} ground pin to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the V_{CC} supply pins.

19. Changed: Primary IDE Connector Requirements, Section 10.2.3; Expanded

Section 10.2.3, *Primary IDE Connector Requirements*, add this bullet to the bulleted list below Figure 50:

- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

20. Changed: Secondary IDE Connector Requirements, Section 10.2.4; Expanded

Section 10.2.4, *Secondary IDE Connector Requirements*, add this bullet to the bullet list below Figure 51:

- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Primary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

21. Changed: Intel® 82562ET / 82562EH Dual Footprint Guidelines, Section 10.11.5; Modified

Reference Section 10.11.5, *Intel® 82562ET / 82562EH Dual Footprint Guidelines*. Beneath Figure 72 is a list of additional guidelines for this configuration. Change the first bullet concerning length to read:

- L = 0.5 inches to 6.5 inches

22. Added: 3.3V/V5REF Sequencing, Section 12.4.3

Section 12.4.3, *3.3V/V5REF Sequencing*, is added as shown:

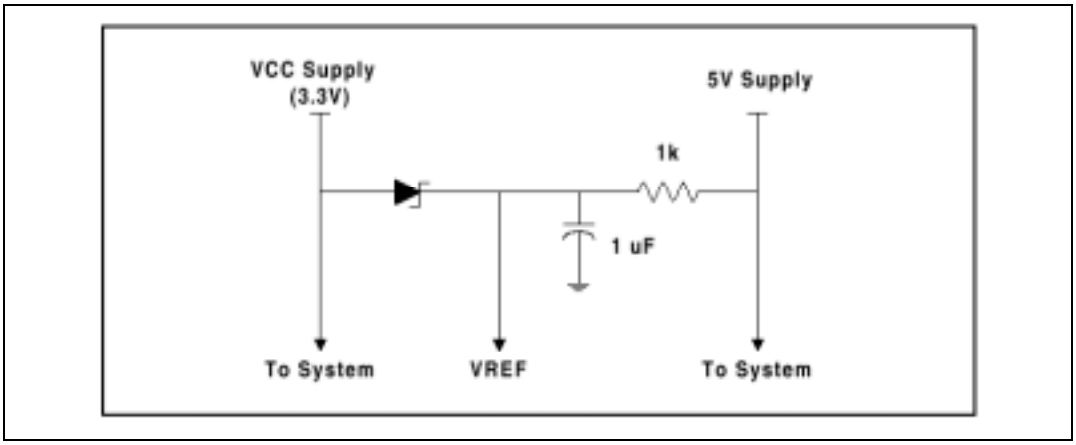
12.4.3 3.3V/V5REF Sequencing

V5REF is the reference voltage for 5V tolerance on inputs to the ICH3. V5REF must be powered up before or simultaneously to VCC3_3. It must also power down after or simultaneous to VCC3_3. The rule must be followed in order to ensure the safety of the ICH3. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 82.a. shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

This rule also applies to the stand-by rails, but in most platforms, the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USBOC. If these signals are not needed during suspend, V5REF_Sus can be hooked to the VccSus3_3 rail.

Figure 82.a. Example 3.3V/V5REF Sequencing Circuitry



23. Added: Section 10.10.8, RTC-Well Input Strap Requirements

Section 10.10.8, *RTC-Well Input Strap Requirements*, is added as shown.

10.10.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VCCRTC or pulled down to ground while in G3 state. RTCRST# when configured as shown in Figure 59 meets this requirement. RSMRST# should have a weak external pull-down to ground and INTRUDER# should have a weak external pull-up to VCCRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent ICCRTC leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

24. Changed: Section 10.11, LAN Layout Guidelines; Modified

Two sentences are added to the first paragraph of Section 10.11, *LAN Layout Guidelines*, as shown:.

10.11 LAN Layout Guidelines

The ICH2 provides several options for integrated LAN capability. The platform supports several components depending on the target market. These guidelines use the 82562ET to refer to both the 82562ET and 82562EM. The 82562EM is specified in those cases where there is a difference.

25. Changed: Section 10.11.1.2, Point-To-Point Interconnect; Table 28 Modified

Table 28, *Single-Solution Interconnect Length Requirement*, modified by Document Change #13 (Changed: LAN Layout Guidelines, Section 10.11; Modified) in the public *Intel® 815E Chipset Platform* design guide update (document number 298249-002), is further changed to show this new 82562ET length of 3.5 inches:

Configuration	L	Comment
82562EH	4.5” to 10”	Signal lines LAN_RXD[2:1] and LAN_TXD[2:1] are not connected.
82562ET	3.5” to 10”	
CNR	3” to 9”	The trace length from the connector to LOM should be 0.5” to 3.0”

26. Changed: Section 10.11.2.1, General Trace Routing Considerations; Modified

Bullet 5 of Section 10.11.2.1, *General Trace Routing Considerations* is changed to read:

- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.

27. Changed: Section 10.11.4.3, Intel® 82562ET / 82562EM Termination Resistors; Modified

The first paragraph shown under Section 10.11.4.3, *Intel® 82562ET / 82562EM Termination Resistors*, has an incorrect resistor value for the 1% receive differential pairs (RDP/RDN). The value is changed from 100 Ω to 120 Ω. The paragraph should read:

The 100 Ω (1%) resistor used to terminate the differential transmit pairs (TDP/TDN) and the 120 Ω (1%) receive differential pairs (RDP/RDN) should be placed as close to the LAN connect component (82562ET or 82562EM) as possible. This is due to the fact these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

28. Changed: Section 10.11.5, Intel® 82562ET / 82562EH Dual Footprint Guidelines; Modified

The first paragraph shown under Section 10.11.5, *Intel® 82562ET / 82562EM Dual Footprint Guidelines*, references an incorrect section of the Design Guide. The fourth sentence of the paragraph should read:

The guidelines called out in Sections 10.11.1 through 10.11.4 apply to this configuration.

29. Changed: Section 12.4.3, 3.3V/V5REF Sequencing; Modified

The first paragraph under Section 12.4.3, *3.3V/V5REF Sequencing*, added to the design guide by Document Change # 21 (Added: 3.3V/V5REF Sequencing, Section 12.4.3) in the public *Intel® 815E Chipset Platform* Design Guide Update (document number 298249-002), incorrectly refers to the “ICH3”. The first paragraph is changed to read:

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH2. V5REF must be powered up before or simultaneously to VCC3_3. It must also power down after or simultaneous to VCC3_3. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 82.a. shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

30. Changed: Section 10.3.1, AC ’97 Audio Codec Detect Circuit and Configuration Options; Table 25a; Modified

Table 25a, *Signal Descriptions*, added to the design guide by Document Change # 10 (Added: *AC ’97 Audio Codec Detect Circuit and Configuration Options*, Section 10.3.1) in the public *Intel® 815E Chipset Platform* Design Guide Update (document number 298249-002), incorrectly refers to the “ICH3”. Table 25a is changed to read:

CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC’ 97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC ’97 Interface (held in reset), because the CNR codec(s) will be the primary device(s) on the AC ’97 Interface.
AC97_RESET#	Reset signal from the AC ’97 Digital Controller (ICH2).
SDATA_I*nn*	AC ’97 serial data from an AC ’97-compliant codec to an AC ’97-compliant controller (i.e., the ICH2).

31. Changed: Section 13.4.1, PCI Interface, PME# Checklist Item; Modified

The PME# checklist item in Section 13.4.1, *PCI Interface*, is changed as shown below:

PME#	This signal has an integrated pull-up of 24 K.

32. Changed: Section 13.4.9, Power Management, PWRBTN# Checklist Item; Modified

The PWRBTN# checklist item in Section 13.4.9, *Power Management*, is changed as shown below:

PWRBTN#	This signal has an integrated pull-up of 24 K.

33. Changed: Title of Section 10.10.8, RTC-Well Input Strap Requirements

The title of Section 10.10.8 is changed to *Power-Well Isolation Control Strap Requirements*.

34. Changed: Section 10.10.1, RTC Crystal, Note 1 under Figure 57; Modified

Note 1 under Figure 57, *External Circuitry for the ICH2 RTC*, in Section 10.10.1, is changed as shown below:

1. The exact capacitor value needs to be based on what the crystal maker recommends.

   (Typical values for C2 and C3 are 18 pF for a crystal with C_{LOAD}=12.5 pF)

35. Changed: Section 13.4.13, RTC, RTCX1-RTCX2 Checklist Item; Modified

The first sentence in the RTCX1-RTCX2 checklist item in Section 13.4.13, *RTC*, is changed as shown below:

RTCX1 RTCX2	Connect a 32.768 kHz Crystal Oscillator across these pins with a 10 MΩ resistor and use 18 pF decoupling caps (assuming crystal with CLOAD=12.5 pF) at each signal.

36. Changed: Section 2, General Design Considerations; Modified

The last paragraph of Section 2, *General Design Considerations*, has the following material added to it so that the paragraph reads as follows:

Additionally, these routing guidelines are created using a PCB stack-up similar to that illustrated in the following figure. If this stack-up is not used, extremely thorough simulations of every interface must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

37. Changed: Section 10.11.5, Intel® 82562ET / 82562EH Dual Footprint Guidelines; Modified

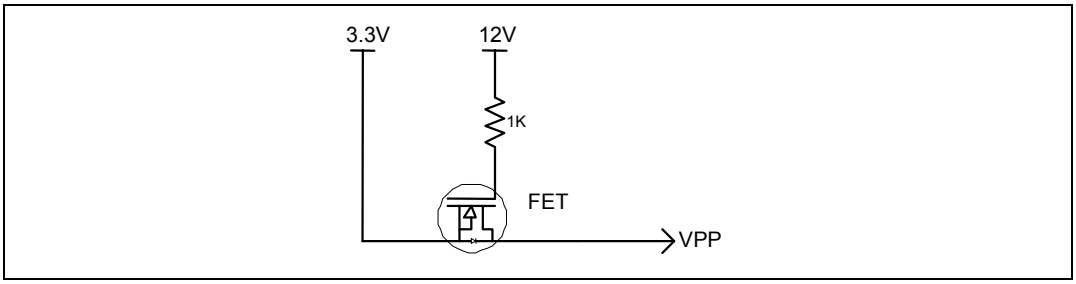
The bullets under Figure 72, *Dual-Footprint Analog Interface*, describe additional guidelines for Figures 71 and 72. The first bullet defines the “L” in Figure 71, *Dual Footprint LAN Connect Interface*. The “L” value is changed to 3.5 inches to 10 inches.

38. Changed: Section 10.12.2, FWH Vpp Design Guidelines; Modified

Section 10.12.2, *FWH Vpp Design Guidelines*, has the following paragraph and figure added as shown below:

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. In order to decrease programming time it becomes necessary to apply 12 V to the V_{PP} pin. The following circuit will allow testers to put 12 V on the V_{PP} pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 72.1 FWH VPP Isolation Circuitry



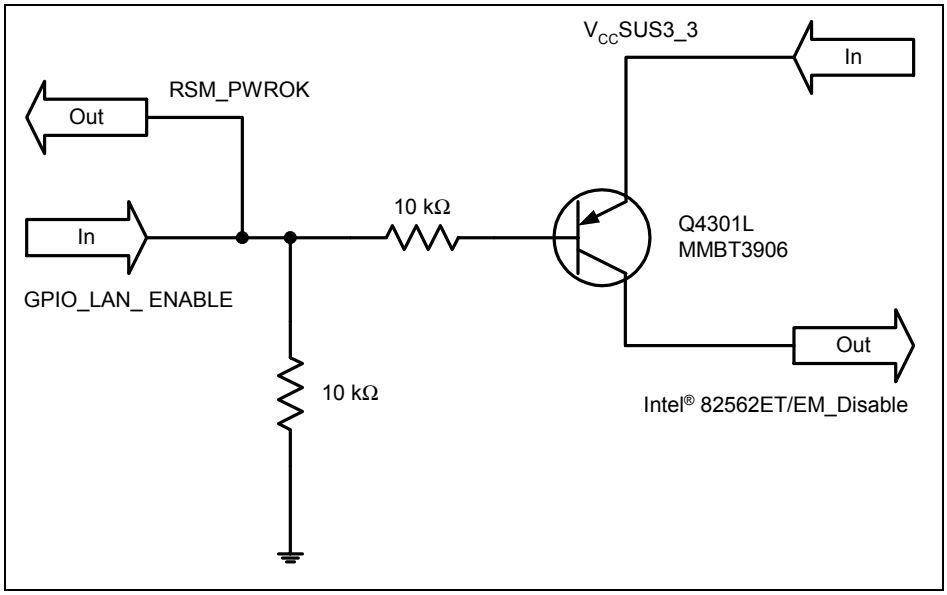
39. Added: Intel® 82562ET/EM Disable Guidelines, Section 10.11.4.6

New Section 10.11.4.6, *Intel® 82562ET/EM Disable Guidelines*, is added as shown below:

10.11.4.6. Intel® 82562ET/EM Disable Guidelines

To disable the 82562ET/EM, the device must be isolated (disabled) prior to reset (RSM_PWROK) asserting. Using a GPIO, such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown below will allow this behavior. The BIOS, by controlling the GPIO, can disable the LAN microcontroller.

Figure 70-1: Intel® 82562ET/EM Disable Circuit



There are 4 pins which are used to put the 82562ET/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. The table below describes the operational/disable features for this design.

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

The four control signals shown in the above table should be configured as follows: Test_En should be pulled-down through a 100 Ω resistor. The remaining three control signals should each be connected through 100 Ω series resistors to the common node “82562ET/EM _Disable” of the disable circuit.

40. Changed: Section 13.4.13, RTC; Modified Checklist Item

The following checklist item is added to Section 13.4.3, *RTC*:

RTCRST#	Ensure 10 ms–20 ms RC delay (8.2 K & 2. 2 µF) See Figure "RTCRST External Circuit for the ICH2 RTC."

41. Changed: Section 10.5, USB; Modified

The third bullet in Section 10.5, *USB*, is changed to read as follows:

An optional cap (0 pF – 47 pF) may be placed as close to the USB connector side of the series resistors on the USB data lines (P0+/-, P1+/-, P2+/-, P3+/-). This cap should be sized to minimize EMI radiation while still maintaining signal quality (rise/fall time, Vcrs, etc)."

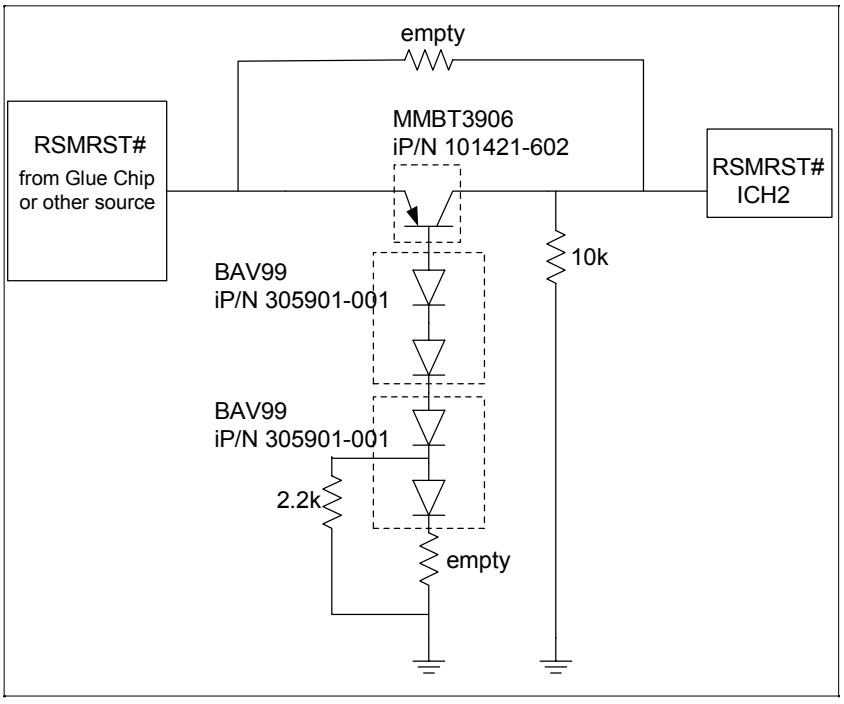
42. Changed: RTC Crystal, Section 10.10.1, Figure 57, ICH2 RTC Crystal Capacitor C1 Value; Modified

Reference Section 10.10.1, Figure 57, *External Circuitry for the ICH2 RTC*. The value of Capacitor C1 in Figure 57 is changed from 2.2 pF to 0.047 µF.

43. Added Information and Figure to Section 10.10.8, Power-Well Isolation Control Strap Requirements

Add the following information and figure to Section 10.8.8, *Power-Well Isolation Control Strap Requirements*:

The circuit shown in the figure below should be implemented to control well isolation between the 3.3V resume and RTC power-wells. Failure to implement this circuit may result in excessive droop on the VCCRTC node during Sx-to-G3 power state transitions (removal of AC power).



44. Changed Section 13.4.9, Power Management

Change the Recommendations for RSMRST# in Section 13.4.9, *Power Management*, to read as shown below:

"Connect to power monitoring logic, and should go high no sooner than 10mS after both VccSUS3_3 and VccSus1_8 have reached their nominal voltages. Requires weak pull-down. Also requires well isolation control as directed in section 10.10.8."

45. Added Information to Section 1.2.2.1, Intel® 82815 GMCH, Packaging Power

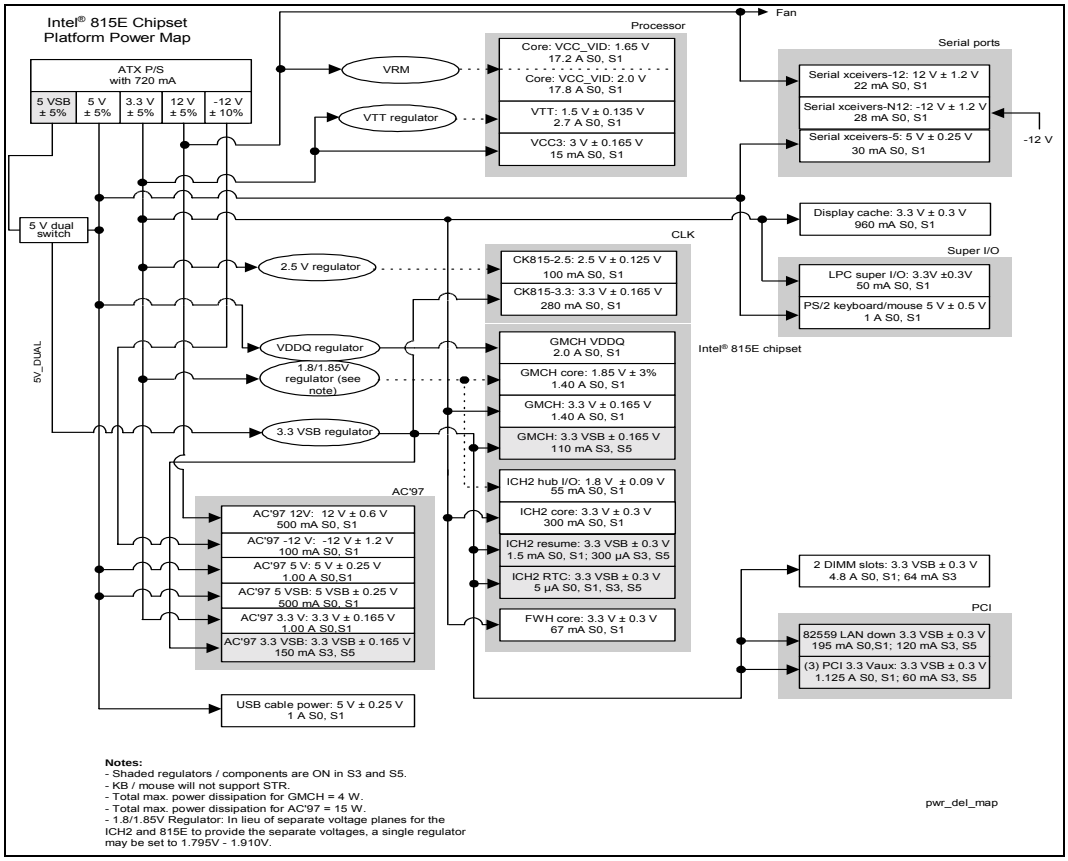
Reference Section 1.2.2.1, *Intel® 82815 GMCH, Packaging Power*. Add the following information to the bullet so that it reads:

- 1.85 V core and mixed 3.3 V, 1.5 V, and AGTL+ IO. Note that the 82801BA ICH2 has a 1.8 V requirement and the 82815 GMCH has a 1.85 V requirement. Instead of separate voltage regulators to meet these requirements, a single voltage regulator can be set to 1.795V to 1.910 V. See Figure 77, the Power Delivery Map.

46. Replaced Figure 77, Power Delivery Map

Figure 77, Power Delivery Map, is replaced with the following:

Figure 77. Power Delivery Map



47. Added Section 9.5 Power_Supply PS_ON Considerations

The following new section is added:

9.5 Power_Supply PS_ON Considerations

– If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10–100 mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

–The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

–The platform designer must ensure that the power supply used with the platform is not affected by this issue.

48. Changed Section 13.4.13, RTC, Add SUSCLK to the Checklist

Add the following as a new checklist item to Section 13.4.13, *RTC*:

SUSCLK	To assist in RTC circuit debug, route SUSCLK to a test point if SUSCLK is unused.

49. Changed Section 13.4.16, Power, Modify Checklist Recommendations for 5V_REF_SUS

Change the second bullet in the Recommendations column of the 5V_REF_SUS to the following:

V5REF_SUS affects 5V-tolerance for all USB pins and can be connected to VccSUS3_3 if ICH2 USB is not supported in the platform. If USB is supported, 5VREF_SUS must be connected to 5V_AUX, which remains powered during S5.

50. Changed Section 12.4.3, 3.3V/V5REF Sequencing

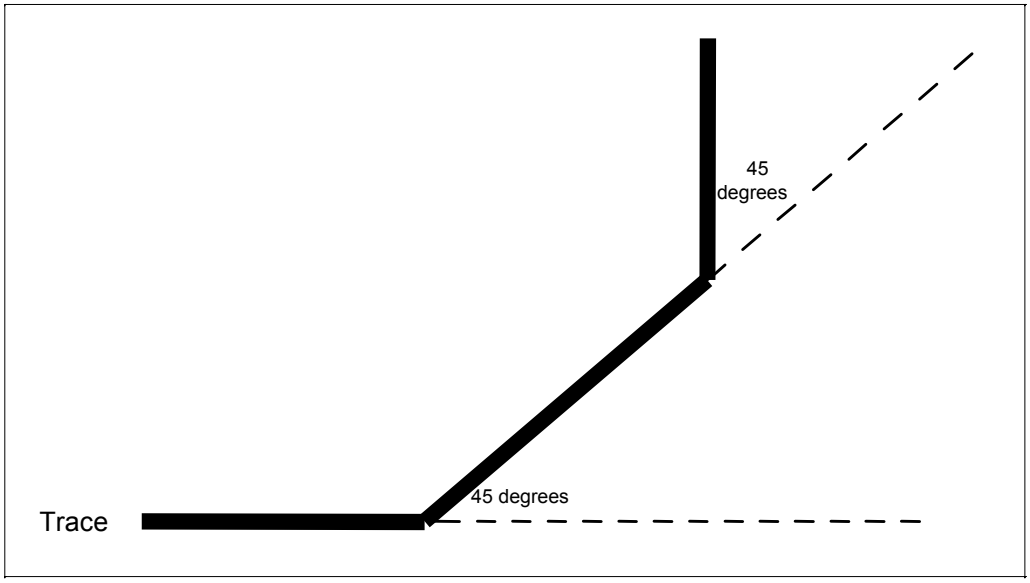
Section 12.4.3, 3.3V/V5REF Sequencing, was added by Document Change #21 of this document. Change the second and third paragraphs of Section 12.4.3, 3.3V/V5REF Sequencing, to the following:

This rule also applies to the stand-by rails. However, in most platforms the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USB pins (both over-current and data lines). If USB is not implemented in the system then V5REF_SUS can be connected to the VccSus3_3 rail. Otherwise when USB is supported, V5REF_SUS must be connected to 5V_AUX, which remains powered during S5.

51. Changed Figure 64, Trace Routing, in Section 10.11.2.1, General Trace Routing Considerations

Figure 64, *Trace Routing*, in Section 10.11.2.1, *General Trace Routing Considerations*, is replaced with the following figure:



52. Changed Table 30, Intel® CK-815 (2-DIMM) Clocks, in Section 11.1, 2-DIMM Clocking

The frequency entry for the 9 SDRAM clocks in Table 30, *Intel® CK-815 (2-DIMM) Clocks*, in Section 11.1, *2-DIMM Clocking*, is changed to “100/133 MHz”.

Also, the first bullet under Table 30 is changed to show “100/133 MHz”.

53. Changed Table 31, Intel® CK-815 (3-DIMM) Clocks, in Section 11.2, 3-DIMM Clocking

The frequency entry for the 9 SDRAM clocks in Table 31, *Intel® CK-815 (3-DIMM) Clocks*, in Section 11.2, *3-DIMM Clocking*, is changed to “100/133 MHz”.

54. Changed: Section 12.4.3, 3.3V/V5REF Sequencing

Section 12.4.3, *3.3V/V5REF Sequencing*, was added by Design Guide Update Rev 1.6, dated 12/05/00, and modified by Document Change #21 in the public *Intel® 815E Chipset Platform Design Guide Update* 298249-004, dated February 2002. Change the first paragraph of Section 12.4.3, 3.3V/V5REF Sequencing, to the following:

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7 V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0 .7 V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 82.a. shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

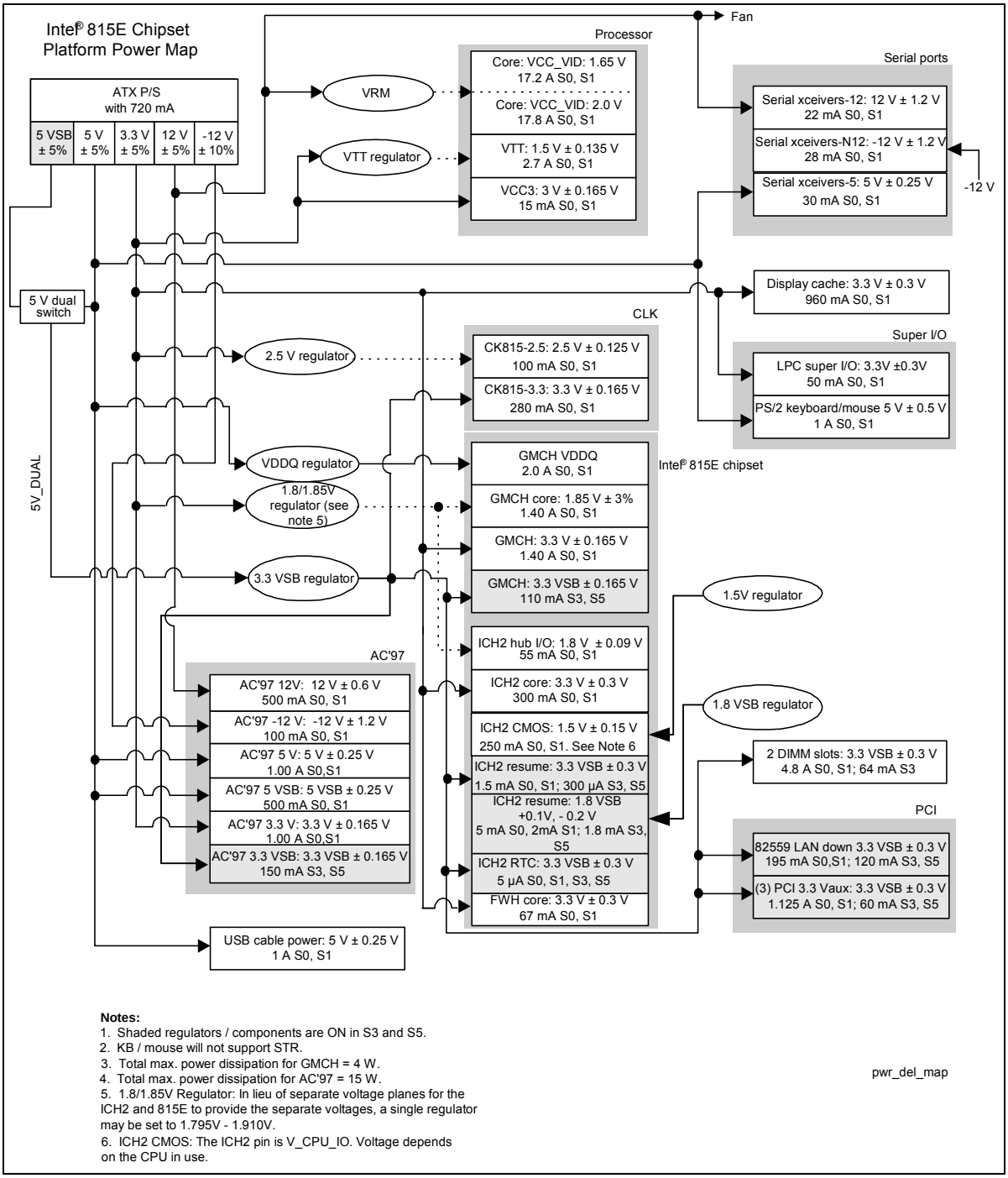
55. Changed: Figure 77, Power Delivery Map, in Section 12, Power Delivery

Figure 77, *Power Delivery Map*, in Section 12, Power Delivery, was replaced by Document Change #45 in the public *Intel® 815E Chipset Platform Design Guide Update* 298249-004, dated February 2002. Figure 77 has two additional changes in the ICH2 section.

1. One ICH2 power plane is added to it. This added ICH2 power plane is “ICH2 V5REF_SUS”. This power plane has always existed in the ICH2. It is not new. This addition to the Power Delivery Map simply shows this ICH2 plane.
2. The block labeled “ICH2 5V” is renamed to “ICH2 V5REF”.

These two changes above also reflect the actual pin names on the ICH2.

Figure 77, *Power Delivery Map*, is replaced with the following:


Intel® 815E Chipset
Platform Power Map
ATX P/S
with 720 mA
5 VSB ± 5%
5 V ± 5%
3.3 V ± 5%
12 V ± 5%
-12 V ± 10%
VRM
VTT regulator
Fan
Processor
Core: VCC_VID: 1.65 V
17.2 A S0, S1
Core: VCC_VID: 2.0 V
17.8 A S0, S1
VTT: 1.5 V ± 0.135 V
2.7 A S0, S1
VCC3: 3 V ± 0.165 V
15 mA S0, S1
Serial ports
Serial xceivers-12: 12 V ± 1.2 V
22 mA S0, S1
Serial xceivers-N12: -12 V ± 1.2 V
28 mA S0, S1
Serial xceivers-5: 5 V ± 0.25 V
30 mA S0, S1
-12 V
5 V dual switch
Display cache: 3.3 V ± 0.3 V
960 mA S0, S1
CLK
2.5 V regulator
CK815-2.5: 2.5 V ± 0.125 V
100 mA S0, S1
CK815-3.3: 3.3 V ± 0.165 V
280 mA S0, S1
Super I/O
LPC super I/O: 3.3V ±0.3V
50 mA S0, S1
PS/2 keyboard/mouse 5 V ± 0.5 V
1 A S0, S1
5V_DUAL
VDDQ regulator
1.8/1.85V regulator (see note 5)
3.3 VSB regulator
GMCH VDDQ
2.0 A S0, S1
GMCH core: 1.85 V ± 3%
1.40 A S0, S1
GMCH: 3.3 V ± 0.165 V
1.40 A S0, S1
GMCH: 3.3 VSB ± 0.165 V
110 mA S3, S5
Intel® 815E chipset
1.5V regulator
AC'97
AC'97 12V: 12 V ± 0.6 V
500 mA S0, S1
AC'97 -12 V: -12 V ± 1.2 V
100 mA S0, S1
AC'97 5 V: 5 V ± 0.25 V
1.00 A S0,S1
AC'97 5 VSB: 5 VSB ± 0.25 V
500 mA S0, S1
AC'97 3.3 V: 3.3 V ± 0.165 V
1.00 A S0,S1
AC'97 3.3 VSB: 3.3 VSB ± 0.165 V
150 mA S3, S5
ICH2 hub I/O: 1.8 V ± 0.09 V
55 mA S0, S1
ICH2 core: 3.3 V ± 0.3 V
300 mA S0, S1
ICH2 CMOS: 1.5 V ± 0.15 V
250 mA S0, S1. See Note 6
ICH2 resume: 3.3 VSB ± 0.3 V
1.5 mA S0, S1; 300 µA S3, S5
ICH2 resume: 1.8 VSB
+0.1V, - 0.2 V
5 mA S0, 2mA S1; 1.8 mA S3, S5
ICH2 RTC: 3.3 VSB ± 0.3 V
5 µA S0, S1, S3, S5
FWH core: 3.3 V ± 0.3 V
67 mA S0, S1
1.8 VSB regulator
2 DIMM slots: 3.3 VSB ± 0.3 V
4.8 A S0, S1; 64 mA S3
PCI
82559 LAN down 3.3 VSB ± 0.3 V
195 mA S0,S1; 120 mA S3, S5
(3) PCI 3.3 Vaux: 3.3 VSB ± 0.3 V
1.125 A S0, S1; 60 mA S3, S5
USB cable power: 5 V ± 0.25 V
1 A S0, S1
Notes:
1. Shaded regulators / components are ON in S3 and S5.
2. KB / mouse will not support STR.
3. Total max. power dissipation for GMCH = 4 W.
4. Total max. power dissipation for AC'97 = 15 W.
5. 1.8/1.85V Regulator: In lieu of separate voltage planes for the ICH2 and 815E to provide the separate voltages, a single regulator may be set to 1.795V - 1.910V.
6. ICH2 CMOS: The ICH2 pin is V_CPU_IO. Voltage depends on the CPU in use.
pwr_del_map