Intel® 815 Chipset Platform

Design Guide Update

January 2001

Notice: The Intel® 815 chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 298250-002

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release: Schematic.Added Layout and Routing Updates 1–2. Added Documentation Changes # 1–5.	August 2000
-002	Added Schematic, Layout and Routing Update 3. Added Documentation Change #6.	January 2001

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 815 Chipset Platform Design Guide	298233-001

Nomenclature

General Design Considerations includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® 815 chipset.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Shaded:	This item is either new or modified from the previous version of the document.

NO.	GENERAL DESIGN CONSIDERATIONS
	There are no known General Design Consideration updates at this time

NO.	SCHEMATIC, LAYOUT AND ROUTING UPDATES
1	Changed: Clock Routing Guidelines, Section 10.3; New Layout Guidelines for SDRAM, SCLK, and GMCH HCLK
2	Changed: Schematic Page 4 of 41; VCOREDET Pin
3	Changed: Schematic Page 12 of 41, SA0 and WP Pullup; Note Added

NO.	DOCUMENTATION CHANGES
1	Changed: Third-Party Vendor Information, Chapter 13; Tables Added
2	Changed: Miscellaneous Checklist for 370-Pin Socket Processors, Section 12.4; Checklist Item No Connects
3	Changed: Clock Synthesizer Checklist, Section 12.16; Table Modified
4	Changed: Digital Video Output Port, Section 12.8; Replaced
5	Changed: Miscellaneous Checklist for 370-Pin Socket Processors, Section 12.4; Checklist Item VCORE_DET (E21)
6	Changed: SMBus, Section 9.5; “RIMM” Reference Removed

General Design Considerations

There are no known General Design Consideration updates at this time.

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Schematic, Layout and Routing Updates

1. Changed: Clock Routing Guidelines, Section 10.3; New Layout Guidelines for SDRAM, SCLK, and GMCH HCLK

These new clock guidelines are for future designs to improve PC133 SDRAM Clock Quality. Replace Section 10.3 with the following:

10.3 Clock Routing Guidelines

This section presents the generic clock routing guidelines for both 2-DIMM and 3-DIMM boards. For 3-DIMM boards, additional analysis must be performed by the motherboard designer to ensure that the clocks generated by the external PCI clock buffer meet the PCI specifications for clock skew at the receiver, when compared with the PCI clock at the ICH.

Figure 59. Clock Routing Topologies

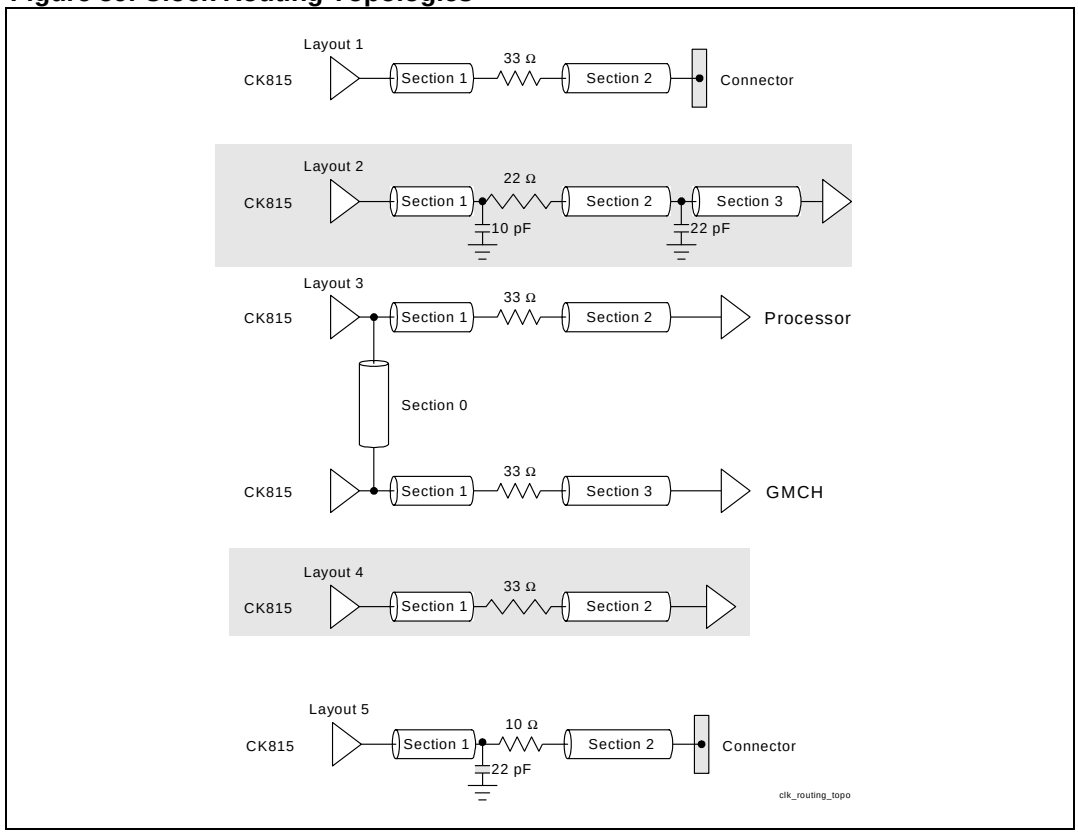

Table 27. Simulated Clock Routing Solution Space

Destination	Topology from Previous Figure	Section 0 Length	Section 1 Length	Section 2 Length	Section 3 Length
SDRAM MCLK	Layout 5	N/A	< 0.5”	A[1]	N/A
GMCH SCLK[3]	Layout 2	N/A	< 0.5”=L1	A + 3.5” – L1	0.5”
Processor BCLK	Layout 3	< 0.1”	< 0.5”	A + 5.2”	A + 8”
GMCH HCLK			<0.5”		
GMCH HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH HUBCLK	Layout 4	N/A	<0.5”	A + 8”	N/A
ICH PCICLK	Layout 4	N/A	<0.5”	A + 8”	N/A
AGP CLK	Layout 4	N/A	<0.5”	A + 3" to A + 4"	N/A
PCI down[2]	Layout 4	N/A	<0.5”	A + 8.5” to A + 14”	N/A
PCI slot[2]	Layout 1	N/A	<0.5”	A + 5” to A + 11”	

NOTES:
1. Length “A” has been simulated up to 6”.
2. All PCI clocks must be within 6” of the ICH PCICLK route length. Routing on PCI add-in cards must be included in this length. In the presented solution space, ICH PCICLK was considered to be the shortest in the 6” trace routing range, and other clocks were adjusted from there. The system designer may choose to alter the relationship of PCI device and slot clocks, as long as all PCI clock lengths are within 6”. Note that the ICH PCICLK length is fixed to meet the skew requirements of ICH PCICLK to ICH HUBCLK
3. 22 pf Load cap should be placed 0.5” from GMCH Pin.

General Clock Layout Guidelines

- All clocks should be routed 5 mils wide with 15-mil spacing to any other signals.
- It is recommended to place capacitor sites within 0.5” of the receiver of all clocks. They are useful in system debug and AC tuning.
- Series resistor for clock guidelines: 22 Ω for GMCH SCLK and 10 Ω for SDRAM clocks. All other clocks use 33 Ω.
- Each DIMM clock should be matched within ±10 mils.

Clock Decoupling

Several general layout guidelines should be followed when laying out the power planes for the CK815 clock generator, as follows:

- Isolate power planes to the each of the clock groups.
- Place local decoupling as close as possible to power pins, and connect with short, wide traces and copper.
- Connect pins to appropriate power plane with power vias (larger than signal vias).
- Bulk decoupling should be connected to a plane with 2 or more power vias.
- Minimize clock signal routing over plane splits.
- Do not route any signals underneath the clock generator on the component side of the board.
- An example signal via is a 14-mil finished hole with a 24-mil to 26-mil path. An example power via is an 18-mil finished hole with a 33-mil to 38-mil path. For large decoupling or power planes with large current transients, a larger power via is recommended.

2. Changed: Schematic Page 4 of 41; VCOREDET Pin

Page 4 of 41 (370-Pin Socket, Part 2) of the 82815 Customer Reference Board (CRB) Schematics show the VCOREDET pin (lower right corner of the schematic) pulled high to VCC3_3 through a 220 Ohm resistor and also connected to VCOREDET page 8 of 42 (GMCH Reset Straps). These connections are not correct.

The VCOREDET pin on the 370-Pin Socket, Part 2, page 4 of 41, should be left as a no-connect.

3. Changed: Schematic Page 12 of 41, SA0 and WP Pullup; Note Added

The following ***note*** should be added to schematic page 12 of 41:

Note: Do not depopulate R30 in an attempt to write to SPD. If R30 is removed, SA0 is left floating which adversely affects SMBus operation.

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Documentation Changes

1. Changed: Third-Party Vendor Information, Chapter 13; Tables Added

The following four new tables are added to Chapter 13, "Third-Party Vendor Information."

TMDS Transmitters

Vendors	Component	Contact	Phone
Silicon Images	SII164	John Nelson	(408) 873- 3111
Texas Instrument	TFP420	Greg Davis [gdavis@ti.com]	(214) 480-3662
Chrontel	CH7301	Chi Tai Hong [cthong@chrontel.com]	(408) 544-2150

TV Encoders

Vendors	Component	Contact	Phone
Chrontel	CH7007 / CH7008	Chi Tai Hong [cthong@chrontel.com]	(408)544-2150
Chrontel	CH7010 / CH7011	Chi Tai Hong [cthong@chrontel.com]	(408)544-2150
Conexant	CN870 / CN871	Eileen Carlson [eileen.carlson@conexant.com]	(858) 713-3203
Focus	FS450 / FS451	Bill Schillhammer [billhammer@focusinfo.com]	(978) 661-0146
Philips	SAA7102A	Marcus Rosin [marcus.rosin@philips.com]	None
Texas Instrument	TFP6022 / TFP6024	Greg Davis [gdavis@ti.com]	(214) 480-3662

Combo TMDS Transmitters/TV Encoders

Vendors	Component	Contact	Phone
Chrontel	CH7009 / CH7010	Chi Tai Hong [cthong@chrontel.com]	(408) 544-2150
Texas Instrument	TFP6422 / TFP6424	Greg Davis [gdavis@ti.com]	(214) 480-3662

LVDS Transmitter

Vendors	Component	Contact	Phone
National Semiconductor	387R	Jason Lu [Jason.Lu@nsc.com]	(408) 721-7540

2. Changed: Miscellaneous Checklist for 370-Pin Socket Processors, Section 12.4; Checklist Item No Connects

In Section 12.4, the removal of eight Vtt no connects is reflected in the last box, which changes as follows:

NO CONNECTS	The following pins must be left as no-connects: AK30, AM2, F10, G37, L33, N33, N35, N37, Q33, Q35, Q37, R2, W35, X2, Y1

3. Changed: Clock Synthesizer Checklist, Section 12.16; Table Modified

In Section 12.16, changes from the Layout Updates are reflected in modifications to the last box as follows:

MEMCLK0/DRAM_0, MEMCLK1/DRAM_1, MEMCLK2/DRAM_2, MEMCLK3/DRAM_3, MEMCLK4/DRAM_4, MEMCLK5/DRAM_5, MEMCLK6/DRAM_6, MEMCLK7/DRAM_7,	Pass through 10 Ω resistor
SCLK	Pass through 22 Ω resistor

4. Changed: Digital Video Output Port, Section 12.8; Replaced

Checklist Section 12.8, page 135, is replaced with the following:

12.8 Digital Video Input Checklist

Checklist Items	Recommendations
DVI Input Reference Circuit	See reference schematics in the documentation of the third party vendor of the device of choice in your design. The Third Party-Vendor information is a part of this Design Guide and its associated Design Guide Updates.

5. Changed: Miscellaneous Checklist for 370-Pin Socket Processors, Section 12.4; Checklist Item VCORE_DET (E21)

Checklist Section 12.4, page 131, change the “Recommendations” section of the VCORE_DET (E21) checklist item as follows:

VCORE_DET (E21)	This pin should be left as a no-connect.

6. Changed: SMBus, Section 9.5; “RIMM” Reference Removed

Reference page 104, Section 9.5, *SMBus*, change the last sentence in the paragraph to read:

“If the SMBus is used only for the SPD EEPROMs on the SDRAM, both SMBus signals should be pulled up with a 4.7 KΩ resistor to 3.3 V.”