Intel® 815 Chipset Platform for Use with Universal Socket 370

Design Guide Update

October 2002

Notice: The Intel® 815 Chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Document Number: 298308-002

Contents

Revision History

Revision	Draft/Changes	Date
-001	Initial Release	October 2001
-002	Added Schematic, Layout and Routing Change #5	October 2002

Preface

This document is an update to the specifications contained in the *Intel® 815 Chipset Platform for Use with Universal Socket 370 Design Guide*, April 2001, document number 298349-001.

The following documents may also be referenced:

- *Intel® 815 Chipset Family: 82815 Graphics and Memory Controller Hub (GMCH) For Use with Universal Socket 370 Datasheet*, April 2001, document number 298351-001.
- *Intel® 82801BA (ICH2) I/O Controller Hub Datasheet*, document number 290687-002.

This update is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. This design guide is primarily targeted at the PC market segment and was first published in 2000. Those using this design guide should check for device availability before designing in any of the components included in this document.

Nomenclature

General Design Considerations includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® 815 Chipset Platform for Use with Universal Socket 370.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc:	Document change or update that will be implemented.
Shaded:	This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
1	Doc	Added Support for P-MOS Kicker “ON”: SMAA[9] Is Strapped High by Internal 50 kΩ Pull-Up

NO.	Plans	SCHEMATIC, LAYOUT AND ROUTING UPDATES
1	Doc	Changed: Appendix A, Schematic Page 6 of 40: Replace R135
2	Doc	Changed: Appendix A, Schematic Page 33 of 40: Replace R332 and R334
3.	Doc	Changed: Appendix A, Schematic Page 31 of 40: Change VTTPWRGD Circuit
4.	Doc	Changed: Appendix A, Schematic Page 7 of 40: Change SMAA[9] Circuit to Enable FSB P-MOS Kicker
5	Doc	Changed: Appendix A, Schematic Page 7 of 40: Delete SM_BS0 and SM_BS1

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Added Workaround for THERMTRIP Erratum
2	Doc	Changed: Processor Frequency for Which Current Heatsink Recommendations Are Valid
3	Doc	Changed: Processor Pin Names, Section 5.4
4	Doc	Changed: Processor Pin Names, Section 4.1

General Design Considerations

1. Added Support for P-MOS Kicker "ON": SMAA[9] Is Strapped High by an Internal 50 kΩ Pull-Up

The PSB P-MOS Kicker circuit should be enabled (SMAA[9] is strapped high through an internal 50 kΩ pull-up resistor to enable P-MOS Kicker) on all new, future 815 Universal Socket 370 designs. Use of the P-MOS Kicker circuit improves PSB timings by improving AGTL and AGTL+ signal flight time.

Existing designs which have implemented the pull-down resistor circuit on the SMAA[9] signal as shown in the Customer Reference Board schematics and populated the resistor site to over-ride the internal pull-up resistor, may depopulate the site to enable the P-MOS Kicker circuit. This activity should be based on timing analysis of the specific platform.

P-MOS Kicker circuit "ON" is the recommended setting for 815 Universal Socket 370 designs using future 0.13 micron technology processors.

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Schematic, Layout and Routing Updates

1. Changed: Appendix A, Schematic Page 6 of 40, Replace R135:

The GTLREF circuit for the GMCH does not reflect the updated recommendation in the design guide. Resistor R135 should be replaced with a 63.4 kΩ, 1% resistor.

2. Changed: Appendix A, Schematic Page 33 of 40, Replace R332 and R334:

With the change in the VRM specification for the Pentium III processor 900 MHz, the reference schematic has been updated to meet that processor's load line requirements. Resistor R332 should be replaced with a 27.4 kΩ, 1% resistor. Resistor R334 should be replaced with a 30.1 kΩ, 1% resistor.

3. Changed: Appendix A, Schematic Page 31 of 40, Change VTTPWRGD Circuit:

To guarantee proper operation of the comparators in the VTTPWRGD circuit, the power rail of U72 should be connected to 5 V-standby instead of normal VCC5.

4. Changed: Appendix A, Schematic Page 7 of 40, Change SMAA[9] Circuit to Enable FSB P-MOS Kicker:

To enable the front side bus P-MOS Kicker, remove Resistor 3-6 of Rpack 37. The SMAA[9] signal has an internal 50 kΩ pull-up which enables the P-MOS Kicker at power-up.

5. Changed: Appendix A, Schematic Page 7 of 40, Delete SM_BS0 and SM_BS1:

SM_BS0 and SM_BS1 are reserved pins, therefore the pull-down circuit shown on page 7 of 40 should be deleted.

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Documentation Changes

1. Addition of Workaround for THERMTRIP Erratum

Reference Paragraph 5.3.1, THERMTRIP Circuit, page 51. The following text has been added to the end of the section as Paragraph 5.3.1.2, THERMTRIP Support For 0.13 Micron Technology Processors, A-1 Stepping:

A platform supporting the 0.13 micron technology processor must implement a workaround required for the A-1 stepping of that processor, identified by CPUID = 6B1h.

The internal control register bit responsible for operation of the THERMTRIP circuit functionality may power up in an un-initialized state. As a result, THERMTRIP# may be incorrectly asserted during de-assertion of RESET# at nominal operating temperatures. When THERMTRIP# is asserted as a result of this, the processor may shut down internally and stop execution. In addition, when the THERMTRIP# pin is asserted the processor may incorrectly continue to execute, leading to intermittent system power-on boot failures. The occurrence and repeatability of failures is system dependent, however all systems and processors are susceptible to failure.

To prevent the risk of power-on boot failures, a platform workaround is required. The system must provide a rising edge on the TCK signal during the power-on sequence that meets all of the following requirements:

•Rising edge occurs after VCC_CORE is valid and stable

•Rising edge occurs before or at the de-assertion of RESET#

•Rising edge occurs after all VREF input signals are at valid voltage levels

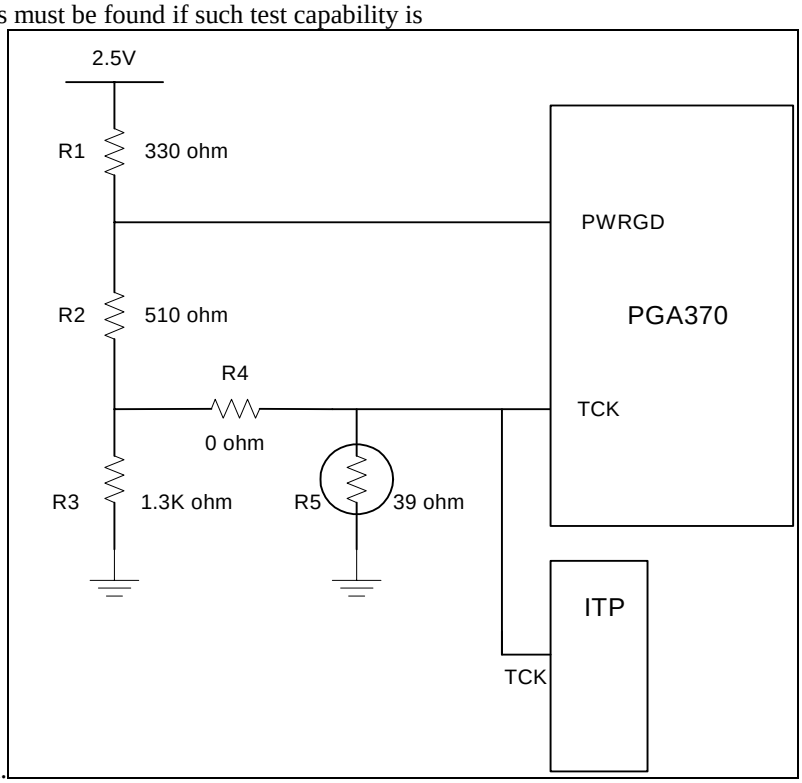
•TCK input meets the VIH min (1.3 V) and max (1.65 V) spec requirements

Specific workaround implementations may be platform-specific. The following examples have been tested as acceptable workaround implementations.

Note: the example workaround circuits attached require circuit modification for ITP tools to function correctly. These modifications must remove the workaround circuitry from the platform and may cause systems to fail to boot. Review the accompanying notes with each workaround for ITP modification details. If the system fails to boot when using ITP, issuing the ITP ‘Reset Target’ command on failing systems will reset the system and provide a sufficient rising edge on the TCK pin to ensure proper system boot.

In addition, the example workaround circuits shown do not support production motherboard test methodologies that require the use of the processor JTAG/TAP port. Alternative workaround

solutions must be found if such test capability is



required.

For Production Boards:
Depopulate R5

To use ITP:
Install R5, Depopulate R4

2. Changed: Processor Frequency for Which Current Heatsink Recommendations Are Valid

Section 5.12.1, first sentence is changed to read, “Current heatsink recommendations are only valid for supported Intel® Celeron® and Intel® Pentium® III processor frequencies up to 1 GHz.”

3. Changed: Processor Pin Names, Section 5.4, PGA370 Socket Definition Details, Table 12, Processor Pin Definition Comparison

Reference Section 5.4, *PGA370 Socket Definition Details*, Table 12, *Processor Pin Definition Comparison*:

Pin# AF36: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “NC” to “DETECT”

Pin# AJ3: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “RESET” to “RESET2#”

Pin# Y1: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “NC” to “RESERVED”

Pin# Z36: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “NC” to “RESERVED”

4. Changed: Processor Pin Names, Section 4.1, Universal Motherboard Definition Details, Table 1, Processor Considerations for Universal Motherboard Design

Reference Section 4.1, *Universal Motherboard Definition Details*, Table 1, *Processor Considerations for Universal Motherboard Design*:

Pin# AF36: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “NC” to “DETECT”

Pin# AJ3: Pin Name Future 0.13 Micron Socket 370 Processors is changed from “RESET” to “RESET2#”