Intel® 815EP Chipset Platform for Use with Universal Socket 370

Design Guide Update

April 2002

Document Number: 298602-003

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	December 2001
-002	Added Document Change #8, Changed Section 12.4.3, 3.3V/V5REF Sequencing	March 2002
-003	Added Document Change #9-10.	April 2002

Preface

This Design Guide Update document is an update to the specifications and information contained in the *Intel® 815EP Chipset Platform for Use with Universal Socket 370 Design Guide*, September 2001. This Design Guide Update may reference other documents listed in the following Affected Documents/Related Documents table. This document is a compilation of updates to the general design considerations; schematic, layout, and routing updates; and documentation changes. This document is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools. The design guide (and this design guide update) is primarily targeted at the PC market segment and was first published in 2001. Those using this design guide and update should check for device availability before designing in any of the components included in this document.

Information types defined in the Nomenclature section of this document are consolidated into the public update document when the public document is first published. This update document contains a complete list of all known information types.

Affected Documents/ Related Documents

Document Title	Document Number
Intel® 815EP Chipset Platform for Use with Universal Socket 370 Design Guide, September 2001	298593-001

Nomenclature

General Design Considerations includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® 815E chipset.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Summary Table of Changes

Codes Used in Summary Table

Doc: Document change or update that will be implemented.

Shaded: This item is either new or modified from the previous version of the document.

NO.	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no General Design Considerations in this Design Guide Update revision.

NO.	Plans	SCHEMATIC, LAYOUT AND ROUTING UPDATES
		There are no Schematic, Layout and Routing Updates in this Design Guide Update revision.

NO.	Plans	DOCUMENTATION CHANGES
1	Doc	Added Section 9.5 Power_Supply PS_ON Considerations
2	Doc	Changed Section 13.4.12, RTC, Add SUSCLK to the Checklist
3	Doc	Changed Section 13.4.15, Power, Modify Checklist Recommendations for 5V_REF_SUS
4	Doc	Changed Section 12.3.3, 3.3V/V5REF Sequencing
5	Doc	Changed Figure 79, RTC Power Well Isolation Control, in Section 10.8.6, Power Well Isolation Control Strap Requirements
6	Doc	Changed Table 40, CK-815 (2-DIMM) Clocks, in Section 11.1, 2-DIMM Clocking
7	Doc	Changed Table 41, CK-815 (3-DIMM) Clocks, in Section 11.2, 3-DIMM Clocking
8	Doc	Changed Section 12.4.3, 3.3V/V5REF Sequencing
9	Doc	Changed Figure 98, Power Delivery Map, in Section 12, Power Delivery
10	Doc	Added Document Change #10, Added Section 2.4, Electrostatic Discharge Platform Recommendations

General Design Considerations

There are no General Design Considerations in this Design Guide Update revision.

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Schematic, Layout and Routing Updates

There are no Schematic, Layout and Routing Updates in this Design Guide Update revision.

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Documentation Changes

1. Added: Section 9.5 Power_Supply PS_ON Considerations

The following new section is added:

9.5 Power_Supply PS_ON Considerations

– If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10–100 mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

–The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

–The platform designer must ensure that the power supply used with the platform is not affected by this issue.

2. Changed: Section 13.4.12, RTC, Add SUSCLK to the Checklist

Add the following as a new checklist item to Section 13.4.12, *RTC*:

SUSCLK	To assist in RTC circuit debug, route SUSCLK to a test point if it is unused.

3. Changed: Section 13.4.15, Power, Modify Checklist Recommendations for 5V_REF_SUS

Change the second bullet in the Recommendations column of the 5V_REF_SUS to the following:

- V5REF_SUS affects 5V-tolerance for all USB pins and can be connected to VccSUS3_3 if ICH2 USB is not supported in the platform. If USB is supported, 5VREF_SUS must be connected to 5V_AUX, which remains powered during S5.

4. Changed: Section 12.4.3, 3.3V/V5REF Sequencing

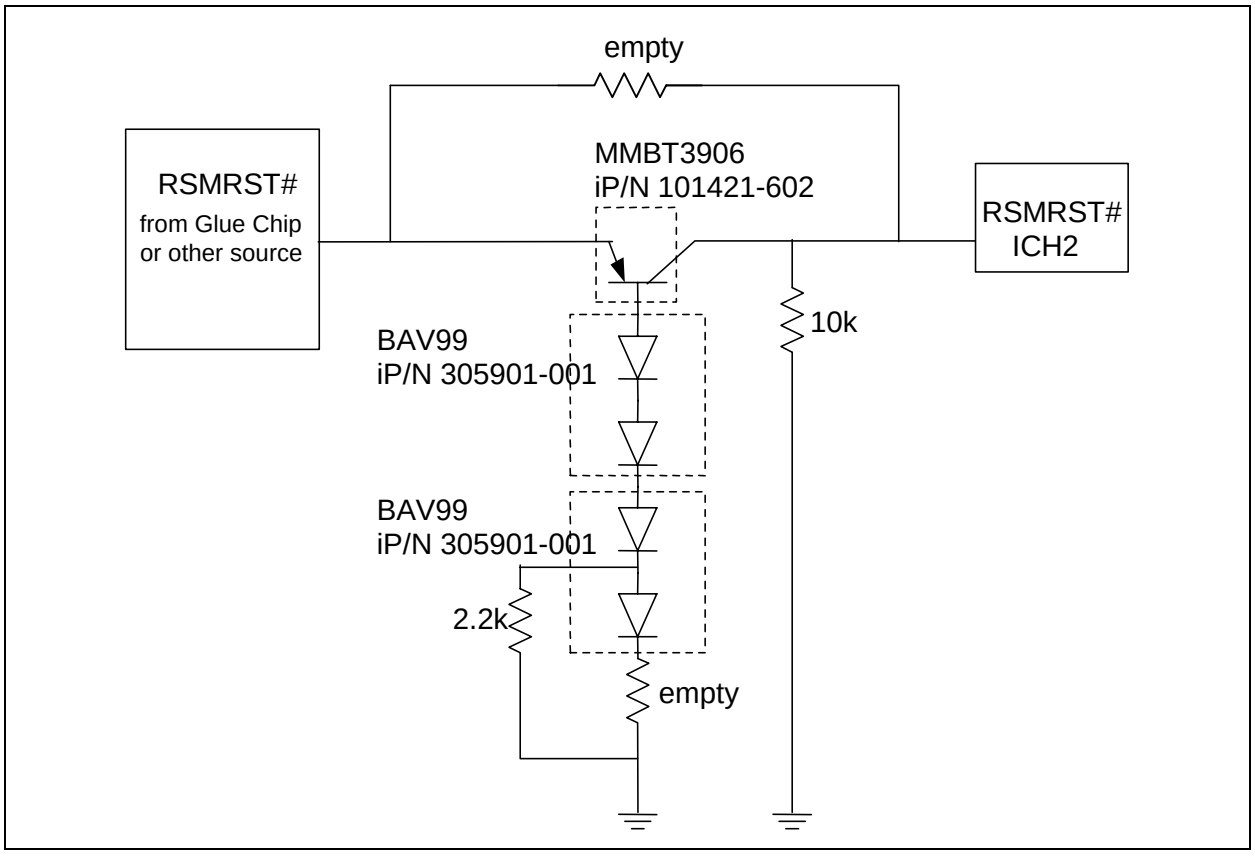
Change the second and third paragraphs of Section 12.4.3, *3.3V/V5REF Sequencing*, to the following:

This rule also applies to the stand-by rails. However, in most platforms the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USB pins (both over-current and data lines). If USB is not implemented in the system then V5REF_SUS can be connected to the VccSus3_3 rail. Otherwise when USB is supported, V5REF_SUS must be connected to 5V_AUX, which remains powered during S5.

5. Changed Figure 79, RTC Power Well Isolation Control, in Section 10.8.6, Power Well Isolation Control Strap Requirements

Figure 79, RTC Power Well Isolation Control, is changed to the following:



6. Changed Table 40, CK-815 (2-DIMM) Clocks, in Section 11.1, 2-DIMM Clocking

The frequency entry for the 9 SDRAM clocks in Table 40, *CK-815 (2-DIMM) Clocks*, in Section 11.1, *2-DIMM Clocking*, is changed to "100/133 MHz".

Also, the first bullet under Table 40 is changed to show "100/133 MHz."

7. Changed Table 41, CK-815 (3-DIMM) Clocks, in Section 11.2, 3-DIMM Clocking

The frequency entry for the 9 SDRAM clocks in Table 41, *CK-815 (3-DIMM) Clocks*, in Section 11.2, *3-DIMM Clocking*, is changed to "100/133 MHz."

8. Changed Section 12.4.3, 3.3V/V5REF Sequencing

The first paragraph in this section is changed to read:

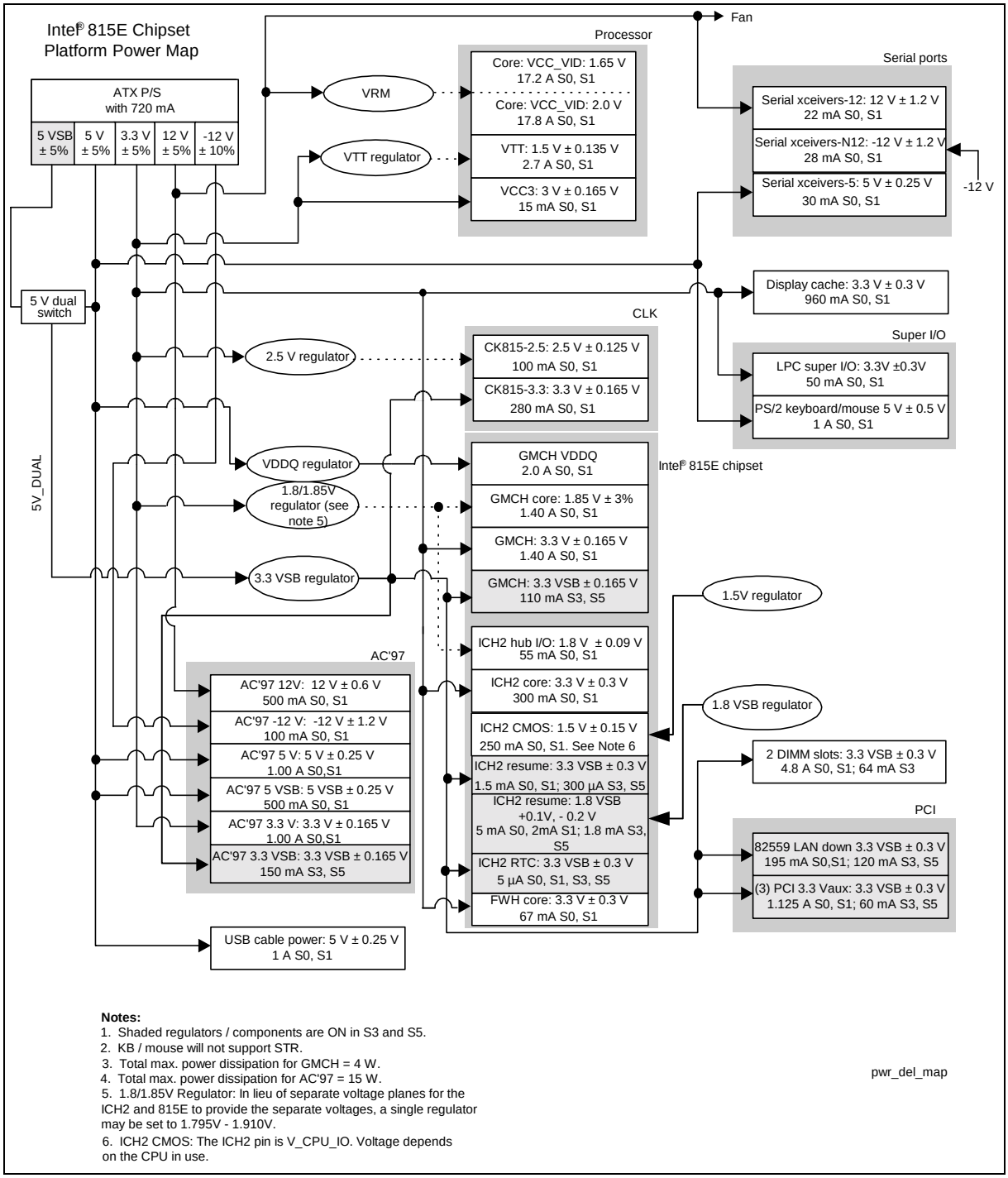
V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within 0.7V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within 0 .7V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 101 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

9. Changed Figure 98, Power Delivery Map, in Section 12, Power Delivery

Figure 98, *Power Delivery Map*, in Section 12, *Power Delivery*, has two changes in the ICH2 section.

1. An ICH2 power plane is added to it. This added ICH2 power plane is "ICH2 CMOS". This power plane has always existed in the ICH2. It is not new. This addition to the Power Delivery Map simply shows this ICH2 plane.
2. An ICH2 power plane is added to it. This added ICH2 power plane is "ICH2 Resume 1.8 VSB". This power plane has always existed in the ICH2. It is not new. This addition to the Power Delivery Map simply shows this ICH2 plane.

Figure 100, *Power Delivery Map*, is replaced with the following:



Notes:
1. Shaded regulators / components are ON in S3 and S5.
2. KB / mouse will not support STR.
3. Total max. power dissipation for GMCH = 4 W.
4. Total max. power dissipation for AC'97 = 15 W.
5. 1.8/1.85V Regulator: In lieu of separate voltage planes for the ICH2 and 815E to provide the separate voltages, a single regulator may be set to 1.795V - 1.910V.
6. ICH2 CMOS: The ICH2 pin is V_CPU_IO. Voltage depends on the CPU in use.

10. Added Section 2.4, Electrostatic Discharge Platform Recommendations

The following new material is added as Section 2.4, Electrostatic Discharge Platform Recommendations:

Electrostatic discharge (ESD) into a system can lead to system instability, and possibly cause functional failures when a system is in use. There are system level design methodologies that when followed can lead to higher ESD immunity. Electromagnetic fields due to ESD are introduced into a system through chassis openings such as the I/O back panel and PCI slots. These fields can introduce noise into signals and cause the system to malfunction. One can reduce the potential for issues at the I/O area by adding more ground plane on the motherboard around the I/O area. This can lead to a higher ESD immunity.

Intel recommends that the I/O area on the top and bottom signal layers of a 4-layer motherboard near the I/O back panel be filled with a ground fill as shown in Figures 1-4. In addition, a ground fill cutout should be placed on the Vcc layer in the area where the ground fill is done on the top and bottom layers. Intel recommends filling the I/O area as much as possible without effecting the signal routing. The board designer should fill the entire I/O area along the board edge.

The spacing from the ground fill to other shapes/traces should be at least 20 mils. It is recommended that these ground fill areas be connected to two chassis mounting holes (as seen in Figure 2). This will allow ESD current to travel to the chassis instead of the board. Ground stitching vias should be placed throughout the entire ground fill if possible. It is important that the vias are placed along the board edge. Ground stitching vias for the ground fill should be 100-150 mils apart or less.

In conclusion, Intel recommends the following:

1. Fill the I/O area with the ground fill in all layers including signal layers whenever possible
2. Extend the ground fill along the entire back I/O area
3. Connect the ground fill to mounting holes
4. Place stitching vias 100-150 mils apart in the entire ground fill

Figure 1 Top Signal Layer before the Ground Fill Near the I/O Layer

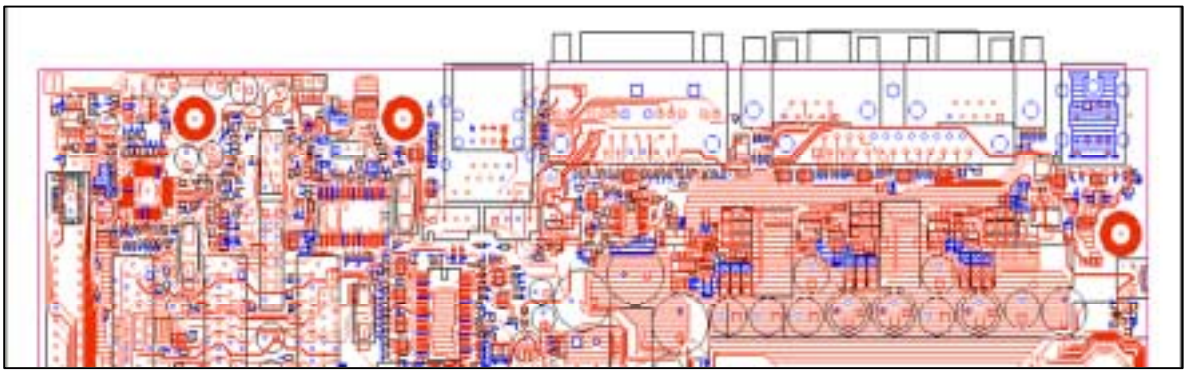


Figure 2 Top Signal Layer after the Ground Fill Near the I/O Layer

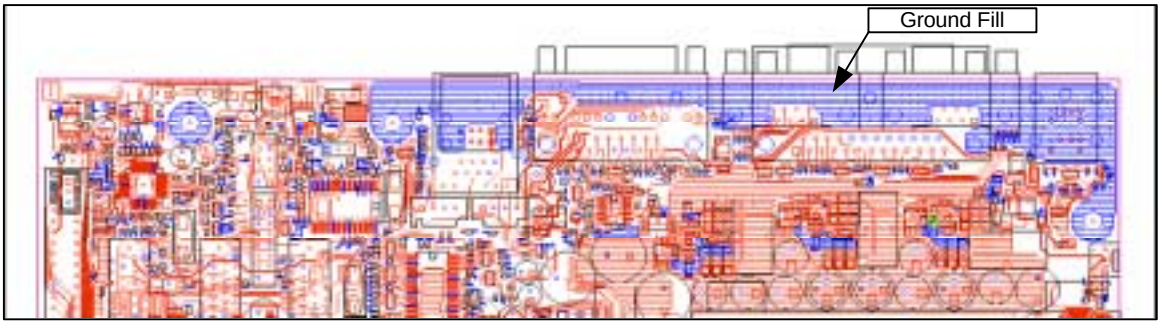


Figure 3 Bottom Signal Layer before the Ground Fill Near the I/O Area

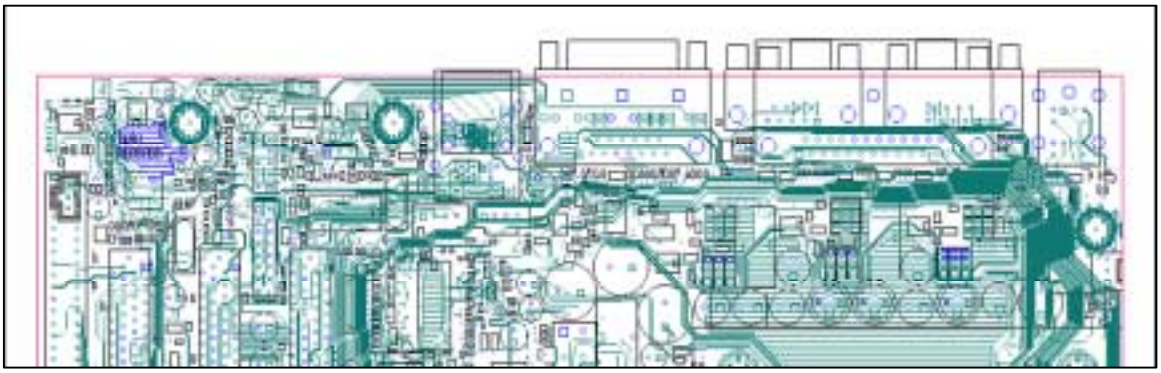


Figure 4 Bottom Signal Layer after the Ground Fill Near the I/O Area