Intel® 810E2 Chipset Platform for Use with Universal Socket 370

Design Guide Update

April 2002

Notice: The Intel® 810E Chipset family may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in the Specification Update.

Order Number: 298650-002

Contents

Revision History

Rev.	Draft/Changes	Date
-001	Initial Release	March 2002
-002	Added Documentation Change #10	April 15, 2002

1. Preface

This update is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. This design guide is primarily targeted at the PC market segment and was first published in 2001. Those using this design guide should check for device availability before designing in any of the components included in this document.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 810E2 Chipset Platform for Use with Universal Socket 370 Design Guide	298303-001
Intel® 810E Chipset: 82810E Graphics and Memory Controller Hub (GMCH) Datasheet	290676-002
Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet	290687-002

Nomenclature

General Design Considerations includes system level considerations that the system designer should account for when developing hardware or software products using the Intel® 810E Chipset Platform for Use with Universal Socket 370.

Schematic, Layout and Routing Updates include suggested changes to the current published schematics or layout, including typos, errors, or omissions from the current published documents.

Documentation Changes include suggested changes to the current published design guide not including the above.

Codes Used in Summary Table

Doc: Document change or update that will be implemented.

Shaded: This item is either new or modified from the previous version of the document.

Number	Plans	GENERAL DESIGN CONSIDERATIONS
		There are no Schematic, Layout, and Routing Updates in this Design Guide Update.

Number	Plans	SCHEMATIC, LAYOUT AND ROUTING UPDATES
		There are no Schematic, Layout, and Routing Updates in this Design Guide Update.

Number	Plans	DOCUMENTATION CHANGES
1	Doc	Added Section 8.5 Power Supply PS_ON Considerations
2	Doc	Changed Section 9.2.13, RTC, Add SUSCLK To The Checklist
3	Doc	Changed Section 9.2.16, Power, Modify Checklist Recommendations for 5V_REF_SUS
4	Doc	Changed Section 8.3.3, 3.3V/V5REF Sequencing
5	Doc	Changed Figure 67, Trace Routing, in Section 6.20.2.1, General Trace Routing Considerations
6	Doc	Changed Figure 61.1-a, RTC Power Well Isolation Control, in Section 6.19.8, Power Well Isolation Control Strap Requirements
7	Doc	Changed Section 8.3.3, 3.3V/5VREF Sequencing
8	Doc	Changed Section 9.2.16, Power, Modify Checklist Recommendations for 5V_REF_SUS
9	Doc	Changed Section 9.2.6, Interrupt interface, Modify Checklist items for APIC
10	Doc	Changed Figure 91, Power Delivery Map

2. General Design Considerations

There are no general design considerations in this Design Guide Update.

3. Schematic, Layout and Routing Updates

There are no schematic, layout, and routing updates in this Design Guide Update.

4. Documentation Changes

1) Added: Section 8.5 Power_Supply PS_ON Considerations

The following new section is added:

8.5 Power_Supply PS_ON Considerations

- If a pulse on SLP_S3# or SLP_S5# is short enough (~ 10-100mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supplies may not be designed to handle this short pulse condition. In this case, the power supply will not respond to this event and never power back up. These power supplies would need to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

- The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Due to variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

- The platform designer must ensure that the power supply used with the platform is not affected by this issue.

2) Changed: Section 9.2.13, RTC, Add SUSCLK To The Checklist

Add the following as a new checklist item to Section 9.2.13, RTC:

SUSCLK	To assist in RTC circuit debug, route SUSCLK to a test point if it is unused.

3) Changed: Section 9.2.16, Power, Modify Checklist Recommendations for 5V_REF_SUS

Change the second bullet in the Recommendations column of the 5V_REF_SUS to the following:

V5REF_SUS affects 5V-tolerance for all USB pins and can be connected to VccSUS3_3 if ICH2 USB is not supported in the platform. If USB is supported, 5VREF_SUS must be connected to 5V_AUX, which remains powered during S5

4) Changed: Section 8.3.3, 3.3V/V5REF Sequencing

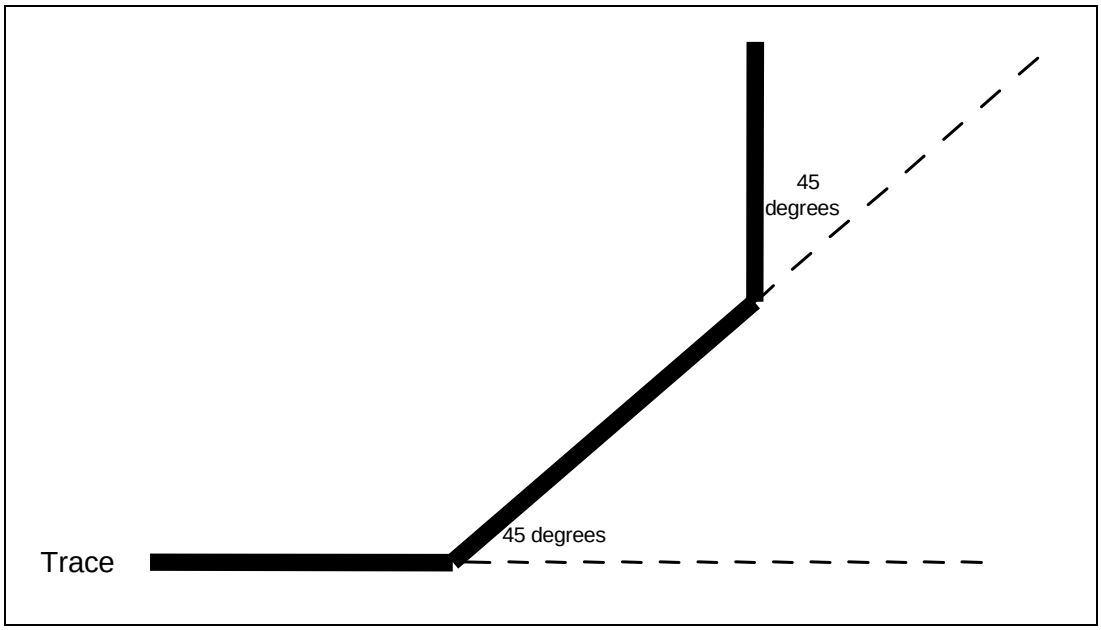
Change the second and third paragraphs of Section 8.3.3, 3.3V/V5REF Sequencing to the following:

This rule also applies to the stand-by rails. However, in most platforms the VccSus3_3 rail is derived from the VccSus5 and therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_Sus will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be comprehended in the platform design.

As an additional consideration, during suspend the only signals that are 5V tolerant are USB pins (both over-current and data lines). If USB is not implemented in the system then V5REF_SUS can be connected to the VccSus3_3 rail. Otherwise when USB is supported, V5REF_SUS must be connected to 5V_AUX, which remains powered during S5.

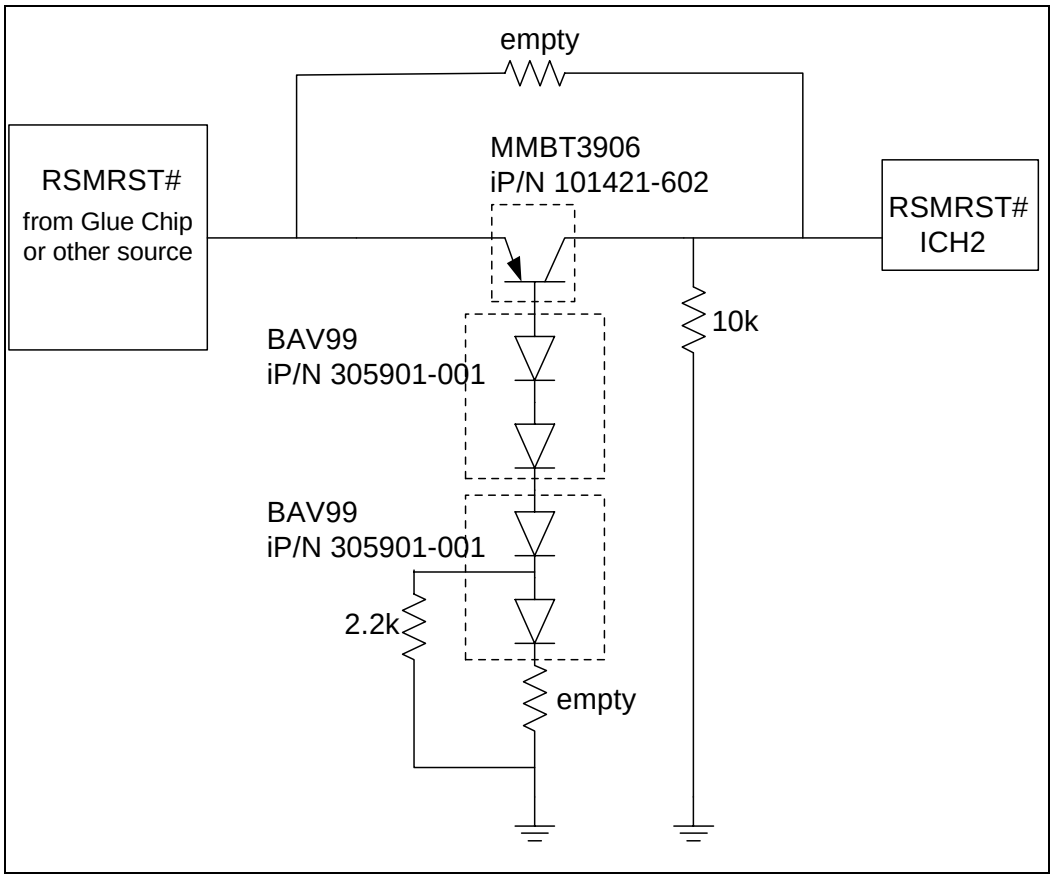
5) Changed: Figure 67, Trace Routing, in Section 6.20.2.1, General Trace Routing Considerations.

Figure 67, Trace Routing, in Section 6.20..2.1, General Trace Routing Considerations, is replaced with the following figure:



6) Changed: Figure 61.1-a, RTC Power Well Isolation Control, in Section 6.19.8, Power Well Isolation Control Strap Requirements

Figure 61.1-a, RTC Power Well Isolation Control, was added by Intel® 810E Chipset Platform for Use With Universal Socket 370 Design Guide Update, dated July 18, 2001, Document Number 298353-001, as document change #1. Figure 61.1-a is now changed to the following:



7) Changed: Section 8.3.3, 3.3V/5VREF Sequencing

Change the first and third paragraphs of Section 8.3.3, 3.3V/5VREF Sequencing to the following:

V5REF is the reference voltage for 5V tolerance on inputs to the ICH2. V5REF must be powered up before Vcc3_3, or after Vcc3_3 within .7V. Also, V5REF must power down after Vcc3_3, or before Vcc3_3 within .7V. The rule must be followed in order to ensure the safety of the ICH2. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the Vcc3_3 rail. Figure 94 shows a sample implementation of how to satisfy the V5REF/3.3V sequencing rule.

As an additional consideration, during suspend, the only signals that are 5V tolerant capable are USB OC:[3:0]#. If these signals are not needed during suspend, V5REF_SUS can be connected to either VccSus3_3

or 5V_Always/5V_AUX. If OC:[3:0]# is needed during suspend and 5V tolerance is required then V5REF_SUS should be connected to 5V_Always/5V_AUX, but if 5V tolerance is not needed in suspend, then V5REF_SUS can be connected to either VccSus3_3 or 5V_Always/5V_AUX rails.

8) Changed: Section 9.2.16, Power, Modify Checklist Recommendations for 5V_REF_SUS

V5REF_SUS only affects 5V-tolerance for USB OC:[3:0]# pins and can be connected to either VccSUS3_3 or 5V_Always/5V_AUX if 5V tolerance on these OC:[3:0]# is not needed. If 5V tolerance on OC:[3:0]# is needed then V5REF_SUS USB must be connected to 5V_Always/5V_AUX which remains powered during S5.

9) Changed: Section 9.2.6, Interrupt interface, Modify Checklist items for APIC

Pentium ® 4 processor based systems:

These processors do not have APIC pins so all platforms using this processor should both tie APICCLK to ground and tie APICD:[1:0] to ground via a 1K-10K pull-down resistor.

Non-Pentium® 4 processor based systems:

If the APIC is used:

150Ω pull-up resistors on APICD[1:0]

Connect APICCLK to CK133 with a 20-33Ω series termination resistor.

If the APIC is not used on UP systems:

The APICCLK can either be tied to GND or connected to CK133, but not left floating.

Pull APICD[1:0] to GND through 10kΩ pull-down resistors.

10. Changed: Figure 91, Power Delivery Map

Two existing ICH2 power planes are added to figure 91, Power Delivery Map.

Figure 91. Power Delivery Map