

Intel® High Definition Audio Specification Document Change Notification

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Change Identification: **DCN No: HDA041-A**
Change Revision: 1.0
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This document discloses changes to the Intel® High Definition Audio Specification and all information contained herein is provided under the terms of the "AZALIA" SPECIFICATION DEVELOPMENT AGREEMENT" also known as Intel® High Definition Audio Specification Developer Agreement, and all the terms of such agreement, including the confidentiality provisions, shall apply to this disclosure.

Title: Copy Bit Polarity Clarification

Brief description of the functional changes:

This DCN clarifies the reversal of the COPY (copyright) bit defined in section 7.3.3.9 of the Intel® High Definition Audio 1.0 Specification.

Definition Text Formatting:

xxx Original text in existing specification or DCN released earlier.
yyy New text inserted by this new DCN.
zzz Deleted text introduced by this new DCN.

New Definitions:

7.3.3.9 Digital Converter Control

The **Digital Converter Controls 1 and 2** operate together to provide a set of bits to control the various aspects of the digital portion of the Converter Widget. The S/PDIF IEC Control (SIC) bits are supported in one of two ways.

In the first case referred to as "Codec Formatted SPDIF," if a PCM bit stream of less than 32 bits is specified in the Converter Format control, then the S/PDIF Control bits, including the "V," "PRE," "/AUDIO," and other such bits are embedded in the stream by the codec using the values (SIC bits) from the Digital Converter Control 1 and 2. On an input PCM stream of less than 32 bits, the codec strips off these SIC bits before transferring the samples to the system and places them in the Digital Converter Control 1 and 2 for later software access.

In the second case referred to as “Software Formatted (or Raw) SPDIF,” if a 32-bit stream is specified in the Converter Format control, the S/PDIF IEC Control (SIC) bits are assumed to be embedded in the stream by software, and the raw 32-bit stream is transferred on the link with no modification by the codec. Similarly, on a 32-bit input stream, the entire stream is transferred into the system without the codec stripping any bits. However, the codec must properly interpret the Sync Preamble bits of the stream and then send the appropriately coded preamble. The IEC60958 specification, Section 4.3, “Preambles,” defines the preambles and the coding to be used. Software will specify the “B,” “M,” or “W” (also known as “X,” “Y,” or “Z”) preambles by encoding the last four bits of the preamble into the Sync Preamble section (bits 0-3) of the frame. The codec must examine the bits specified and encode the proper preamble based on the previous state. The previous state is to be maintained by the codec hardware. For more information on Preamble Coding, consult Section 4.3 of the IEC 60958 specification.

Table 76. SPDIF Sync Preamble Bits

Preamble Bits Set by Software (Bits 3:0 of Frame)	Preamble Coding	
	Previous State = 0	Previous State = 1
1000b (“B” or “Z”)	11101000	00010111
0010b (“M” or “X”)	11100010	00011101
0100b (“W” or “Y”)	11100100	00011011

Command Options:

Table 77. S/PDIF Converter Control 1 and 2

	Verb ID	Payload (8 Bits)	Response (32 Bits)
Get	F0Dh	0	Bits 31:0 are SIC bits
Set 1	70Dh	SIC bits [7:0]	0
Set 2	70Eh	SIC bits [15:8]	0
Set 3	73Eh	SIC bits [23:16]	0
Set 4	73Fh	SIC bits [31:24]	0

31:24	23	22:20	19:16	15	14:8	7	6	5	4	3	2	1	0
Rsvd	KAE	Rsvd	ICT	Rsvd	CC[6:0]	L	PRO	/AUDIO	COPY /CP	PRE	VCFG	V	DigEn

Figure 62. S/PDIF IEC Control (SIC) Bits

KAE (Keep Alive Enable): This bit is applicable only to digital converter widget that is associated (selected by) an Output Digital Pin Widget. This bit allows for software programmed control of S/P-DIF, HDMI and Display Port interfaces to continue to provide clocking information to an attached device. Many such digitally connected audio devices can take more than one second to start playing audio after the clock has stopped, which occurs for example when the Converter and/or Digital Pin Widget is placed into a low power state or even just when a stream is stopped for S/P-DIF. Although this capability is more closely associated with the output port and thus the converter widget, the generation of a valid digital stream and clock is normally provided by the Converter Widget and thus this functionality is included here. Support for the KAE is mandatory after July 1st 2011, if EPSS is reported set to 1. When

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KAE is set to 1 the output will supply a continuous clock and a valid but ‘silent’ data stream (even when no stream is selected by this Converter Widget) and while the Digital Converter and/or Digital Pin Widget connected to this Converter Widget is in D0-D3 . If D3cold state is supported, then the “Keep Alive” shall not be operational while in the D3cold state.

When the output from the Pin Widget connected to this Converter Widget is connected to a combination electrical and optical (TOSLINK) jack, the jack-detection capability of the electrical 3.5 mm jack must also be used to report Presence Detection in the Digital Pin Widget associated with this Digital Converter’s S/PDIF output, and must also support an unsolicited response generation when the jack state changes. It is recommended that driver software disable the KAE bit when the output port is not connected and enable it when the output port is connected to reduce the power consumed during idle. It is also recommended that driver software disable the KAE bit when the associated output port is connected but when the Optical S/PDIF output is not the default output device.

As mentioned above, the KAE bit is not applicable to input converters of digital ports. In the case of an input port, the driver software should periodically (e.g. every few seconds) wake up the Function Group out of D3 state and poll the port to see if it has locked to an input stream. If the input port is connected to a combo jack, jack-detection capability must be supported and an unsolicited response must be generated when the jack state changes. In that case, software will have to periodically poll for lock status only when it knows that the port is connected to an external transmitter.

ICT[3:0] (IEC Coding Type): Programmed according to IEC standards to enable stream types for High Bit Rate Encoding. This is valid only for HDMI and Display port digital Pin Widgets.

CC[6:0] (Category Code): Programmed according to IEC standards, or as appropriate.

L (Generation Level): Programmed according to IEC standards, or as appropriate.

PRO (Professional): 1 indicates Professional use of channel status; 0 indicates Consumer.

/AUDIO (Non-Audio): 1 indicates data is non-PCM format; 0 indicates data is PCM.

~~COPY/CP~~ (No Copyright Protection): 1 indicates **no** copyright is asserted; 0 indicates copyright is **not** asserted.

PRE (Preemphasis): 1 indicates filter preemphasis is 50/15 μ s; 0 preemphasis is none.