Intel® High Definition Audio Specification
Document Change Notification

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Change Identification:	**DCN No: HDA043-A**
Change Revision:	1.0
Document Revision:	Intel® High Definition Audio 1.0a

Title: Energy efficient audio buffering and dynamic FIFO limit change

Brief description of the functional changes:

This DCN proposes a new mechanism for software to communicate the valid portion of the ring buffer to hardware. This information allows hardware to know how far into the future it may fetch, which may reduce memory accesses and reduce platform power.

This DCN also proposes a means for software to dynamically communicate changes in to this 'valid' ring buffer size while stream is active. This is intended to support dynamic transforming from latency-insensitive to real-time streams without halting the hardware.

Definition Text Formatting:

xxx	Original text in existing specification or DCN released earlier.
yyy	New text inserted by this new DCN.
~~zzz~~	Deleted text introduced by this new DCN.

New Definitions:

3.3.11 Offset 12h: GCAP2 – Global Capabilities 2

Length: 2 bytes

Table 12. Global Capabilities 2

Bit	Type	Description
15:2	**RsvdZ**	**Reserved**
1	**RO**	**Dynamic FIFO Limit Change Capability (DFFLCC):** This bit is used by

		HW to indicate it supports dynamic FIFO size change request when the stream is active. Value of 0 means feature is not supported by HW (static FIFO limit operation). A value of '1' indicates HW supports programming of FIFOL and FIFOSC after the RUN bit has been set.
0	**RO**	**Energy Efficient Audio Capability (EEAC):** This bit is used by HW to indicate it supports energy efficient audio buffering capability. Value of 0 means feature is not supported by HW. A value of '1' indicates HW supports FIFOL and FIFOSC operations.

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3.3.36 Offset 80: {IOB}SDnCTL – Stream Descriptor Control register

Length: 3 bytes

Table 35. Stream Descriptor *n* Control

Bit	Type	Reset Value	Description
5	**RW or RO**	**0**	**FIFO Size Change (FIFOSC):** This bit is RO if GCAP2.EEAC = 0. In static case (GCAP2.EEAC = 1 and GCAP2.DFFLCC = 0), this bit will only have effect before the first time RUN bit is set. Software must not attempt to write this bit, unless EECAP.EEAC bit is set. HW will treat this bit as read-only if the capability is not supported. In dynamic case (GCAP2.EEAC = 1 and GCAP2.DFFLCC = 1), on top of supporting the static behavior describe above, this bit can also be used to communicate the dynamic change request in FIFO size between SW and HW when the stream is active. Writing a '1' successfully will cause the corresponding stream effective FIFO size to be changed to new value based on the FIFOL value and eligible HW buffer space. After the stream hardware has completed sequencing into the new effective FIFO size, it will reset this bit to '0'. Software is recommended to wait for [FIFOL_prior + 1 granular time unit] after writing 1 to FIFOSC before starting to poll for HW to set to 0.

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3.3.41 Offset 90: {IOB}SDnFIFOS – Input/Output/Bidirectional Stream Descriptor *n* FIFO Size

Length: 2 bytes

Table 40. Stream Descriptor *n* FIFO Size

Bit	Type	Reset Value	Description
15:0	**RO**	**Imp.Dep**	**FIFO Size (FIFOS):** Indicates the maximum number of bytes that

			could be fetched by the controller at one time. This is the maximum number of bytes that may have been DMA'd into memory but not yet transmitted on the link, and is also the maximum possible value that the PICB count will increase by at one time. This number may be static to indicate a static buffer size, or may change after the data format has been programmed if the controller is able to vary its FIFO size based on the stream format. When GCAP2.EEAC = 1, this FIFOS value represent the minimum FIFO size HW required to operate efficiently. SW can program FIFOL register to extend the effective FIFO size in HW beyond this minimum value advertised.

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3.3.43 Offset 94h: {IOB}SDnFIFOL – Input/Output/Bidirectional Stream Descriptor *n* FIFO Limit

Length: 2 bytes

Table 42. Stream Descriptor n FIFO Limit

Bit	Type	Reset Value	Description
15	**RsvdP**	**0**	Reserved
14	**RW**	**0**	**Granularity (GNL):** Associated with FIFOL definition. The FIFO Limit unit needs to be multiplied with 125us or 1ms to get the actual value. Default: 1'b0 – indicates 125us increments. 1'b1 – indicates 1ms increments. A stream reset will also reset this register to default value.
13:0	**RW**	**0's**	**FIFO Limit (FIFOL):** SW uses this field to indicate to hardware how far the media player / application intends to process ahead, in units of time. HW can extend the effective FIFO size to fetch (for output stream) or evict (for input stream) more data beyond the minimum FIFO size advertised in FIFOS register, up to this access limit. Need to use the granularity bit (125us vs. 1ms) as defined in GNL, to get the actual processing ahead time. Where 0000h = Disabled and 0001 – 3FFF = 1 to 16383 units. Default value is '0x0', indicates the access limit is the same as the HW advertised FIFO size (as indicated in FIFOS). A stream reset will also reset this register to default value. FIFOL shall be changed before setting the FIFOSC bit, and remain static until FIFOSC bit is read back as 0. When HW supports EE Audio capability, the FIFOS this value will represent the minimum size of cyclic buffer for efficient HW operation. SW should look at the FMT register and update FIFOL register to allow the extension of effective FIFO size beyond this FIFOS advertised value, up till the FIFOL limit. If hardware indicates EEAC, software must presume that a larger

			time value written to FIFOL can be exploited by hardware. This register must not be written with a value representing a smaller time quantity than the time converted FIFOS. FIFOS continues to indicate the baseline hardware buffering software must support.

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4.6 Energy Efficient HD Audio (EEAudio) Mechanism

The Energy Efficient HD Audio (EEAudio) mechanism enables the SW to control the HD Audio Controller DMA engine effective buffer size extension for power saving versus latency consideration. When configured to use larger extended buffering, it allows the DMA engine to reduce associated system memory accesses, thus allows the CPU to go in to deeper power saving states and reduces the platform power associated with audio streams. When configured to use smaller extended buffering (or disabled), it suits the application where low latency audio processing is required.

The GCAP2 register EEAC bit indicates the HW capabilities of supporting EEAudio. When EEAC bit is set, the FIFOL register is available for SW to specify the limit (in unit of time) that HD Audio Controller DMA engine can access in the Cyclic Buffer, ahead of the Link Position in Buffer; in other words, that defines the maximum limit that DMA engine effective buffer size (in number of bytes) can be extended to. SW shall guarantee processing ahead of this boundary in the Cyclic Buffer. Note that the translation of FIFOL value to effective buffer size needs to take into consideration of number of channels, sample size, multiplier, divider, and base rate.

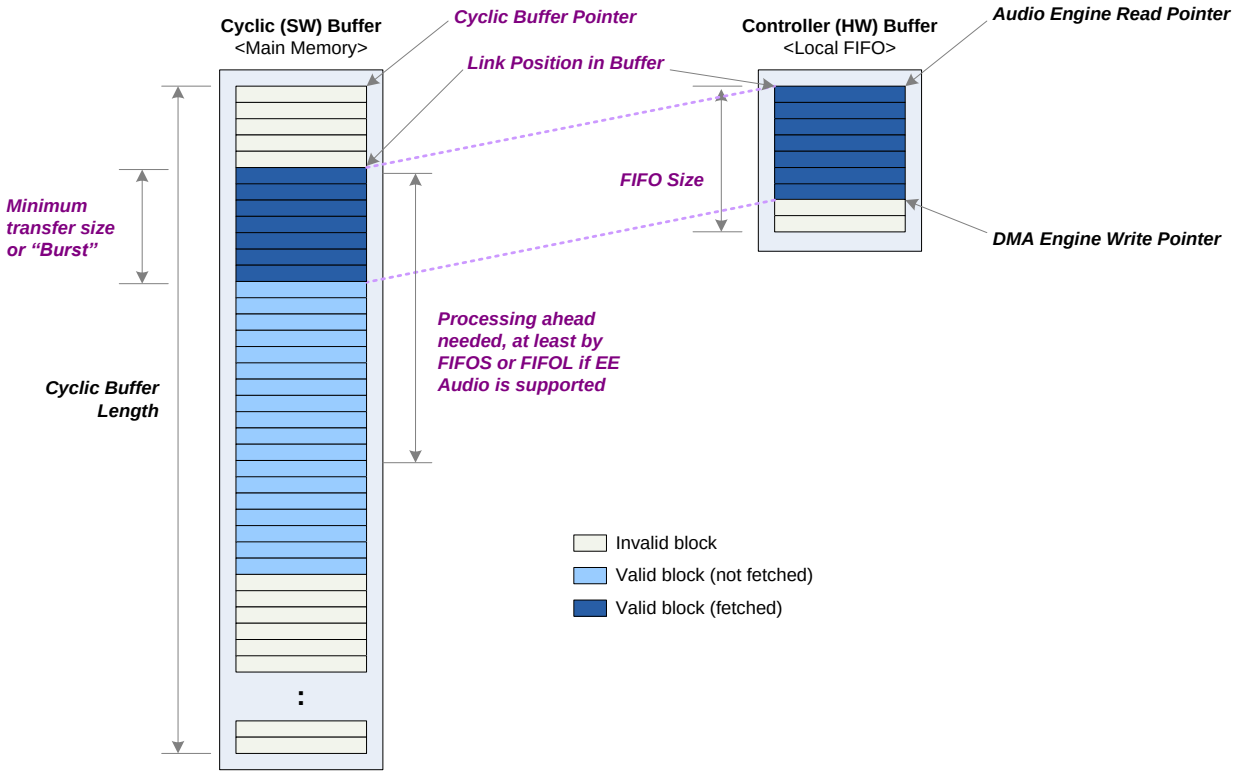

Figure 14: HD Audio DMA and buffering

When EEAudio is supported as indicated by EEAC bit being set, the FIFOS register will expose the minimum buffer size required by HW for efficient operation. SW can allow the extension of the DMA engine effective buffer size beyond the minimum buffer size advertised in FIFOS register for better power management, by writing to FIFOL register followed by setting FIFOSC bit. Depending on the eligible HW buffer size available, DMA engine can then extend its effective buffer size to a value not exceeding the FIFOL specified. Note that some HD Audio Controller DMA engine implementations are capable of changing FIFOS register value based on FMT register programmed, hence, SW shall always read the FIFOS register to find out the FIFO size advertised before writing to FIFOL register.

The FIFOL register and FIFOSC bit implementation of the EEAudio may support static mode or dynamic mode of programming, as indicated by the DFFLCC bit in GCAP2 register. When static mode is supported, FIFOL register is only allowed to be programmed before the RUN bit is set for the very first time of an audio stream being played. When dynamic mode is supported, the FIFOL register may be programmed even when the RUN bit remains set (in addition to the static mode of programming behavior).

Steps involved in FIFO re-sizing:

1) Software writes a new value in FIFOL register.
2) Software sets FIFOSC bit to 1 (from 0).
    a. Hardware will clear the FIFOSC bit (to 0) once it has completed the resizing.
    b. For static programming mode, this typically happens almost immediately.
    c. For dynamic programming mode, this may take up to the streaming time required for flushing the prior effective FIFO size content (i.e. up to the prior FIFOL value in unit of time).
3) SW can request next resize only after the FIFOSC bit is cleared by HW.

Note: There are cases where FIFOSC may not be able to clear itself due to the RUN bit is cleared, as the DMA engine data movement has been halted. E.g. FIFOSC bit is set after the RUN bit has been cleared for pausing audio stream; or FIFOSC bit has been set for FIFO re-sizing, but SW clear the RUN bit to pause the audio stream before the FIFOSC bit is cleared. In these cases, FIFOSC may only be cleared naturally when the RUN bit is set again for resuming the audio stream, or stream reset is triggered.