440LX CUSTOMER REFERENCE DESIGN

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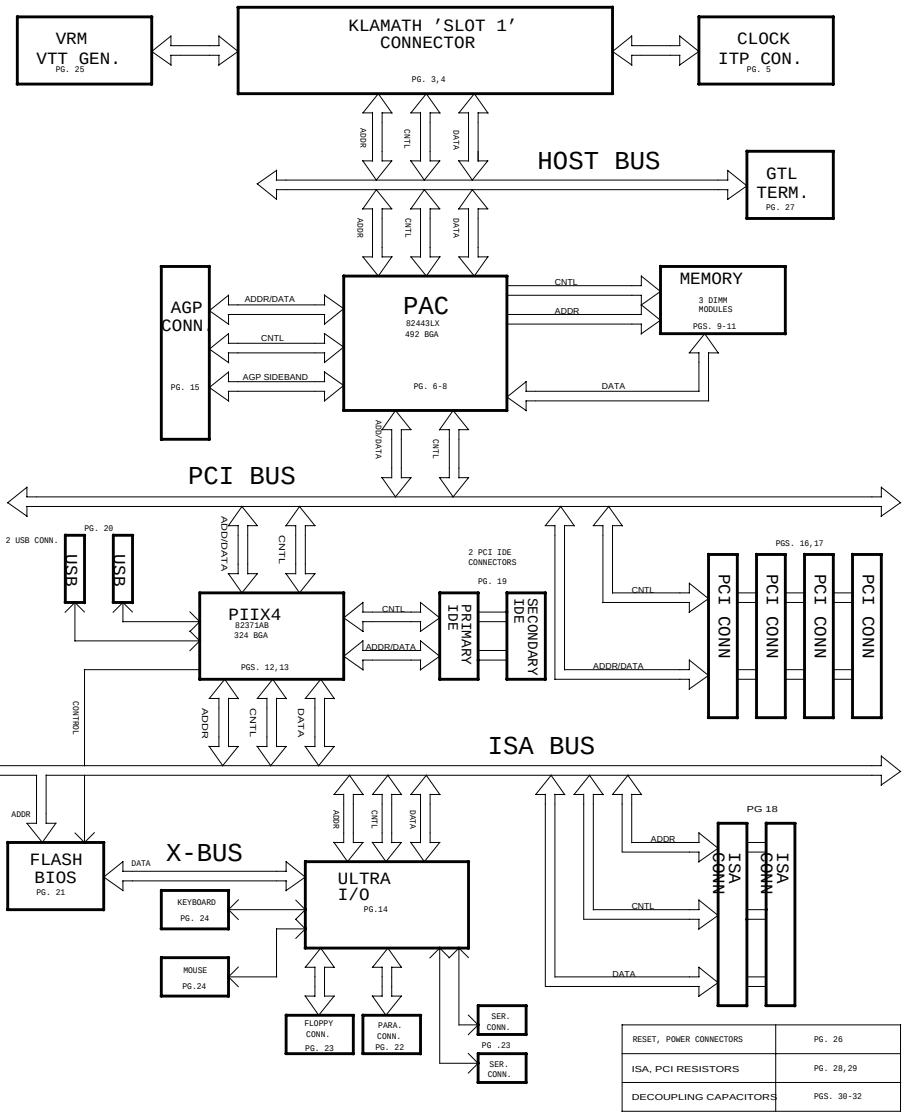
Title		
Size: A	Document Number: Intel 440LX PCIset	Rev: 1.4
Date:	Sheet 1 of 33	



RESET, POWER CONNECTORS	PG. 26
ISA, PCI RESISTORS	PG. 28,29
DECOUPLING CAPACITORS	PGS. 30-32

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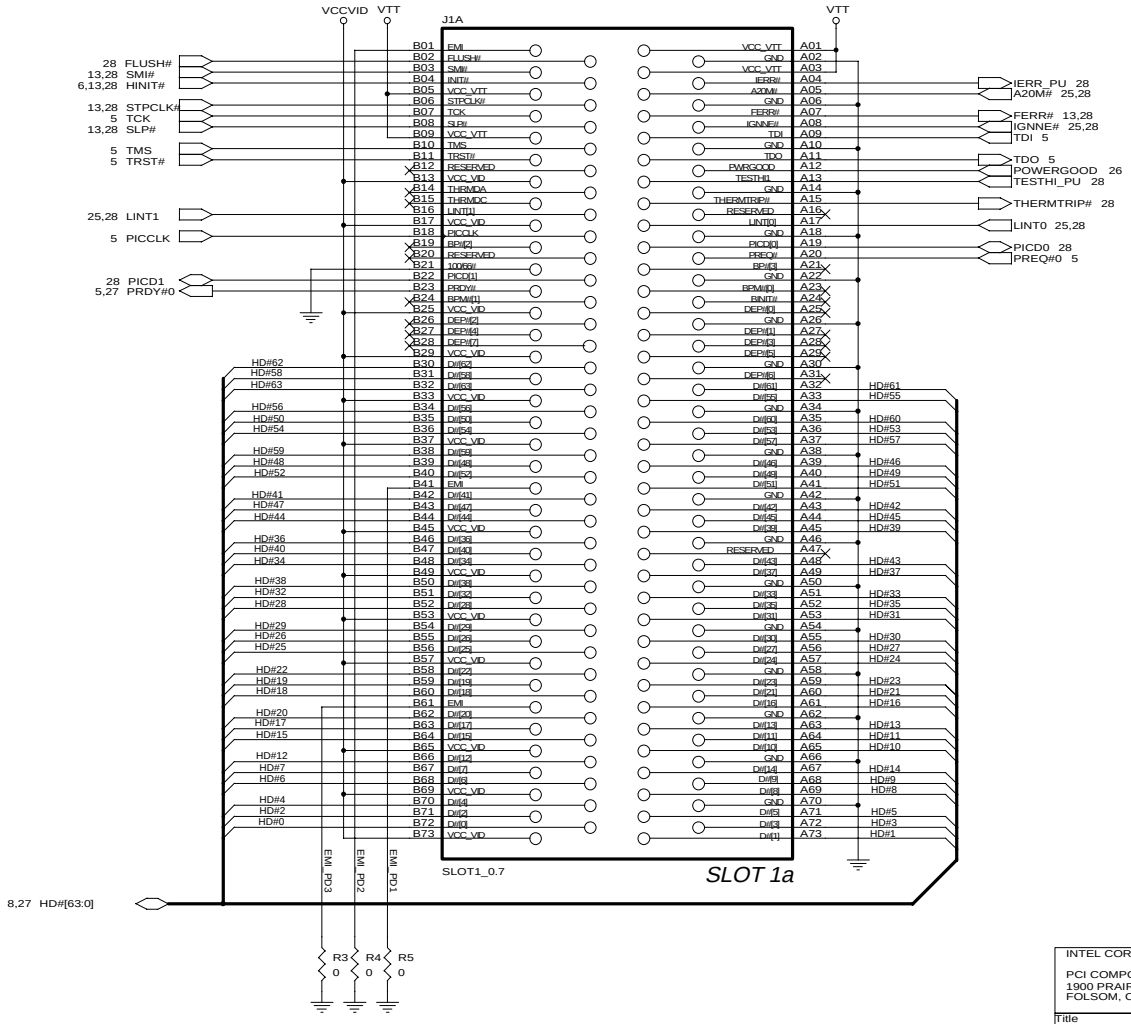
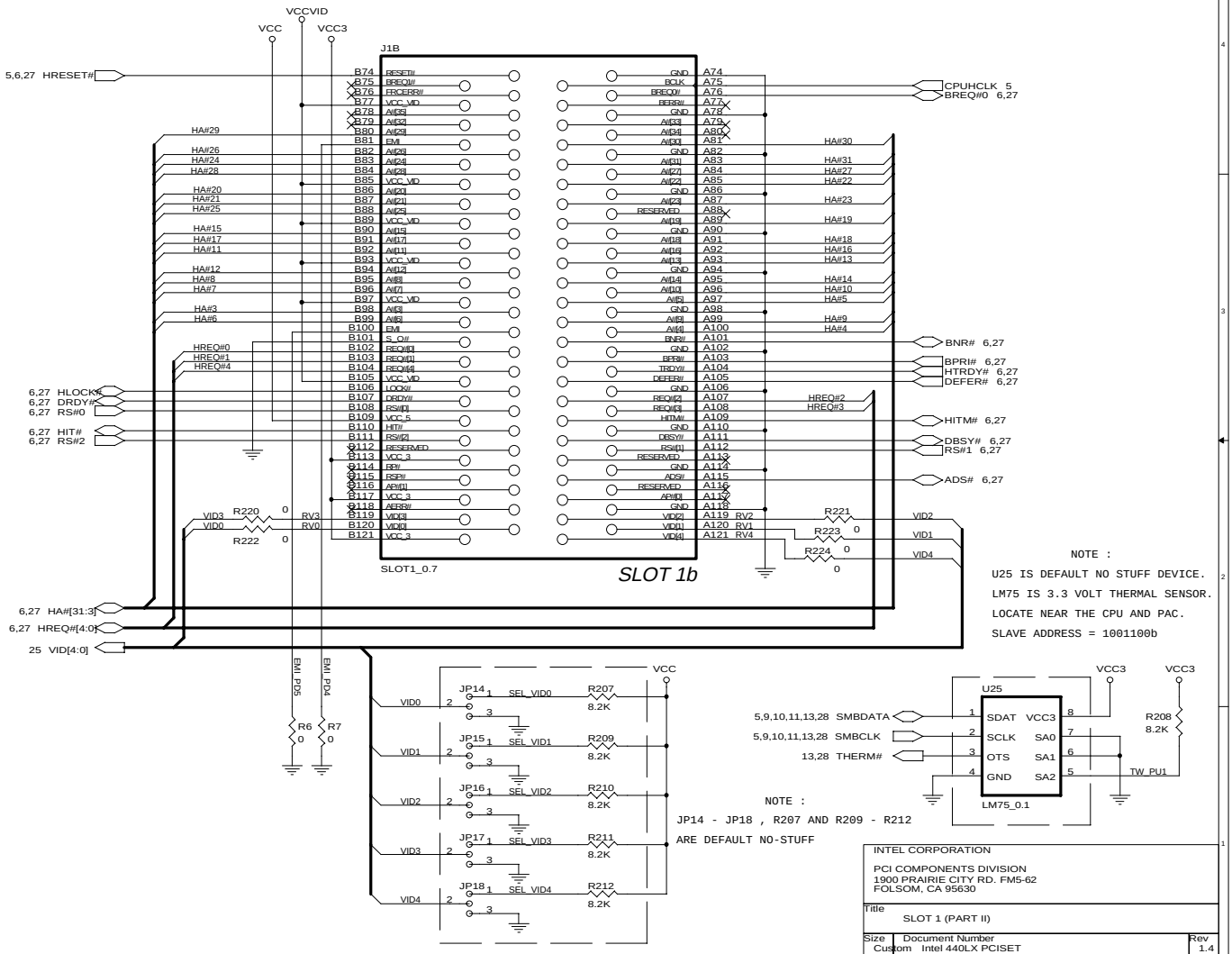
Title: Intel 440LX PCIset Block Diagram

Size: Custom | Document Number: Intel 440LX PCISET | Rev: 1.4

Date: Thursday, May 07, 1998 | Sheet 2 of 33



INTEL CORPORATION PCI COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: SLOT 1 (PART I)		
Size: Custom	Document Number: Intel 440LX PCISET	Rev: 1.4
Date: Thursday, May 07, 1998	Sheet 3 of 33	



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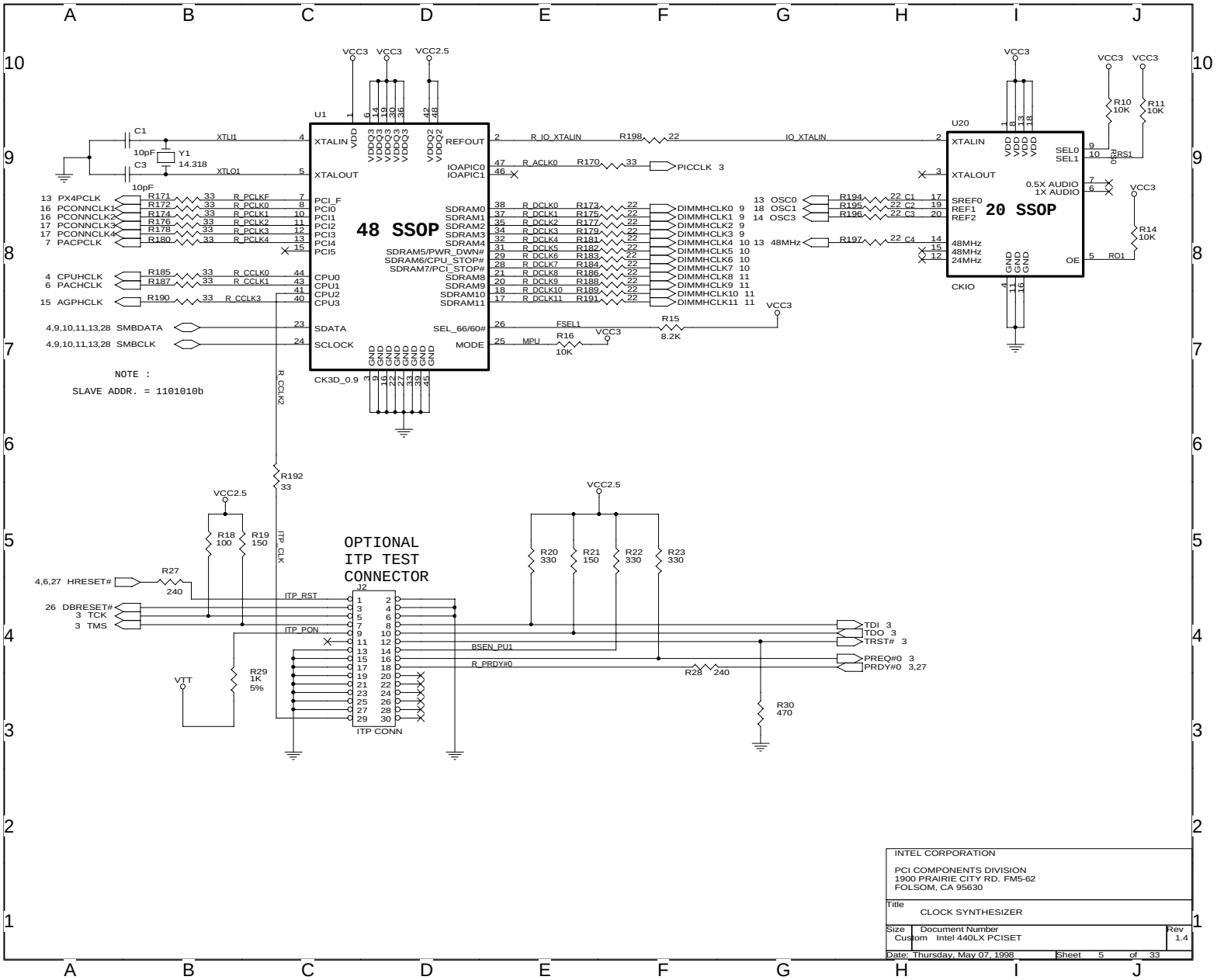
Title: SLOT 1 (PART II)	
Size: Custom	Document Number: Intel 440LX PCISET — Rev: 1.4
Date: Thursday, May 07, 1998	Sheet 4 of 33



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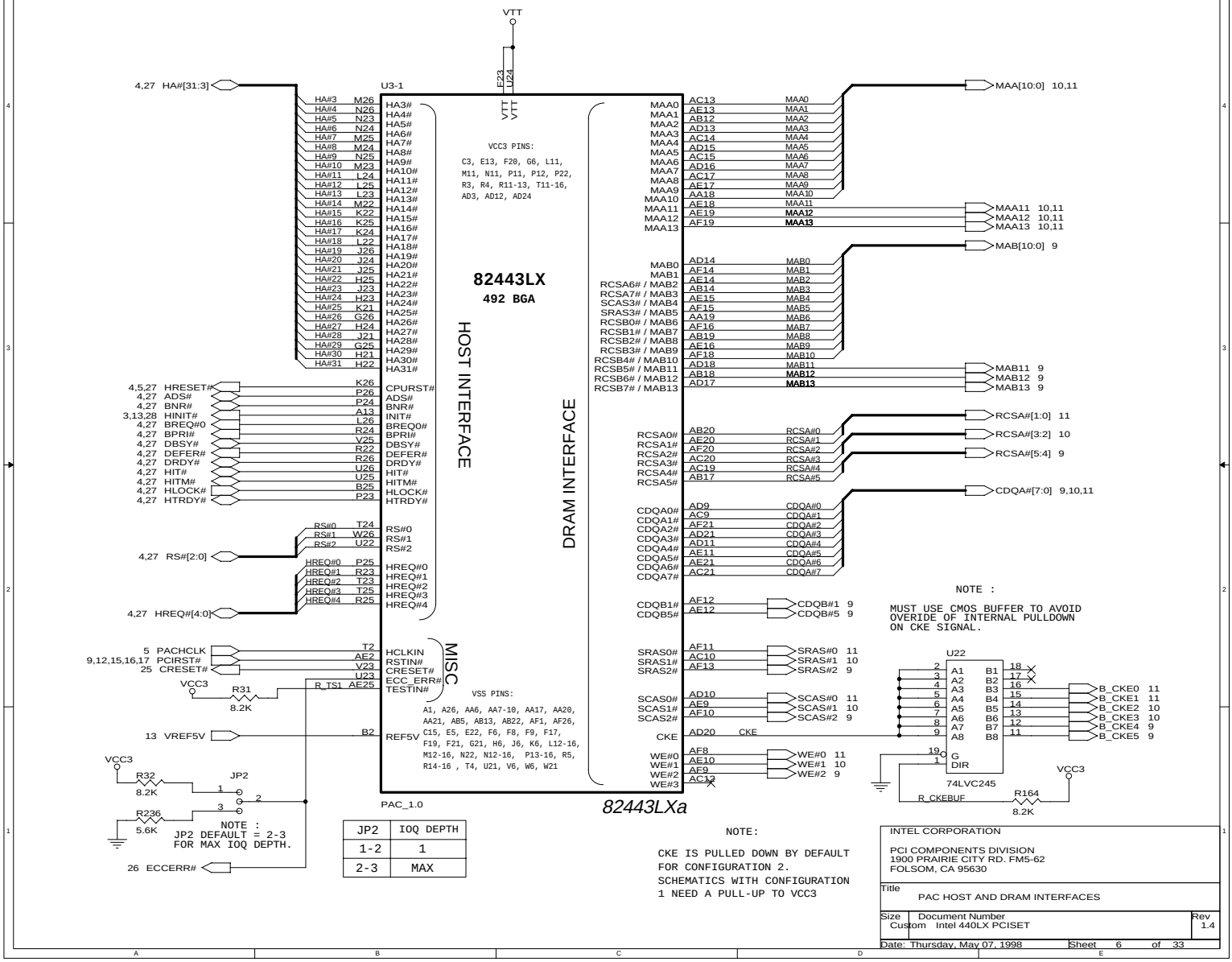
Title	CLOCK SYNTHESIZER
Size: Custom	Document Number: Intel 440LX PCISET — Rev: 1.4
Date: Thursday, May 07, 1998	Sheet 5 of 33



JP2	IOQ DEPTH
1-2	1
2-3	MAX

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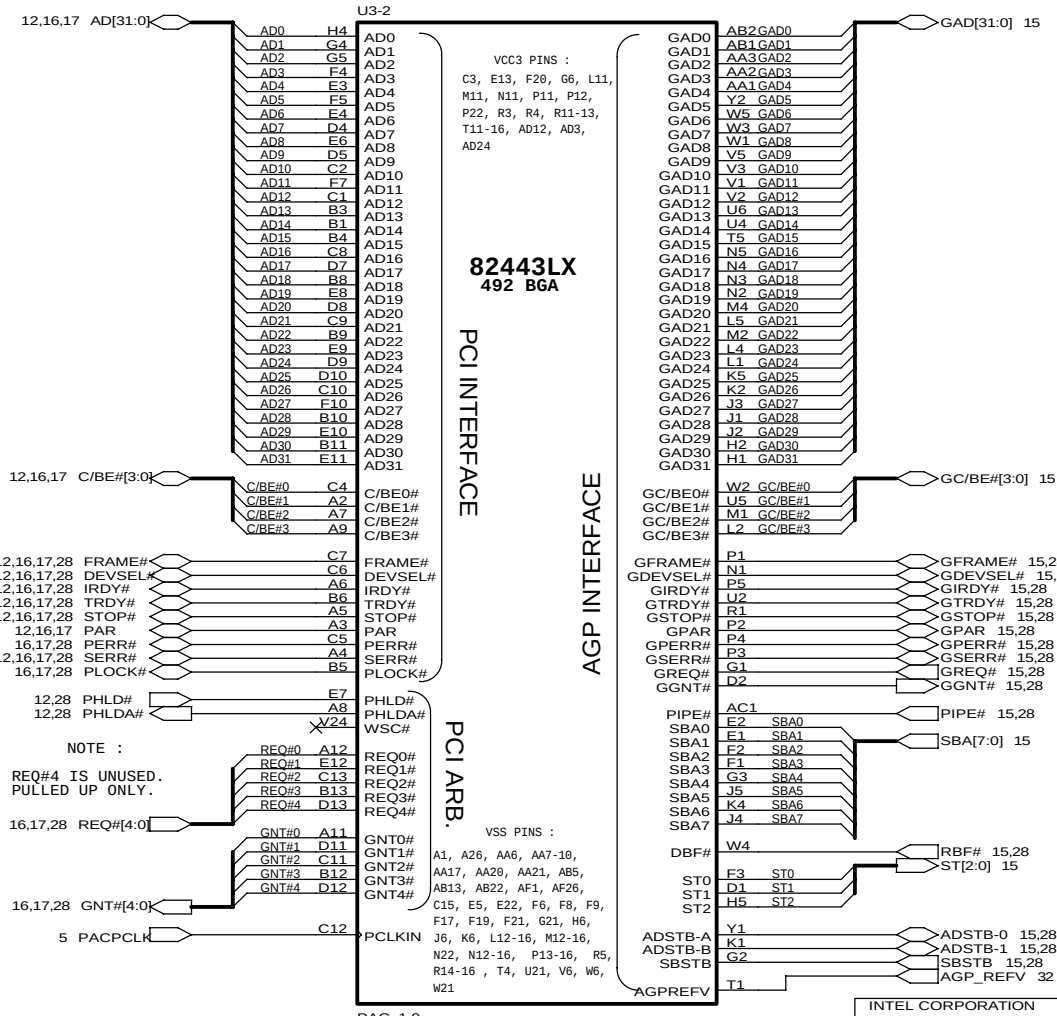
Title: PAC HOST AND DRAM INTERFACES

Size: Custom | Document Number: Intel 440LX PCISET | Rev: 1.4

Date: Thursday, May 07, 1998 | Sheet 6 of 33



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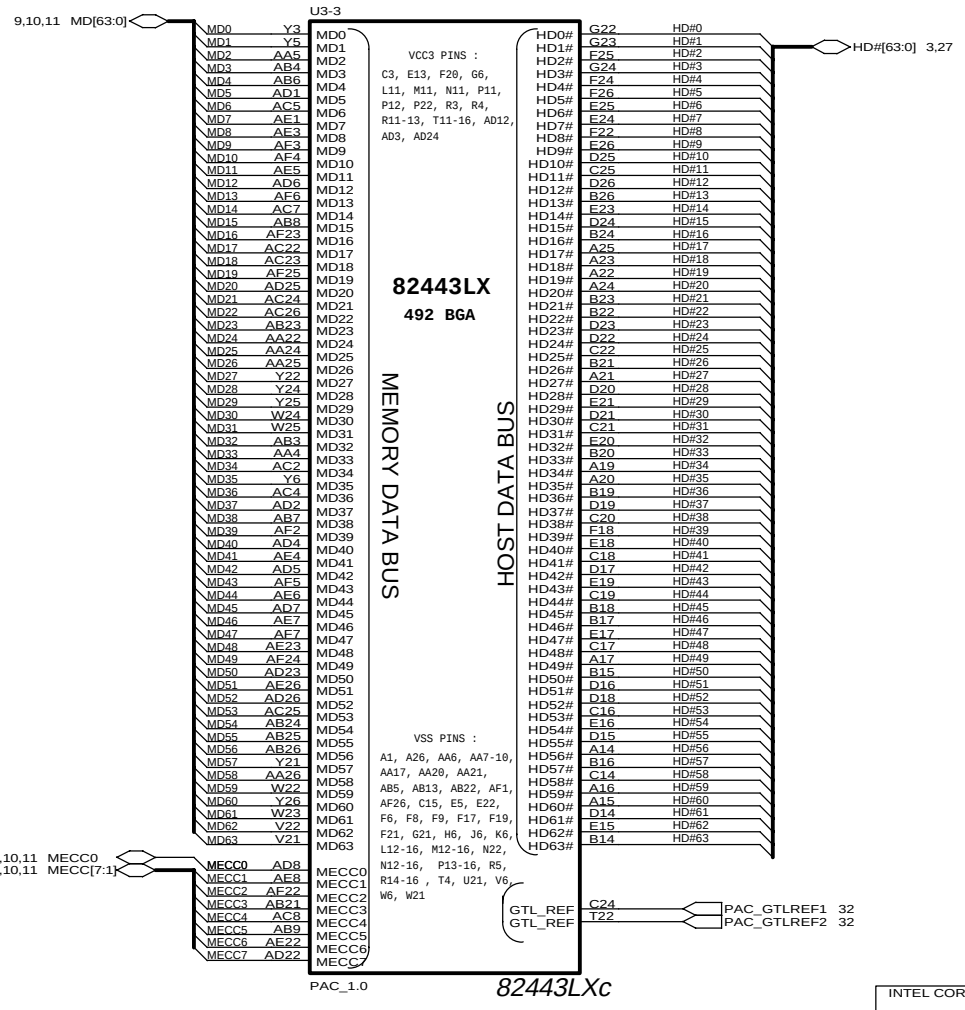
Title	PAC PCI AND AGP INTERFACES
Size: Custom	Document Number: Intel 440LX PCISET — Rev: 1.4
Date: Thursday, May 07, 1998	Sheet 7 of 33



INTEL CORPORATION PCI COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title: PAC DATA BUSES		
Size: Custom	Document Number: Intel 440LX PCISET	Rev: 1.4
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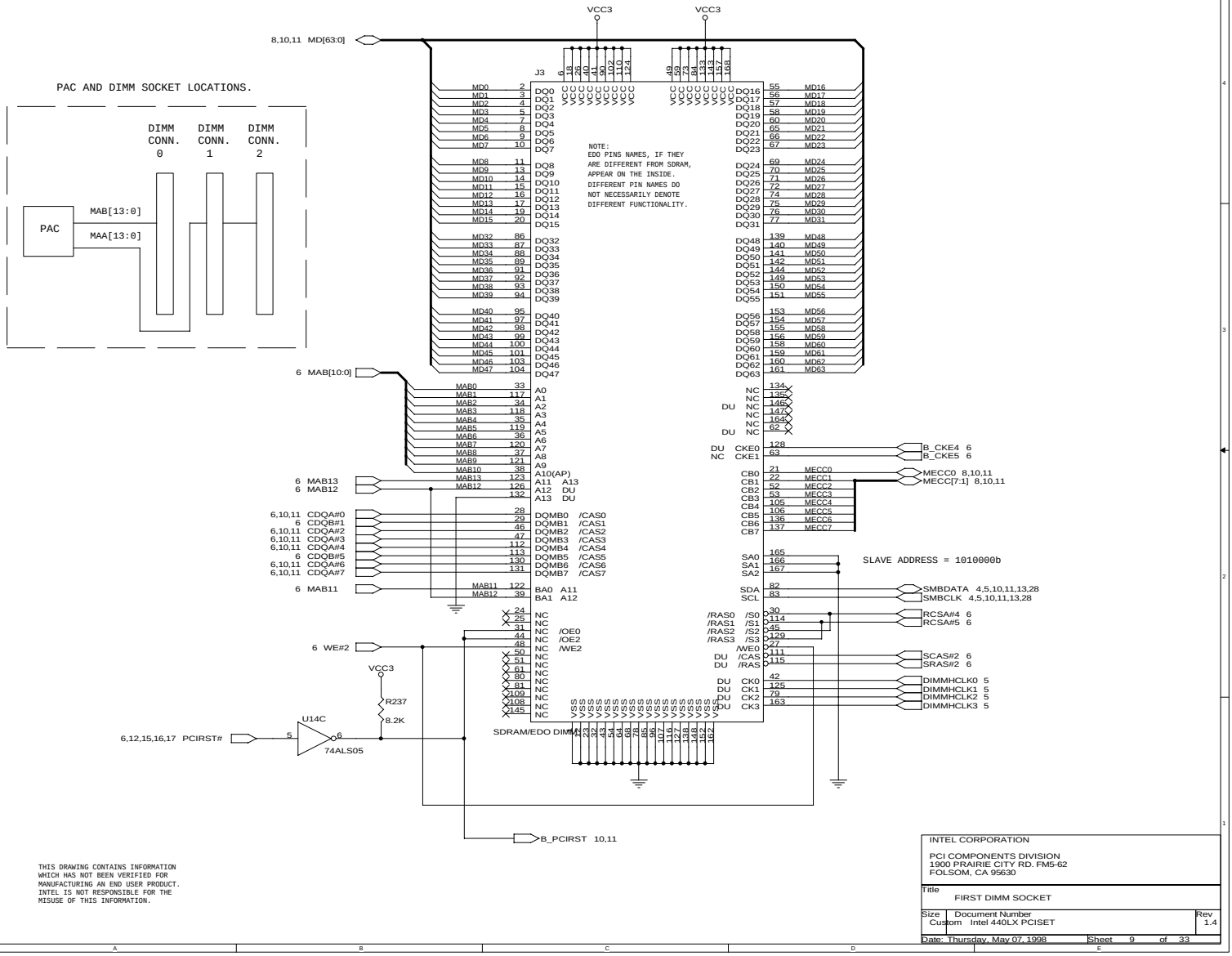
DIMM CONNECTOR 0



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Title: FIRST DIMM SOCKET

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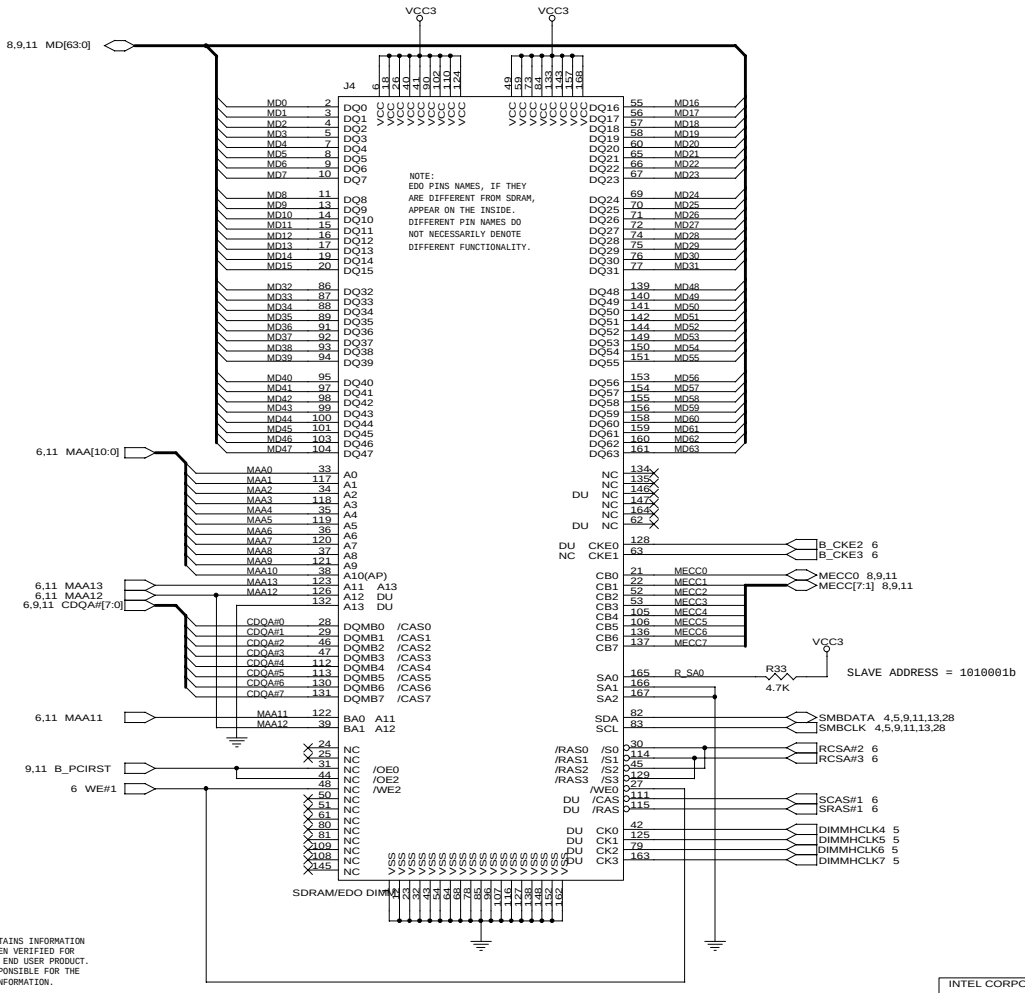
Date: Thursday, May 07, 1998 | Sheet 9 of 33

DIMM CONNECTOR 1



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Title: SECOND DIMM SOCKET

Size: Custom | Document Number: Intel 440LX PCISET | Rev: 1.4

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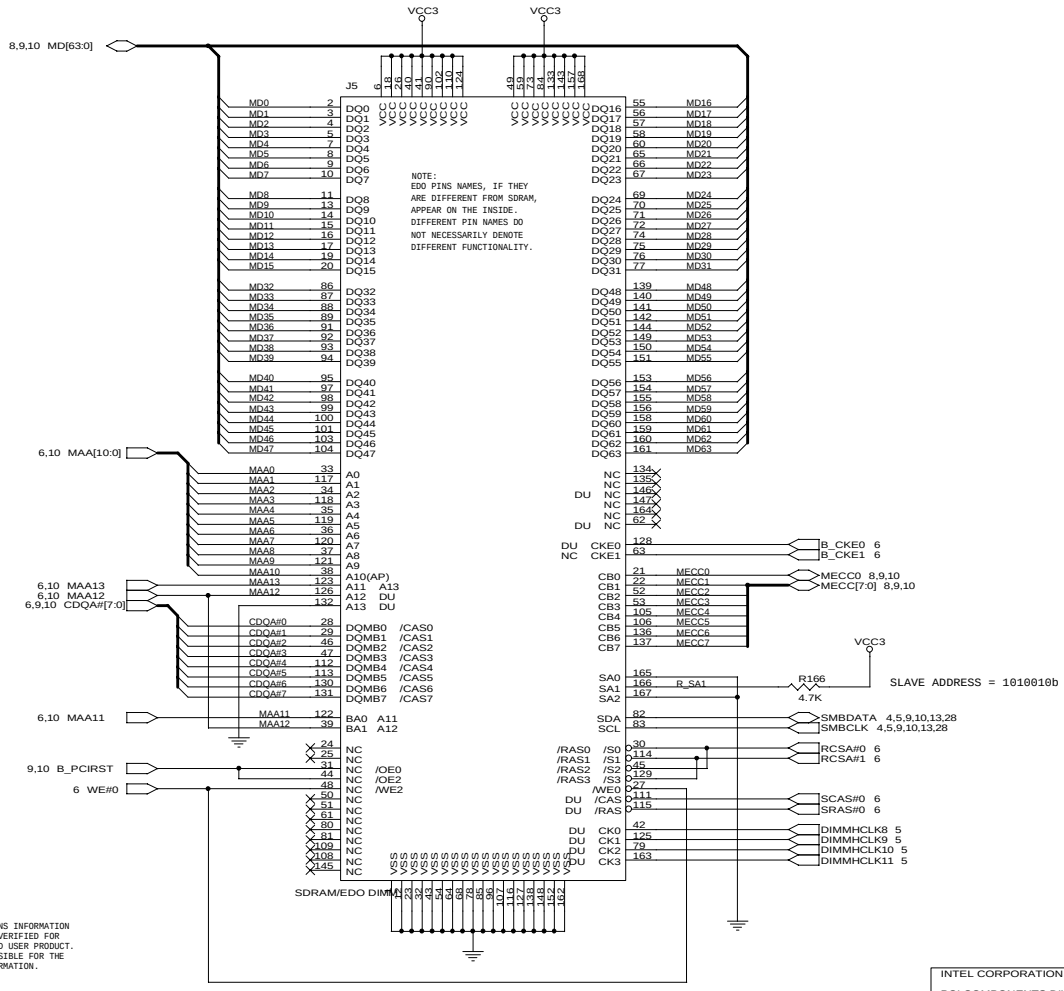
DIMM CONNECTOR 2



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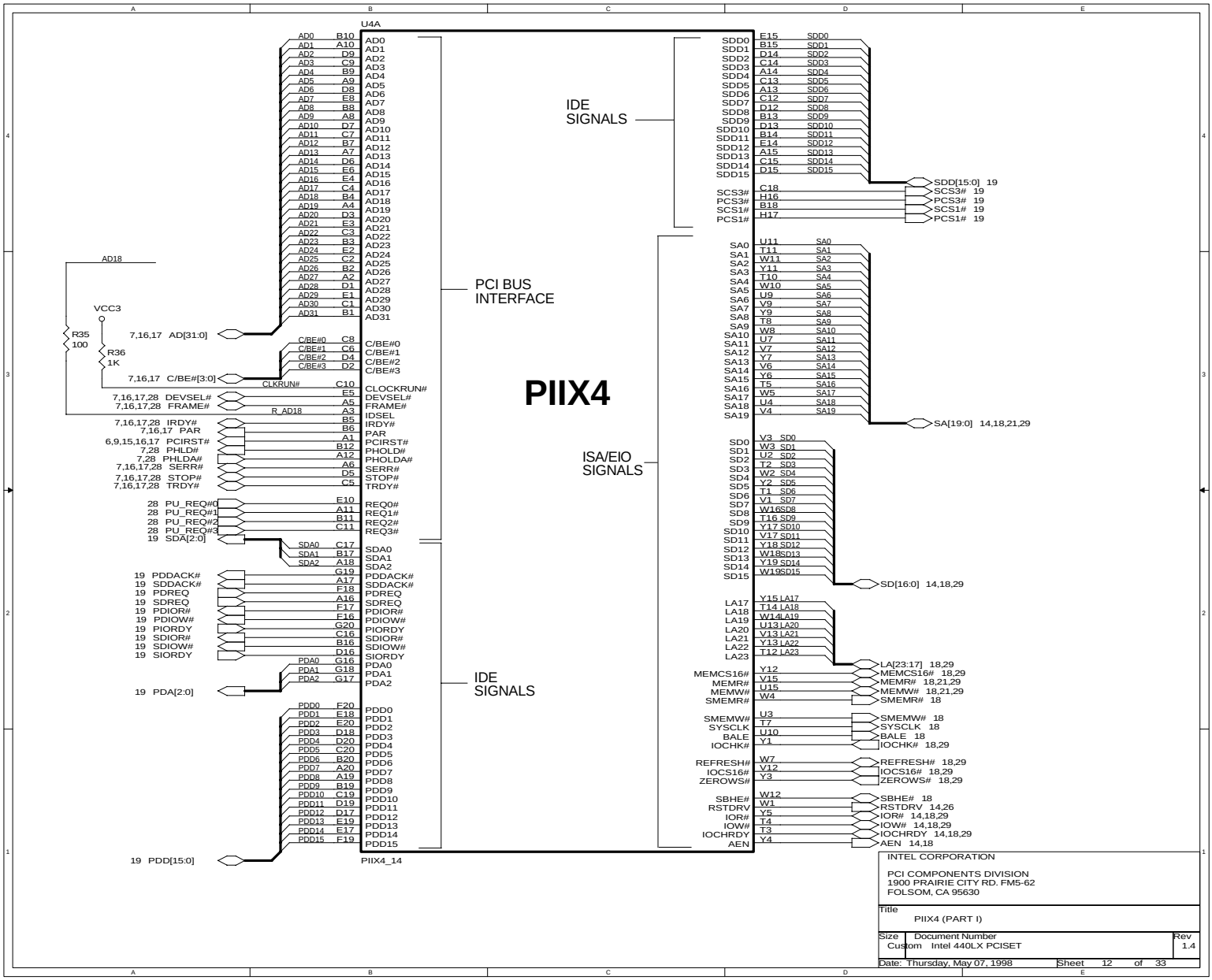
Title: THIRD DIMM SOCKET

Size: Custom | Document Number: Intel 440LX PCISET | Rev: 1.4

Date: Thursday, May 07, 1998 | Sheet 11 of 33



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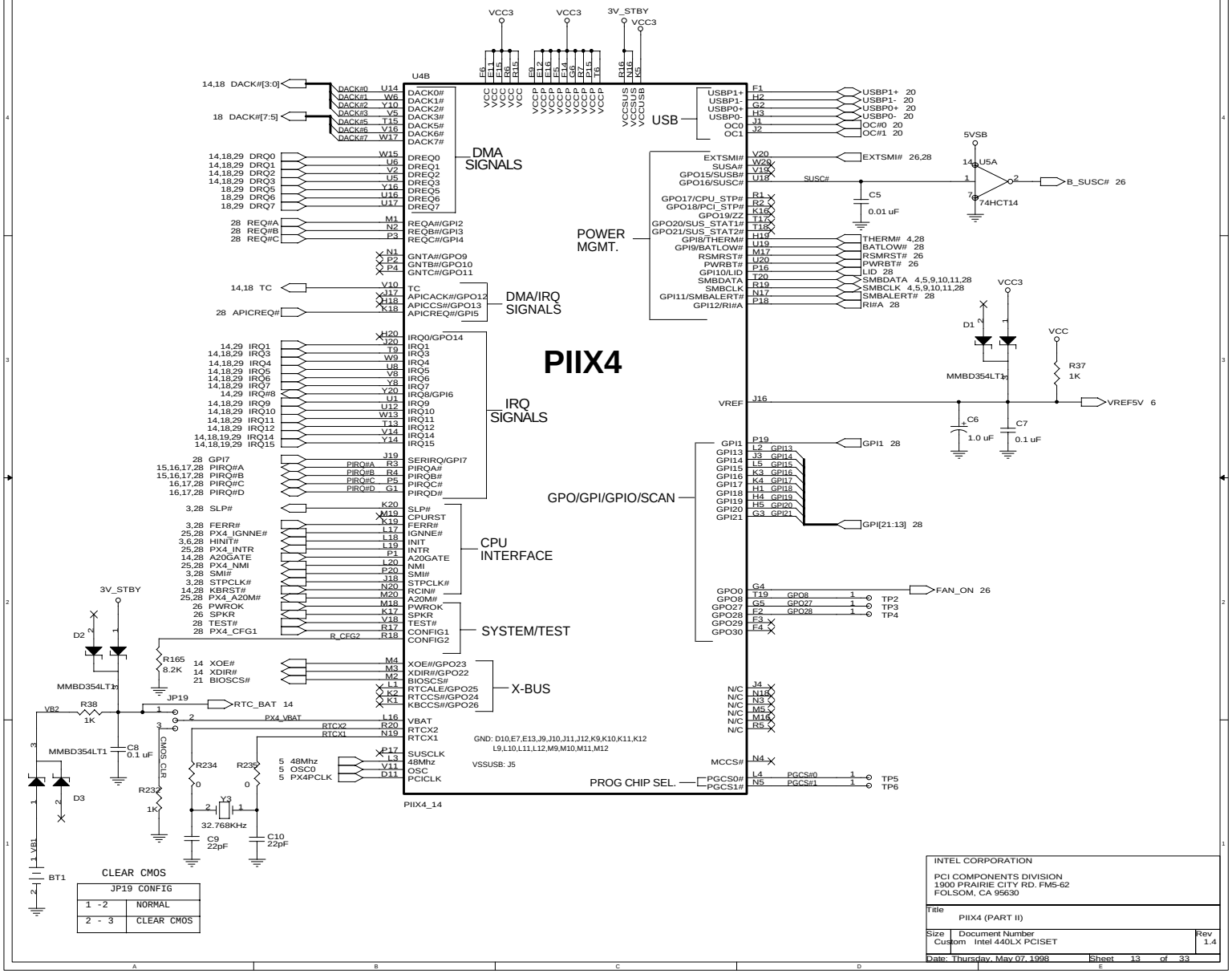
Title: PIIX4 (PART I)

Size	Document Number	Rev
Custom	Intel 440LX PCISET	1.4

Date: Thursday, May 07, 1998 Sheet 12 of 33


PIIX4
U4B
DMA SIGNALS
DMA/IRQ SIGNALS
IRQ SIGNALS
CPU INTERFACE
SYSTEM/TEST
X-BUS
USB
POWER MGMT.
GPO/GPI/GPIO/SCAN
PROG CHIP SEL.
VCC3
3V_STBY
5VSB
VREF
VREF5V 6
B_SUSC# 26
FAN_ON 26
RTC_BAT 14
CLEAR CMOS
JP19 CONFIG
1 -2 NORMAL
2 - 3 CLEAR CMOS
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Title
PIIX4 (PART II)
Size Custom
Document Number Intel 440LX PCISET
Rev 1.4
Date: Thursday, May 07, 1998
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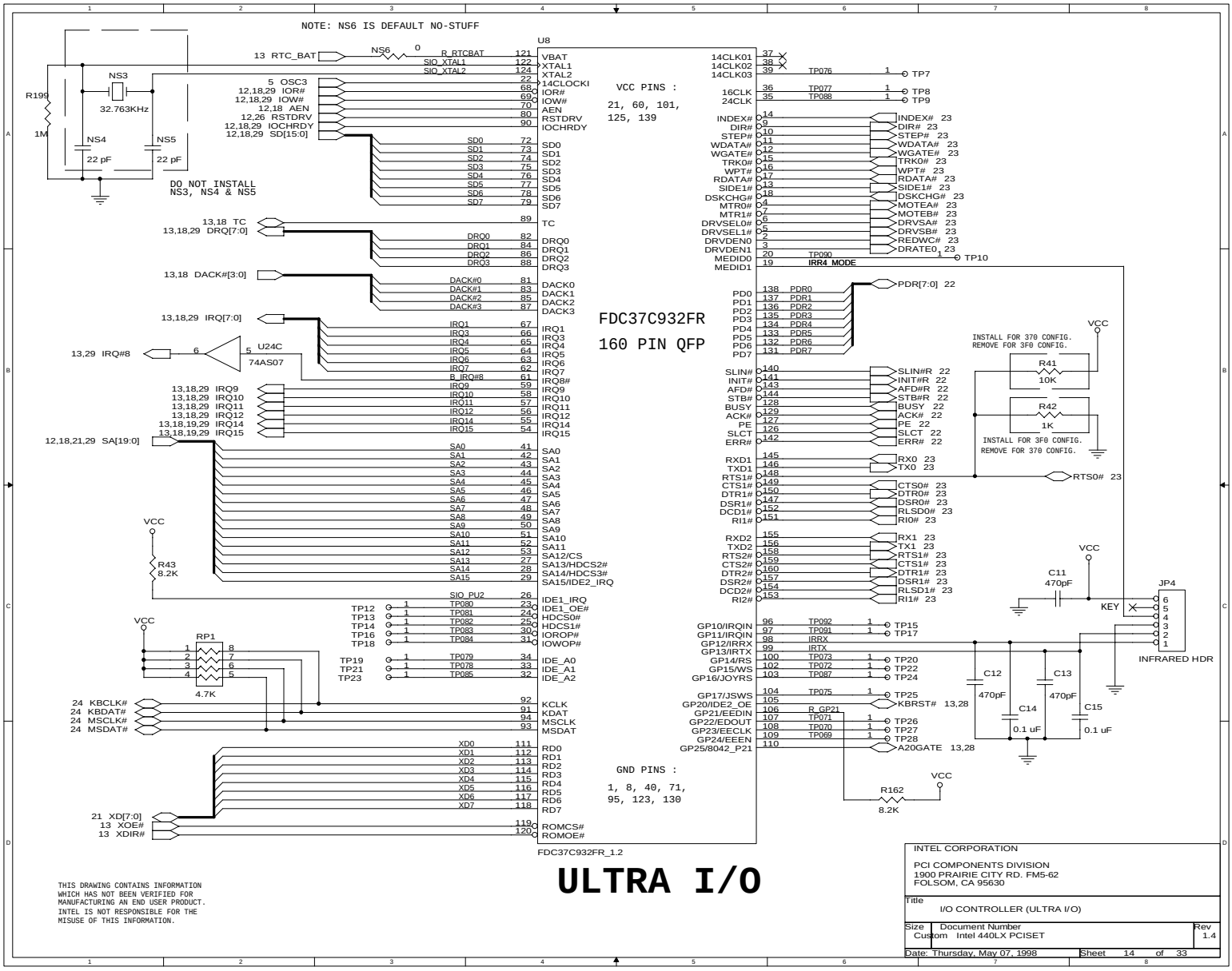
NOTE: NS6 IS DEFAULT NO-STUFF
U8
FDC37C932FR
160 PIN QFP
VCC PINS :
21, 60, 101,
125, 139
GND PINS :
1, 8, 40, 71,
95, 123, 130
FDC37C932FR_1.2
DO NOT INSTALL
NS3, NS4 & NS5
32.763KHz
R199
1M
NS3
NS4
NS5
22 pF
22 pF
NS6
INSTALL FOR 370 CONFIG.
REMOVE FOR 3F0 CONFIG.
INSTALL FOR 3F0 CONFIG.
REMOVE FOR 370 CONFIG.
IRR4_MODE
INFRARED HDR
KEY
4.7K
8.2K
74AS07
U24C
ULTRA I/O
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Title
I/O CONTROLLER (ULTRA I/O)
Size
Custom
Document Number
Intel 440LX PCISET
Rev
1.4
Date: Thursday, May 07, 1998
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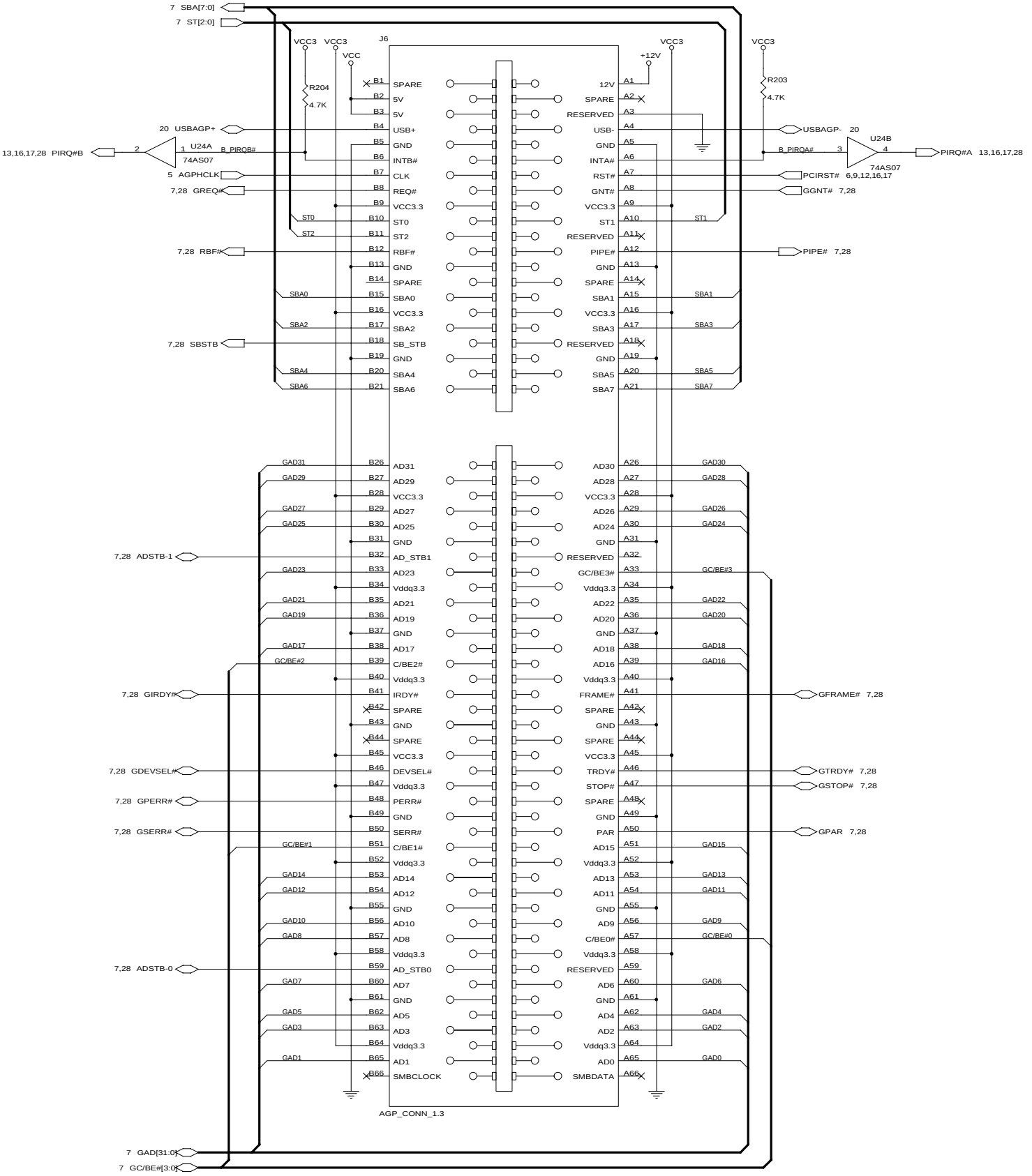

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Title: ACCELERATED GRAPHICS PORT (AGP) CONNECTOR		
Size: Custom	Document Number: Intel 440LX PCISET	Rev: 1.4
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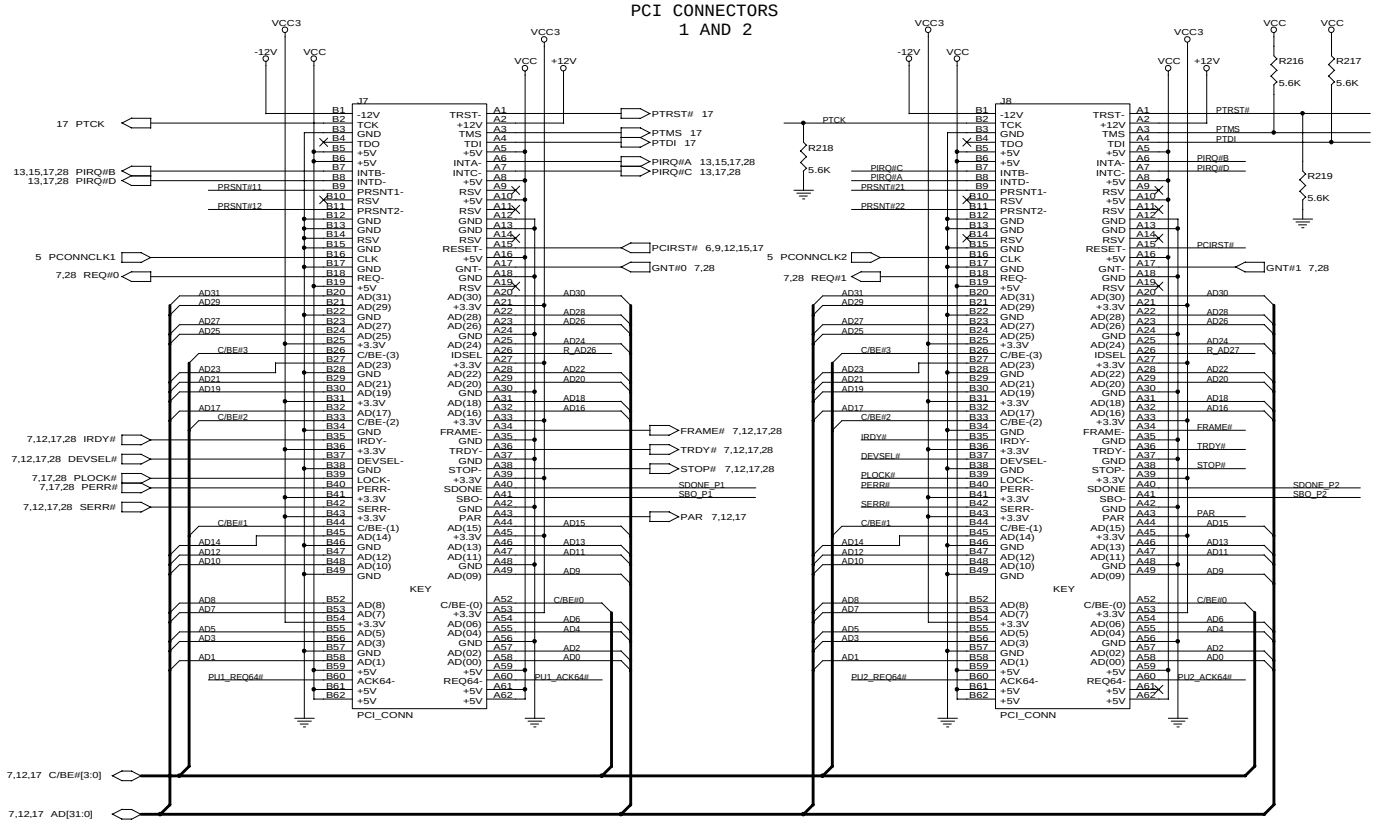
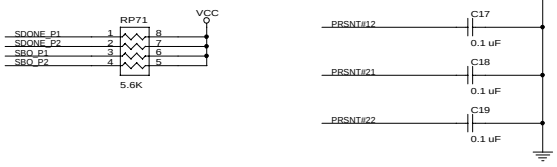
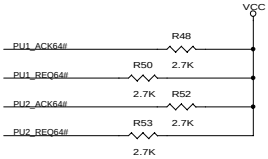
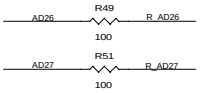
DO NOT REPRODUCE

PCI CONNECTORS 1 AND 2









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Title: PCI CONNECTORS 1 & 2

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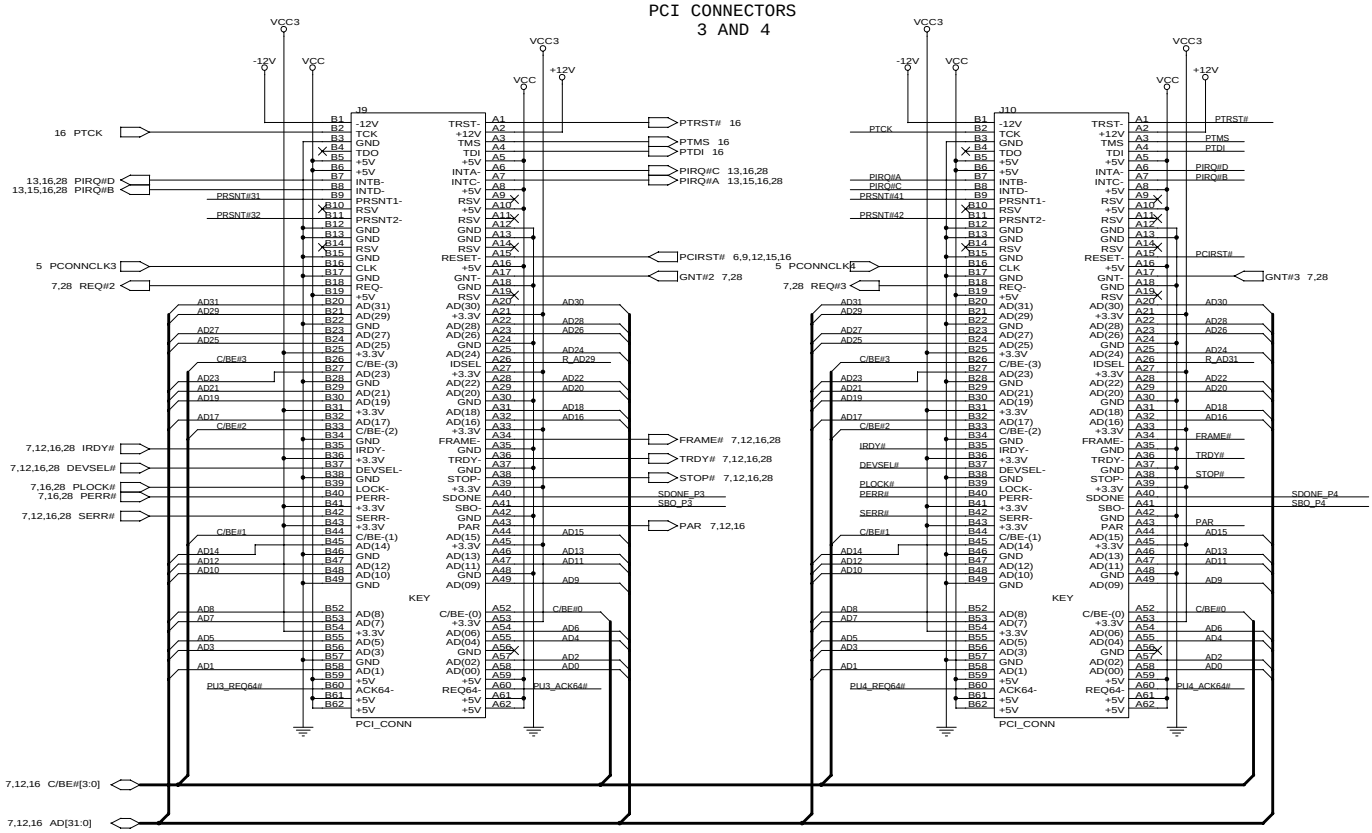
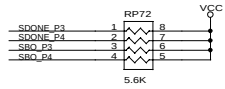
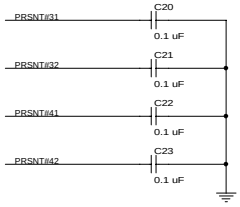
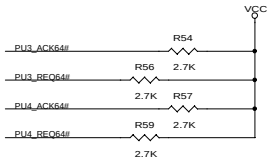
DO NOT REPRODUCE

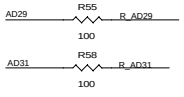
PCI CONNECTORS 3 AND 4











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Title: PCI CONNECTORS 3 & 4

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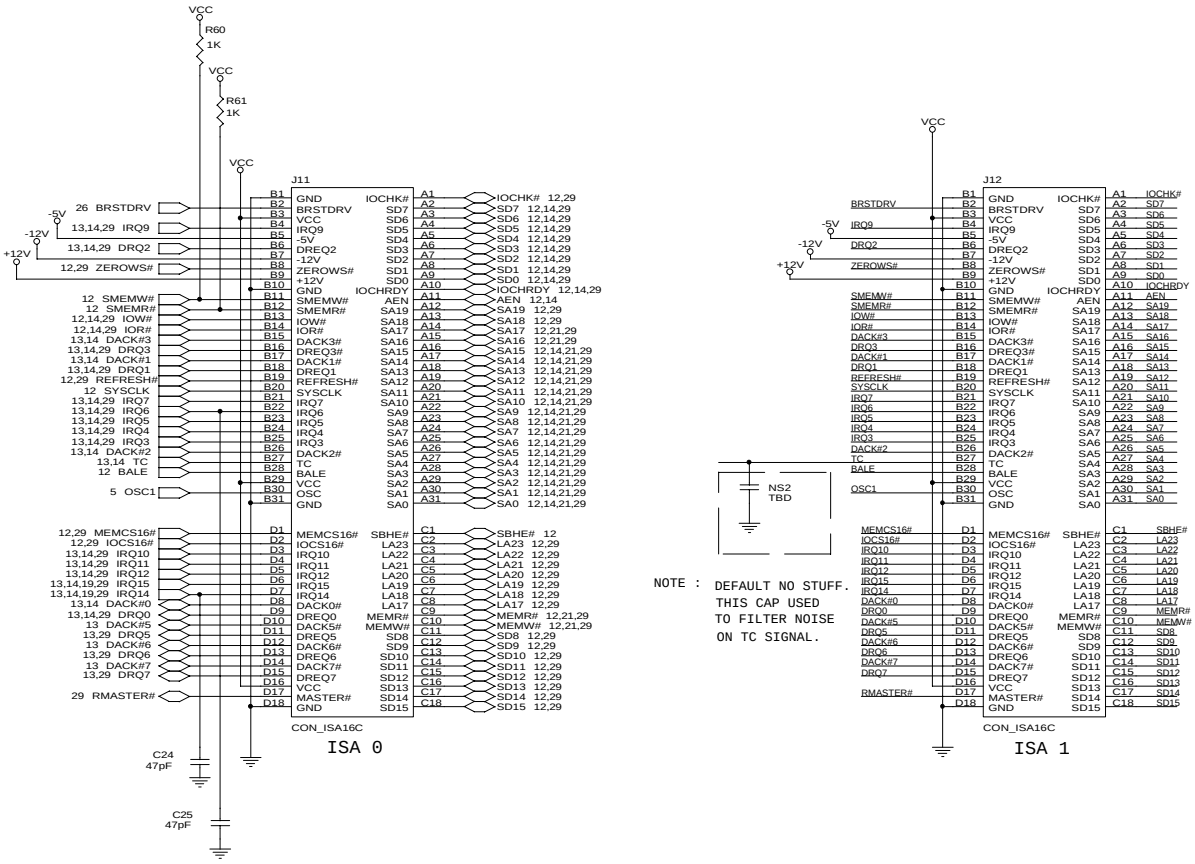
ISA SLOTS



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Title	ISA SLOTS
Size / Document Number	Custom Intel 440LX PCISET
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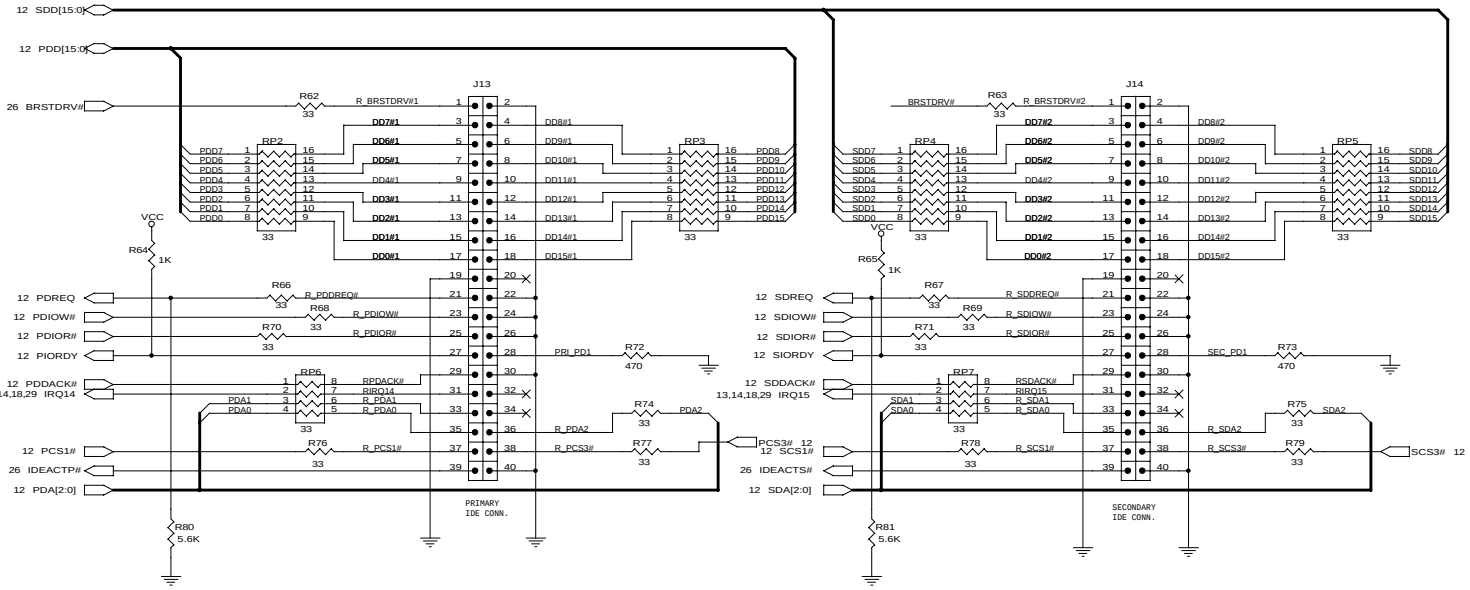
IDE CONNECTORS



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FOLSOM, CA 95630

Title: PCI IDE CONNECTORS

Size: Custom | Document Number: Intel 440LX PCISET | Rev: 1.4

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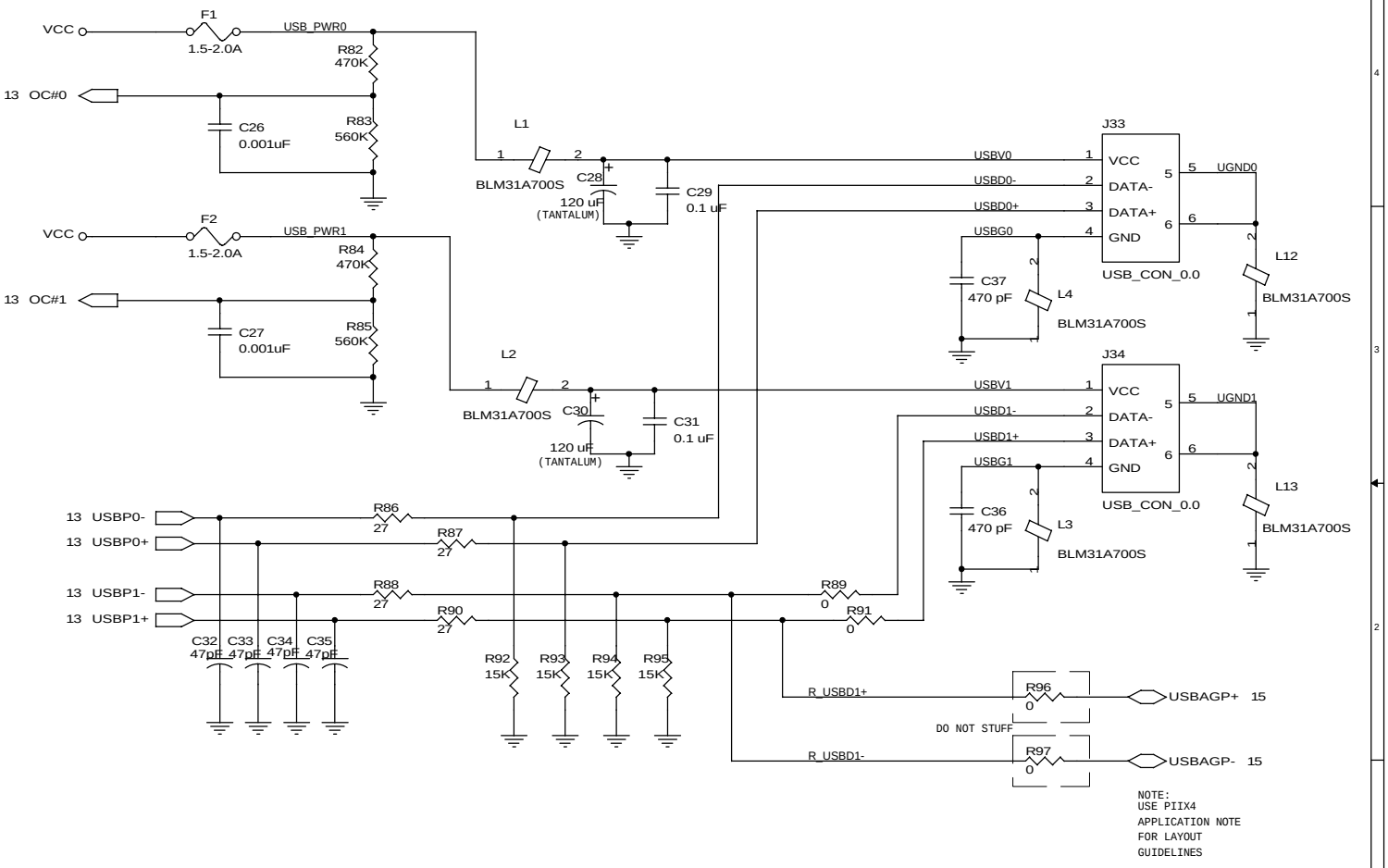

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FOLSOM, CA 95630

Title: USB HEADER

Size	Document Number	Rev
Custom	Intel 440LX PCISET	1.4

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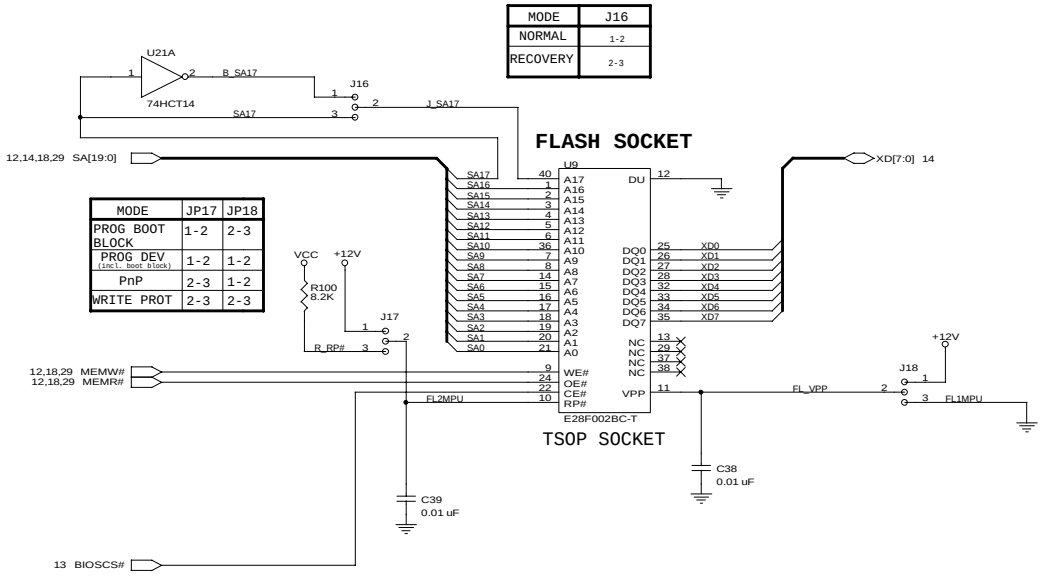
SYSTEM ROM



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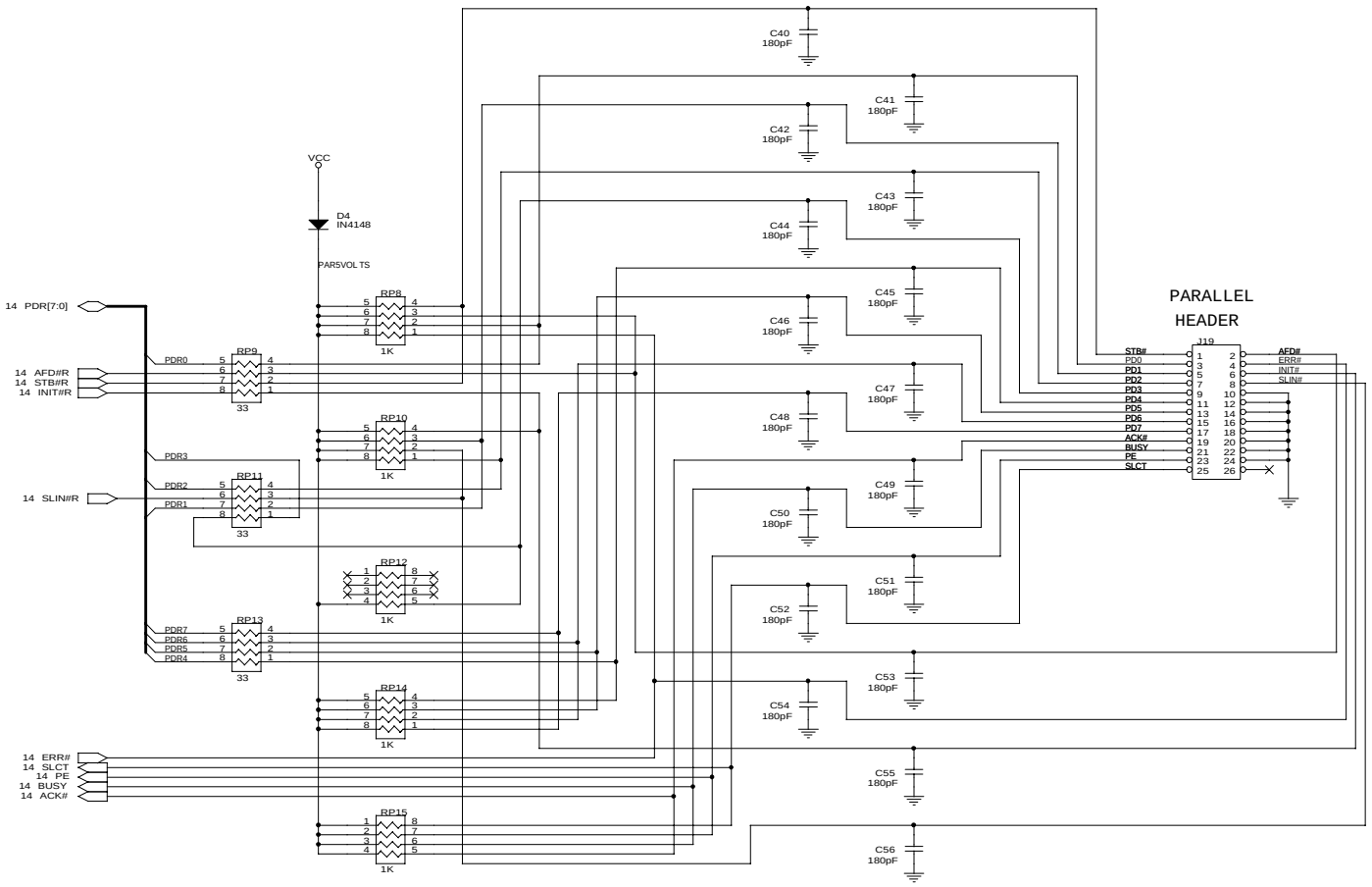
FOLSOM, CA 95630

Title: SYSTEM ROM

Size: Custom | Document Number: Intel 440LX PCISET | Rev: 1.4

Date: Thursday, May 07, 1998 | Sheet 21 of 33



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Title
PARALLEL PORT

Size	Document Number	Rev
Custom	Intel 440LX PCISET	1.4

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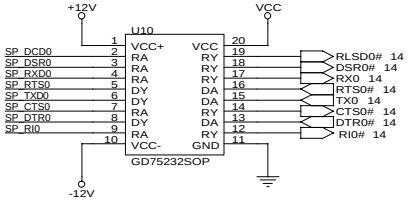
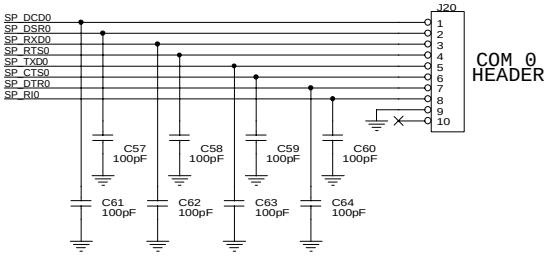
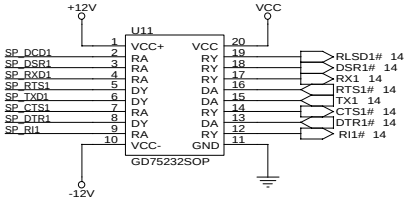
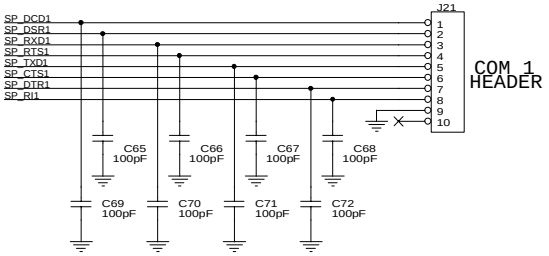
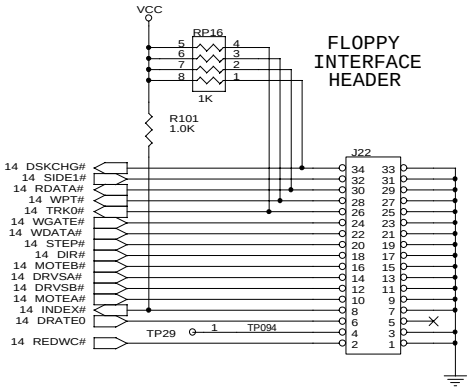


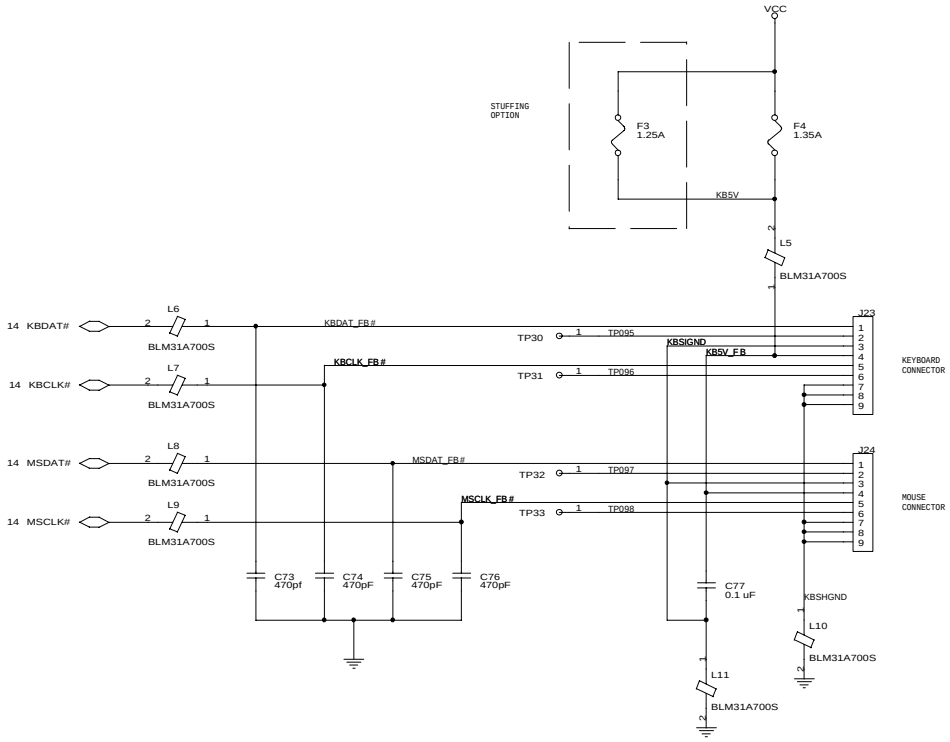








INTEL CORPORATION PCI COMPONENTS DIVISION 1900 PRAIRIE CITY RD. FM5-62 FOLSOM, CA 95630		
Title SERIAL AND FLOPPY		
Size Custom	Document Number Intel 440LX PCISET	Rev 1.4
Date: Thursday, May 07, 1998	Sheet 23 of 33	



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FOLSOM, CA 95630

Title: KEYBOARD/MOUSE INTERFACE

Size: Custom | Document Number: Intel 440LX PCISET | Rev: 1.4

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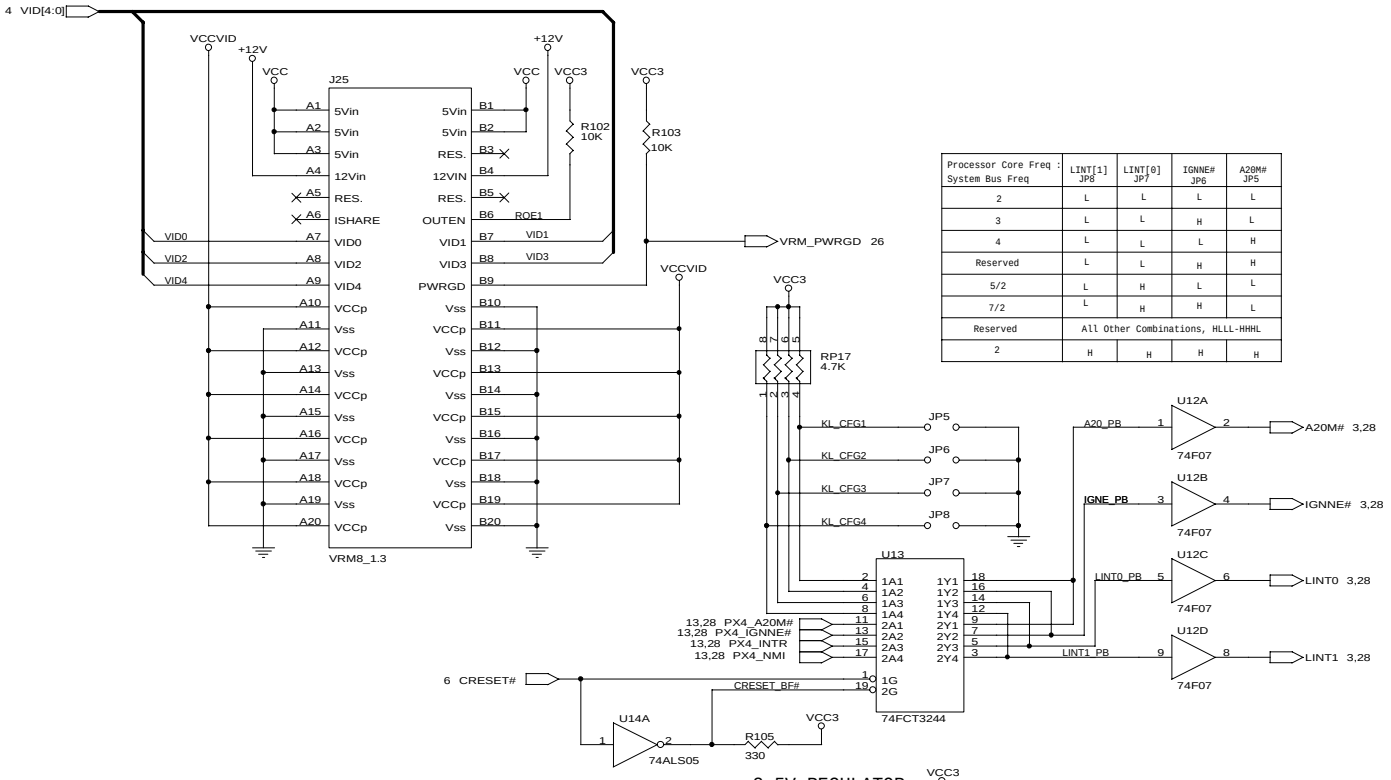
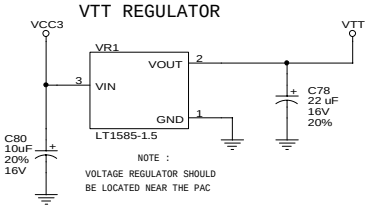


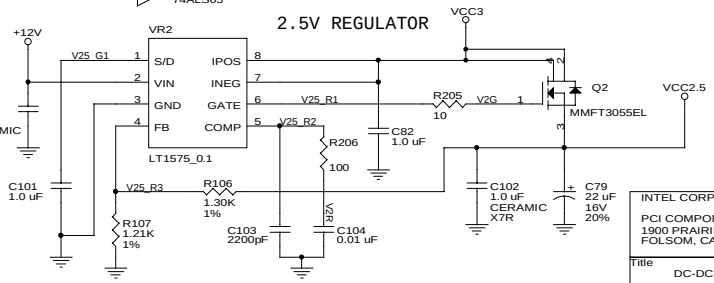
Processor Core Freq : System Bus Freq	LINT[1] JP8	LINT[0] JP7	IGNNE# JP6	A20M# JP5
2	L	L	L	L
3	L	L	H	L
4	L	L	L	H
Reserved	L	L	H	H
5/2	L	H	L	L
7/2	L	H	H	L
Reserved	All Other Combinations, HLLL-HHHL			
2	H	H	H	H

VTT REGULATOR



NOTE :
VOLTAGE REGULATOR SHOULD BE LOCATED NEAR THE PAC

2.5V REGULATOR



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PCI COMPONENTS DIVISION
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Title: DC-DC CONVERTER CONNECTORS

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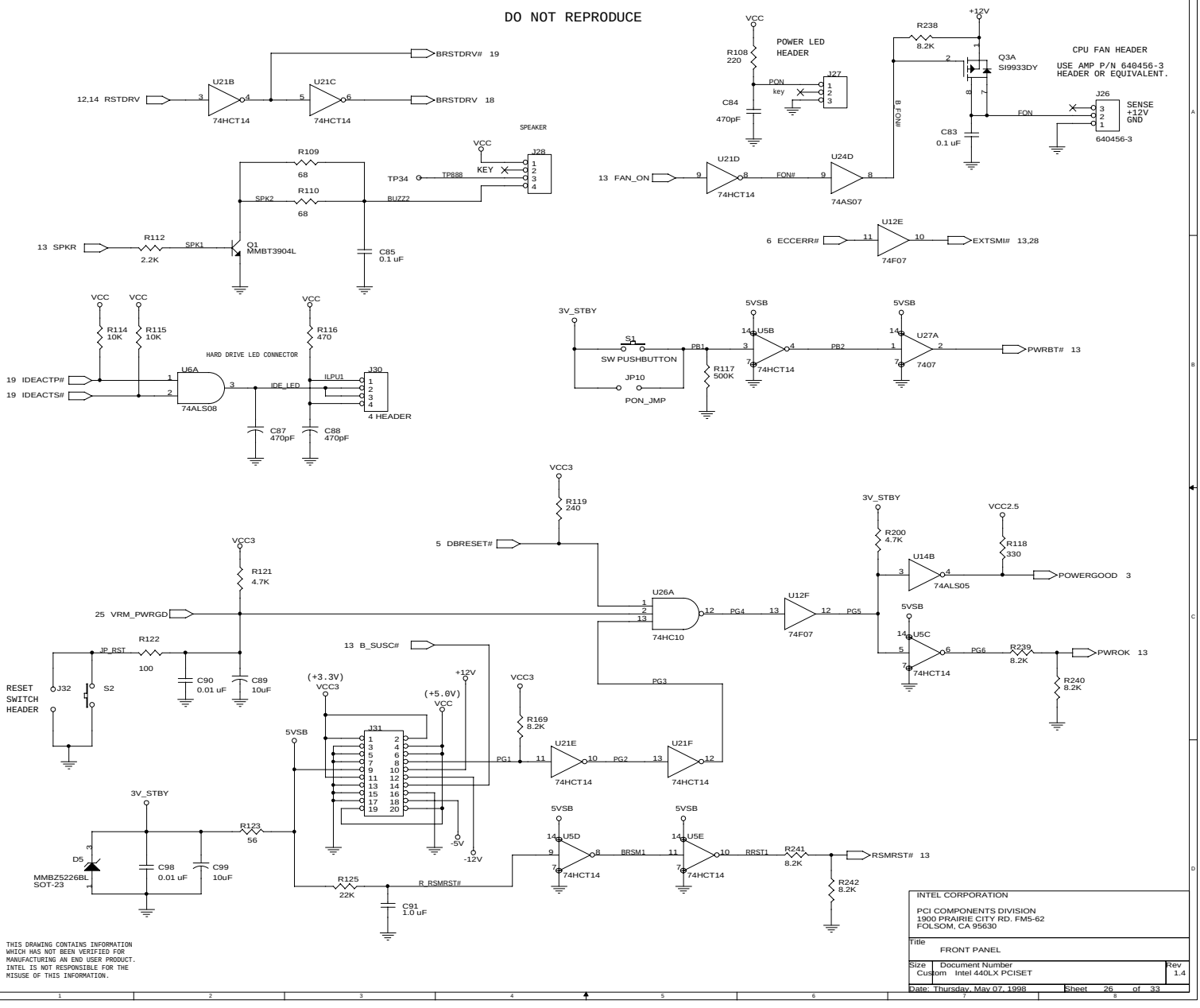
DO NOT REPRODUCE



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Title: FRONT PANEL

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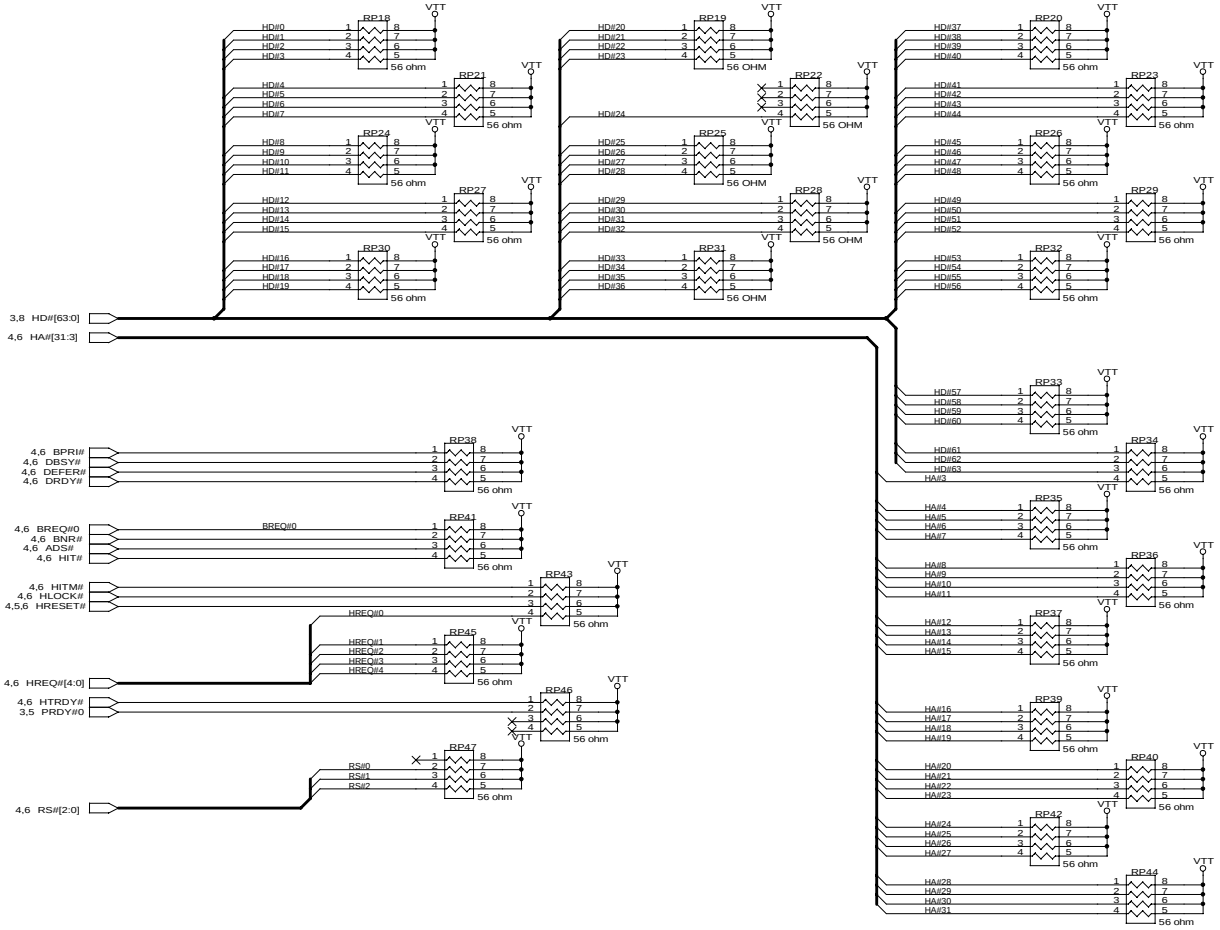
GTL+ TERMINATION RESISTORS



NOTE : VTT = TERMINATION VOLTAGE

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Title		
GTL TERMINATION		
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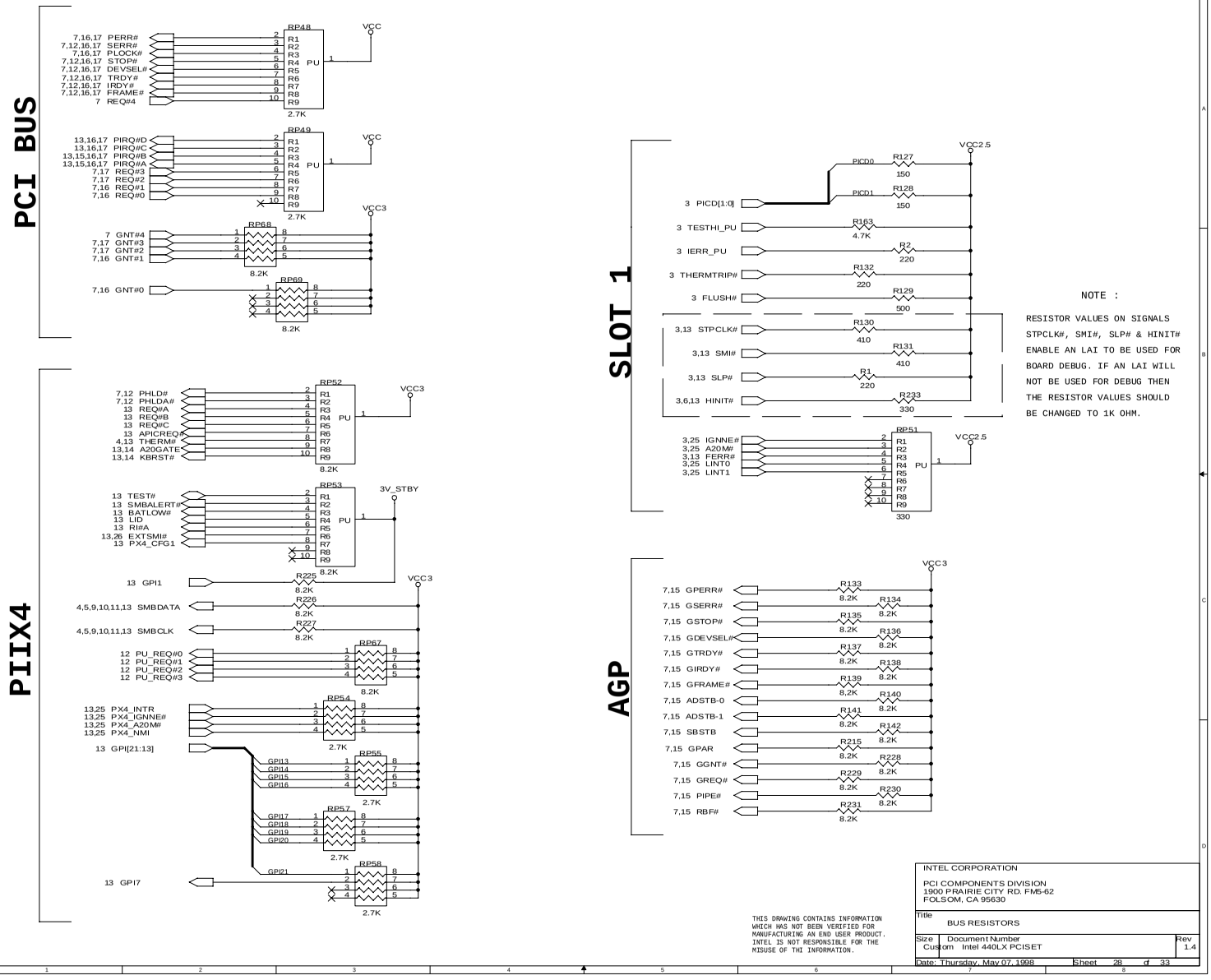
PCI BUS
RP48
VCC
7,16,17 PERR#
7,12,16,17 SERR#
7,16,17 PLOCK#
7,12,16,17 STOP#
7,12,16,17 DEVSEL#
7,12,16,17 TRDY#
7,12,16,17 IRDY#
7,12,16,17 FRAME#
7 REQ#4
R1 R2 R3 R4 R5 R6 R7 R8 R9 PU
2.7K
RP49
VCC
13,16,17 PIRQ#D
13,16,17 PIRQ#C
13,15,16,17 PIRQ#B
13,15,16,17 PIRQ#A
7,17 REQ#3
7,17 REQ#2
7,16 REQ#1
7,16 REQ#0
2.7K
VCC3
RP68
7 GNT#4
7,17 GNT#3
7,17 GNT#2
7,16 GNT#1
8.2K
RP69
7,16 GNT#0
8.2K
PIIX4
RP52
VCC3
7,12 PHLD#
7,12 PHLDA#
13 REQ#A
13 REQ#B
13 REQ#C
13 APICREQ#
4,13 THERM#
13,14 A20GATE
13,14 KBRST#
8.2K
RP53
3V_STBY
13 TEST#
13 SMBALERT#
13 BATLOW#
13 LID
13 RI#A
13,26 EXTSMI#
13 PX4_CFG1
8.2K
13 GPI1
R225 8.2K
VCC3
4,5,9,10,11,13 SMBDATA
R226 8.2K
4,5,9,10,11,13 SMBCLK
R227 8.2K
RP67
12 PU_REQ#0
12 PU_REQ#1
12 PU_REQ#2
12 PU_REQ#3
8.2K
RP54
13,25 PX4_INTR
13,25 PX4_IGNNE#
13,25 PX4_A20M#
13,25 PX4_NMI
2.7K
13 GPI[21:13]
RP55
GPI13
GPI14
GPI15
GPI16
2.7K
RP57
GPI17
GPI18
GPI19
GPI20
2.7K
RP58
GPI21
13 GPI7
2.7K
SLOT 1
VCC2.5
PICD0
R127 150
PICD1
R128 150
3 PICD[1:0]
3 TESTHI_PU
R163 4.7K
3 IERR_PU
R2 220
3 THERMTRIP#
R132 220
3 FLUSH#
R129 500
3,13 STPCLK#
R130 410
3,13 SMI#
R131 410
3,13 SLP#
R1 220
3,6,13 HINIT#
R233 330
RP51
VCC2.5
3,25 IGNNE#
3,25 A20M#
3,13 FERR#
3,25 LINT0
3,25 LINT1
R1 R2 R3 R4 R5 R6 R7 R8 R9 PU
330
NOTE :
RESISTOR VALUES ON SIGNALS STPCLK#, SMI#, SLP# & HINIT# ENABLE AN LAI TO BE USED FOR BOARD DEBUG. IF AN LAI WILL NOT BE USED FOR DEBUG THEN THE RESISTOR VALUES SHOULD BE CHANGED TO 1K OHM.
AGP
VCC3
7,15 GPERR#
7,15 GSERR#
7,15 GSTOP#
7,15 GDEVSEL#
7,15 GTRDY#
7,15 GIRDY#
7,15 GFRAME#
7,15 ADSTB-0
7,15 ADSTB-1
7,15 SBSTB
7,15 GPAR
7,15 GGNT#
7,15 GREQ#
7,15 PIPE#
7,15 RBF#
R133 8.2K
R134 8.2K
R135 8.2K
R136 8.2K
R137 8.2K
R138 8.2K
R139 8.2K
R140 8.2K
R141 8.2K
R142 8.2K
R215 8.2K
R228 8.2K
R229 8.2K
R230 8.2K
R231 8.2K
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BUS RESISTORS
Size Custom
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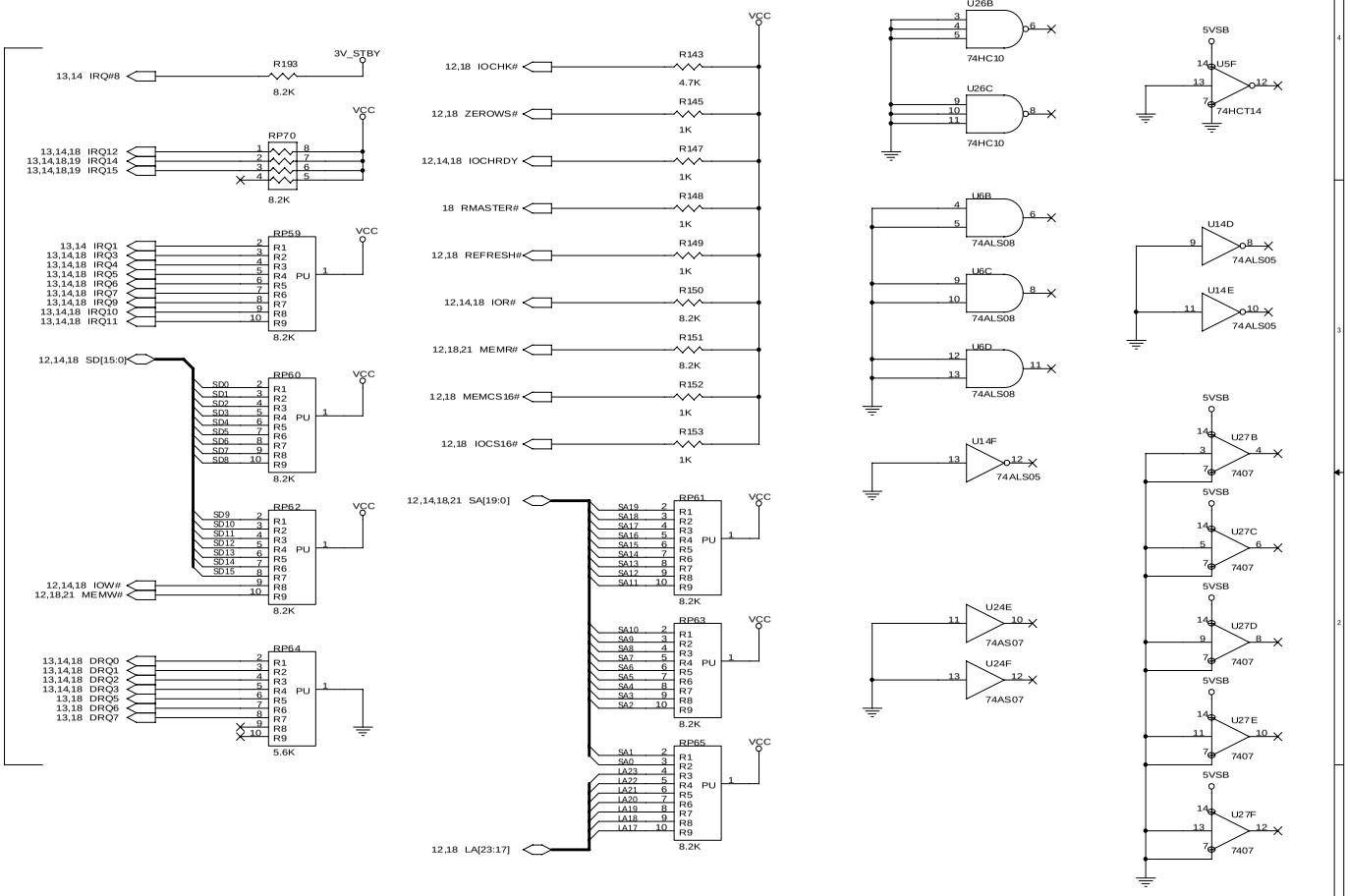
ISA BUS



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Title	ISA BUS PULLUPS
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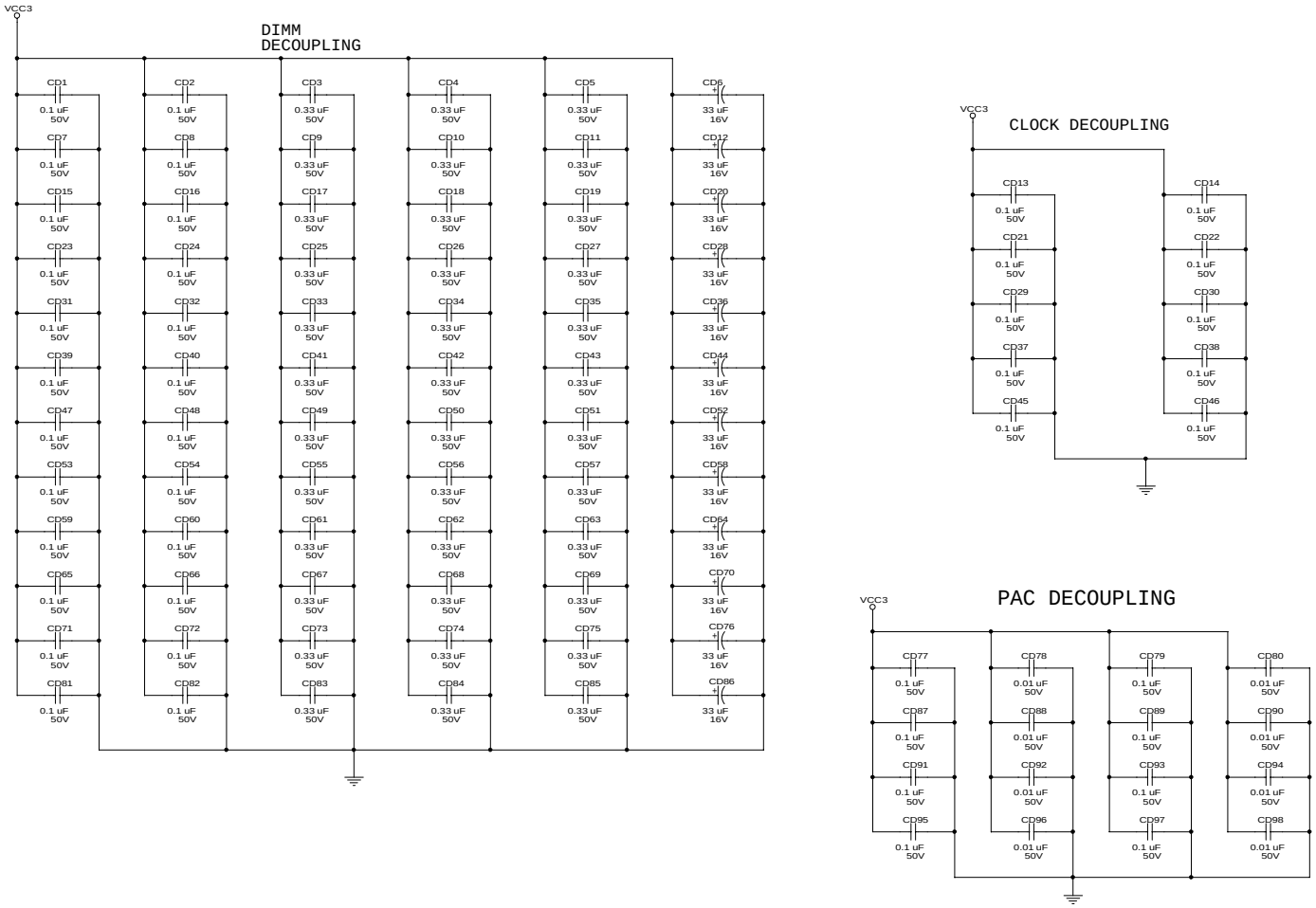

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Title: DRAM AND PAC DECOUPLING CAPACITORS

Size	Document Number	Rev
Custom	Intel 440LX PCISET	1.4

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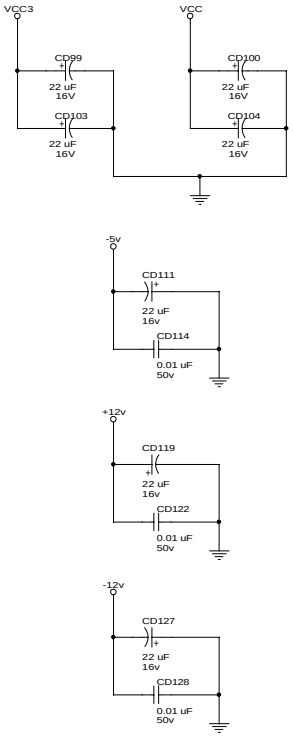
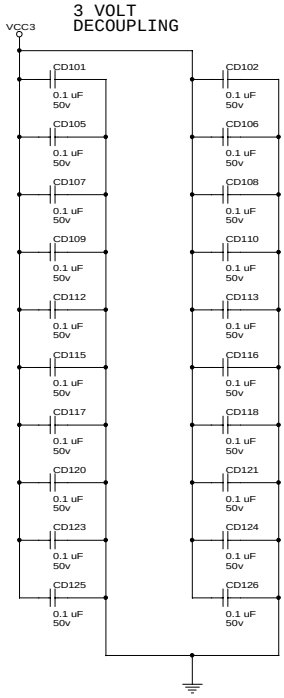
BULK DECOUPLING



3 VOLT DECOUPLING



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Title: 3.3 VOLT AND BULK POWER DECOUPLING

Size	Document Number	Rev
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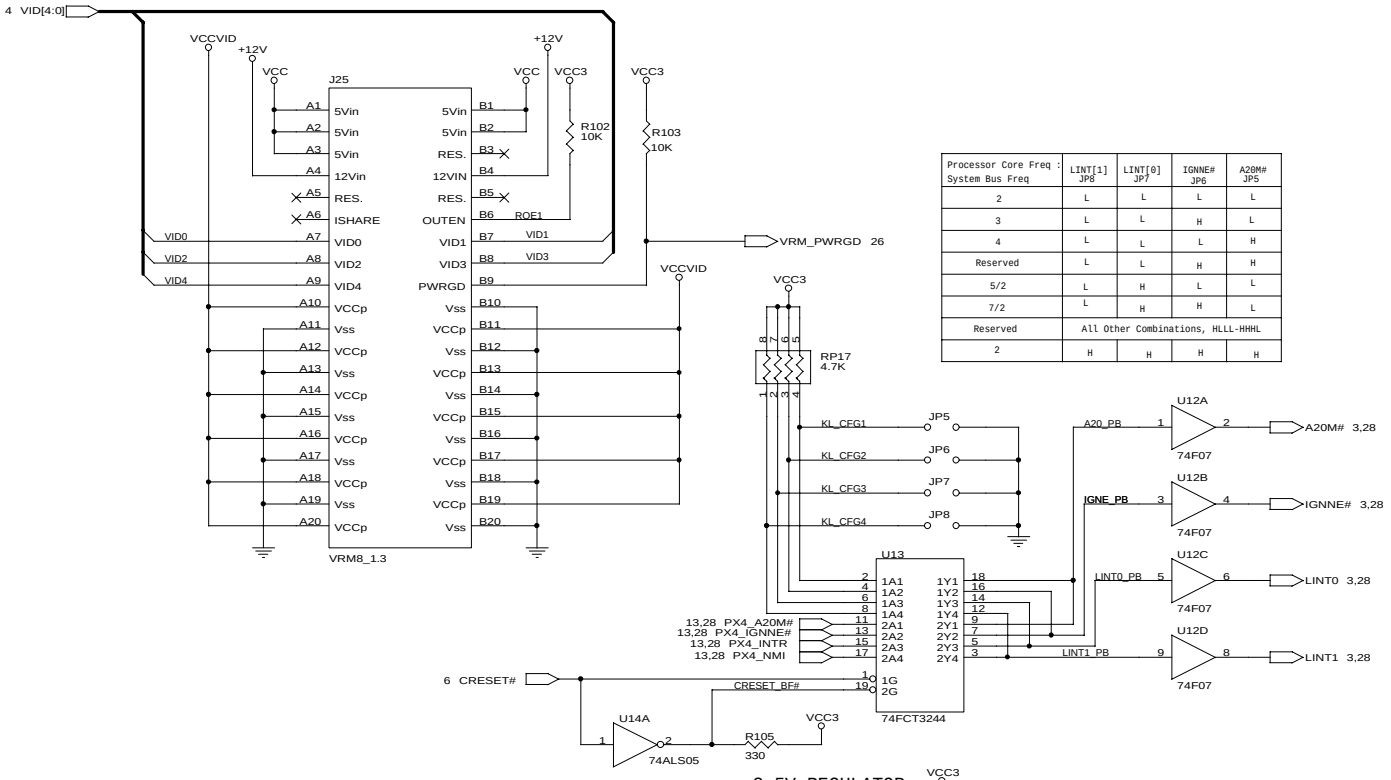
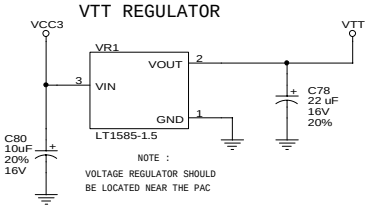


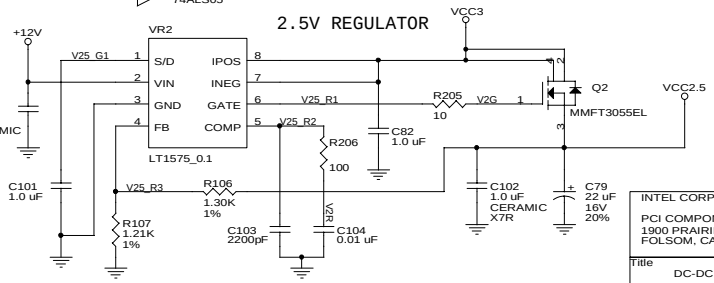
Processor Core Freq : System Bus Freq	LINT[1] JP8	LINT[0] JP7	IGNNE# JP6	A20M# JP5
2	L	L	L	L
3	L	L	H	L
4	L	L	L	H
Reserved	L	L	H	H
5/2	L	H	L	L
7/2	L	H	H	L
Reserved	All Other Combinations, HLLL-HHHL			
2	H	H	H	H

VTT REGULATOR



NOTE :
VOLTAGE REGULATOR SHOULD BE LOCATED NEAR THE PAC

2.5V REGULATOR



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Title: DC-DC CONVERTER CONNECTORS

Size: Custom | Document Number: Intel 440LX PCISET | Rev: 1.4

Date: Thursday, May 07, 1998 | Sheet 25 of 33

REVISION 1.0 - First release of 440LX PCISet schematics.

REVISION 1.1 - Update of Rev 1.0 440LX PCISet schematics.

PAGE 3 : TESTHI pulled to 2.5 volts thru 220 ohms.

PAGE 5 : Pinout of 20-pin I/O clock synthesizer device updated.

330 ohm pullup to 2.5 volts added to PREQ#0.
Pullups on PREQ#[3:1], SMBDATA, and SMBCLK deleted.

PG 6,7,8 : PAC ballout as of 9-26-96 used.

CKE from PAC buffered with 74LVC245 CMOS device.

PG 9,10,11 : MAA11 routed to DIMM SA0, MAA12 to SA1, MAA13 to A11.

DIMM pins 31 and 44 grounded and pin 48 -> WEx# for EDO DIMMs.

DIMM control signals (WEx#, SRASx#, SCASx#, RCSAx#, and CDQxx#) for DIMMs 0 and 2 swapped.

SMBus address starts from 02H on DIMMs (SA2:0).

PAGE 11 : CDQA#x signals re-ordered on the pins of DIMM connector #2.

PAGE 13 : SUSCLK pin on PIIX4 became no-connect.

IRQ#8 now shown as a bi-directional signal.

'ALS08 and '07 deleted because INIT# on PAC is now OD output.

CONFIG2 pin on PIIX4 pulled to ground with 8.2K resistor.

RCIN# name changed to KBRST# and pulled to 3.3V thru 8.2K.

Signal A20GATE pulled to 3.3V thru 8.2K resistor.

PAGE 14 : OSC0 clock to PIIX4 deleted due to redundancy.

XTAL1 input pulled up to VCC through 8.2K resistor.

KEYLOCK# input pulled up to VCC through 8.2K resistor.

Infrared header rewired, IRRX - pin 1, IRTX - pin2.

PAGE 15 : SMB0 & SMB1 pins on AGP connector now noconnects.

PAGE 18 : New symbol used for ISA connectors.

PAGE 19 : Pullup on SDIOR# moved to SIORDY.

PAGE 21 : Deleted 0 ohm resistors R98 and R99, updated jumper tables.

FLASH changed to TSOP pinout instead of PSOP.

PAGE 26 : Capacitor on CPU Fan header changed from 470pF to 0.1uF.

POWEROK circuitry revised with HC14 & HC32 replacing HCT14 & F32 and power from 3.3V Standby.

PAGE 27 : Swapped signals PX4_INTR and PX4_A20M# on 74FCT3244 and 7407 buffers.

PAGE 28 : Pullups on PCI control signals changed from 10K to 2.7K.

PAGE 29 : Pullup on REFRESH# changed from 300 to 1K.

REVISION 1.2 - Update of Rev 1.1 440LX PCISet schematics.

PAGE 3 : Slot 1 pin B12, UP#, now no-connect.

PAGE 4 : Slot 1 pin B109, VCC, now no-connect.

PAGE 5 : New CK3D pinout used for Host/DRAM/PCI clock.

REFOUT routed to XTALIN of CKIO, crystal circuit removed from CKIO XTALIN/OUT.

10 ohm series termination added to clock outputs.

MECC0 and Freq. Sel. jumper. removed, Sel pin pulled up.

PG 9,10,11 : DIMM SA[2:0] changed to match S.V. board for BIOS compatibility. DIMM0=2H, DIMM1=4H, DIMM2=0H.

PAGE 12 : PIIX4 pinout modified, GPI8/HCT# renamed GPI8/THERM#.

PCI REQ#[3:0] routed to pullups only.

PAGE 13 : Added 2 jumpers,'HCT14 and 'HC32 to A20M# from PIIX4.

Schottky diodes converted to dual Schottky diodes.

Renamed IDE interface signals on the PIIX4 and IDE page.

PAGE 14 : Added crystal and 2 caps to XTAL circuit of Ultra I/O.

PAGE 15 : Deleted 74AS07 buffers and pullups on PIRQ#x .

SMBCLK connected to pin B66,SMBDATA to A66.

PAGE 20 : Header broken into 2 USB connectors.

Polarity symbols added to polarized caps.

PAGE 25 : UP# now no-connect on Slot1, pulled up on VRM.

PAGE 26 : External SMI jumper and circuit deleted (jumper, U6B 'ALS08, U12F 'F07, debounce circuit)
PWROK circuit modified : U5C,D & E from 74HC14 to 74ALS05 powered by VCC, U17 (74HC32) deleted.
R120 & R124 changed to 8.1K on PWROK circuit.

R126 replaced with Zener diode, R123 changed from 3.48K to 410 ohm on 3V_STBY circuit.
C91 on RSMRST# changed from 0.01uF to 1.0uF.

RSMRST# now powered from 5VSB, added 2 'HCT14 gates and voltage divider to circuit.
Deleted R168 & C96, added 2 'HC14 gates to PWROK from power connector.

CPU fan header changed to 3-pin header.

Added 0.1 uF cap for debounce to PWR_BTN circuit.

PAGE 28 : All PCI control signals pulled through 8.2K to 3.3V.

PIPE# and DBF# pulled to 3.3V through 8.2K.

GPI1 and PX4_CFG1 pulled to 3V_STBY thru 8.2K.

RP55, 57 & 58 changed from 1K to 2.7K.

PAGE 29 : IRQ12 pulled to 5.0V through 8.2K.

Pullup on REFRESH# changed from 300 to 1K ohms.

IRQ8# now pulled to 3V_STBY thru 8.2K.

Unused gates added to ISA pullup page.

REVISION 1.3 - Update of Rev 1.2 440LX PCISet schematics.

PAGE 3 : Slot 1 pinout changed : pin B01 from RESERVED to EMI; pin B15 from FANFAIL# to RESERVED; pin B21 from EMI to 100/66#; pin B100 from RESERVED to EMI; pin B101 from EMI to S_O#.
Connected signal SLP# from PIIX4 to Slot 1 to support sleep state.

PAGE 4 : Added LM75 Thermal Sensor device to THERM# and SMB bus.

Added zero ohm resistors and jumpers to VID[4:0] for voltage select on VRM.

Connected pin B101 to GND.

Connected pin B109 to VCC (5 volts).

PAGE 7 : PAC pin W4 name changed from DBF# to RBF#.
Signal renamed from DBF# to RBF# also.

PG 9,10,11 : DIMM SA[2:0] changed to DIMM0=0H, DIMM1=1H, DIMM2=2H.

PAGE 13 : Removed resistor NS1 from PIIX4 RTC crystal circuit.

Signal GPI17 named incorrectly for PIIX4 pin J19, changed to GPI7 and pulled to 3.3V through 2.7K.
Device U5 changed from 74HC14 to 74LVC14 for 3V compatibility.

Removed JP3, route RTC_BAT direct to PIIX4, placed 0 ohm in series to SMC input. Added JP19 to clear CMOS.
Removed JP11 & 12, U21 & U23. A20M# circuit not needed for B-0 PIIX4 units.

PAGE 14 : Added 74AS07 gate to IRQ#8 to convert from 5V to 3V_STBY.

PAGE 15 : Added 74AS07 gates with 4.7K pullups to 3.3V on PIRQ#A and PIRQ#B.

Pin A66 name changed, SMB1 -> SMBDATA, B66 name changed, SMB0 -> SMBCLOCK.

PAGE 16,17 : Added pullups to SBO, SDONE, TMS & TDI, pulldowns to TRST# & TCK to comply with PCI 2.1 Spec.
Changed PCI connector IDSELs from AD28 - 31 to AD26, AD27, AD29, AD31.

PAGE 25 : Changed 2.5V generation from LT1587 to LT1575 plus power FET and associated circuit.

VRM8 pinout changed, pin B5 from UP# to RESERVED. Pullup R104 deleted.

PAGE 26 : Removed voltage divider resistors R120, 124, 201 & 202 on RSMRST# and PWROK .

Replaced three 74ALS05 gates wire-ored with 74HC10 and 74F07 on POWERGOOD circuit.

Device U5 changed from 74HC14 to 74LVC14, RSMRST# powered by 3V_STBY .

R123 changed from 410 to 56 ohmon 3V_STBY, R125 changed from 1K to 22K on RSMRST#.

PAGE 28 : PCI control pullups changed to 2.7K -> 5V from 8.2K -> 3.3V. GNTx still pulled to 3.3V thru 8.2K.
GPAR pulled to 3.3V through 8.2K per DCN #70.

RP56 broken into discrete resistors for AGP layout considerations. R133 - R138 converted from 10K to 8.2K.
RP66 broken into discrete resistors. SMBDATA and SMBCLK pulled to 3.3V thru 8.2K.

PAGE 29 : R-Pack added to pull IRQ1 to VCC thru 8.2K.

Pullup on ZEROWS#, MEMCS16# & IOCS16# changed from 300 ohm to 1K.

REVISION 1.4 - Update of Rev 1.3 440LX PCIset schematics.

PAGE 3 : Pullups on SLP#, IERR# and TESTHI moved to Page 28.

PAGE 4 : VID[4:0] jumpers pulled to VCC instead of VCC3.

PAGE 5 : Series termination changed from 10 ohms to 22 ohms on SDRAM-I/O clocks and 33 ohms on all other clocks.

PAGE 6 : VCCA pin R3 renamed VCC. AGND pin R5 renamed GND.
VCC_pins AD12 & R4 added to list of VCC pins on part.

JP2 changed to 3-pin jumper. Pulldown R236 added to config PAC with IOQD = MAX.

PG 9,10,11 : PCIRST routed through U14, 74ALS05, to OE pins on all DIMM modules to disable MECC[7:0] output during board reset.

PAGE 13 : Added R234 & R235 to PIIX4 RTC crystal inputs.

GPO0 connected to signal FAN_ON instead of TP1.

U5A changed to 74HCT14 powered by 5VSB on signal B_SUSC#.

PAGE 15 : SMBDATA & SMBCLK no longer routed to AGP connector.

PAGE 26 : Circuitry on signals PWRBT#, PWROK, RSMRST# and FAN_ON modified and converted from 3V_STBY to 5VSB.

PAGE 28 : Added pullups for SLP#,IERR# and TESTHI. Added note about resistor changes for LAI use.

PAGE 29 : Added unused 74AS07 gates.

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Title: REVISION HISTORY

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