Intel® E7501 Chipset Memory Controller Hub (MCH)

Specification Update

October 2004

Notice: The Intel® E7501 chipset MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 251928-003

Contents

Revision History

Version	Description	Date
-001	Initial Release	December 2002
-002	Added Documentation Change regarding Thermal Management Functionality	February 2003
-003	Added Documentation Change #2	October 2004

Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating systems, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents/Related Documents

Document Title	Document Number
Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet	251927-001

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the behavior of the Intel® E7501 chipset MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The Intel® E7501 chipset MCH stepping can be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A1	8086h	254Ch	01h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel® E7501 Chipset MCH may be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
A1	SL6NV	RGE7501MC	Production

Summary Tables of Changes

The following tables indicate the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed Intel® E7501 chipset MCH steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Erratum, Specification Change or Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component, if the component is stepped in the future.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This item is either new or modified from the previous version of the document.

Number	A1	Plans	ERRATA
1	X	NoFix	Receive Enable Timing Marginality

Number	SPECIFICATION CHANGES
	There are no Specification Changes in this Specification Update revision.

Number	SPECIFICATION CLARIFICATIONS
	There are no Specification Clarifications in this Specification Update revision.

Number	DOCUMENTATION CHANGES
1	Thermal Management Functionality
2	CONFIG_ADDRESS Description Correction

Errata

1. Receive Enable Timing Marginality

Problem: Under very specific test conditions that includes a combination of low MCH core voltage, high temperature and slow silicon, the Intel® E7501 MCH may cause a system hang when the currently recommended Receive Enable Delay settings are used and the system is populated with CL=2.5 registered DIMMs. The system hang observed is caused by a timing marginality in the MCH.

Implication: When using previously recommended Receive Enable Delay settings and with CL2.5 DIMMs populated in the system, the MCH could hang the system with minimal memory traffic.

Workaround: The BIOS must initialize the Receive Enable delay settings as described in *Rev 1.01 or later version of the Intel E7501 MCH BIOS Specification Update* and *Rev1.01 or later version of the Intel E7501 MCH DDR Memory Reference Code.*

The new Receive Enable delay settings are required for platforms that adhere to the MCH to Memory layout design recommendations in the *Intel® Xeon™ Processor and Intel® E7500 / E7501 Chipset Compatible Platform Design Guide.*

Contact your Intel Field Representative to obtain the latest versions of these documents.

Status: No Fix.

Specification Changes

There are no Specification Changes in this Specification Update revision.

Specification Clarifications

There are no Specification Clarifications in this Specification Update revision.

Documentation Changes

1. Thermal Management Functionality.

On page 124, replace Section 5.5.7 with the following, more in-depth, description of the Thermal Management functionality of the Intel® E7501 chipset.

5.5.7 Thermal Management Functionality

The MCH provides a thermal management method that selectively reduces read and write accesses to DRAM when the access rate crosses the predetermined thermal threshold. Read and write management operate independently; each has its own 64-bit register to control operation. Memory reads typically cause power dissipation in the DRAM chips, while memory writes typically cause power dissipation in the MCH.

5.5.7.1 Thermal Management Enabling

Thermal management may be enabled by one of two mechanisms:

- Software forcing thermal management via the SRTM (SWTM) bit
- Counter Mechanism

Mechanism one allows software to enable throttling independent of the counter mechanism. This is controlled via the Start Read/Write Thermal Management (SRTM / SWTM) bit and will put thermal management into effect (if threshold values are crossed) until the SRTM / SWTM bit is cleared. Mechanism two requires programming a specific value for Read/Write Thermal Management Mode (RTMM / WTMM), to enable use of the counter mechanism for thermal management.

When the counter mechanism is used, the number of hex words (in 32 byte chunks) read/written is counted within a global sampling window. If the number exceeds the programmed threshold, thermal management comes into effect and will remain in effect until the Read/Write Thermal Management Time (RTMT / WTMT) has expired.

5.5.7.2 Thermal Management Parameters

While the software enabling and counter mechanism settings determine *when* to thermal manage, additional bits determine *how much* to thermal manage.

Once thermal management is invoked, users can specify with precise granularity how many reads/writes to allow in a specific time period. If the programmed number of hex words is read/written within the time period, no more reads/writes will occur until the time period ends.

The detailed hexword number and time period are set in the Read/Write Thermal Management Hexword Maximum (RTMHM / WTMHM) and Read/Write Thermal Monitoring Window (RTMW / WTMW), respectively. Note that these are NOT the same as the global sampling windows mentioned above. The

global values mentioned above are used to determine whether or not to go into thermal management mode. Once thermal management is invoked, the Thermal Management Hexword Max and Thermal Monitoring Window provide finer granularity regarding the amount of reads/writes to allow.

5.5.7.3 Thermal Management Duration

As previously stated, when thermal management is enabled by the SRTM (or SWTM) bit, it will remain enabled until the SRTM (or SWTM) bit is cleared by software. Note, thermal management will only go into effect when the access thresholds are crossed.

For thermal management invoked via the counter mechanism mode, a Read/Write Thermal Management Time (RTMT / WTMT) determines how long thermal management remains in effect, once invoked. This is a multiplier of the number of global sampling windows. Therefore, if thermal management is enabled via the counter mechanism (RTMM / WTMM setting), and the number of allowable hexwords in the global sampling window is exceeded, thermal management will be in effect for a period equal to the value in RTMT times the length of time defined by the global sampling window.

5.5.7.4 Thermal Management Lock

The write thermal management control register contains lock bits, which control both the read and write registers. These lock bits can force some or all of the values in the thermal management control registers to become read-only, so no later writes can change either register until reset. Three lock modes are possible:

- Not locked
- All bits except the SRTM & SWTM are locked
- All bits including SRTM & SWTM are locked

2. CONFIG_ADDRESS Description Correction

On Page 33 of the Intel® E7501 Datasheet, section 3.4.1, the definition of Bit 31 is stated incorrectly. The table below contains the correct definition of this bit.

3.4.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address:	0CF8h Accessed as a DWord
Default Value:	00000000h
Access:	R/W
Size:	32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DWord. A Byte or Word reference will pass through the Configuration Address Register and HI_A onto the PCI_A bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CFGE).** 1 = Enable. 0 = Disable.
30:24	**Reserved.** These bits are read only and have a value of 0.
23:16	**Bus Number.** This field contains the bus number being targeted by the config cycle.
15:11	**Device Number.** This field selects one of the 32 possible devices per bus.
10:8	**Function Number.** This field selects one of 8 possible functions within a device.
7:2	**Register Number.** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to A[7:2] during HI_A-D Configuration cycles.
1:0	**Reserved**