Intel® 865PE/P Chipset

Specification Update

Intel® 82865PE/82865P Chipset Memory Controller Hub (MCH)

September 2003

Notice: The Intel® 82865PE/Intel® 82865P MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 252524

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Revision History

Rev.	Draft/Changes	Date
-001	Initial Release.	May 2003
-002	Added DC levels spec update and clarification	September 2003

Preface

This public document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 865PE/P Chipset: Intel® 82865PE/82865P Chipset Memory Controller Hub (MCH) Specification Update	252523-001

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the Intel 82865PE/82865P MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The 82865PE/82865P MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	2560h	02h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The 82865PE/82865P MCH may be identified by the following component markings:

Stepping	Q-Spec	S-Spec	Top Marking	Notes
A2	QE46	SL722	RG82865PE	

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed 82865PE and 82865P MCH steppings. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Errata that applies to this stepping.
Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Shaded: This item is either new or modified from the previous version of the document

NO.	A2	PLANS	ERRATA
1	X	NoFix	VGA Timing
2	X	Doc	DDR400 Write to Read Turnaround Latency Erratum
3	X	NoFix	FSB800 / DDR333 Running at 320 MHz Refresh Timing Erratum

NO.	SPECIFICATION CHANGES
1	Updated leakage current spec for GVREF pin.

NO.	SPECIFICATION CLARIFICATIONS
1	Added AC noise spec for VCC supply.

NO.	DOCUMENTATION CHANGES
1	VCCA_DPLL Signal Description
2	VCCA_DAC Signal Description
3	VCCA_DAC and VCCA_DPLL Electrical Characteristics

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Errata

1. VGA Timing

Products: Some VGA applications, running in 40-column modes, that use a non-black border color, may experience color/visual issues on systems configured with certain monitors.

Implication: 40-column VGA modes may experience visual color anomalies on some CRT monitors. This was observed using VGA focused Intel test software. With certain monitors, colors in active areas may change as the border color changes. As observed while using the test software, visual color anomalies can range from a slight color change difference to a blank screen. Based on the lack of customer or end user reported issues related to this erratum, the number of VGA applications that run in 40-column modes and also use non-black border colors is low. Based on Intel's validation and compatibility testing, the number of CRT monitors that exhibit this color anomaly is also low.

Workaround: No workaround exists.

Status: This will not be fixed in future steppings.

2. DDR400 Write to Read Turnaround Latency Erratum

Products: Under a specific read / write sequence with DDR400 memory, the chipset waits only 1 tCK between issuing memory write to read cycles to the same rank which violates the DDR400 device internal write to read command delay spec of 2 tCKs.

Note: DDR333/266 JEDEC device internal write to read command spec is 1 tCK.

Implication: No system or memory failures have been observed during extensive testing. However, the DDR400 device write to read spec is violated which may result in unpredictable memory device operation depending on the memory device being used.

Workaround: Please see the latest Springdale BIOS specification and specification update for details.

Status: No silicon fix planned. See latest Springdale BIOS specification update and memory reference code for details.

3. FSB800 / DDR333 Running at 320MHz Refresh Timing Erratum

Problem: When a system is configured with an 800MHz FSB processor and DDR333 DIMM(s), the chipset's memory interface operates at 320MHz. At this specific memory frequency, the chipset issues refresh cycles at a slower rate than the DDR333 JEDEC specification documents.

Chipset, with memory frequency at 320MHz, issues refresh cycles every:
8.1 µs with 256-Mb and 512-Mb memory technology
16.2 µs with 64-Mb and 128-Mb memory technology

JEDEC spec for DDR333 devices is:
7.8 µs with 256-Mb and 512-Mb memory technology
15.6 µs with 64-Mb and 128-Mb memory technology

Implication: None

Workaround: None

Status: No silicon fix planned. Intel has contacted the major memory suppliers about this issue and has modified the DDR validation specification that Intel uses to test memory. Feedback from memory suppliers is that they can meet Intel's updated DDR validation specification.

Specification Changes

1. Refer to the Intel® 82865PE/82865P Chipset MCH Datasheet Table 32, footnote 6. The footnote has been changed to: “Max leakage current spec for the GVREF pin is 65uA. Max leakage current spec for the GVSWING pin is 50uA. Refer to Intel® 865G/865GV865PE/865PChipset Platform Design Guide for the resistor divider circuit details that take this spec into account.”.

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Specification Clarifications

1. Refer to the Intel® 82865PE/82865P MCH Datasheet Table 31. Footnote 12 is added to the VCC Core Voltage supply: “For AC noise components >20MHz, the maximum allowable noise component at the MCH is +/-180mV at VCC_nom, +180/-105mV at VCC_min, and +105/-180mV at VCC_max. For AC noise components <20MHz, the sum of the DC voltage and AC noise component must be within the spec'd DC min/max operating range.”

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Documentation Changes

1. VCCA_DPLL Signal Description

In Section 2.9, “Power and Ground Signals”, replace the VCCA_DPLL table row with the following:

VCCA_DPLL	Refer to the *Intel® 865G/865PE/865P Chipset Platform Design Guide* for details on how these supply pins should be connected.

2. VCCA_DAC Signal Description

In Section 2.9, “Power and Ground Signals”, replace the VCCA_DAC table row with the following:

VCCA_DAC	Refer to the *Intel® 865G/865PE/865P Chipset Platform Design Guide* for details on how these supply pins should be connected.

3. VCCA_DAC and VCCA_DPLL Electrical Characteristics

The VCCA_DAC and VCCA_DPLL electrical characteristics are not part of the 82865PE/82865P MCH and should be removed from Chapter 6, “Electrical Characteristics”. The following changes should be made:

- Table 28, “Absolute Maximum Ratings”. Remove 2 rows from this table. Remove the row with VCCA_DAC in the “Symbol” column and the row with VCCA_DPLL in the “Symbol” column.
- Table 29, “Power Characteristics”. Remove 2 rows from this table. Remove the row with I_{VCCA_DAC} in the “Symbol” column and the row with I_{VCCA_DPLL} in the “Symbol” column.
- Table 31, “DC Operating Characteritics”. Remove 2 rows from this table. Remove the row with VCCA_DAC in the “Signal Name” column and the row with VCCA_DPLL in the “Signal Name” column.