Intel® 848P Chipset

Specification Update

Intel® 82848P Memory Controller Hub (MCH)

August 2003

Notice: The Intel® 82848P MCH may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 253642-001

Contents

Revision History

Revision History	Description	Date
-001	Initial Release.	August 2003

Preface

This public document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents.

Affected Documents/Related Documents

Document Title	Document Number
Intel® 848P Chipset: Intel® 82848P Memory Controller Hub (MCH) Datasheet	253575-001

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the Intel 82848P MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Component Identification via Programming Interface

The 82848P MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
A2	8086h	2560h	02h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The 82848P MCH may be identified by the following component markings:

Stepping	Q-Spec	S-Spec	Top Marking	Notes
A2	QE58	SL77Y	RG82848P	

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes that apply to the listed 82848P MCH steppings. Intel may intend to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

X:	Errata that applies to this stepping.
Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Shaded: This item is either new or modified from the previous version of the document

NO.	A2	PLANS	ERRATA
1	X	Doc	DDR400 Write to Read Turnaround Latency Erratum
2	X	NoFix	FSB800 / DDR333 Running at 320 MHz Refresh Timing Erratum

NO.	SPECIFICATION CHANGES
	There are no specification changes in this Specification Update revision.

NO.	SPECIFICATION CLARIFICATIONS
	There are no specification clarifications in this Specification Update revision.

NO.	DOCUMENTATION CHANGES
	There are no documentation changes in this Specification Update revision.

This page is intentionally left blank.

Errata

1. DDR400 Write to Read Turnaround Latency Erratum

Problem: Under a specific read / write sequence with DDR400 memory, the chipset waits only 1 tCK between issuing memory write to read cycles to the same rank which violates the DDR400 device internal write to read command delay spec of 2 tCKs.

Note: DDR333/266 JEDEC device internal write to read command spec is 1 tCK.

Implication: No system or memory failures have been observed during extensive testing. However, the DDR400 device write to read spec is violated which may result in unpredictable memory device operation depending on the memory device being used.

Workaround: See the latest BIOS specification and specification update for details.

Status: No silicon fix planned. See latest BIOS specification update and memory reference code for details.

2. FSB800 / DDR333 Running at 320 MHz Refresh Timing Erratum

Problem: When a system is configured with an 800 MHz FSB processor and DDR333 DIMM(s), the chipset's memory interface operates at 320 MHz. At this specific memory frequency, the chipset issues refresh cycles at a slower rate than the DDR333 JEDEC specification documents.

Chipset, with memory frequency at 320 MHz, issues refresh cycles every:
8.1 µs with 256-Mb and 512-Mb memory technology
16.2 µs with 64-Mb and 128-Mb memory technology

JEDEC spec for DDR333 devices is:
7.8 µs with 256-Mb and 512-Mb memory technology
15.6 µs with 64-Mb and 128-Mb memory technology

Implication: None

Workaround: None

Status: No silicon fix planned. Intel has contacted the major memory suppliers about this issue and has modified the DDR validation specification that Intel uses to test memory. Feedback from memory suppliers is that they can meet Intel's updated DDR validation specification

This page is intentionally left blank.

Specification Changes

There are no specification changes in this Specification Update revision.

This page is intentionally left blank.

Specification Clarifications

There are no specification claraifications in this Specification Update revision.

This page is intentionally left blank.

Documentation Changes

There are no documentation changes in this Specification Update revision.