Intel® 82801E Communications I/O Controller Hub (C-ICH)

Specification Update

January, 2002

Notice: The Intel® 82801E Communications I/O Controller Hub (C-ICH) product may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 273645-002

Contents

Revision History

Revision	Description	Date
-002	Updated doc changes section. Updated Spec Clarifications.	January 2002
-001	First release of the 82801E C-ICH specification update to FDBL.	December 2001

Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Order
Intel® 82801E Communications I/O Controller Hub (C-ICH) Datasheet	273598
Intel® 82801E Communications I/O Controller Hub (C-ICH) Developer's Manual	273599

Nomenclature

Errata are design defects or errors. Errata may cause the Intel® 82801E Communications I/O Controller Hub behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

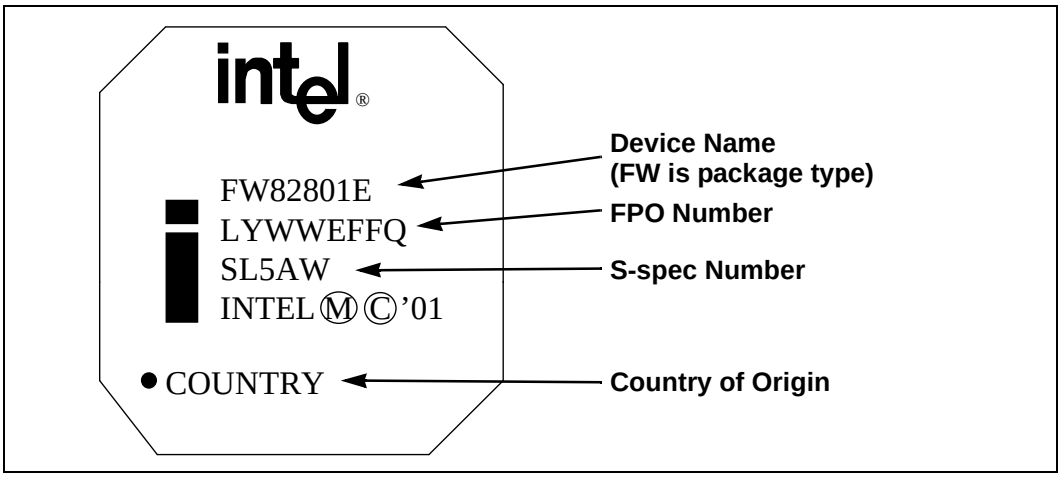
Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Identification Information

Markings

Topside Markings



C-ICH Stepping	S-Spec	Top Marking	Notes
C-ICH A0	Q255	FW82801E Q255	Engineering Sample
C-ICH A0	SL5AW	FW82801E SL5AW	Production version

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel® 82801E Communications I/O Controller Hub. Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification applies to this stepping.
(No mark) or (Blank box):	This Erratum, Specification Change or Specification Clarification is fixed in the listed stepping or does not apply.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Table Row

	A change bar to the left of a table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Errata Number	Stepping	Status	Page	ERRATA
	A0			
1	X	No Fix	9	Inadvertent Setting of C-ICH SMBus BYTE_DONE_STS Bit
2	X	No Fix	9	Top Block Swap and Delayed Transaction
3	X	No Fix	9	Hub Interface Parity Error Response
4	X	No Fix	9	LPC Signaled Target Abort Generation
5	X	No Fix	10	USB Handshake
6	X	No Fix	10	Frequency Strap
7	X	No Fix	10	USB Rise Fall Matching (Trfm)
8	X	No Fix	10	DMA Mode-0
9	X	No Fix	11	Parity Error
10	X	No Fix	11	Special Cycle Non-Zero Address
11	X	No Fix	11	TRDY# Behavior
12	X	No Fix	11	LAN Microcontroller PCI Protocol Violation
13	X	No Fix	12	SM Bus Arbitration
14	X	No Fix	12	I2C Read Command Issue
15	X	No Fix	12	PERR# Detection Issue
16	X	No Fix	12	PERR# Response Issue

Specification Changes

Number	Affected Document	SPECIFICATION CHANGES
1	273599	DMA Mode-0 Not Supported

Specification Clarifications

Number	Affected Document	SPECIFICATION CLARIFICATIONS
1	273599	Clarification of Alternate Access Mode Usage for Timer (8254)
2	273599	GPE Event Handling under ACPI
3	273599	Virtual Wire Mode B Usage on the Intel® C-ICH
4	273599	APIC Controller Behavior Clarification
5	273599	IDE Hot Swap
6	273599	Power Management

Documentation Changes

No.	Affected Document	DOCUMENTATION CHANGES
1	273599	PCI Device Revision ID Table Added

Errata

1. Inadvertent Setting of C-ICH SMBus BYTE_DONE_STS Bit

Issue: The C-ICH may inadvertently set the BYTE_DONE_STS bit, in the SMBus Host Status register, when the INTR bit for the n+1 interrupt is set at the end of a block write transfer of two bytes or more.

Implication: The C-ICH will hang the next attempted transfer causing an SMBus lockup if this BYTE_DONE_STS bit is not cleared before the next attempted transfer. This can result in a system lock-up requiring an AC power-cycle to recover from.

Workaround: Ensure that a 1 is written to the BYTE_DONE_STS bit at the same time the INTR bit (both in the SMBus Host Status register) is being cleared for the "n+1" interrupt, regardless if interrupts are used or not.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

2. Top Block Swap and Delayed Transaction

Issue: The Top Block Swap feature of the C-ICH doesn't work correctly if the PCI Delayed Transaction feature is enabled.

Implication: Re-programming the Boot Block of the FWH will fail if the Top Block Swap feature is used with Delayed Transactions enabled.

Workaround: When updating BIOS, disable Delayed Transactions by clearing the DTE bit (D31:F0, offset D0h, bit 1) before setting the TOP_SWAP bit (D31:F0, offset D4h, bit 13). After the update is completed and verified, re-enable Delayed Transactions by setting DTE after clearing TOP_SWAP.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

3. Hub Interface Parity Error Response

Problem: The C-ICH does not generate a valid Hub Interface Parity message when Parity Error Response is disabled for the Hub/PCI Bridge function.

Implication: System hang if Hub Interface Parity Error Response is enabled in the MCH when it is disabled in the C-ICH. This issue only affects platforms in which the MCH supports Hub Interface Parity checking. The issue has only been observed with the Linux* OS.

Workaround: Software must not disable Hub Interface Parity Error Response in the ICH while it is enabled in the MCH.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

4. LPC Signaled Target Abort Generation

Problem: If there is a downstream I/O cycle followed by posted memory writes, both targeted towards PCI with different BE#s and with Delayed Transaction enabled (D31:F0;GEN_CNTL(D0-D3h):[1]), the C-ICH can erroneously set the STA bit (bit-11) in D31:F0;PCISTS configuration space even though there is no Target Abort on the PCI bus. This has only been observed on DP systems.

Implication: The STA bit in D31:F0;PCISTS is incorrectly set. No NMI or SERR# will be generated due to the STA bit being set. Software which polls this STA bit may incorrectly indicate a Target Abort has occurred.

Workaround: There are two possible workarounds:

1. Ignore the STA bit (bit-11) in D31:F0;PCISTS(06-07h) when Delayed Transaction is enabled. The D30:F0;SECSTS(1E-1Fh):[RTA (bit-12)] bit remains an accurate reflection of downstream cycles towards PCI that get Target Aborted.
2. Disable Delayed Transaction (which may induce a performance penalty on PCI)

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

5. USB Handshake

Problem: The C-ICH UHCI will fail to provide a handshake if it receives an incoming data packet where CRC has five consecutive ones in the least significant bit of CRC and is immediately followed by an EOP for Bulk, Interrupt, and Isoc transfers ONLY IF a K-state is being signalled on the other port at the time of this EOP. This behavior, to date, has only been observed during artificial testing procedures.

Implication: USB devices may stall. The OS will attempt to recover, but if it fails to do, an error message will be displayed.

Workaround: None. The user may have to unplug then re-install the USB device that has stalled.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

6. Frequency Strap

Problem: The C-ICH will not drive the CPU frequency straps signal (A20M#, INTR, NMI, IGNNE#) to 1's as VCC comes up prior to PWROK assertion (t184). The C-ICH drives these signals to 0 instead.

Implication: No implication to qualification and productions processors as they drive their own "start" straps internally. Implication to pre-qual processors is that the "start ratio" may be set to an illegal value and the system may not boot.

Workaround: (Not required for systems using qualification or production processors)

1. Re-implement Legacy mux that drives 1's prior to PWROK.
2. Place a 1.2 ms RC delay on CPUPWRGD so that it asserts when the C-ICH Run ratio Freq Strap values are present.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

7. USB Rise Fall Matching (Trfm)

Problem: The USB Specification defines a rise/fall time matching (Trfm) which is calculated by dividing rise time by fall time (Tr/Tf). The C-ICH does not meet this specification.

Implication: This erratum will result in a lower crossover voltage which is still within the specification (Vcrs)

Workaround: None

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

8. DMA Mode-0

Problem: If a device on one of the IDE interfaces, such as the secondary channel, is operating in Multi-Word DMA Mode with compatible timings where the cycle time is 600 ns, while a device on the other interface (primary channel), is running in PIO mode, the IDE PIO prefetch buffer will inadvertently provide an extra piece of secondary channel data to the primary device, resulting in data corruption. This happens when DMAREQ is deasserted and a DMA transaction is running while a PIO transaction is outstanding on the other channel. Note that DMA Mode-0 is an unsupported mode of the C-ICH.

Implication: Systems configured in this manner may experience a situation in which the DMA IDE controller transfers incorrect data from the PIO configured device. Exactly how this manifests itself in a system is dependent on the system activity at that time.

Workaround: When BIOS is determining which mode(s) an IDE device is capable of, it must not set the DMA capable bits in the C-ICH if that device only supports Mode-0 DMA or slower. That device should be configured for PIO instead.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

9. Parity Error

Problem: When enabled, a Parity Error will not be signaled or detected, via either D30:F0;1Eh bit-8 or D31:F0;06h bit-8 (SECSTS:[DPD] or PD_STS:[DPD]), if two Double-Word up-bound writes are followed by a down-bound read. Neither PERR# will be asserted, nor the indicated status bits will be set, resulting in failure to generate NMI or SMI. Note that the Hub I/F Parity Error detect mechanism remains fully functional with regards to this erratum.

Implication: This results in loss of indication to PCI target and system software when bad PCI data is received. This could result in data corruption to either memory or hard drive data.

Workaround: None.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

10. Special Cycle Non-Zero Address

Problem: Special Cycles immediately followed by any cycle(s) (within three Hub I/F clocks) may result in the C-ICH driving non-zero data during the address phase of the special cycle The PCI specification only requires that stable data be driven during the address phase; it does not require that it be 0x0h data.

Implication: Non-PCI compliant devices may attempt to claim this special cycle and it may not function properly. This has only been seen on one PCI graphics card, which is no longer produced.

Workaround: None.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

11. TRDY# Behavior

Problem: The C-ICH may not assert TRDY# for more than 16 PCI clocks (up-to 32 clocks) after a bus master asserts FRAME# if there are no other masters requesting the bus. This behavior is inconsistent with its Sub-class code of a PCI-to-PCI Bridge device.

Implication: The C-ICH may not respond with a data phase within 16 PCI clocks, as required by the *PCI Specification*. This has not been found to cause any functional problems. Since prior generations of chipsets were required to meet 32 clock requirements for a Host-to-PCI Bridge, PCI adapters that worked in these systems should also work in a C-ICH based system.

Workaround: None.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

12. LAN Microcontroller PCI Protocol Violation

Problem: When the C-ICH (using the 82562ET PLC) is receiving large files from a peer LAN device using the 10 Mbps data rate, the C-ICH can cause a system lock-up. Specifically, if the LAN controller has Standby Enable set (EEPROM Word 0Ah bit-1 = 1), while receiving large files using the 10 Mbps data rate and receives a CU_RESUME command when it is just entering IDLE state, the C-ICH will cause a PCI protocol violation (typically by asserting FRAME# and IRDY# together) within the next few PCI cycles. This will cause the PCI bus to lock-up, further resulting in system lock-up.

Implication: Large file transfers to the C-ICH using 10 Mbps can cause the receiving system to lock-up.

Workaround: Clear EEPROM Word 0Ah bit-1 to 0. This will result in an increase power consumption of the C-ICH of ~ 40 mW.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

13. SM Bus Arbitration

Problem: The C-ICH will not detect a bus collision when attempting to STOP at the end of a SM Bus transaction as a master. If there is another external Bus Master attempting to access the bus at the same time and wins the arbitration during STOP bit, the C-ICH may not set the Bus Error bit.

Implication: A master attempting a transfer that had actually "lost" may think that its transaction was completed.

Workaround: None.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

14. I2C Read Command Issue

Problem: The C-ICH uses the HST_D0 register (Dev31, Func 3, Offset 05h) as the byte count register instead of depending on the LAST_BYTE bit in the Host Control register (Dev 31, Func 3, Offset 02h:[bit-5]) to end the transaction.

Implication: The transaction will stop pre-maturely if HST_D0 contains a number smaller than the intended transaction.

Workaround: No workaround for 10-bit addressing I2C devices. Can use the SM Bus read command for 7-bit addressing of I2C devices.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

15. PERR# Detection Issue

Problem: The C-ICH's Detected Parity Error (DPE) bit in SECSTS register (D30:F0, offset 1Eh: bit-15) and PD_STS register (D31:F0, offset 06h: bit-15) will get set when PERR# is asserted by external PCI devices. This issue was found during ongoing validation using a synthetic test environment and there have been no failures reported by customers.

Implication: DPE bit of SECSTS and PCISTA may erroneously get set.

Workaround: BIOS needs to clear DPE of SECSTS and PCISTA when those bits are set.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

16. PERR# Response Issue

Problem: If the C-ICH's Parity Error Response Enable (PER) bit in Bridge_CNT register (D30:F0, offset 3Eh: bit-0) is disabled (default), it will block PERR# from being asserted when data parity error is detected on PCI bus during LPC or legacy DMA master read cycles, or when the C-ICH is the target for write cycles to Device 31 Functions 0 and 3. This bit should only block PERR# from being asserted when a PCI data parity error is detected during PCI-to-memory writes or CPU-to-PCI read cycles. This issue was found during ongoing internal validation using a synthetic test environment and there have been no failures reported by customers.

Implication: PERR# will not be asserted when PCI Parity Error detected during LPC or legacy DMA master read cycles, or when the C-ICH is the target for write cycles to Device 31 Functions 0 and 3.

Workaround: BIOS needs to set PER of Bridge_CNT when the parity error detection is supported on LPC or legacy DMA.

Status: See the "Summary Table of Changes" on page 7 for the status of this erratum.

Specification Changes

1. DMA Mode-0 Not Supported

Issue: DMA Mode-0 is not supported by the C-ICH.

Affected Docs: *Intel® 82801E Communications I/O Controller Hub (C-ICH) Developer's Manual*

Specification Clarifications

1. Clarification of Alternate Access Mode Usage for Timer (8254)

Issue: If the ALT Access Mode is entered and exited after reading the registers of the C-ICH timer (8254), the timer starts counting faster (13.5 ms). The following steps listed below can cause problems:

1. BIOS enters ALT Access Mode for reading the C-ICH timer related registers.
2. BIOS exits ALT Access Mode.
3. BIOS continues through the execution of other needed steps and passes control to the OS.

After getting control in step #3, if the OS does not reprogram the system timer again the timer ticks may be happening faster than expected. For example DOS and its associated software assume that the system timer is running at 54.6 ms and as a result the timeouts in the software may be happening faster than expected.

For some other OS's, such as DOS, the BIOS should restore the timer back to 54.6 ms before passing control to the OS. If the BIOS is entering ALT Access Mode before entering the suspend state it is not necessary to restore the timer contents after the exit from ALT Access Mode.

Affected Docs: *Intel® 82801E Communications I/O Controller Hub (C-ICH) Developer's Manual*

2. GPE Event Handling under ACPI

Issue: The C-ICH uses the same GPE1_EN register (I/O address: PMBase+2EH) to enable/disable both SMI and ACPI SCI general purpose input events. APCI OS assumes that it owns the entire GPE1_EN register per ACPI spec. Problems arise when some of the general-purpose inputs are enabled as SMI by BIOS, and some of the general purpose inputs are enabled for SCI. In this case, ACPI OS turns off the enabled bit for any GPIx input signals that are not indicated as SCI general-purpose events at boot, and exit from sleeping states.

Affected Docs: *Intel® 82801E Communications I/O Controller Hub (C-ICH) Developer's Manual*

3. Virtual Wire Mode B Usage on the Intel® C-ICH

Issue: When an I/O APIC based system is configured in Virtual Wire Mode B with edge triggered interrupt delivery on the I/O APIC input pin INITIN_0 (INTR output from the 8259), a high priority interrupt occurring just as the C-ICH receives INTACK for a preceding low-priority interrupt can cause an unusually small interrupt de-assertion on INTR signal which can be missed at either the I/O APIC or the processor, depending on the configuration, and most likely cause a system hang.

The unusually small interrupt de-assertion time does not meet the input minimum specifications for the device receiving this signal. This may result in a system lockup.

When using Virtual Wire Mode B, where the INTR output of the 8259 is routed to the I/O APIC INTIN_0, software must program the I/O APIC redirection table entry 0, Trigger Mode (bit-15 of redirection table) to Level Sensitive, rather than Edge Sensitive. This may result in infrequent spurious interrupts which should have minimal adverse impact on system performance.

Another consideration is to use Virtual Wire Mode A with the local APICs set to Level Trigger.

Affected Docs: *Intel® 82801E Communications I/O Controller Hub (C-ICH) Developer's Manual*

4. APIC Controller Behavior Clarification

Issue: Section 3.8.5 (APIC) describes the APIC controller behavior.

The local APIC (in the processor) has a delivery mode option to interpret Processor Side Bus (PSB) messages as an SMI in which case the processor treats the incoming interrupt as an SMI instead of as an interrupt. This does not mean that the C-ICH has any way to have an SMI source from the power management logic cause the I/O APIC to send an SMI message - there is no way to do this. The C-ICH's I/O APIC can only send interrupts due to interrupts which do not include SMI, NMI or INIT. This means that in IA32/IA64 based platforms, PSB interrupt message format delivery modes 010 (SMI/PMI), 100 (NMI), and 101 (INIT), must not be used and is not supported. Only the hardware pin connection is supported by C-ICH.

Affected Docs: *Intel® 82801E Communications I/O Controller Hub (C-ICH) Developer's Manual*

5. IDE Hot Swap

Issue: In an IDE Hot Swap Operation an IDE device is removed and a new one inserted while the IDE interface is powered down and the rest of the system is in a fully powered-on state (S0). During an IDE Hot Swap, if the OS executes cycles to the IDE interface after it has been powered down, which causes the C-ICH to hang the system waiting for IORDY to be asserted from the drive.

To correct this issue, the following BIOS procedures are required prior to performing an IDE Hot Swap:

1. Program IDE SIG_MODE (configuration register 54h) to 10b (Drive Low mode).
2. Clear IORDY Sample Point Enable (bits 1 or 5 of IDE Timing register).

This will prevent the C-ICH from not waiting for IORDY assertion when the OS accesses an IDE device after the IDE drive powers down, and ensure that zeros will always be returned for read cycles that occur during a hot swap operation.

Affected Docs: *Intel® 82801E Communications I/O Controller Hub (C-ICH) Developer's Manual*

6. Power Management

Issue: The 82801E C-ICH is an "on" or "off" device; it does not support power management features or sleep states. The following functions, mechanisms and signals are not supported.

- Wake Events
- Suspend Power Planes
- Sleep Lines/States s1, s2, s3, s4, s5
- SUS_STAT#
- PME#
- SLP_S3#
- SLP_S5#
- PWRBTN# (Soft Off/g2, s5)

Note: Care must be taken to properly set and disable Power Management Status/Enable and control registers in the OS and BIOS.

Affected Docs: *Intel® 82801E Communications I/O Controller Hub (C-ICH) Developer's Manual*

Documentation Changes

1. PCI Device Revision ID Table Added

Issue: PCI Revision ID Register Values (PCI Offset 08h) for all C-ICH functions are shown below. This information is not listed in the datasheet or developer's manual. This is the standard reference document.

Table 1. Revision ID Table

Function	C-ICH A0
D8:F0	0
D30:F0	0
D31:F1	0
D31:F2	0
D31:F3	0
D31:F4	0
D31:F5	0
D31:F6	0

Note: From a software perspective, the integrated LAN Controller (D8:F0) appears to reside on the secondary side of the C-ICH's virtual PCI-to-PCI Bridge. This is typically Bus 1, but may be assigned a different number, depending upon system configuration.

Note: The C-ICH's integrated LAN Controller (D8:F0) provides support for configurable Subsystem ID and Subsystem Vendor ID fields. After reset, the LAN Controller automatically reads addresses Ah through Ch of the EEPROM. The LAN Controller checks bits 15:13 in the EEPROM word Ah.

Affected Docs: *Intel® 82801E Communications I/O Controller Hub (C-ICH) Developer's Manual*