# Intel® 440BX AGPset: 82443BX Host Bridge/Controller

## Specification Update

*January 2001*

**Notice:** The Intel® 82443BX AGPset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Document Number: 290639-006

# Contents

# Revision History

| Rev. | Draft/Changes | Date |
|---|---|---|
| -001 | Initial Release | May 1998 |
| -002 | Added Specification Changes #2 and #3 | July 1998 |
| -003 | Added Specification Changes #4, #5 and C1 Stepping Information | October 1998 |
| -004 | Added Documentation Change #1 | November 1998 |
| -005 | Added Documentation Change #2 | April 1999 |
| -006 | Renumbered Specifiation Changes and added Specification Changes #3, 4, 5B–12, 17, & 18. Renumbered Errata and added errata 1–9. Added Specification Clarifications 1–11. Renumbered Documentation Changes and added Documentation Changes 1–2. | January 2001 |

# Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

### Affected Documents/Related Documents

| Document Title | Document Number |
|---|---|
| *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet | 290633-001 |
| *82443BX Host Bridge/Controller Electrical and Thermal Timing Specification* datasheet addendum | 273219-002 |

## Nomenclature

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

**Errata** are design defects or errors. Errata may cause the Intel® 82443BX, behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

# Component Identification via Programming Interface

The Intel® 82443BX may be identified by the following register contents:

| Stepping | Vendor ID[1] | Device ID[2] | Revision Number[3] |
|---|---|---|---|
| A-0 | 8086h | 7190h/7192h | 00h |
| B-0 | 8086h | 7190h/7192h | 01h |
| B-1 | 8086h | 7190h/7192h | 02h |
| C-0 | 8086h | 7190h/7192h | 03h |
| C-1 | 8086h | 7190h/7192h | 03h (note 4) |

**NOTES:**

1. The Vendor ID corresponds to bits 15-0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15-0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space. The default value is 7190h. When AGP is disabled, the value is 7192h.
3. The Revision Number corresponds to bits 7-0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.
4. The C-0 step device never entered production. As a result the C-1 step revision number ID remains 03h.

# Component Marking Information

The Intel 82443BX may be identified by the following component markings:

| Stepping | S-Spec | Top Marking | Freq. | Notes |
|---|---|---|---|---|
| A-0 | | FW82443BX<br>Q575ES | 100/66 | Engineering Sample, FM Test |
| A-0 | | FW82443BX<br>~~Q575ES~~<br>Q607ES-100(1) | 100 | Engineering Sample, FM Test Remarked Q575ES with Q607ES-100 |
| A-0 | | FW82443BX<br>Q607ES-100 | 100 | Engineering Sample, FM Test |
| A-0 | | FW82443BX<br>~~Q575ES~~<br>Q608ES-66(1) | 66 | Engineering Sample, FM Test Remarked Q575ES with Q608ES-66 |
| A-0 | | FW82443BX<br>Q608ES-66 | 66 | Engineering Sample, FM Test |
| B-0 | | FW82443BX<br>Q578ES | 100/66 | Engineering Sample, FM Test |
| B-0 | | FW82443BX<br>Q577ES | 100/66 | Engineering Sample, FM Test |
| B-0 | | FW82443BX<br>Q579ES | 100/66 | Engineering Sample, T03 Test with Burn-In |
| B-1 | | FW82443BX<br>Q628ES | 100/66 | Engineering Sample, FM Test |

| Stepping | S-Spec | Top Marking | Freq. | Notes |
|---|---|---|---|---|
| B-1 | | FW82443BX Q629ES | 100/66 | Engineering Sample, FM Test |
| B-1 | | FW82443BX Q630ES | 100/66 | Engineering Sample, T03 Test with Burn-In Full Production Flow |
| B-1 | SL2T5 | FW82443BX SL2T5 | 100/66 | 82443BX B-1 Production ASSY |
| B-1 | SL2T6 | FW82443BX SL2T6 | 100/66 | 82443BX B-1 Remnants |
| C-0 | SL2VH | FW82443BX SL2VH | 100/66 | 82443BX C-0 Production ASSY |
| C-1 | SL2VH(2) | FW82443BX SL2VH | 100/66 | 82443BX C-1 Production ASSY |
| C-1 | SL378 | FW82443BX SL378 | 100/66 | 82443BX C-1 Remnants |

**NOTES:**

1. Pound signs (######) are used over “Q57ES” on components instead of the “strike-through” lines that are shown.
2. The C-0 Step SL2VH device never entered production and was never sampled to customers. As a result, the C-1 step S-Spec remains SL2VH.

# Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes which apply to the listed Intel 82443BX steppings. Intel intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

### Codes Used in Summary Table

| | |
|---|---|
| X: | Erratum, Specification Change or Clarification that applies to this stepping. |
| Doc: | Document change or update that will be implemented. |
| Fix: | This erratum is intended to be fixed in a future stepping of the component. |
| Fixed: | This erratum has been previously fixed. |
| NoFix | There are no plans to fix this erratum. |
| (No mark) or (Blank Box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |
| Shaded: | This item is either new or modified from the previous version of the document. |

| Number | Steppings | | | | | | SPECIFICATION CHANGES |
|---|---|---|---|---|---|---|---|
| | A0 | B0 | B1 | C0 | C1 | | |
| 1 | X | X | X | X | X | | PCI Configuration Register 50-53, Bits 12 & 13(1) |
| 2 | X | X | X | X | X | | AGP Reads Outside of the AGP Aperture(1) |
| 3 | | X | X | X | X | | Memory Buffer Strength Control Register |
| 4 | | X | X | X | X | | Memory Buffer Frequency Select Register |
| 5A | X | X | X | X | X | | Processor PLL Lock Time Affects Intel® 82443BX |
| 5B | | X | X | X | X | | DRAM Write Thermal Throttling Control Register |
| 6 | | X | X | X | X | | DRAM Read Thermal Throttling Control Register |
| 7 | | X | X | X | X | | Error Command Register |
| 8 | | X | X | X | X | | Error Status Register |
| 9 | | X | X | X | X | | DCLKRD (Pin AB22) Changed to No Connect(1) |
| 10 | | X | X | X | X | | Reserved Straps |
| 11 | | X | X | X | X | | MAB13 Polarity Change |
| 12 | | X | X | X | X | | SERR# on Target Abort(1) |
| 13 | X | X | X | X | X | | Abort Disable Test Mode Configuration Bits |
| 14 | X | X | X | X | X | | Selective Auto Precharge |

| Number | Steppings | | | | | | SPECIFICATION CHANGES |
|---|---|---|---|---|---|---|---|
| | A0 | B0 | B1 | C0 | C1 | | |
| 15 | X | X | X | X | X | | Memory Data Buffer Strength Programming |
| 16 | X | X | X | X | X | | Intel® 82443BX Host Bridge/Controller NAND Tree Testing |
| 17 | N/A | N/A | N/A | N/A | N/A | | GTL+Termination Voltage (Mobile Only) |
| 18 | N/A | N/A | N/A | N/A | N/A | | Undershoot Specification Changed to –750 mV (Mobile Only) |

**NOTES:**

1. This specification change has been incorporated into the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet, and has been removed from this document.

| Number | Steppings | | | | | | Plans | ERRATA |
|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | B1 | C0 | C1 | | | |
| 1 | X | | | | | | FIX | Locked Cycle Retry |
| 2 | X | | | | | | FIX | Error Address Pointer Register |
| 3 | X | | | | | | FIX | AGP Read/Write Cycles with Auto Precharge Enabled |
| 4 | X | | | | | | FIX | Global SMRAM Enable Bit |
| 5 | X | | | | | | FIX | MAB11# during MRS Command |
| 6 | X | | | | | | FIX | PCI Memory Read Line |
| 7 | X | | | | | | FIX | PLL Operation at 100 MHz |
| 8 | X | X | | | | | FIX | Snoop Ahead |
| 9 | | X | | | | | FIX | Power Dissipation |
| 10 | X | X | X | | | | FIX | Hard Reset Collision with Refresh |
| 11 | X | X | X | | | | FIX | IPDLT Bit Setting |
| 12 | X | X | X | | | | FIX | SDRAM Suspend Refresh |
| 13 | X | X | X | | | | FIX | Refresh Collision with SUS_STAT# Assertion (EDO Memory) |

| Number | SPECIFICATION CLARIFICATIONS |
|---|---|
| 1 | Normal Refresh Enable |
| 2 | CKE Function with Registered DIMMs |
| 3 | Memory Initialization with ECC Enabled |
| 4 | DCLKO State during POS/STR |
| 5 | DCLKRD Pin Is Connected to NAND Chain |
| 6 | Modifying DRAM Configuration Registers during DRAM Cycles |
| 7 | Side Band Addressing Signals Float before SBA Enable Is Set |
| 8 | 128-Mbit Technology SDRAM Memory Use |
| 9 | HCLKIN Lead Time to PCLKIN Timing |
| 10 | MBSC – Memory Buffer Strength Control Register (Device 0), Address Offset 69-6Eh |
| 11 | Multi-Bit Memory Error Clarification |

| Number | DOCUMENTATION CHANGES |
|---|---|
| 1 | Correct Intel® 82443BX Simplified Block Diagram |
| 2 | Note 3, Table 3-1 |
| 3 | Page iii, Features List Is Changed |

# Specification Changes

## 1. PCI Configuration Register 50-53, Bits 12 & 13

This specification change has been incorporated into the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet.

## 2. AGP Reads Outside of the AGP Aperture

This specification change has been incorporated into the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet.

## 3. Memory Buffer Strength Control (MBSC) Register

The following register definition is for the B-0, B-1 and C-0 steppings of the 82443BX.

**MBSC—Memory Buffer Strength Control Register**
Address Offset: 69–6Eh
Default Value: 000000000000h
Access: Read/Write

This register programs the various DRAM interface signal buffer strengths, based on non-mixed memory configurations of DRAM type (EDO or SDRAM), DRAM density (x8, x16, or x32), DRAM technology (16 Mb or 64 Mb), and rows populated. Note that x4 DRAM may only be supported when used on registered DIMMs.

| Bit | Description |
|---|---|
| 47:40 | Reserved |
| 39:38 | **MAA[13:0], WEA#, SRASA#, SCASA# Buffer Strengths.** This field sets the buffer strength for the MAA[13:0], WEA#, SRASA#, SCASA# pins.<br>Value — Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz & 100 MHz |
| 37:36 | **MAB[13:11, 9:0]# & MAB10, WEB#, SRASB#, SCASB# Buffer Strengths.** This field sets the buffer strength for MAB[13:11, 9:0]# & MAB10, WEB#, SRASB#,SCASB# pins.<br>Note: The address's MAB[13:11, 9:0]# are inverted copies of MAA[13:0], with the exception of MAB10.<br>Value — Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz & 100 MHz |

| Bit | Description |
|---|---|
| 35:34 | **MD [63:0] Buffer Strength Control 2.**<br><br>**4 DIMM (FET) Configuration:** This field sets the buffer strength for the MD[63:0] path that is connected to DIMM2 and DIMM3. The buffer strength is programmable based upon the SDRAM load in detected in DIMM slots 2&3. This path is enabled when FENA is asserted (High) by the 443BX.<br><br>**3 DIMM & 4 DIMM (No FET)Configuration:** This field should be programmed to the same value as MD[63:0] Buffer Strength Control 1. This buffer strength is programmable based upon the SDRAM load in detected in all 3 DIMM connectors.<br><br>Value Buffer Strength<br><br>00 1x 66 MHz & 100 MHz<br>01 Reserved Invalid setting for 66 MHz and 100 MHz<br>10 2x 66 MHz & 100 MHz<br>11 3x 100 MHz Only |
| 33:32 | **MD [63:0] Buffer Strength Control 1.**<br><br>**4 DIMM (FET) Configuration:** This field sets the buffer strength for the MD[63:0] path that is connected to DIMM0 and DIMM1. The buffer strength is programmable based upon the SDRAM load in detected in DIMM slots 0&1. This path is enabled when FENA is de-asserted (Low) by the 443BX.<br><br>**3 DIMM & 4 DIMM (No FET) Configuration:** The buffer strength is programmable based upon the SDRAM load in detected in all 3 DIMM connectors.<br><br>Value Buffer Strength<br><br>00 1x 66 MHz & 100 MHz<br>01 Reserved Invalid setting for 66 MHz and 100 MHz<br>10 2x 66 MHz & 100 MHz<br>11 3x 100 MHz Only |
| 31:30 | **MECC [7:0] Buffer Strength Control 2.**<br><br>**4 DIMM (FET) Configuration:** This field sets the buffer strength for the MECC[7:0] path that is connected to DIMM2 and DIMM3 The buffer strength is programmable based upon the SDRAM ECC load detected in DIMM slots 2&3. This path is enabled when FENA is asserted (High) by the 443BX.<br><br>**3 DIMM & 4 DIMM (No FET)Configuration:** This field should be programmed to the same value as MECC[7:0] Buffer Strength Control 1. This buffer strength is programmable based upon the SDRAM load detected in all 3 DIMM connectors.<br><br>Value Buffer Strength<br><br>00 1x 66 MHz & 100 MHz<br>01 Reserved Invalid setting for 66 MHz and 100 MHz<br>10 2x 66 MHz & 100 MHz<br>11 3x 100 MHz Only |
| 29:28 | **MECC [7:0] Buffer Strength Control 1.**<br><br>**4 DIMM (FET) Configuration:** This field sets the buffer strength for the MECC[7:0] path that is connected to DIMM0 and DIMM1. The buffer strength is programmable based upon the SDRAM ECC load detected in DIMM slots 0&1. This path is enabled when FENA is de-asserted (High) by the 443BX.<br><br>**3 DIMM & 4 DIMM (No FET) Configuration:** The buffer strength is programmable based upon the SDRAM ECC load detected in all 3 DIMM slots.<br><br>Value Buffer Strength<br><br>00 1x 66 MHz & 100 MHz<br>01 Reserved Invalid setting for 66 MHz and 100 MHz<br>10 2x 66 MHz & 100 MHz<br>11 3x 100 MHz Only |

| Bit | Description |
|---|---|
| 27:26 | **CSB7#/CKE5 Buffer Strength.** This field sets the buffer strength for CSB7#/CKE5 pins.<br>Value / Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz & 100 MHz |
| 25:24 | **CSA7#/CKE3 Buffer Strength.** This field sets the buffer strength for CSA7#/CKE3 pins.<br>Value / Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz & 100 MHz |
| 23:22 | **CSB6#/CKE4 Buffer Strength.** This field sets the buffer strength for CSB6#/CKE4 pins.<br>Value / Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz & 100 MHz |
| 21:20 | **CSA6#/CKE2 Buffer Strength.** This field sets the buffer strength for CSA6#/CKE2pins.<br>Value / Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz & 100 MHz |
| 19 | **CSA5#/RASA5#, CSB5#/RASB5# Buffer Strength.** This field sets the buffer strength for the CSA5#/RASA5#, CSB5#/RASB5# pins.<br>Value / Buffer Strength<br>0 — 1x — 66 MHz & 100 MHz<br>1 — 2x — 66 MHz & 100 MHz |
| 18 | **CSA4#/RASA4#, CSB4#/RASB4# Buffer Strength.** This field sets the buffer strength for the CSA4#/RASA4#, CSB4#/RASB4# pins.<br>Value / Buffer Strength<br>0 — 1x — 66 MHz & 100 MHz<br>1 — 2x — 66 MHz & 100 MHz |
| 17 | **CSA3#/RASA3#, CSB3#/RASB3# Buffer Strength.** This field sets the buffer strength for the CSA3#/RASA3#, CSB3#/RASB3# pins.<br>Value / Buffer Strength<br>0 — 1x — 66 MHz & 100 MHz<br>1 — 2x — 66 MHz & 100 MHz |
| 16 | **CSA2#/RASA2#, CSB2#/RASB2# Buffer Strength.** This field sets the buffer strength for the CSA2#/RASA2#, CSB2#/RASB2# pins.<br>Value / Buffer Strength<br>0 — 1x — 66 MHz & 100 MHz<br>1 — 2x — 66 MHz & 100 MHz |

| Bit | Description |
|---|---|
| 15 | **CSA1#/RASA1#, CSB1#/RASB1# Buffer Strength.** This field sets the buffer strength for the CSA1#/RASA1#, CSB1#/RASB1# pins.<br>Value — Buffer Strength<br>0 — 1x — 66 MHz & 100 MHz<br>1 — 2x — 66 MHz & 100 MHz |
| 14 | **CSA0#/RASA0#, CSB0#/RASB0# Buffer Strength.** This field sets the buffer strength for the CSA0#/RASA0#, CSB0#/RASB0# pins.<br>Value — Buffer Strength<br>0 — 1x — 66 MHz & 100 MHz<br>1 — 2x — 66 MHz & 100 MHz |
| 13:12 | **DQMA5/CASA5# Buffer Strength.** This field sets the buffer strength for the DQMA5/CASA5# pins.<br>Value — Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz Only |
| 11:10 | **DQMA1/CASA1# Buffer Strength.** This field sets the buffer strength for the DQMA1/CASA1# pin.<br>Value — Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz Only |
| 9:8 | **DQMB5/CASB5# Buffer Strength.** This field sets the buffer strength for the DQMB5/CASB5# pin.<br>Value — Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz Only |
| 7:6 | **DQMB1/CASB1# Buffer Strength.** This field sets the buffer strength for the DQMB1/CASB1# pin.<br>Value — Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz Only |
| 5:4 | **DQMA[7:6,4:2,0]/CASA[7:6,4:2,0]# Buffer Strength.** This field sets the buffer strength for the DQMA[7:6]/CASA[7:6]#, DQMA[4:2]/CASA[4:2]#, and the DQMA[0]/CASA[0]# pins.<br>Value — Buffer Strength<br>00 — 1x — 66 MHz & 100 MHz<br>01 — Reserved — Invalid setting for 66 MHz and 100 MHz<br>10 — 2x — 66 MHz & 100 MHz<br>11 — 3x — 66 MHz & 100 MHz |

| Bit | Description |
|---|---|
| 3:2 | **CKE1/GCKE Buffer Strength.** This field sets the buffer strength for the CKE1 pin.<br>Value Buffer Strength<br>00 1x 66 MHz & 100 MHz<br>01 Reserved Invalid setting for 66 MHz and 100 MHz<br>10 2x 66 MHz & 100 MHz<br>11 3x 66 MHz & 100 MHz |
| 1:0 | **CKE0/FENA Buffer Strength.** This field sets the buffer strength for the CKE0/FENA pin.<br>Value Buffer Strength<br>00 1x 66 MHz & 100 MHz<br>01 Reserved Invalid setting for 66 MHz and 100 MHz<br>10 2x 66 MHz & 100 MHz<br>11 3x 66 MHz & 100 MHz |

## 4. Memory Buffer Frequency Select (MBFS) Register

The following register definition is for the B-0, B-1 and C-0 steppings of the 82443BX.

### MBFS—Memory Buffer Frequency Select Register

Address Offset: CA–CCh
Default Value: 000000h
Access: Read/Write

The settings in this register enable the 100 MHz or 66 MHz buffers for each of the following signal groups. For example: Setting MBFS bit 22 equal to ‘1’ enables the selection of the 100 MHz buffers (1x, 2x, or 3x) for MAA[13:0], WEA#, SRASA#, and SCASA#. If the MBFS bit 22 equals ‘0’ then the 66 MHz buffers (1x, 2x, or 3x) are enabled for MAA[13:0], WEA#, SRASA#, and SCASA#. The actual buffer strength (1x, 2x, or 3x) is determined by the settings in the MBSC register for the specific signal group.

| Bit | Description |
|---|---|
| 23 | Reserved |
| 22 | **MAA[13:0], WEA#, SRASA#, SCASA# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: MAA[13:0], WEA#, SRASA#, SCASA#.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 21 | **MAB[13:11, 9:0]# & MAB10, WEB#, SRASB#, SCASB# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: MAB[13:11, 9:0]# & MAB10, WEB#, SRASB#, SCASB#.<br>Note: The address’s MAB[13:11, 9:0]# are inverted copies of MAA[13:0], with the exception of MAB10.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |

| Bit | Description |
|---|---|
| 20 | **MD [63:0] (100 MHz / 66 MHz buffer select bit [Control 2]).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: MD [63:0] [Control 2] (Refer to the corresponding MBSC register for programming details).<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 19 | **MD [63:0] (100 MHz / 66 MHz buffer select bit [Control 1]).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: MD [63:0] [Control 1] (Refer to the corresponding MBSC register for programming details).<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 18 | **MECC [7:0] (100 MHz / 66 MHz buffer select bit [Control 2]).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: MECC [7:0] [Control 2] (Refer to the corresponding MBSC register for programming details).<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 17 | **MECC [7:0] (100 MHz / 66 MHz buffer select bit [Control 1]).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: MECC [7:0] [Control 1] (Refer to the corresponding MBSC register for programming details)<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 16 | **CSB7#/CKE5 (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSB7#/CKE5.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 15 | **CSA7#/CKE3 (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSA7#/CKE3.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 14 | **CSB6# / CKE4 (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSB6# / CKE4.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 13 | **CSA6# / CKE2 (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSA6# / CKE2.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 12 | **CSA5# / RASA5#,CSB5# / RASB5# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSA5#/RASA5#, CSB5#/RASB5#.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |

| Bit | Description |
|---|---|
| 11 | **CSA4#/RASA4#, CSB4#/RASB4# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSA4#/RASA4#, CSB4#/RASB4#.<br><br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 10 | **CSA3#/RASA3#, CSB3#/RASB3# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSA3#/RASA3#, CSB3#/RASB3#.<br><br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 9 | **CSA2#/RASA2#, CSB2#/RASB2# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSA2#/RASA2#, CSB2#/RASB2#.<br><br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 8 | **CSA1#/RASA1#, CSB1#/RASB1# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSA1#/RASA1#, CSB1#/RASB1#.<br><br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 7 | **CSA0#/RASA0#, CSB0#/RASB0# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CSA0#/RASA0#, CSB0#/RASB0#.<br><br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 6 | **DQMA5/CASA5# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: DQMA5/CASA5#.<br><br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 5 | **DQMA1/CASA1# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: DQMA1/CASA1#.<br><br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 4 | **DQMB5/CASB5# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: DQMB5/CASB5#.<br><br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 3 | **DQMB1/CASB1# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: DQMB1/CASB1#.<br><br>Value Buffer<br>0 66 MHz<br>1 100 MHz |

| Bit | Description |
|---|---|
| 2 | **DQMA[7:6,4:2,0]/CASA[7:6,4:2,0]# (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: DQMA[7:6]/CASA[7:6]#, DQMA[4:2]/CASA[4:2]#, and the DQMA[0]/CASA[0]#.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 1 | **CKE1/GCKE (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CKE1.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |
| 0 | **CKE0/FENA (100 MHz / 66 MHz buffer select bit).** This bit enables either 100 MHz or 66 MHz buffers for the following signals: CKE0/FENA.<br>Value Buffer<br>0 66 MHz<br>1 100 MHz |

## 5A. Processor PLL Lock Time Affects Intel® 82443BX

The 82443BX requires a minimum of 60 µs between the deassertion of CPU__STP# and the deassertion of SUSTAT# for a processor C3 exit. The 82443BX requires a minimum of 100 µs between the deassertion of CPU__STP# and the deassertion of SUSTAT# for a cold boot.

## 5B. DRAM Write Thermal Throttling Control Register

### DRAM Write Throttling Control Register

Offset: E0h–E7h
Default: 0000_0000_0000_0000h
Access: Read/Write/Lock
Size: 64b

The DRAM Write Throttling Control register defines the maximum sustained bandwidth of writes to DRAM which can be tolerated before a throttling mechanism is invoked. It also specifies the maximum DRAM write bandwidth that will be permitted by the throttling mechanism. Both of these bandwidths are specified by providing a sampling period and a maximum number of QWords which may be written in the sampling period.

The first bandwidth described is specified by the Global DRAM Write Sampling Window (GDWSW) and the Global QW Threshold (GQT). Large values are used for the GDWSW (4 ms – 1020 ms) in order to allow short bursts of writes at peak bandwidth to occur without invoking throttling.

Once the throttling mechanism is invoked, QWords written to DRAM are counted during a Throttle Monitoring Window (TMW), and writes are temporarily masked for the remainder of the TMW if the number of QW exceeds the Throttle QW Maximum (TQM). The Throttle Monitoring Window is much smaller than the Global Sampling window, programmable from 0–2048 clocks. This small window allows throttling to be implemented with a minimal latency impact.

This register also defines Throttle Time, which is measured as a multiple of Global DRAM Write Sampling Windows. Throttle Time is the amount of time that the throttling mechanism remains in

effect after being triggered. Once the throttle time has expired, the Intel 440BX AGPset returns to use of the GDWSW to determine if throttling must be invoked again.

A locking mechanism is included to protect contents of this register as well as the DRAM read throttling control register described below.

| Bits | Description |
|---|---|
| 63 | **Throttle Lock (TLOCK).** This bit secures the DRAM throttling control registers. The bit defaults to '0', then once a '1' is written to it, all configuration register bits in E0h–E7h and E8h–EFh (read throttle control) become read-only. |
| 62:46 | Reserved |
| 45:38 | **Global DRAM Write Sampling Window (GDWSW).** This eight bit value is multiplied by 4 to define the length of time in milliseconds (0–1020) over which the number of QWords written is counted. If the number of QW written during this window exceeds the Global QW Threshold defined below, then the throttling mechanism will be invoked to limit DRAM writes to a lower bandwidth checked over smaller time windows. |
| 37:26 | **Global QW Threshold (GQT).** The twelve-bit value held in this field is multiplied by $2^{15}$ to arrive at the number of QW that must be written within the Global DRAM Write Sampling Window in order to cause the throttling mechanism to be invoked. |
| 25:20 | **Throttle Time (TT).** This value provides a multiplier between 0 and 63 which specifies how long throttling remains in effect as a number of Global DRAM Write Sampling Windows. For example, if GDWSW is programmed to 1000_0000b and TT is set to 01_0000b, then throttling will be performed for ~2 seconds once invoked (128 ms * 16) |
| 19:13 | **Throttle Monitoring Window (TMW).** The value in this register is padded with four 0s to specify a window of 0–2047 DRAM CLKs with 16 clock granularity. While the throttling mechanism is invoked, DRAM writes are monitored during this window—if the number of QW written during the window reaches the Throttle QW Maximum, then write requests are blocked for the remainder of the window. |
| 12:3 | **Throttle QWord Maximum (TQM).** The Throttle QWord Maximum defines the maximum number of QWords between 0–1023 which are permitted to be written to DRAM within one Throttle Monitoring Window while the throttling mechanism is in effect. |
| 2:0 | Reserved |

## 6. DRAM Read Thermal Throttling Control Register

### DRAM Read Throttling Control Register

Offset: E8h–EFh
Default: 0000_0000_0000_0000h
Access: Read/Write/Lock
Size: 64b

The DRAM Read Throttling Control register defines the maximum sustained bandwidth of reads to DRAM which can be tolerated before a throttling mechanism is invoked. It also specifies the maximum DRAM read bandwidth that will be permitted by the throttling mechanism. Both of these bandwidths are specified by providing a sampling period and a maximum number of QWords which may be read in the sampling period.

The first bandwidth described is specified by the Global DRAM Read Sampling Window (GDRSW) and the Global QW Read Threshold (GQRT). Large values are used for the GDRSW (4 ms–1020 ms) in order to allow short bursts of reads at peak bandwidth to occur without invoking throttling.

Once the throttling mechanism is invoked, Q-words read from DRAM are counted during a Read Throttle Monitoring Window (RTMW), and IOQ and AGP traffic is temporarily masked for the remainder of the RTMW if the number of QW exceeds the Read Throttle QW Maximum (RTQM). The Read Throttle Monitoring Window is much smaller than the Global Sampling window, programmable from 0–2048 clocks. This small window allows throttling to be implemented with a minimal latency impact.

This register also defines Read Throttle Time, which is measured as a multiple of Global DRAM Read Sampling Windows. Read Throttle Time is the amount of time that the throttling mechanism remains in effect after being triggered. Once the read throttle time has expired, the NBX returns to use of the GDRSW to determine if throttling must be invoked again.

The contents of this register are protected by making the bits read-only once a 1 is written to the Throttle Lock bit (bit 63 of config register E0–E7h).

| Bits | Description |
|---|---|
| 63:46 | Reserved |
| 45:38 | **Global DRAM Read Sampling Window (GDRSW). This** eight bit value is multiplied by 4 to define the length of time in milliseconds (0–1020) over which the number of QWords read from DRAM is counted. If the number of QW read during this window exceeds the Global QW Threshold defined below, then the throttling mechanism will be invoked to limit DRAM reads to a lower bandwidth checked over smaller time windows. |
| 37:26 | **Global Read QW Threshold (GRQT).** The twelve-bit value held in this field is multiplied by $2^{15}$ to arrive at the number of QW that must be written within the Global DRAM Read Sampling Window in order to cause the throttling mechanism to be invoked. |
| 25:20 | **Read Throttle Time (RTT).** This value provides a multiplier between 0 and 63 which specifies how long read throttling remains in effect as a number of Global DRAM Read Sampling Windows. For example, if GDRSW is programmed to 1000_0000b and RTT is set to 01_0000b, then read throttling will be performed for ~2 seconds once invoked (128 ms * 16) |
| 19:13 | **Read Throttle Monitoring Window (RTMW).** The value in this register is padded with 4 0s to specify a window of 0–2047 DRAM CLKs with 16 clock granularity. While the throttling mechanism is invoked, DRAM reads are monitored during this window—if the number of QW read during the window reaches the Throttle QW Maximum, then Host and PCI read requests, as well as all AGP requests, are blocked for the remainder of the window. |
| 12:3 | **Read Throttle QWord Maximum (RTQM).** The Read Throttle Q-word Maximum defines the maximum number of QWords between 0–1023 which are permitted to be read from DRAM within one Read Throttle Monitoring Window while throttling mechanism is in effect. |
| 2:0 | Reserved |

# 7. Error Command Register

## ERRCMD—Error Command Register

This is an existing register. Bit 3 is now used to enable SERR# generation when throttling conditions are met. All other bit fields remain unchanged.

Address Offset: 90h
Default Value: 80h
Access: Read/Write
Size: 8 bits

This 8-bit register controls the Intel 440BX AGPset responses to various system errors. The actual assertion of SERR# is enabled via the PCI Command register.

| Bit | Description |
|---|---|
| 7 | **SERR# on AGP Non-snoopable Access Outside of Graphics Aperture.** When this bit is set and bit 10 of ERRSTS registers transitions from 0 to 1 (during an AGP access to the address outside of the graphics aperture) then an SERR# assertion event will be generated. If this bit is "0" then reporting of this condition is disabled. Default=1 |
| 6 | **SERR# on Invalid AGP DRAM Access.** AGP non-snoopable READ accesses to locations outside the graphics aperture and outside the main DRAM range (i.e., in 640 KB – 1 MB range or above top of memory) are invalid. Consider the scenario when an AGP agent generates a READ access using enhanced AGP protocol, which the 82443BX must accept without qualification from address decode logic since there is no protocol mechanism to reject it. When this bit is set, bit 9 of the ERRSTS will be set and SERR# will be asserted if these read accesses are not directed to main memory or the aperture range. If this bit is 0, then reporting of this condition via SERR# is disabled. |
| 5 | **SERR# on Access to Invalid Graphics Aperture Translation Table Entry.** When this bit is set to 1, the 82443BX will set bit 8 of the ERRSTS and assert SERR# following a read or write access to an invalid entry in the Graphics Aperture Translation Table residing in main memory. If this bit is 0, then reporting of this condition via SERR# is disabled. |
| 4 | **SERR# on Receiving Target Abort.** When this bit is 1, the 82443BX asserts SERR# upon receiving a target abort on either the PCI0. When this bit is set to 0, the 82443BX does not assert SERR# upon receipt of a target abort. |
| 3 | **SERR# on Detected Power Throttling Condition.** When this bit is 1, the 82443BX asserts SERR# when power throttling condition is detected for either the read or the write function. When this bit is set to 0, the 82443BX does not assert SERR# for power throttling. |
| 2 | **SERR# assertion mode.** When this bit is set to 0 (default), SERR# is asserted for 1 PCI clock (standard PCI mode). When this bit is set to 1, SERR# becomes a level mode signal. Systems that connect SERR# to EXTSMI# for error reporting should set this bit to 1. |
| 1 | **SERR# on Receiving Multiple-Bit ECC/Parity Error.** When this bit is set to 1, the 82443BX asserts SERR# when it detects a multiple-bit error reported by the DRAM controller. For systems not supporting ECC this bit must be disabled. |
| 0 | **SERR# on Receiving Single-bit ECC Error.** When this bit is set to 1, the 82443BX asserts SERR# when it detects a single-bit ECC error. For systems that do not support ECC this bit must be disabled. |

# 8. Error Status Register

## ERRSTS—Error Status Register

This is an existing register of which its bits 12:11 are now used to reflect when read and write throttling conditions are met. All other bit fields remain unchanged.

Address Offset: 91–92h
Default Value: 0000h
Access: Read Only, Read/Write Clear
Size: 16 bits

SERR# is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD register).

| Bit | Description |
|---|---|
| 15:13 | Reserved. |
| 12 | **Read throttling condition.** When this bit is set it indicates that read throttling condition occurred. Software has to write 1 to clear this bit. Default=0 |
| 11 | **Write throttling condition.** When this bit is set it indicates that write throttling condition occurred. Software has to write 1 to clear this bit. Default=0 |
| 10 | **AGP. non-snoopable access outside of Graphics Aperture.** When this bit is set, it indicates that an AGP access occurred to the address that is outside of the graphics aperture range. Software has to write 1 to clear this bit. Default=0 |
| 9 | **Invalid AGP non-snoopable DRAM read access (R/WC).** When this bit is set to 1, it indicates that an AGP non-snoopable READ access was attempted outside of the graphics aperture and outside of main memory (i.e., in 640 KB – 1 MB range or above top of memory). Software must write a 1 to clear this status bit. |
| 8 | **Access to Invalid Graphics Aperture Translation Table Entry (AIGATT) (R\WC).** When this bit is set to 1, it indicates that an invalid translation table entry was returned in response to a graphics aperture read or write access. Software must write a 1 to clear this bit. |
| 7:5 | **Multi-bit First Error (MBFRE) (RO).** This field contains the encoded value of the DRAM row in which the first multi-bit error occurred. A simple binary encoding is used to indicate the row containing the multi-bit error: 000b indicates row 0, 001b row 1, on through 111b indicating row 7. When an error is detected, this field is updated and the MEF bit is set. This field will then be locked (no further updates) until the MEF flag has been reset. If MEF is 0, the value in this field is undefined. |
| 4 | **Multiple-bit ECC (uncorrectable) Error Flag (MEF) (R/WC).** If this bit is set to 1, the memory data transfer had an uncorrectable error (i.e., multiple-bit error). When enabled, a multiple bit error is reported by the DRAM controller and propagated to the SERR# pin, if enabled by bit 1 in the ERRCMD register. BIOS has to write a 1 to clear this bit and unlock the MBFRE field.<br>Default value of this bit is zero. |
| 3:1 | **Single-bit First Row Error (SBFRE) (RO).** This field contains the encoded value of the DRAM row in which the first single-bit error occurred. A simple binary encoding is used to indicate the row containing the single-bit error: 000b indicates row 0, 001b row 1, on through 111b indicating row 7. When an error is detected, this field is updated and SEF is set. This field is then locked (no further updates) until the SEF flag has been reset. If SEF is 0, the value in this field is undefined. |

| Bit | Description |
|---|---|
| 0 | **Single-bit (correctable) ECC Error Flag (SEF) (R/WC).** If this bit is set to 1, the memory data transfer had a single-bit correctable error and the corrected data was sent for the access. When ECC is enabled, a single bit error is reported and propagated to the SERR# pin, if enabled by bit 0 in the ERRCMD register. BIOS has to write a 1 to clear this bit and unlock the SBFRE field. |

## 9. DCLKRD (Pin AB22) Changed to No Connect

This specification change has been incorporated into the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet.

## 10. Reserved Straps

MAB8# and MAB13 have been defined as “reserved” strapping options. The function of these straps is currently undefined, but is reserved for future use. These signals are sampled during power up reset. Internal pull down resistors set the default strap value to ‘0’. Provisions should be made on the motherboard for an external pull up resistor option (i.e., resistor pads), but no resistor should be populated.

## 11. MAB13 Polarity Change

For the B-0 step of 82443BX, the polarity of the B-copy of memory address bit 13 will be changed from MAB13# to MAB13 (see errata #5).

## 12. SERR# on Target Abort

This specification change has been incorporated into the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet.

## 13. Abort Disable Test Mode Configuration Bits

Intel Reserved Register bits at offset F4h, bits 29 and 30 should be set to 1 for normal operation.

## 14. Selective Auto Precharge

Due to inconsistent behavior of the selective auto precharge feature with different SDRAM components, this feature will be removed from further revisions of the This specification change has been incorporated into the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet Bit 4 of the Paging Policy register, Offset 78–79h should be set to 0 (default). Bit 4 at Offset 78h will become an Intel Reserved bit location.

## 15. Memory Data Buffer Strength Programming

Characterization of the MD buffers has shown that the actual buffers are stronger than the simulated buffer strengths. As a result, new buffer strength settings are recommended in order to improve system noise margin.

## 16. Intel® 82443BX Host Bridge/Controller NAND Tree Testing

This section provides information about the NAND tree testability features of the Intel 82443BX.

### Test Mode Activation

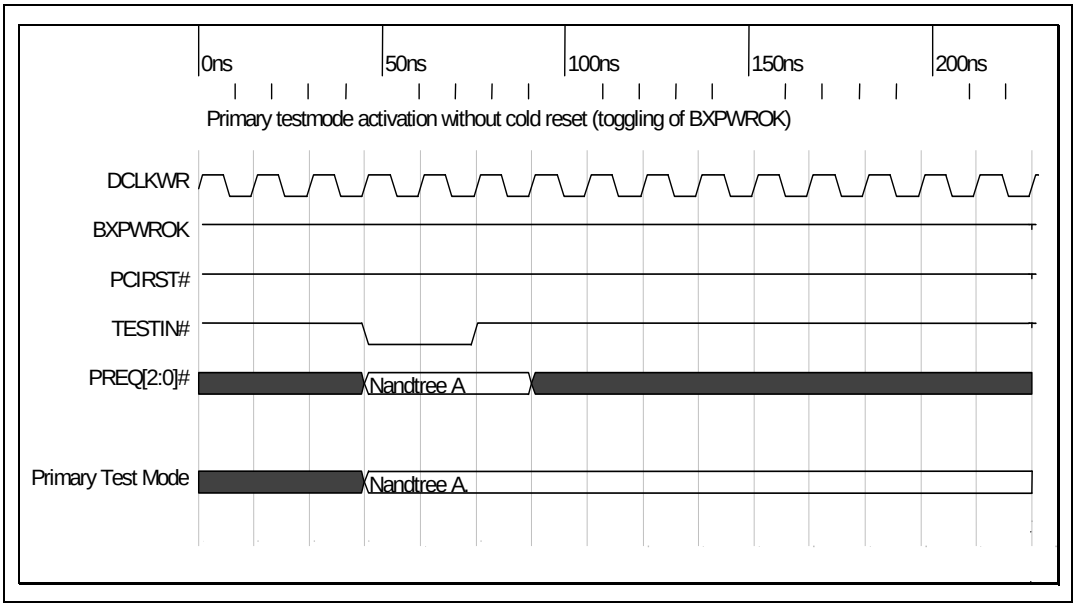
The primary test mode is enabled via TESTIN# pin. To enable a NAND Tree primary test mode, the TESTIN# input pin is asserted low and a 3-bit binary pattern is presented on the PCI PREQ[2:0]# input pins. Table 1 shows the PREQ[2:0]# signal encoding for NAND tree test modes enabled via the TESTIN# pin.

**Table 1. Primary Test Modes**

| PREQ[2:0]# | Test Mode Enabled |
|---|---|
| 000 | NANDtree A |
| 001 | NANDtree B |

The Figure 1 timing diagram shows the sequence required to enable a primary test mode. Note that the TESTIN# input pin acts as a latch enable, and the PREQ[2:0]# pins act as latch inputs. The test mode is decoded from the output of the latch.

**Figure 1. Waveform of Primary Test Mode**



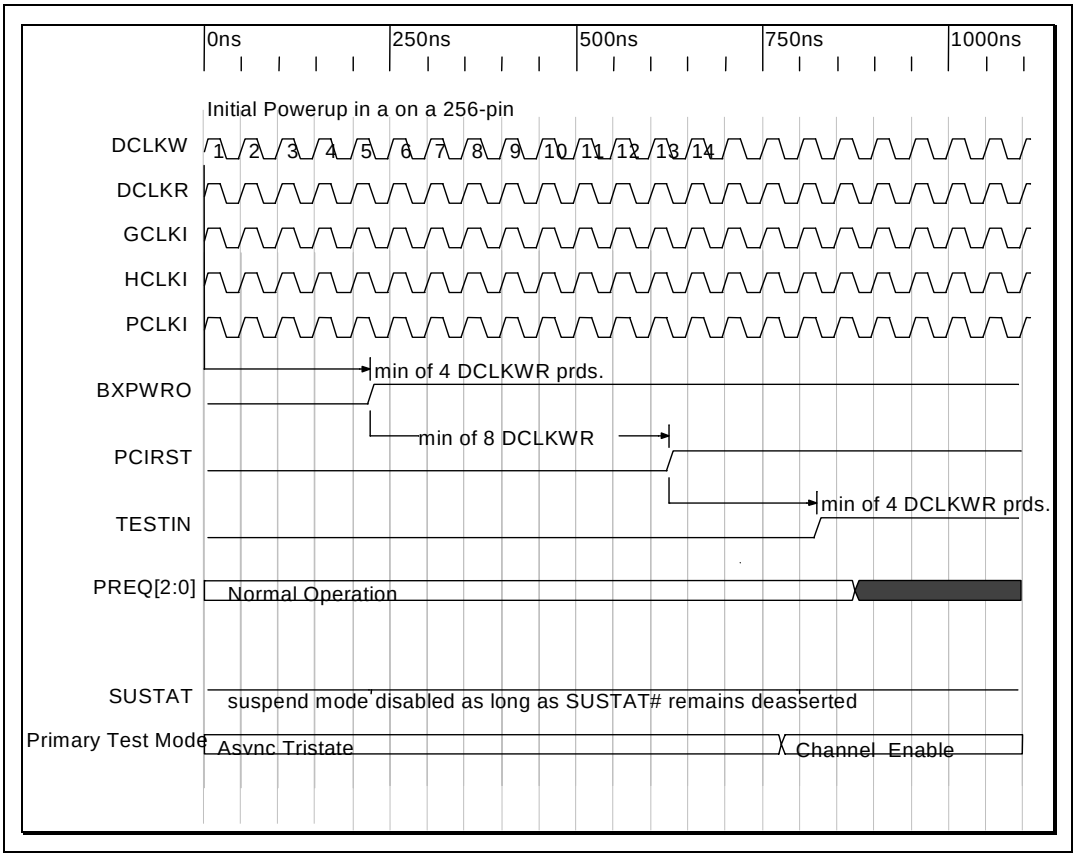
## Tester Power-Up Sequence

Figure 2 shows the typical power-up sequence of an 82443BX on a 256-pin tester.

At time 0, PCIRST# and TESTIN# must be asserted. The BXPWROK signal must also be asserted to indicate that a cold reset is in progress.

Once PCIRST# is deasserted, on the fourth DCLKWR positive edge, the TESTIN# can also be safely deasserted. PCIRST# and TESTIN# should not deassert at the same time because a race condition prevents the circuit from guaranteeing proper latching of primary test modes.

**Figure 2. Typical Power-Up Sequence**



## Primary Test Mode Details

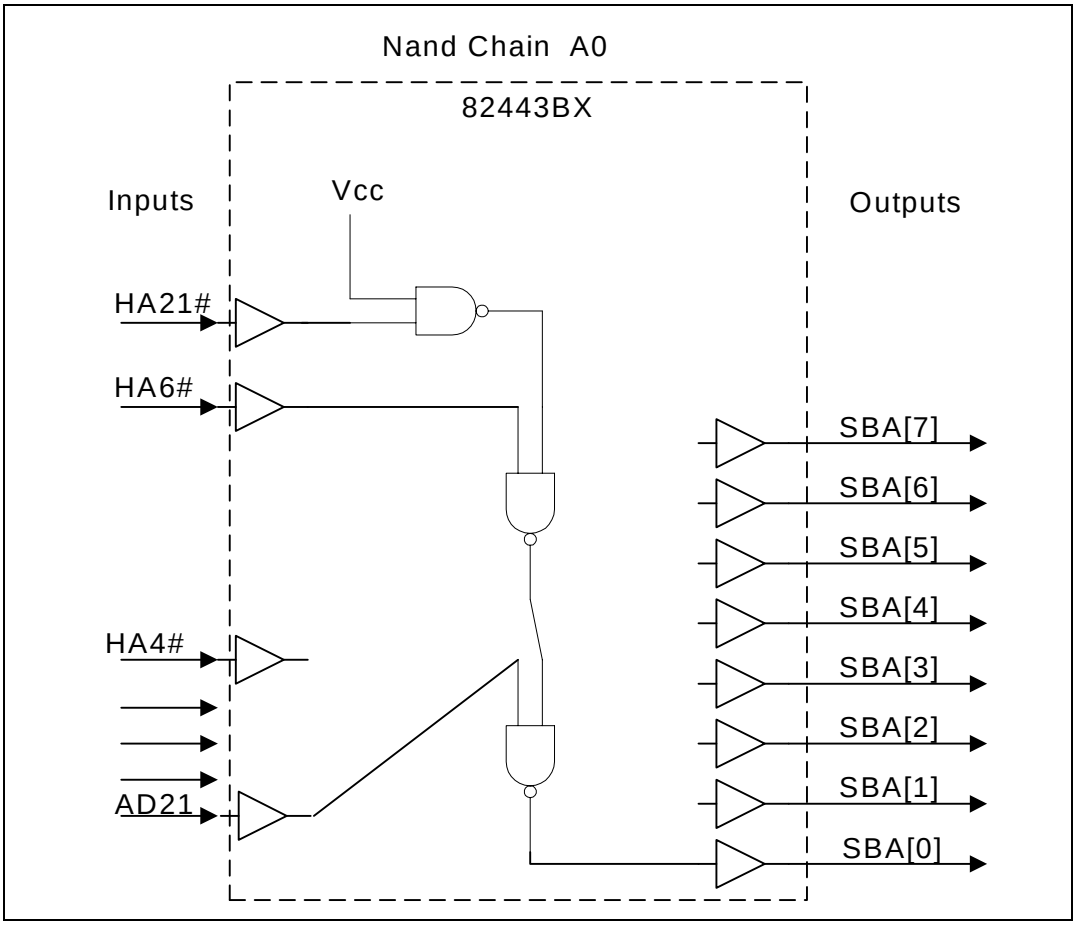
### NANDtree A

The NANDtree A test mode is used for board level connectivity test. Its main purpose is to detect connectivity shorts between adjacent pins and to check proper bonding between I/O pads and I/O pins.

To help reduce the board level test cost, the NAND chain is limited to 60 pins per chain. This is accomplished by implementing 8 separate NAND chains.

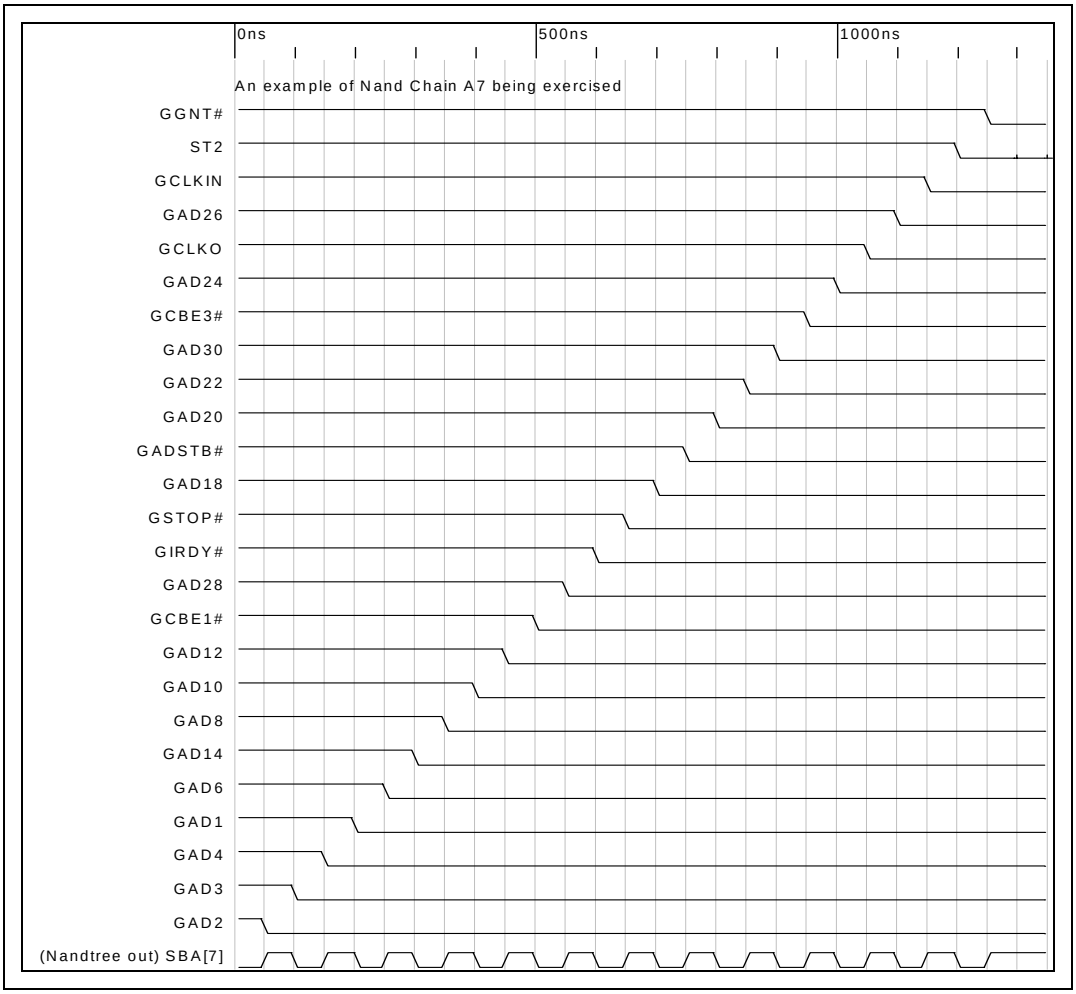
A conceptual diagram of the NANDtree is shown in Figure 3.

**Figure 3. NAND Chain A0 Connectivity**



An example NANDtree test is shown in Figure 4. At first, all the input pins are driven to logic 1. Next, each input pin is driven to logic 0, in a sequence, so that the output pin, in this case SBA[0], toggles. By observing the NANDtree output pin, one can detect shorted and unconnected pins.

**Figure 4. Waveform of NAND Chain #A7 Test**



NAND chain pin assignments are shown in the following tables.

**Table 2. Signals Not Included in NANDtree A or NANDtree B**

| Signals | Purpose |
|---|---|
| BXPWROK | Used for cold reset |
| PCIRST# | Used for cold and warm reset |
| TESTIN# | Used to enter NANDtree A and B test modes |

**Table 3. NANDtree A Outputs**

| Signals | Purpose |
|---|---|
| SBA[0] | NAND-Chain A0 Output |
| SBA[1] | NAND-Chain A1 Output |
| SBA[2] | NAND-Chain A2 Output |
| SBA[3] | NAND-Chain A3 Output |
| SBA[4] | NAND-Chain A4[1] and A8 Output |
| SBA[5] | NAND-Chain A5[1] and A9 Output |
| SBA[6] | NAND-Chain A6 Output |
| SBA[7] | NAND-Chain A7 Output |

Legend for Table 3:

[1] - When MMO mode is disabled, NANDtree chains A4 and A5 are also deactivated. When MMO mode is enabled, NAND chains A4 and A5 are active during NANDtree A test mode. The output of NANDtree chains A4 and A5 (when MMO mode is enabled) must always go through chains A8 and A9, respectively, before it comes out on SBA[4] and SBA[5]. MMO mode is the MAB7# strap configuration controlling the “mobile mode operation.” When MMO mode is enabled the lower order NAND tree chains of the paired groups are also tested.

| # | Chain #A0 | | Chain #A1 | | Chain #A2 | | Chain #A3 | |
|---|---|---|---|---|---|---|---|---|
| | Pin Name | Pad# | Pin Name | Pad# | Pin Name | Pad# | Pin Name | Pad# |
| 1 | HA21# | 111 | HA15# | 105 | GNT3# | 244 | AD30 | 249 |
| 2 | HA6# | 114 | HREQ0# | 108 | GNTO# | 246 | AD24 | 256 |
| 3 | HA4# | 116 | HA18# | 110 | AD19 | 255 | TRDY# | 256 |
| 4 | HA28# | 119 | HA23# | 113 | AD17 | 257 | AD18 | 259 |
| 5 | HA20# | 121 | HA31# | 115 | AD11 | 260 | AD16 | 261 |
| 6 | HA26# | 131 | BREQ0# | 117 | PAR | 262 | FRAME# | 265 |
| 7 | HA27# | 133 | HA10# | 120 | C/BE2# | 263 | IRDY# | 267 |
| 8 | HA30# | 134 | HA22# | 123 | AD15 | 266 | AD12 | 268 |
| 9 | HA24# | 135 | HD1# | 129 | STOP# | 269 | PLOCK# | 270 |
| 10 | CPURST# | 137 | HA11# | 132 | DEVSEL# | 271 | C/BE1# | 275 |
| 11 | HD32# | 177 | HD2# | 138 | SERR# | 273 | AD14 | 277 |
| 12 | HD33# | 179 | HA29# | 139 | AD13 | 276 | AD10 | 279 |
| 13 | HD37# | 181 | HD4# | 140 | AD9 | 278 | AD9 | 283 |
| 14 | HD434# | 182 | HD0# | 141 | AD0 | 280 | AD4 | 284 |
| 15 | HD40# | 183 | HD3# | 143 | AD7 | 281 | AD6 | 287 |
| 16 | HD36# | 185 | HD8# | 144 | C/BEO# | 285 | AD2 | 288 |
| 17 | HD35# | 186 | HD5# | 145 | AD5 | 289 | AD1 | 291 |
| 18 | HD44# | 187 | HD9# | 146 | AD3 | 290 | CLKRUN# | 373 |
| 19 | HD34# | 188 | HD6# | 147 | MD34 | 382 | WSC# | 381 |
| 20 | HD47# | 189 | HD7# | 149 | MD32 | 384 | SUSTAT# | 385 |
| 21 | HD42# | 191 | HD10# | 150 | MD35 | 386 | MD1 | 387 |
| 22 | HD38# | 192 | HD12# | 151 | MD33 | 391 | MD0 | 389 |
| 23 | HD51# | 193 | HD14# | 152 | MD36 | 396 | MD5 | 390 |
| 24 | HD49# | 194 | HD15# | 153 | MD37 | 399 | MD2 | 393 |
| 25 | HD54# | 195 | HD17# | 155 | MD38 | 403 | MD3 | 395 |
| 26 | HD48# | 197 | HD11# | 156 | MD42 | 406 | MD4 | 397 |
| 27 | HD45# | 198 | HD18# | 157 | MD40 | 407 | MD6 | 400 |
| 28 | HD59# | 199 | HD13# | 158 | MD39 | 410 | MD8 | 401 |
| 29 | HD39# | 200 | HD20# | 159 | MD41 | 411 | MD7 | 405 |
| 30 | HD53# | 201 | HD16# | 161 | MD44 | 414 | MD9 | 409 |
| 31 | HD60# | 203 | HD21# | 162 | MD43 | 415 | MD11 | 413 |
| 32 | HD55# | 204 | HD19# | 163 | MD45 | 417 | MD15 | 419 |
| 33 | HD63# | 205 | HD22# | 165 | WEB# | 427 | MD10 | 420 |
| 34 | HD41# | 206 | HD25# | 167 | SCASA# | 433 | MECC0 | 421 |

| # | Chain #A0 | | Chain #A1 | | Chain #A2 | | Chain #A3 | |
|---|---|---|---|---|---|---|---|---|
| | Pin Name | Pad# | Pin Name | Pad# | Pin Name | Pad# | Pin Name | Pad# |
| 35 | HD58# | 207 | HD23# | 168 | DQMA4 | 437 | MD14 | 423 |
| 36 | HD62# | 209 | HD26# | 169 | MD46 | 438 | MECC1 | 424 |
| 37 | HD46# | 210 | HD29# | 170 | MD47 | 442 | MECC4 | 425 |
| 38 | HD61# | 211 | HD27# | 171 | SCASB# | 444 | MD12 | 428 |
| 39 | HD57# | 212 | HD31# | 173 | MAB0# | 453 | MECC5 | 429 |
| 40 | HD52# | 213 | HD29# | 175 | MAB2# | 457 | WEA# | 431 |
| 41 | HD56# | 215 | HD24# | 176 | MAB4# | 459 | MD13 | 432 |
| 42 | HD50# | 216 | HD30# | 180 | MAB1# | 464 | DQMA0 | 434 |
| 43 | REQ1# | 217 | GNT1# | 219 | MAB5# | 465 | CSA1# | 441 |
| 44 | REQ0# | 221 | REQ4# | 220 | MAB8# | 467 | CSA2# | 443 |
| 45 | GNT2# | 222 | PHLDA# | 226 | MAB9# | 473 | CSA4# | 445 |
| 46 | PHOLD# | 223 | REQ2# | 228 | MAB11# | 476 | CSA3# | 446 |
| 47 | AD31 | 225 | AD28 | 229 | MAB12# | 477 | SRASA# | 447 |
| 48 | AD29 | 227 | AD26 | 232 | MAB3# | 480 | DQMA1 | 450 |
| 49 | AD25 | 231 | C/BE3# | 235 | MAB13# | 481 | SCA5# | 451 |
| 50 | GNTA4# | 233 | AD22 | 237 | MAB6# | 494 | CSA0# | 452 |
| 51 | AD27 | 234 | REQ3# | 242 | MAB7# | 496 | DQMA5 | 456 |
| 52 | AD23 | 293 | AD20 | 243 | MAB10 | 498 | CKE0 | 483 |
| 53 | AD21 | 241 | PCLKIN | 245 | DCLKWR | 499 | SRASB# | 484 |

| # | Chain #A4 Pin Name | Chain #A4 Pad# | Chain #A5 Pin Name | Chain #A5 Pad# |
|---|---|---|---|---|
| 1 | DQMB1 | 435 | MAA0 | 449 |
| 2 | DQMB5 | 439 | MAA2 | 455 |
| 3 | CKE3 | 488 | MAA4 | 458 |
| 4 | CKE2 | 489 | MAA6 | 461 |
| 5 | CKE4 | 491 | MAA5 | 463 |
| 6 | CSB1# | 495 | MAA8 | 466 |
| 7 | CSB0# | 497 | MAA9 | 469 |
| 8 | CSB2# | 501 | MAA1 | 470 |
| 9 | CSB3# | 3 | MAA10 | 471 |
| 10 | CSB5# | 5 | MAA3 | 474 |
| 11 | DCLKO | 6 | MAA11 | 475 |
| 12 | CSB4# | 9 | MAA12 | 479 |
| 13 | | | CKE1 | 485 |
| 14 | | | CKE5 | 487 |
| 15 | | | MAA7 | 490 |
| 16 | | | MAA13 | 493 |
| 17* | | | DCLKRD* | 4* |

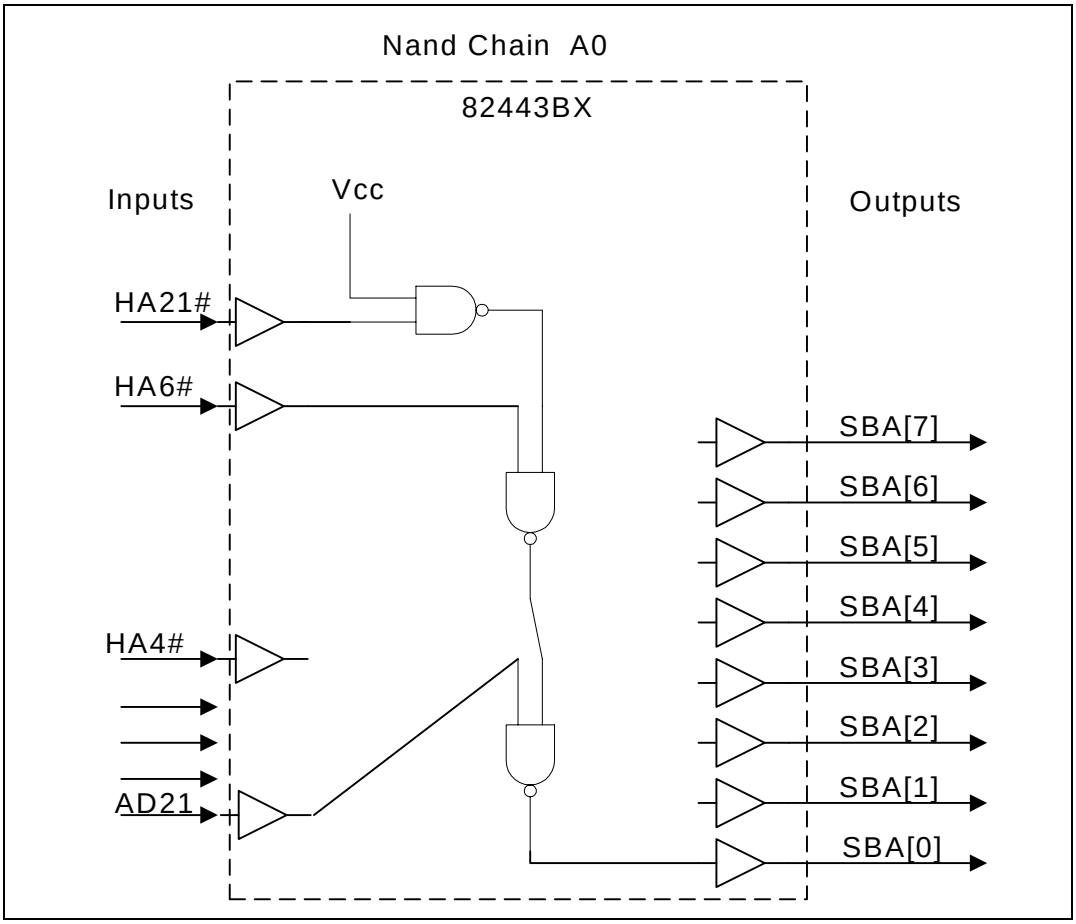
*__NOTE__: Chain #A5, DCLKRD: This pad/pin was in use as part of this chain for the B1 stepping of the 82443BX. This pad/pin was removed from the chain for the C1 stepping. This should be the only chain that fails on the 82443BX C1 stepping if the 82443BX B1 stepping NAND tree test are used. All pins tested after DCLKRD will give the opposite data when testing an 82443BX C1 step device with the 82443BX B1 step NAND tree test.

To repair the NAND tree test of Chain #A5/#A9 (MMO enabled) for the 82443BX C1 stepping, remove DCLCKRD from the test and invert the expected data for all pins (MAA13, MAA7, CKE5, CKE1, MAA12, MAA11, MAA3, MAA10, MAA1, MAA9, MAA8, MAA5, MAA6, MAA4, MAA2, and MAA0) which were tested following the DCLKRD pin.

| # | Chain #A6 Pin Name | Pad# | Chain #A7 Pin Name | Pad# |
|---|---|---|---|---|
| 1 | RBF# | 292 | GGNT# | 293 |
| 2 | GREQ# | 294 | ST2 | 298 |
| 3 | ST1 | 295 | GCLKIN | 312 |
| 4 | PIPE# | 299 | GAD26 | 323 |
| 5 | ST0 | 302 | GCLKO | 324 |
| 6 | SB-STB | 305 | GAD24 | 325 |
| 7 | GAD31 | 315 | GC/BE3# | 327 |
| 8 | GAD29 | 317 | GAD30 | 328 |
| 9 | GAD27 | 319 | GAD22 | 329 |
| 10 | GAD23 | 322 | GAD20 | 331 |
| 11 | GAD25 | 332 | GAD-STBB | 336 |
| 12 | GAD17 | 333 | GAD16 | 337 |
| 13 | GC/BE2# | 335 | GAD18 | 339 |
| 14 | GFRAME# | 340 | GSTOP# | 343 |
| 15 | GTRDY# | 341 | GIRDY# | 346 |
| 16 | GAD21 | 342 | GAD28 | 349 |
| 17 | GPAR | 345 | GC/BE1# | 351 |
| 18 | GAD19 | 347 | GAD12 | 353 |
| 19 | GAD15 | 350 | GAD10 | 356 |
| 20 | GAD13 | 352 | GAD8 | 359 |
| 21 | GDEVSEL# | 355 | GAD14 | 360 |
| 22 | GAD11 | 357 | GAD6 | 363 |
| 23 | GAD7 | 361 | GAD1 | 366 |
| 24 | GC/BE0# | 362 | GAD4 | 369 |
| 25 | GAD-STBA | 365 | GAD3 | 371 |
| 26 | GAD5 | 367 | GAD2 | 375 |
| 27 | GAD9 | 370 | | |
| 28 | GAD0 | 374 | | |

| # | Chain #A8 Pin Name | Chain #A8 Pad# | Chain #A9 Pin Name | Chain #A9 Pad# |
|---|---|---|---|---|
| 1 | DQMA6 | 8 | | |
| 2 | MECC2 | 13 | DQMA2 | 7 |
| 3 | DQMA7 | 15 | DQMA3 | 11 |
| 4 | MD50 | 18 | MECC7 | 14 |
| 5 | MD48 | 21 | MECC6 | 17 |
| 6 | MD49 | 27 | MECC3 | 19 |
| 7 | MD51 | 28 | MD16 | 23 |
| 8 | MD59 | 34 | MD17 | 24 |
| 9 | MD52 | 35 | MD18 | 25 |
| 10 | MD53 | 37 | MD19 | 29 |
| 11 | MD54 | 38 | MD21 | 31 |
| 12 | MD55 | 43 | MD20 | 33 |
| 13 | MD57 | 45 | MD22 | 39 |
| 14 | MD58 | 47 | MD23 | 41 |
| 15 | MD56 | 49 | MD24 | 44 |
| 16 | MD61 | 55 | MD25 | 48 |
| 17 | MD62 | 57 | MD27 | 51 |
| 18 | MD63 | 59 | MD28 | 53 |
| 19 | CRESET# | 63 | MD29 | 54 |
| 20 | MD60 | 64 | MD26 | 58 |
| 21 | RS0# | 69 | MD31 | 61 |
| 22 | RS2# | 71 | MD30 | 66 |
| 23 | HREQ3# | 75 | RS1# | 68 |
| 24 | HREQ2# | 77 | HCLKIN | 70 |
| 25 | HREQ4# | 81 | HIT# | 73 |
| 26 | HREQ1# | 83 | DBSY# | 76 |
| 27 | BPRI# | 85 | DEFER# | 79 |
| 28 | BNR# | 88 | HITM# | 82 |
| 29 | HLOCK# | 90 | DRDY# | 84 |
| 30 | HA5# | 93 | HTRDY# | 87 |
| 31 | HA14# | 95 | HA9# | 89 |
| 32 | HA13# | 97 | HA3# | 91 |
| 33 | ADS# | 101 | HA7# | 94 |
| 34 | HA16# | 104 | HA8# | 96 |
| 35 | HA19# | 107 | HA12# | 99 |
| 36 | HA25# | 109 | HA17# | 103 |

**Figure 5. Waveform of NANDtree Chain Pair up (A4 and A8) and (A5 and A9)**



### NANDtree B

The NANDtree B test mode is used to test the SBA[7:0] pins. These pins are outputs during the NANDtree A test mode and are not tested in that mode. In NANDtree B test mode, the SBA[7:0] signals become inputs and the CRESET# pin becomes the output.

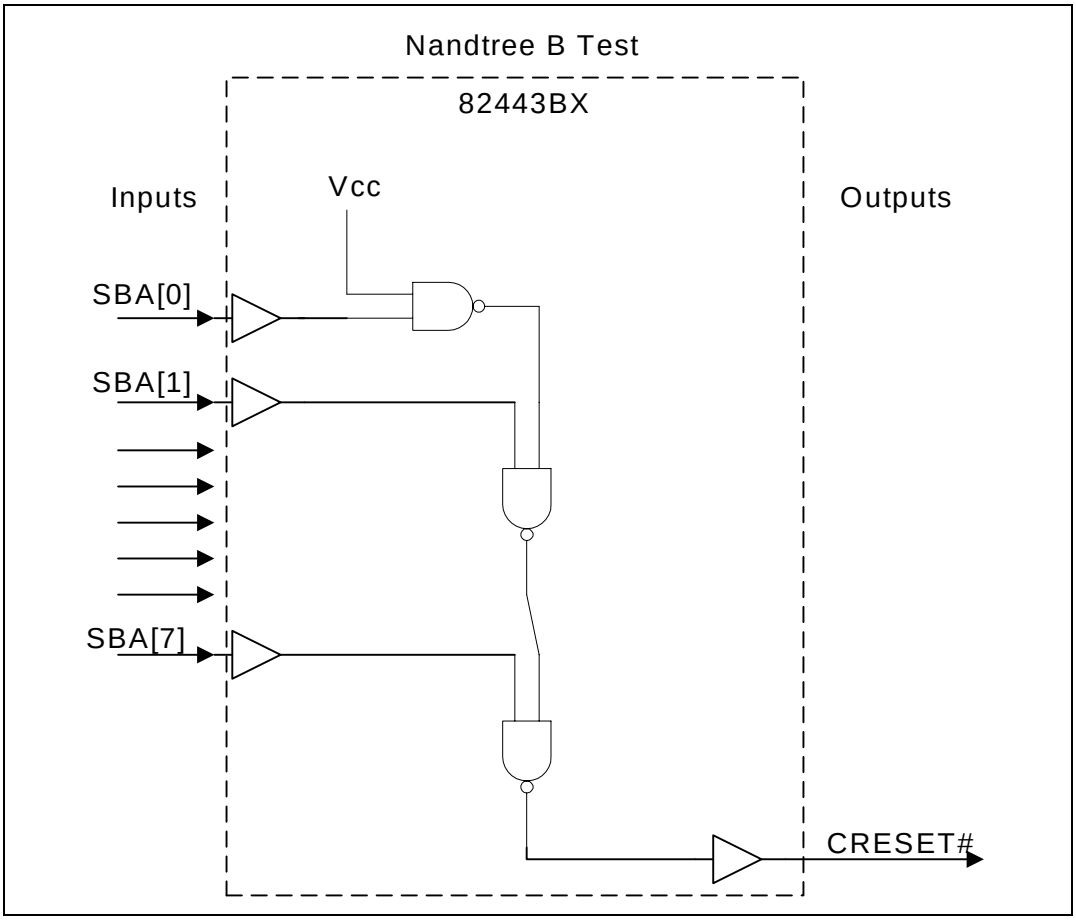
**Table 5: NANDtree B Outputs**

| Signals | Purpose |
|---|---|
| CRESET# | NAND-Chain B0 Output |

**Table 6: NANDtree B Chain #B0**

| | Chain #B0 | |
|---|---|---|
| # | Pin Name | Pad# |
| 1 | SBA0 | 297 |
| 2 | SBA1 | 301 |
| 3 | SBA2 | 303 |
| 4 | SBA3 | 307 |
| 5 | SBA4 | 308 |
| 6 | SBA6 | 309 |
| 7 | SBA5 | 311 |
| 8 | SBA7 | 313 |

**Figure 6. Diagram of NANDtree B Test mode**




## 17. GTL+Termination Voltage (Mobile Only)

The values for GTL + termination Voltage (mobile), VTTm have been changed to Max = 2.035 V in Table 6, 82443BX DC Characteristics, of the *82443BX Host Bridge/Controller Electrical and Thermal Timing Specification* datasheet addendum.

## 18. Undershoot Specification Changed to –750 mV (Mobile Only)

The undershoot specification has been changed to –750 mV in Table 6, 82443BX DC Characteristics, Note 2 of the *82443BX Host Bridge/Controller Electrical and Thermal Timing Specification* datasheet addendum.

The PIIX4/PIIX4E register CNTB-Count B (Function 3) at address offset 48h – 4Bh [10:6] (processor PLL lock count bits) and [5] (processor PLL lock resolution bit) control the processor lock time and resolution function. The default value of this register is 00h. These bits must be programmed to insure the 82443BX minimum time requirements between the deassertion of the signals are met.

# Errata

## 1. Locked Cycle Retry

**Problem:** The following sequence of events following a locked retry cycle to DRAM may result in system failure.
UP Scenario:

a) The Intel 440BX AGPset is in the PIIX regime (i.e., PIIX4 has a pending cycle to DRAM).
b) The processor issues a locked read to DRAM which results in a write back.
c) The Intel 440BX AGPset retries the locked cycle to DRAM (due to pending PCI cycle to DRAM).
d) The Intel 440BX AGPset accepts the write data for the write back cycle and posts it.
e) System fails

DP Scenarios:

Case 1:

a) A PCI master initiated cycle is deferred.
b) The processor issues a locked read to DRAM which results in a write back.
c) The Intel 440BX AGPset retries the locked cycle to DRAM (due to pending PCI cycle to DRAM).
e) The Intel 440BX AGPset accepts the write data for the write back cycle and posts it.
f) System fails

Case 2:

a) CPU1 performs a locked cycle to DRAM.
b) CPU2 attempts to execute a locked cycle to DRAM which results in a write back.
c) The Intel 440BX AGPset retries the cycle from CPU2.
d) The Intel 440BX AGPset accepts the write data for the write back cycle and posts it.
e) System fails

**Implication:** System failure may occur.

**Workaround:** UP workaround - Set PCI Configuration Register 0F4h, bit 5 to 1. This will force the BX to continuously assert BPRI# when there is a pending cycle from the PIIX to DRAM
DP workaround – Assert BNR# whenever LOCK# is asserted

**Status:** This erratum is intended to be fixed in the next stepping of the 82443BX.

## 2. Error Address Pointer Register

**Problem:** When an ECC error occurs, the Error Address Pointer register, (80h) records the address of the error. As specified in the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet, the Intel 440BX AGPset should not change the EAP register value if a new error occurs. In the A-0 stepping, however, when a new error occurs, the address for the first error is overwritten.

**Implication:** The EAP register will not retain the address of the first error

**Workaround:** None

**Status:** This erratum is intended to be fixed in the next stepping of the 82443BX.

### 3. AGP Read/Write Cycles with Auto Precharge Enabled

**Problem:** When Selective Auto Precharge is enabled, AGP Read and Write cycles to DRAM may result in data errors.

**Implication:** Incorrect data may be read from or written to DRAM.

**Workaround:** Set Register 78, bit 4 to 0 to disable selective auto precharge.

**Status:** This erratum is intended to be fixed in the next stepping of the 82443BX.

### 4. Global SMRAM Enable Bit

**Problem:** The Global SMRAM Enable, (PCI Config Register 72, bit 3) can be modified even when D_LCK (PCI Configuration Register 72, bit 4) is set.

**Implication:** Software can disable SMRAM space, even though the D_LCK bit has been set.

**Workaround:** None

**Status:** This erratum is intended to be fixed in the next stepping of the 82443BX.

### 5. MA11 High during MRS Command

**Problem:** According to the PC100 SDRAM Specification, Rev 1.5 during an MRS command to SDRAM MA11 must be low. The 82443BX A-0 step drives MAB13# high, which is connected to MA11 on the SDRAM component.

**Implication:** Some SDRAM DIMMs may not be properly initialized.

**Workaround:** None

**Status:** This erratum is intended to be fixed in the next stepping of the 82443BX.

### 6. PCI Memory Read Line

**Problem:** While in the process of performing a PCIx memory read line cycle, two back-to-back snoop cycles occur which are successfully completed. The following CPU initiated cycles do not get a response.

**Implication:** System will fail.

**Workaround:** Set PCI Configuration Register F4, bit 0 to 1.

**Status:** This erratum is intended to be fixed in the next stepping of the 82443BX.

### 7. PLL Operation at 100 MHz

**Problem:** The PLL used to generate the 100 MHz DRAM clock output is not stable over the specified operating range.

**Implication:** This may cause system failures when running at 100 MHz. Systems will operate normally at 66 MHz.

**Workaround:** Screened A-0 components are available. Reducing the 3.3V power supply voltage may also eliminate the failures.

**Status:** This erratum is intended to be fixed in the next stepping of the 82443BX.

### 8. Snoop Ahead

**Problem:** The following sequence of events may cause incorrect data to be transferred and/or a system hang:

1. PCIx device performs a memory read multiple.
2. The first snoop for the PCIx read is clean.
3. The second snoop for the PCIx read is dirty, which requires a writeback cycle.
4. When the second snoop begins, there is an outstanding write (CPU initiated) on the host bus (the data has not transferred yet).
5. The destination for the outstanding write data initiated by the CPU must be different than the destination for the writeback caused by the second snoop cycle.

**Implication:** Incorrect data will be transferred and/or the system will hang.

**Workaround:** Set PCI Configuration Register F4, bit 0 to 1.

**Status:** This erratum is intended to be fixed in the B-1 stepping of the 82443BX.

### 9. Power Dissipation

**Problem:** Internal diodes that were connected incorrectly caused higher standby and operating power on the B-0 step of 82443BX.

**Implication:** Power dissipation on the B-0 step silicon will be higher.

**Workaround:** None.

**Status:** This erratum is intended to be fixed in the B-1 stepping of the 82443BX.

### 10. Hard Reset Collision with Refresh

**Problem:** During a software generated hard reset, if a DRAM refresh cycle coincides with the activation of PCIRST#, the system will hang.

**Implication:** The system will hang.

**Workaround:** The system BIOS must disable refresh before generating the reset sequence

**Status:** This erratum will **not** be fixed in the B-1 stepping of the 82443BX. This erratum is intended to be fixed in the C-0 stepping of the 82443BX.

### 11. IPDLT Bit Setting

**Problem:** System validation has uncovered a marginal internal timing path.

**Implication:** An incorrect address may be driven on the DRAM bus, resulting in memory data being fetched from the wrong location.

**Workaround:** The IPDLT bits (register offset 76h, bits 8 and 9) should be set to 01 (i.e., set bit 8 to 1).

**Status:** BIOS workaround (configuration register change). This erratum is intended to be fixed in the next stepping of the 82443BX.

### 12. SDRAM Suspend Refresh

**Problem:** This erratum may occur in Intel 440BX AGPset platforms that implement suspend or Stop Clock (C3) states. Platforms that are affected include mobile SDRAM platforms using module MM-config mode (single CKE) and 4 DIMM desktop platforms using GCKE.

These platforms require the Intel 440BX AGPset memory controller to stop the normal refresh and place the SDRAM in a self-refresh mode before the system transitions to one of these states. If the self-refresh trigger (SUSTAT1# signal asserted) occurs at the same time as an internally generated normal refresh request, the Intel 440BX AGPset generates an incorrect CKE# and CS# signal sequence to the SDRAM. The SDRAM is not placed in self-refresh mode and memory contents may be lost.

Mobile SDRAM platforms using normal mode (not MM-config) and 3 DIMM desktop platforms are not affected. 4 DIMM desktop platforms that do not use GCKE are also not affected.

**Implication:** The observed effect of the erratum is a system hang, although data loss or corruption is theoretically possible.

**Workaround:** APM BIOS workaround:

POS, POSCCL, POSCL, STR and C3 states
The workaround disables normal refresh prior to entering these states and before the 82443BX automatically generates the SDRAM self-refresh command. BIOS will re-enabling normal refresh on exit from these states.

ACPI BIOS workaround (TBD):

**Status:** Implement BIOS workaround. This erratum is intended to be fixed in the next stepping of the 82443BX.

### 13. Refresh Collision with SUS_STAT# Assertion (EDO Memory)

**Problem:** On entry to STR or POSCL in a system with EDO memory, if SUSSTAT1# is asserted at the same time a DRAM refresh cycle occurs the normal refresh state machine is left in an improper state. Refresh control is transferred to the suspend refresh state machine which is not affected. When the system resumes from STR, refresh control is returned to the normal refresh state machine which is in an improper state.

**Implication:** The system will hang, typically with RAS# stuck high and CAS stuck low. During the execution of the resume code, operation will continue until the BIOS sets the NREF_EN bit to a 1 (82443BX, Device#0, Register Offset 7Ah, bit 4).

**Workaround:** A BIOS workaround consisting of aligning the occurrence of the 82443BX north bridge refresh cycles away from the transitions of PIIX4 south bridge SUSCLK# (which controls the assertion of SUSSTAT#) is available.

**Status:** Implement BIOS workaround. This erratum is intended to be fixed in the next stepping of the 82443BX.

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# Specification Clarifications

## 1. Normal Refresh Enable

When the user performs a soft reset, the PIIX will drive SUSTAT# to BX. This will force the BX to switch to a suspend refresh state. When the BIOS attempts to execute cycles to DRAM, the BX will not accept these cycles because it believes that it is in a suspend state

After coming out of reset the software must set the normal refresh enable bit (bit 4, power management control register Offset 7Ah) in the 82443BX before doing an access to memory.

## 2. CKE Function with Registered DIMMs

The stacking technology used for registered DIMMs prohibits the use of the CKE function. For registered DIMMs, components are stacked on top of one another. The stacked components are physically in the same row, but logically in separate rows. The stacked components connect all pins together, except for the CS# pin, in order to address components in different rows. Since the CKE pins for the components are connected together, and the components are logically in different rows, the CKE function is not supported.

## 3. Memory Initialization with ECC Enabled

For Intel 440BX AGPset systems using ECC memory, the memory must be initialized with ECC enabled (NBXCFG bits 31 through 24 and bits 7 and 8). Any ECC errors received during initialization should be ignored.

## 4. DCLKO State during POS/STR

The state of DCLKO during POS/STR may be high or low. As a result, mobile or desktop designs implementing POS/STR should move the CKBF component to the same VCC3 plane as the 82443BX component.

## 5. DCLKRD Pin Is Connected to NAND Chain

Even though DCLKRD (pin AB22) has been changed to a no connect (see Specification Change 9), the DCLKRD pin is still routed internally as part of the NAND chain.

## 6. Modifying DRAM Configuration Registers during DRAM Cycles

Modifying any configuration registers that affect DRAM (SDRAM or EDO) while DRAM cycles are running may cause system problems. The DRAM configuration registers should be completely initialized before running DRAM cycles.

## 7. Side Band Addressing Signals Float before SBA Enable Is Set

The 82443BX does not have internal pull-ups on the SBA[7:0] signals. Some AGP devices do not drive the SBA[7:0] signals prior to the SBA Enable AGP enable bits being set. This may cause failures in an Intel 440BX AGPset-based system. For AGP devices that do not drive SBA[7:0] prior to SBA and AGP enable bits being set, a workaround is required.

## 8. 128-Mbit Technology SDRAM Memory Use

Reference the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet. Add the following comments to page 4-14, paragraph 4.3, DRAM Interface, after the last sentence of the first paragraph:

128-Mbit technology SDRAM using 16MX8 devices have been tested in the Intel 82440BX AGPset System Validation (SV) platform using the 82443BX C-1 stepping. This SDRAM memory configuration was double-sided. Each SDRAM DIMM module therefore contained a total of 256 Mb of memory. A total of four DIMM modules were available for testing. There were no detection or sizing problems with this SDRAM memory array using the 82443BX SV board and 82443BX SV BIOS. The Intel 440BX AGPset supports the use of 128-Mbit technology SDRAM memory using the 82443BX C-1 stepping as described in this paragraph. It is recommended that OEMs wishing to use 128-Mbit technology SDRAM perform validation using their own BIOS on their own Intel 440BX AGPset systems.

## 9. HCLKIN Lead Time to PCLKIN Timing

Reference the *82443BX Host Bridge/Controller Electrical and Thermal Specification* datasheet addendum, Table 11, *PCI Clock Timing; 33 MHz.* Add the following row to the table after the symbol t34, HCLKIN Lead Time to PCLKIN:

| | | | | | |
|---|---|---|---|---|---|
| t34a | HCLKIN Lead Time to PCLKIN (mm config enabled) | 1.0 | 5 | | Ns |

## 10. MBSC – Memory Buffer Strength Control Register (Device 0) Address Offset 69-6Eh

Reference Section 3.3.20, *MBSC – Memory Buffer Strength Control Register (Device 0),* Address Offset 69-6Eh, *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet The "NOTE" is changed to read:

***Note:***

1. The Intel recommended settings for this register in the 440BX/440GX and 440BX/440GX BIOS specifications and specification updates reflect validation by Intel of specific platforms and memory. These register settings can be revised or modified for new platforms or new memory combinations when functionality and signal quality is confirmed by follow-up validation by OEMs.
2. The choice of a 100 MHz or a 66 MHz buffer setting is independent of bus frequency. It is possible to select a 100 MHz memory buffer even though the bus frequency is 66 MHz (and vice versa).

3. These bit values can be used in combination and can be manipulated in order to obtain the best characteristics at platform level.

## 11. Multi-Bit Memory Error Clarification

When an Intel 440BX AGPset platform is configured for ECC support, if a multi-bit uncorrectable memory error is detected during a memory read by a system device, an SERR, SCI, or SMI will be generated. This typically results in an NMI, however bad data may still reach the intended target before the NMI can be generated or before NMI interrupt handler can service the problem. This may result in bad data being returned to the target and may be permanently stored, resulting in system data corruption. This chipset was not architected or designed to ensure that targets are protected from this corrupted data in these situations.

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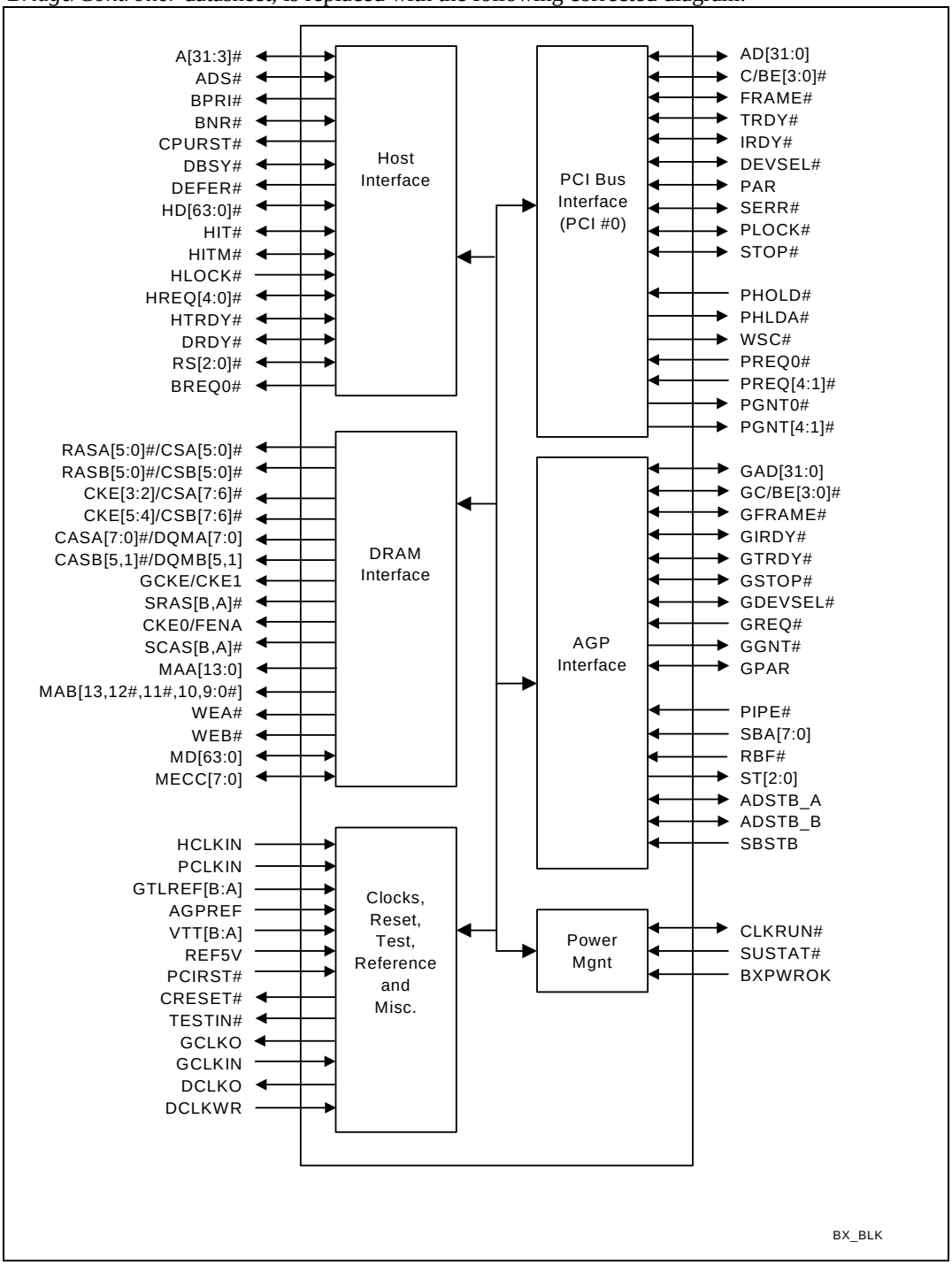
# Documentation Changes

## 1. Correct Intel® 82443BX Simplified Block Diagram

The 82443BX Simplified Block Diagram, page iv, *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet, is replaced with the following corrected diagram:



## 2. Note 3, Table 3-1

The following is added as Note 3 to Table 3-1, *82443 Register Map – Device 0 (Sheet 2 of 2),* of the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet:

"3. Missing leading values of the default value settings are zeros. For example, address offset 30–33h (reserved) is shown with a default value of "00h". The actual default value is "00000000h". Another example is address offset F2–F7h. The default value of this reserved register is shown as "0000F800h". The actual default value is "00000000F800h"."

## 3. Page iii, Features List, Is Changed

(See Specification Change #8, above.)

The *Integrated DRAM Controller* section of the *Intel 82443BX Features List* on page iii of the *Intel® 440BX AGPset: 82443BX Host Bridge/Controller* datasheet is changed as follows:

The first item is changed to read:

"…128-Mbit SDRAM technology is supported as stated in paragraph 4.3 of page 4-14 of this document. As a result, 8 Mbytes to 1 Gbyte of memory is available depending on system implementation."

The last item is changed to read:

"…Enhanced SDRAM Open Page Architecture Support for 16-, 64-, and 128-Mbit SDRAM technology devices with 2K, 4K, and 8K page sizes."